SLD-2083CZ

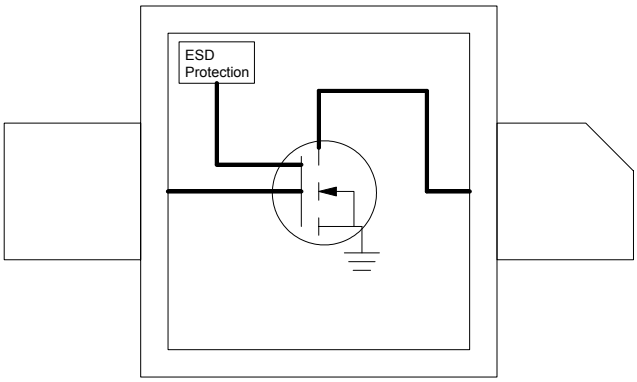
RoHS Compliant & Green Package

12 Watt Discrete LDMOS FET in Ceramic Package

Product Description

Sirenza Microdevices' **SLD-2083CZ** is a robust 12 Watt high performance LDMOS transistor designed for operation to 2700MHz. It is an excellent solution for applications requiring high linearity and efficiency at a low cost. The SLD-2083CZ is typically used in the design of driver stages for power amplifiers, repeaters, and RFID applications. The power transistor is fabricated using Sirenza's high performance XeMOS II™ process.

Functional Schematic Diagram



Case Flange = Ground

Product Features

- **12 Watt Output P_{1dB}**
- **Single Polarity Supply Voltage**
- **High Gain: 18 dB at 915 MHz**
- **High Efficiency: 47% at 10W CW**
- **XeMOS II LDMOS**
- **Integrated ESD Protection, Class 1B**

Applications

- **Base Station PA driver**
- **Repeaters**
- **RFID**
- **Military Communication**
- **GSM/CDMA**

RF Specifications

Symbol	Parameter	Unit	Min	Typ	Max
Frequency	Frequency of Operation	MHz	10	-	2700
Gain	10 Watt CW, 902 - 928MHz	dB	17	18	-
Efficiency	Drain Efficiency at 10 Watt CW, 915MHz	%	40	47	-
IRL	Input Return Loss, 10 Watt Output Power, 915MHz	dB	-	-15	-10
Linearity	3rd Order IMD at 10 Watt PEP (Two Tone), 915MHz	dBc	-	-28	-26
	1dB Compression (P_{1dB}), 915MHz	Watt		12	-
	IS-95, 9 Ch Fwd, Offset=750KHz, ACPR Integrated Bandwidth, ACPR=-55dB	Watt		1.6	-
	IS-95, 9 Ch Fwd, Offset=750KHz, ACPR Integrated Bandwidth, ACPR=-45dB	Watt		3.6	-
R_{TH}	Thermal Resistance (Junction-to-Case)	ºC/W		4	

Test Conditions V_{DS} = 28.0V, I_{DQ} = 125mA, T_{Flange} = 25ºC

DC Specifications

Symbol	Parameter	Unit	Min	Typical	Max
g_m	Forward Transconductance @ 125mA I_{DS}	mA / V		590	
V_{GS}Threshold	I_{DS}=3mA	Volt		3.8	
V_{DS} Breakdown	1mA I_{DS} current	Volt		65	
C_{iss}	Input Capacitance (Gate to Source) V_{GS}=0V, V_{DS}=28V	pF		27.5	
C_{rss}	Reverse Capacitance (Gate to Drain) V_{GS}=0V, V_{DS}=28V	pF		0.81	
C_{oss}	Output Capacitance (Drain to Source) V_{GS}=0V, V_{DS}=28V	pF		14.65	
R_{DSon}	Drain to Source Resistance, V_{GS}=10V, V_{DS}=250mV	Ω		0.6	

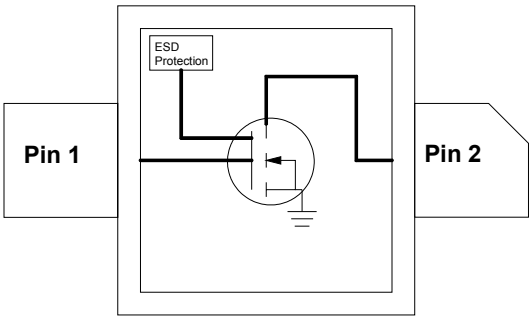
Quality Specifications

Parameter	Description	Unit	Typical
ESD Rating	Human Body Model	Volts	750
MTTF	85°C Leadframe, 200°C Channel	Hours	1.2 X 10^6

Pin Description

Pin #	Function	Description
1	Gate	Transistor RF input and gate bias voltage. The gate bias voltage must be temperature compensated to maintain constant bias current over the operating temperature range. Care must be taken to protect against video transients that exceed the recommended maximum input power or voltage. .
2	Drain	Transistor RF output and drain bias voltage. Typical voltage is 28V.
Flange	Source, Gnd	Exposed area on the bottom side of the package needs to be mechanically attached to the ground plane of the board for optimum thermal and RF performance. See mounting instructions for recommendation.

Pin Diagram



Case Flange = Ground

Note 1:
Gate voltage must be applied to V_{GS} lead concurrently or after application of drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to the transistor unless it is properly terminated on both input and output.

Note 2:
The required V_{GS} corresponding to a specific I_{DQ} will vary from device to device due to the normal die-to-die variation in threshold voltage withLDMOS transistors.

Note 3:
The threshold voltage (V_{GSTH}) of LDMOS transistors varies with device temperature. External temperature compensation may be required. See Sirenza application notes AN-067 LDMOS Bias Temperature Compensation.

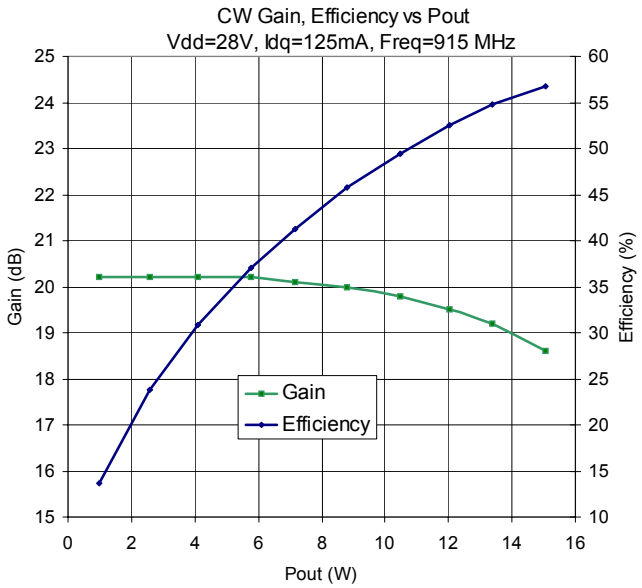
Absolute Maximum Ratings

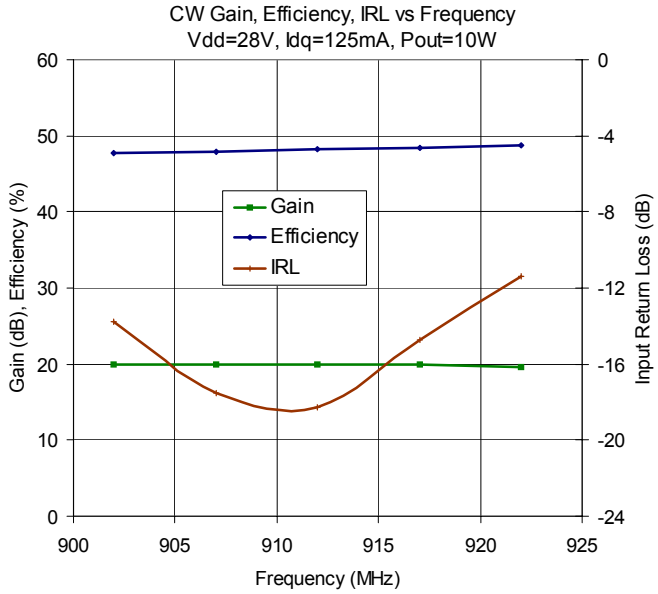
Parameters	Value	Unit
Drain Voltage (V_{DS})	35	V
Gate Voltage (V_{GS})	20	V
RF Input Power	+33	dBm
Load Impedance for Continuous Operation Without Damage	10:1	VSWR
Output Device Channel Temperature	+200	ºC
Lead Temperature During Solder Reflow	+270	ºC
Operating Temperature Range	-20 to +90	ºC
Storage Temperature Range	-40 to +100	ºC

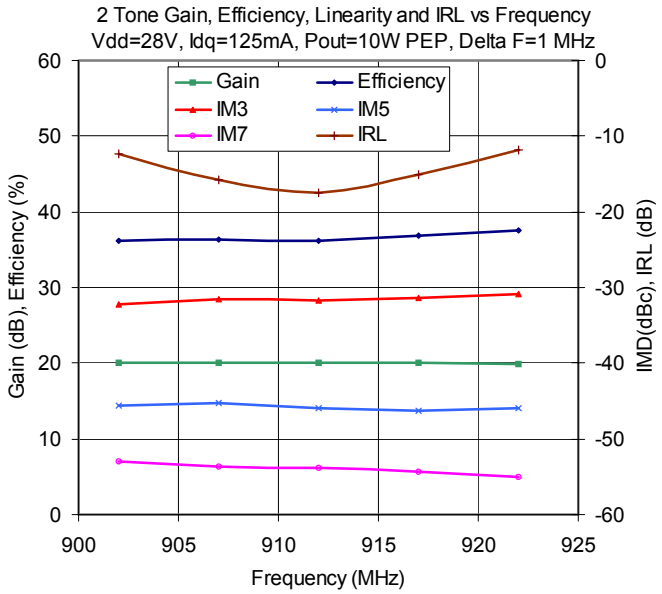
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

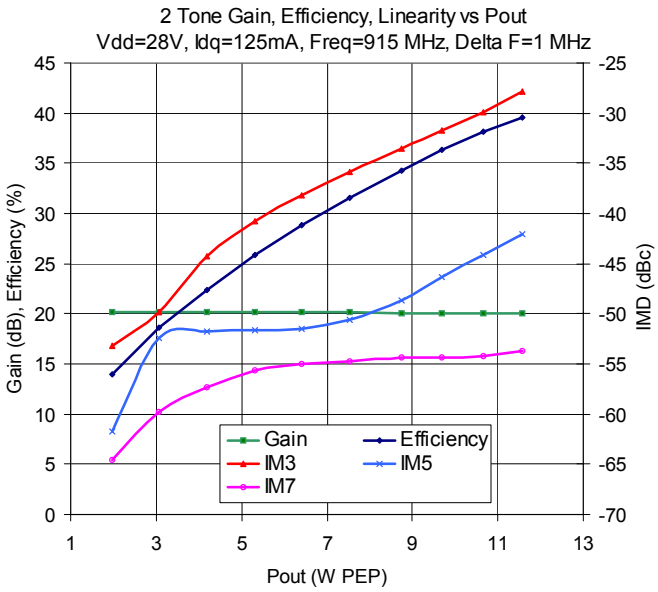
Caution: ESD Sensitive
Appropriate precaution in handling, packaging and testing devices must be observed.

Typical Performance Curves in 900 MHz Application Circuit



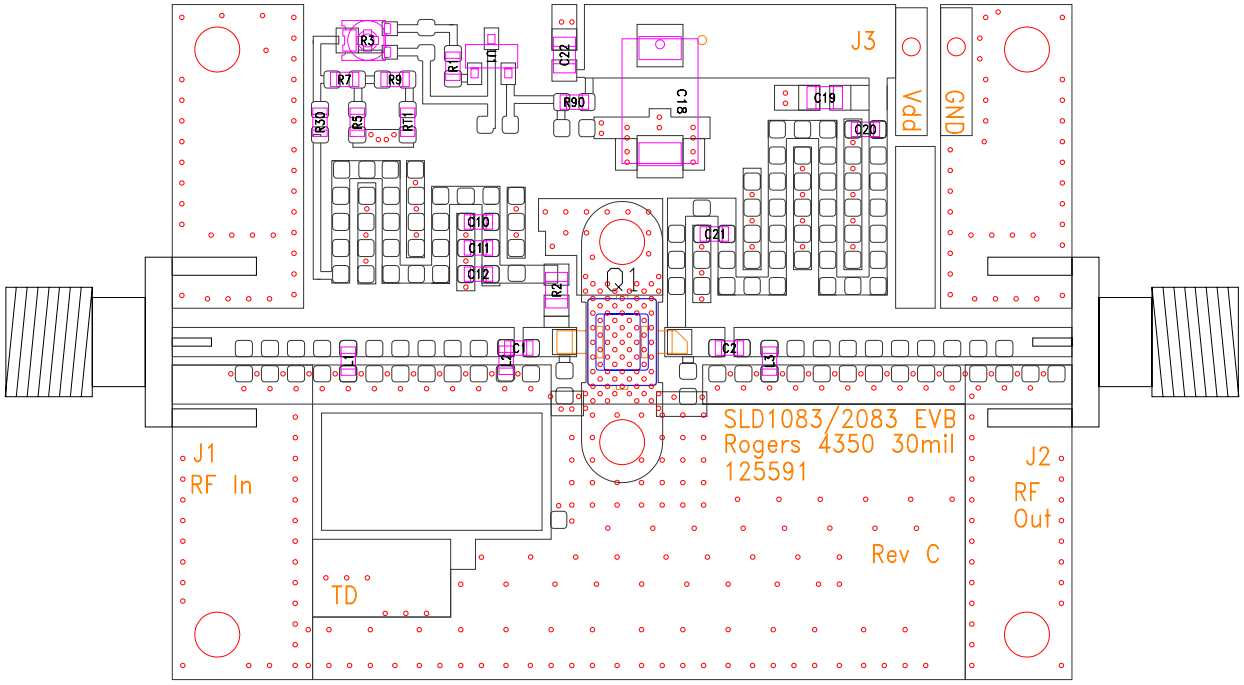






To receive Gerber files, DXF drawings, and assembly recommendations for the test board with fixture, contact applications support at support@sirenza.com.

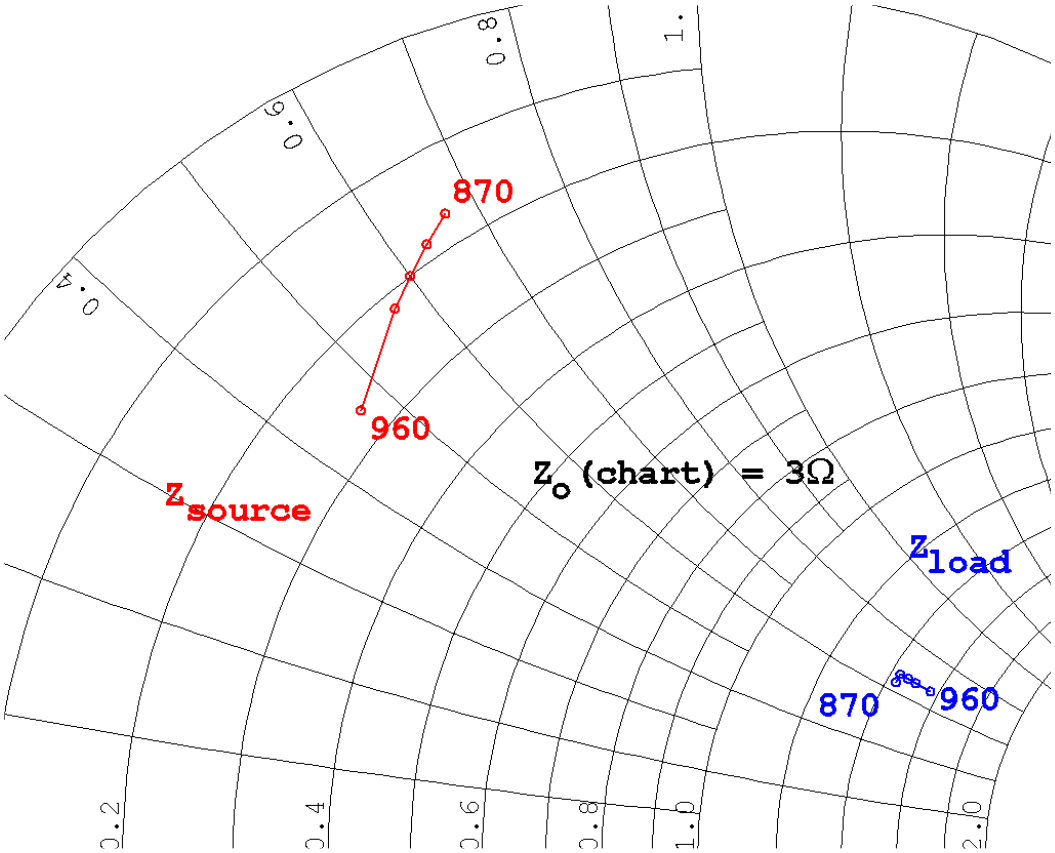
900 MHz Application Circuit

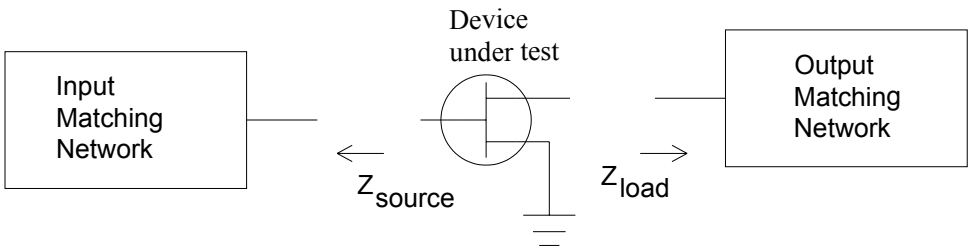


Bill of Materials - 900 MHz Application Circuit

Reference Designation	Description	Mfg	Mfg part #
C1, C2	CAP 68PF250V 5% 0603	ATC	600S680JT250XT
L1	IND, 5.1 Nh 5% 0603	coilcraft	0603CS-5N1XJB
L2	IND, 2.7 nH +/- 0.3 nH 0603	Toko	LL1608-F2N7S
L3	IND, 4.7 nH 10% 0603	Toko	LL1608-F4N7K
C10	CAP 0.1 UF 16V 10% 0603	AVX	0603YG104ZA2A
C11,C20	CAP 1000 PF 50V 10% 603	AVX	06035C102KAT2A
C12, C21	CAP 68PF 250V 5% 603 LF	ATC	600S680JT250XT
C18	CAP 10 UF 35V 20% TAN T ELECT	Kemet	T494D106M035AS
C19, C22	CAP 0.1 UF 50V 10% 805	Panasonic	ECJ2YB1H104K
J1, J2	Connector SMA END 0.037	Johnson	142-0751-821
J3	Connector MTA SMD R/A 2 PIN	Amp	640455-2
R1	RES 324 1/16W 1% 603	Panasonic	ERJ-3EKF3240V
R2	RES 49.9 1/10W 1% 805	Panasonic	ERJ-6ENF49R9V
R3	POT TRIM 500 OHM 2MM	Panasonic	EVM-2WSX80B52
R30	RES 49.9 1/16W 1% 603	Panasonic	ERJ-EKF49R9V
R5	RES 130 1/16W 1% 603	Panasonic	ERJ-3EKF1300V
R7	RES 210 1/16W 1% 603	Phillips	9C06031A2100FKHFT
R9	RES 0 1/16W 5% 603	Panasonic	ERJ-3GSY0R00V
R90	RES 1.0K 1/16W 1% 603	Panasonic	ERJ-3EKF1001V
RT1	THERMISTOR 100K 5% 603	Panasonic	ERT-J1VV104J
U1	IC VOLT REG 100 MA 5 V SOT-23	National	LM3480IM3-5.0
6 Screws	SCREW #2-56 PHILIPS PAN HEAD	various	-
6 Washers	WASHER #2 FLAT SS	various	-
PCB	PCB, 30 mils thick Dk=3.48	Rogers	4350
Heatsink	machined aluminum	various	-

Impedance data



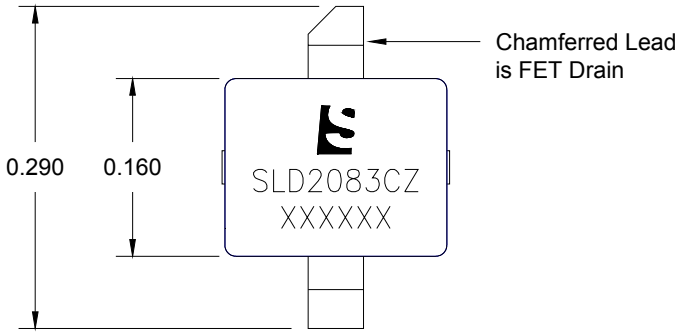


Z_{source} and Z_{load} are the optimal impedances presented to the SLD-2083CZ when operating at 28V, Idq=125mA, Pout=10 W PEP

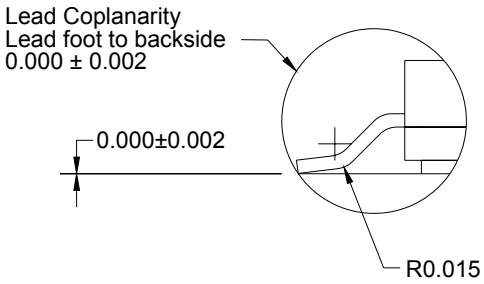
Impedance Data

Frequency (MHz)	Z_{source}	Z_{load}
870	0.50 + j 2.0	4.3+ j 1.9
880	0.55 + j 1.9	4.3 + j 2.0
900	0.60 + j 1.8	4.4+ j 2.0
930	0.65 + j 1.7	4.5 + j 2.0
960	0.80 + j 1.4	4.7 + j 2.0

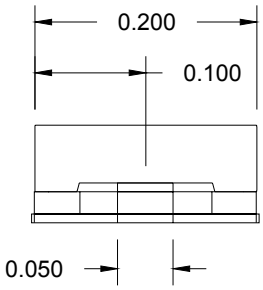
Package Outline Drawing



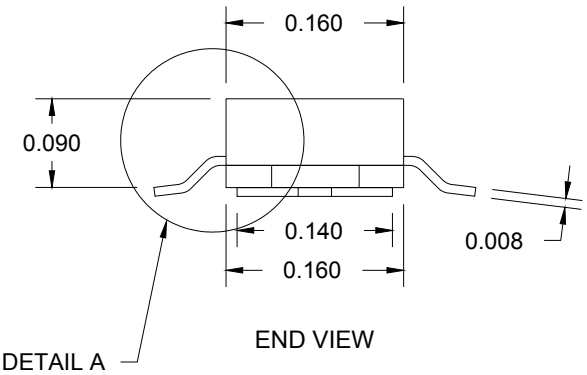
TOP VIEW



DETAIL A

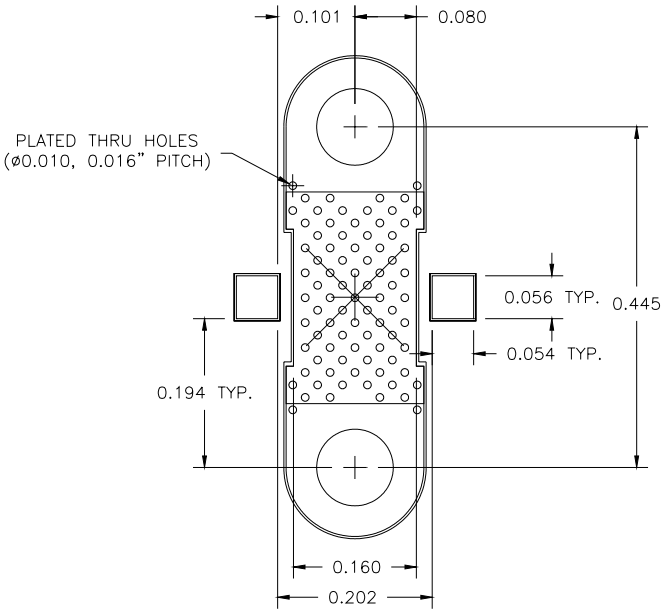


SIDE VIEW



END VIEW

Recommended Landing Pads for the RF083 Package



All Dimensions are in inches

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
SLD-2083CZ	500	7"