VNQ830P-E

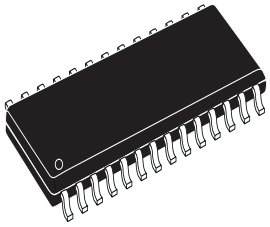
Quad channel high-side driver

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VNQ830P-E	65 mΩ(1)	6 A	36 V

1. Per each channel.

- ECOPACK®: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Very low standby current
- CMOS compatible input
- On-state open-load detection
- Off-state open-load detection
- Thermal shutdown protection and diagnosis
- Undervoltage shutdown
- Overvoltage clamp
- Output stuck to V_{CC} detection
- Load current limitation
- Reverse battery protection
- Electrostatic discharge protection



SO-28 (double island)

Description

The VNQ830P-E is a quad HSD formed by assembling two VND830P-E chips in the same SO-28 package. The VND830P-E is a monolithic device made using STMicroelectronics™ VIPower™ M0-3 technology. The VNQ830P-E is intended for driving any type of multiple load with one side connected to ground.

The active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protects the device against over-load. The device detects the open-load condition in both the on and off-state.

In the off-state the device detects if the output is shorted to V_{CC}. The device automatically turns off in the case where the ground pin becomes disconnected.

Table 1. Device summary

Package	Tube	Tape and reel
SO-28	VNQ830P-E	VNQ830PTR-E

Contents

1 **Block diagram and pin description 5**

2 **Electrical specifications 7**

2.1 Absolute maximum ratings 7

2.2 Thermal data 8

2.3 Electrical characteristics 8

2.4 Electrical characteristics curves 15

3 **Application information 18**

3.1 GND protection network against reverse battery 18

3.1.1 Solution 1: a resistor in the ground line (RGND only) 18

3.1.2 Solution 2: a diode (D_{GND}) in the ground line 19

3.2 Load dump protection 19

3.3 MCU I/O protection 19

3.4 Open-load detection in off-state 20

3.5 Maximum demagnetization energy (V_{CC} = 13.5 V) 21

4 **Package and PCB thermal data 22**

4.1 SO-28 thermal data 22

5 **Package and packing information 25**

5.1 ECOPACK® packages 25

5.2 SO-28 packing information 26

6 **Revision history 27**

List of tables

Table 1. Device summary . . . 1
Table 2. Suggested connections for unused and not connected pins . . . 6
Table 3. Absolute maximum ratings . . . 7
Table 4. Thermal data (per island) . . . 8
Table 5. Power . . . 8
Table 6. Protections . . . 9
Table 7. V_{CC} - output diode . . . 9
Table 8. Switching (V_{CC} = 13V; Tj = 25°C) . . . 10
Table 9. Logic inputs . . . 10
Table 10. Status pin . . . 10
Table 11. Open-load detection . . . 11
Table 12. Truth table . . . 12
Table 13. Electrical transient requirements . . . 13
Table 14. Thermal calculation according to the PCB heatsink area . . . 22
Table 15. Thermal parameters . . . 24
Table 16. SO-28 mechanical data . . . 25
Table 17. Document revision history . . . 27

List of figures

Figure 1. Block diagram . . . 5
Figure 2. Configuration diagram (top view) . . . 6
Figure 3. Current and voltage conventions . . . 8
Figure 4. Status timings . . . 11
Figure 5. Switching characteristics . . . 12
Figure 6. Waveforms . . . 14
Figure 7. Off-state output current . . . 15
Figure 8. High level input current . . . 15
Figure 9. Input clamp voltage . . . 15
Figure 10. Turn-on voltage slope . . . 15
Figure 11. Overvoltage shutdown . . . 15
Figure 12. Turn-off voltage slope . . . 15
Figure 13. ILIM vs Tcase . . . 16
Figure 14. On-state resistance vs VCC . . . 16
Figure 15. Input high level . . . 16
Figure 16. Input hysteresis voltage . . . 16
Figure 17. On-state resistance vs Tcase . . . 16
Figure 18. Input low level . . . 16
Figure 19. Status leakage current . . . 17
Figure 20. Status low output voltage . . . 17
Figure 21. Status clamp voltage . . . 17
Figure 22. Open-load on-state detection threshold . . . 17
Figure 23. Open-load off-state voltage detection threshold . . . 17
Figure 24. Application schematic . . . 18
Figure 25. Open-load detection in off-state . . . 20
Figure 26. Maximum turn-off current versus load inductance . . . 21
Figure 27. SO-28 PC board . . . 22
Figure 28. Rthj-amb vs PCB copper area in open box free air condition . . . 23
Figure 29. SO-28 thermal impedance junction ambient single pulse . . . 23
Figure 30. Thermal fitting model of a quad channel HSD in SO-28 . . . 24
Figure 31. SO-28 package dimensions . . . 25
Figure 32. SO-28 tube shipment (no suffix) . . . 26
Figure 33. SO-28 tape and reel shipment (suffix “TR”) . . . 26

1 Block diagram and pin description

Figure 1. Block diagram

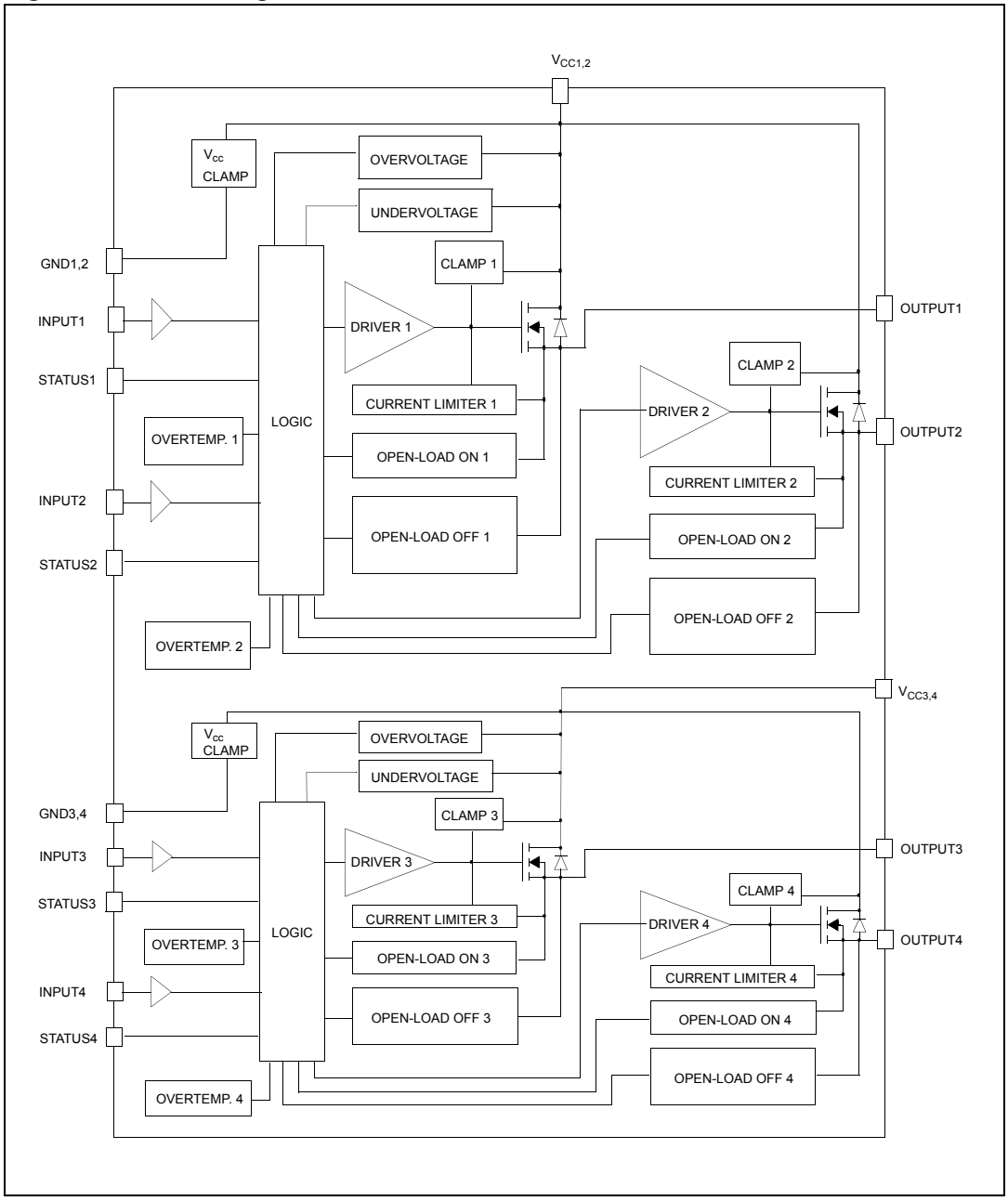


Figure 2. Configuration diagram (top view)

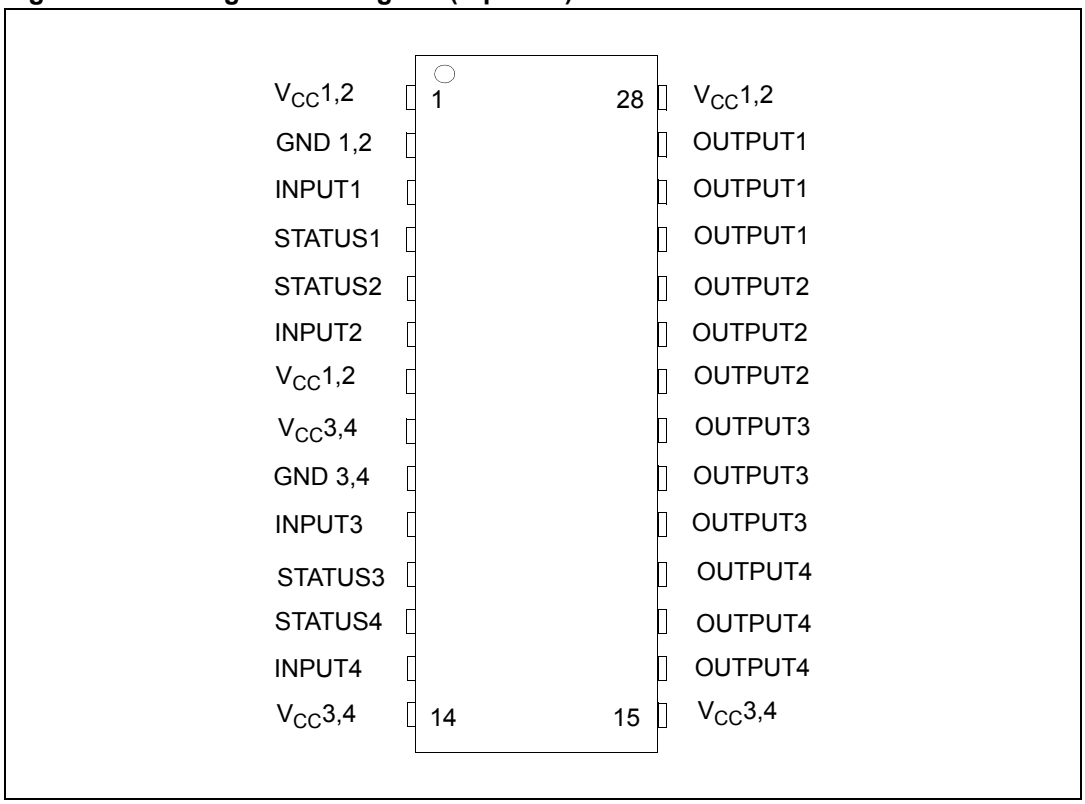


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10 KΩ resistor

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
- V_{CC}	Reverse DC supply voltage	- 0.3	V
- I_{GND}	DC reverse ground pin current	- 200	mA
I_{OUT}	DC output current	Internally limited	A
- I_{OUT}	Reverse DC output current	- 6	A
I_{IN}	DC input current	+/- 10	mA
I_{STAT}	DC status current	+/- 10	mA
V_{ESD}	Electrostatic discharge (Human Body Model: R=1.5 KΩ; C = 100 pF) - INPUT - STATUS - OUTPUT - V_{CC}	 4000 4000 5000 5000	 V V V V
E_{MAX}	Maximum switching energy (L = 1.5 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_L = 9 A)	85	mJ
P_{tot}	Power dissipation (per island) at T_{lead} = 25 °C	6.25	W
T_j	Junction operating temperature	Internally limited	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 4. Thermal data (per island)

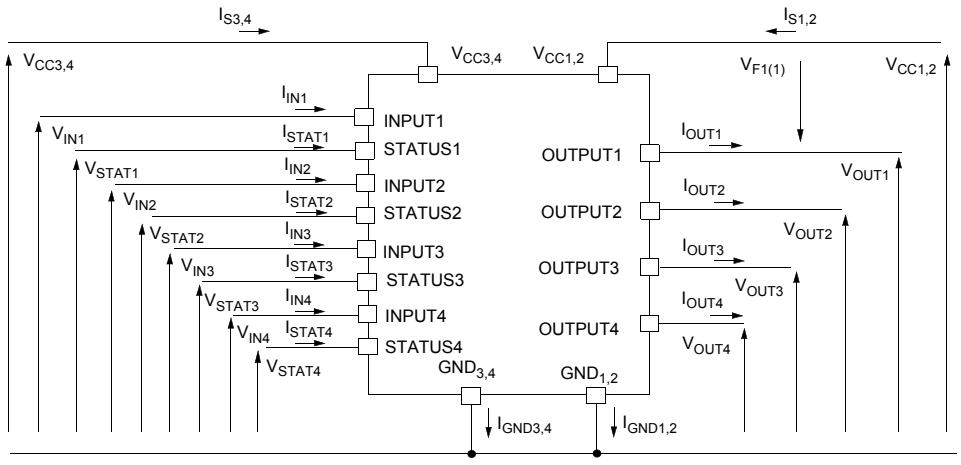
Symbol	Parameter	Value		Unit
$R_{thj\text{-}lead}$	Thermal resistance junction-lead	15		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (one chip ON)	60(1)	44(2)	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (two chips ON)	46(1)	31(2)	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35 µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 6cm^2 of Cu (at least 35 µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 36 V; -40°C < T_j < 150°C, unless otherwise stated.

Figure 3. Current and voltage conventions



1. $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown		36			V

Table 5. Power (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON}	On-state resistance	I_{OUT} = 2 A; T_j = 25°C I_{OUT} = 2 A; V_{CC} > 8 V			65 130	mΩ mΩ
I_S	Supply current	Off-state; V_{CC} = 13 V; V_{IN} = V_{OUT} = 0 V Off-state; V_{CC} = 13 V; V_{IN} = V_{OUT} = 0 V; T_j = 25°C On-state; V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		12 12 5	40 25 7	µA µA mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN} = 0V; V_{OUT} = 3.5 V	-75		0	µA
$I_{L(off3)}$	Off-state output current	V_{IN} = V_{OUT} = 0V; V_{CC} = 13 V; T_j = 125°C			5	µA
$I_{L(off4)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j =25°C			3	µA

Table 6. Protections

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
t_{SDL}	Status delay in overload conditions	T_j > T_{TSD}			20	µs
I_{lim}	Current limitation	V_{CC} = 13 V 5.5 V < V_{CC} < 36 V	6	9	15 15	A A
V_{demag}	Turn-off output clamp voltage	I_{OUT} = 2 A; L = 6 mH	V_{CC} -41	V_{CC} -48	V_{CC} -55	V

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 7. V_{CC} - output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	- I_{OUT} = 1.2 A; T_j = 150°C	-	-	0.6	V

Table 8. Switching (V_{CC} = 13V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 6.5Ω from V_{IN} rising edge to V_{OUT} = 1.3 V (see *Figure 5*)	-	30	-	µs
$t_{d(off)}$	Turn-off delay time	R_L = 6.5 Ω from V_{IN} falling edge to V_{OUT} = 11.7 V (see *Figure 5*)	-	30	-	µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 6.5 Ω from V_{OUT} = 1.3 V to V_{OUT} = 10.4 V (see *Figure 5*)	-	See *Figure 10*	-	V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 6.5 Ω from V_{OUT} = 11.7 V to V_{OUT} = 1.3 V (see *Figure 5*)	-	See *Figure 12*	-	V/µs

Table 9. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25 V	1			µA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	V_{IN} = 3.25 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA I_{IN} = -1 mA	6	6.8 - 0.7	8	V V

Table 10. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1.6 mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT} = 5 V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT} = 5 V			100	pF
V_{SCL}	Status clamp voltage	I_{STAT} = 1 mA I_{STAT} = - 1 mA	6	6.8 - 0.7	8	V V

Table 11. Open-load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Open-load on-state detection threshold	V_{IN} = 5 V	50	100	200	mA
$t_{DOL(on)}$	Open-load on-state detection delay	I_{OUT} = 0 A			200	µs
V_{OL}	Open-load off-state voltage detection threshold	V_{IN} = 0 V	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open-load detection delay at turn-off				1000	µs

Figure 4. Status timings

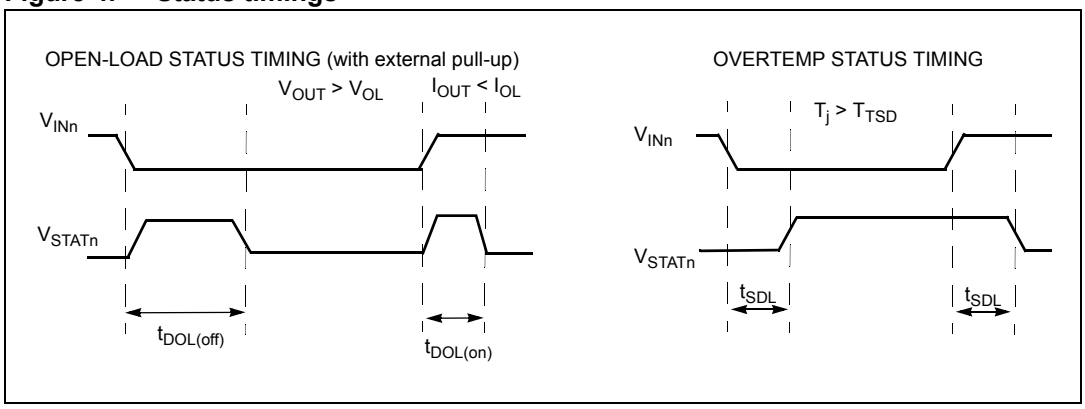


Figure 5. Switching characteristics

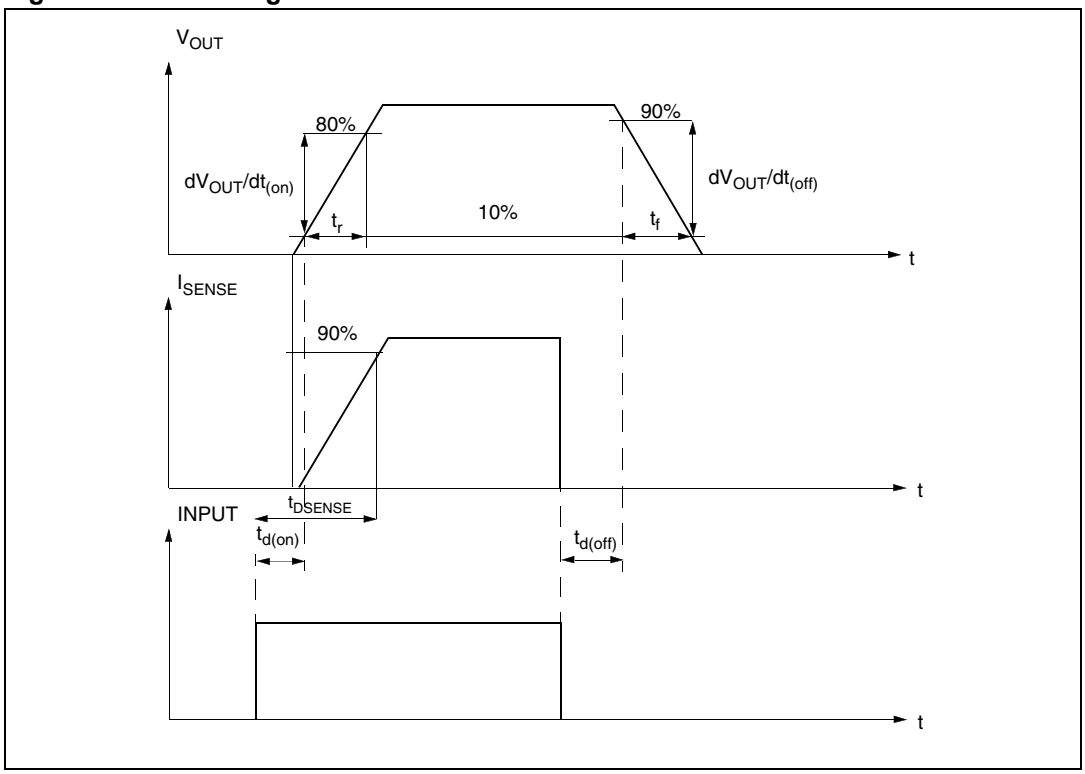


Table 12. Truth table

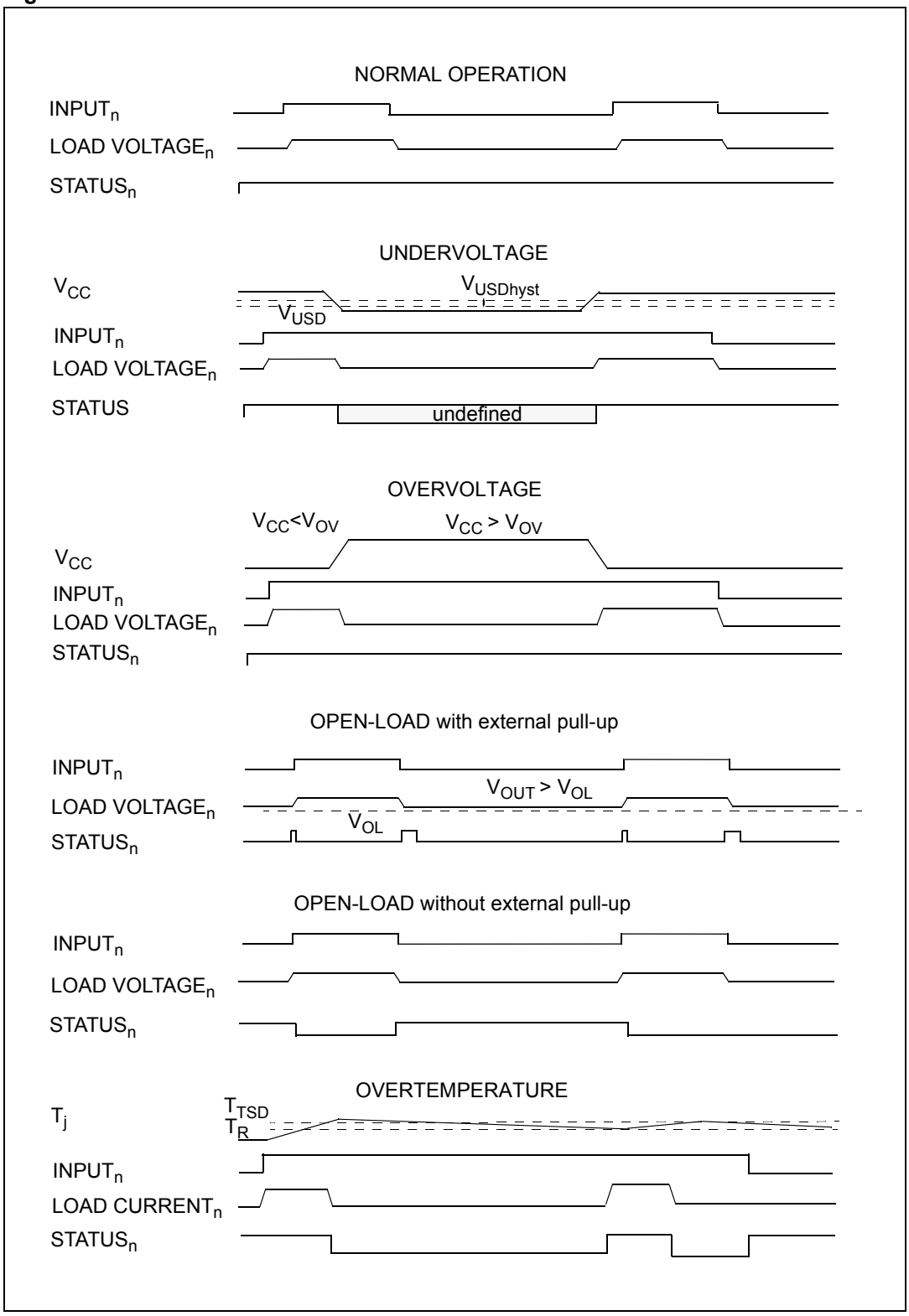
Conditions	Input	Output	Status
Normal operation	L H	L H	H H
Current limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output voltage > V_{OL}	L H	H H	L H
Output current < I_{OL}	L H	L H	H L

Table 13. Electrical transient requirements

ISO T/R 7637/1 test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25 V(1)	- 50 V(1)	- 75 V(1)	- 100 V(1)	2 ms, 10 Ω
2	+ 25 V(1)	+ 50 V(1)	+ 75 V(1)	+ 100 V(1)	0.2 ms, 10 Ω
3a	- 25 V(1)	- 50 V(1)	- 100 V(1)	- 150 V(1)	0.1 µs, 50 Ω
3b	+ 25 V(1)	+ 50 V(1)	+ 75 V(1)	+ 100 V(1)	0.1 µs, 50 Ω
4	- 4 V(1)	- 5 V(1)	- 6 V(1)	- 7 V(1)	100 ms, 0.01 Ω
5	+ 26.5 V(1)	+ 46.5 V(2)	+ 66.5 V(2)	+ 86.5 V(2)	400 ms, 2 Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

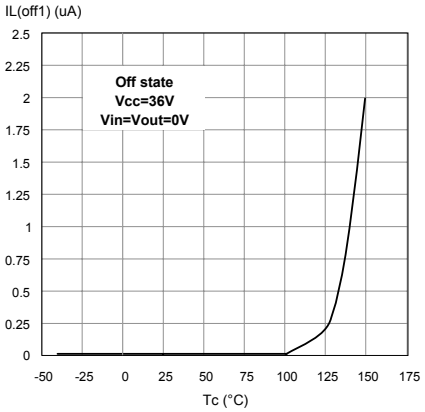


Figure 8. High level input current

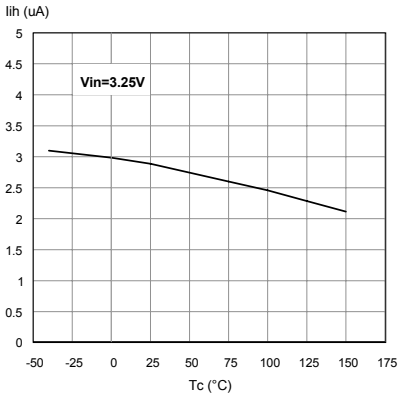


Figure 9. Input clamp voltage

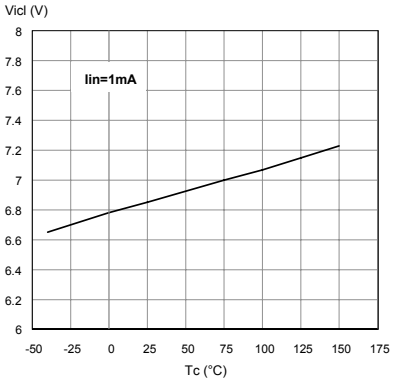


Figure 10. Turn-on voltage slope

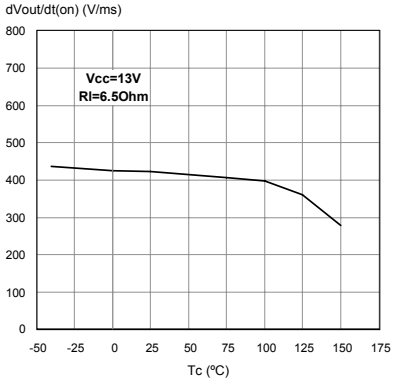


Figure 11. Overvoltage shutdown

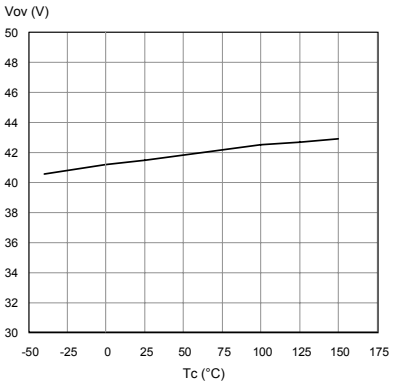


Figure 12. Turn-off voltage slope

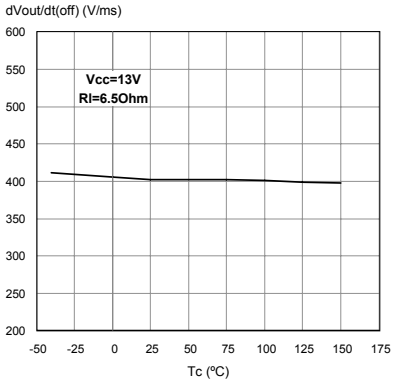


Figure 13. I_{LIM} vs T_{case}

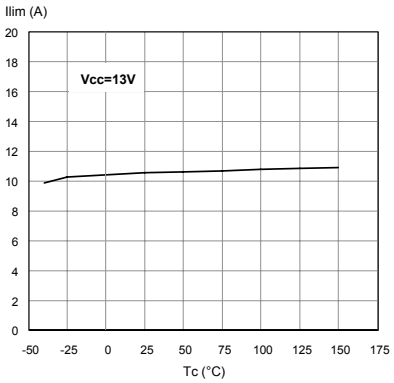


Figure 14. On-state resistance vs V_{CC}

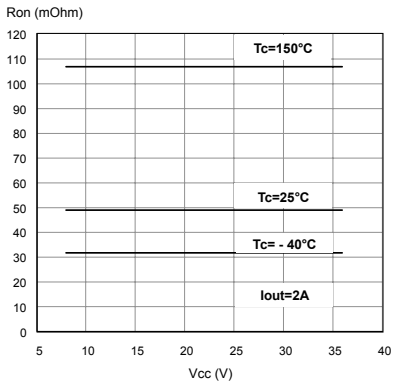


Figure 15. Input high level

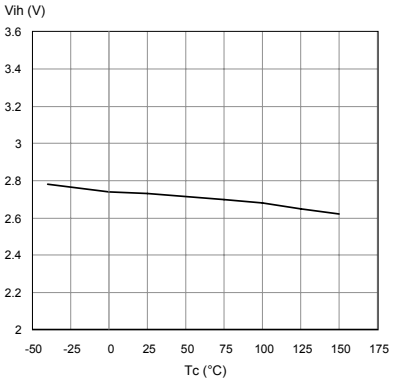


Figure 16. Input hysteresis voltage

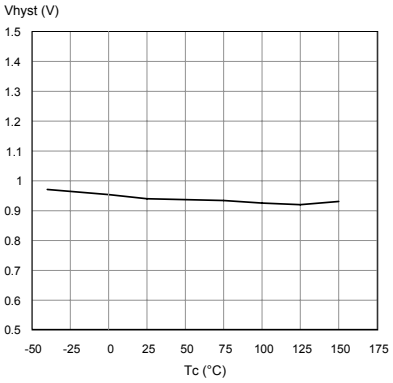


Figure 17. On-state resistance vs Tcase

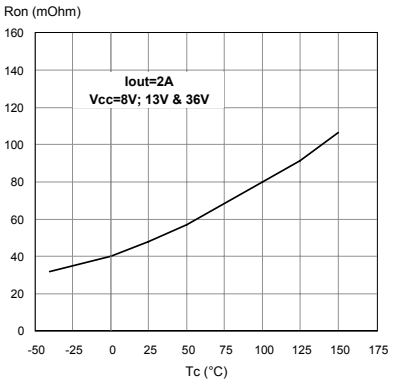


Figure 18. Input low level

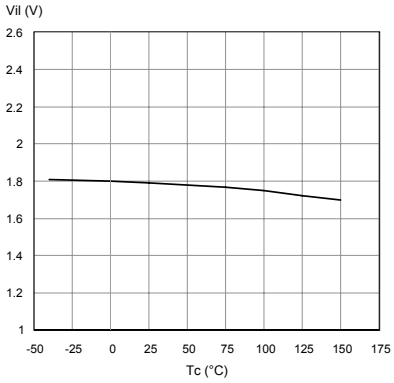


Figure 19. Status leakage current

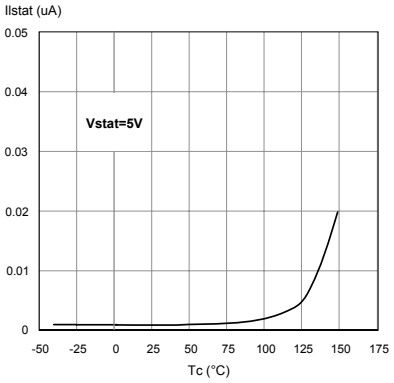


Figure 20. Status low output voltage

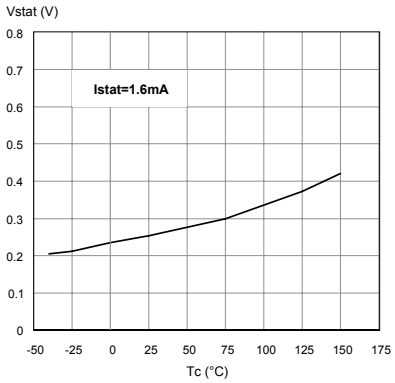


Figure 21. Status clamp voltage

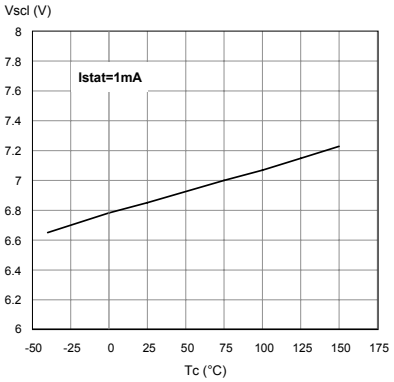


Figure 22. Open-load on-state detection threshold

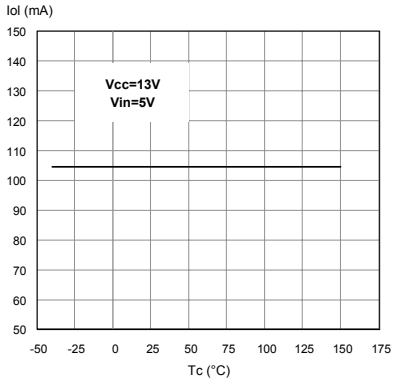
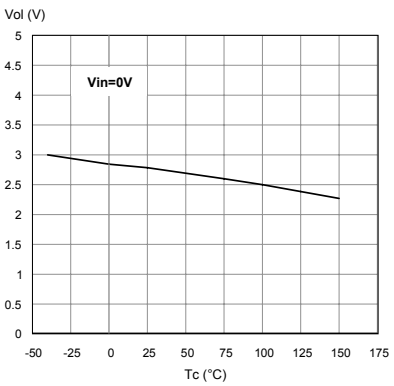
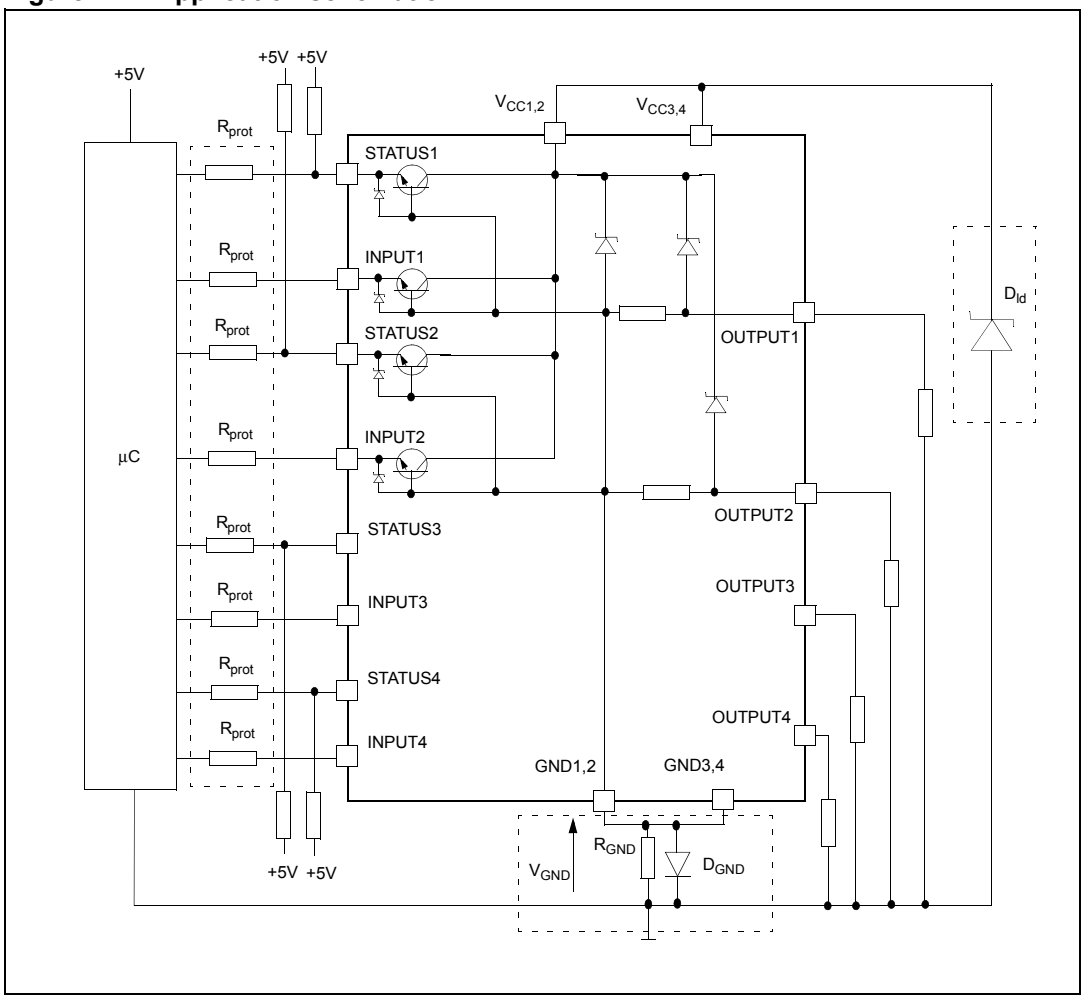


Figure 23. Open-load off-state voltage detection threshold



3 Application information

Figure 24. Application schematic



Note: Channels 3 & 4 have the same internal circuit as channel 1 & 2.

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: a resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following show how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600\ mV / 2\ (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where - I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ during reverse battery situations) is:

$$P_D = (- V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND} .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1 kΩ) should be inserted in parallel to D_{GND} if the device is driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network produces a shift (~600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift not varies if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than those shown in *Table 13*.

3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

$$- V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Example

For the following conditions:

V_{CCpeak} = - 100 V

$I_{latchup} \geq 20$ mA

$V_{OH\mu C} \geq 4.5$ V

5 kΩ ≤ R_{prot} ≤ 65 kΩ.

Recommended values are:

R_{prot} = 10 kΩ

3.4 Open-load detection in off-state

Off-state open-load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

1. No false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition:

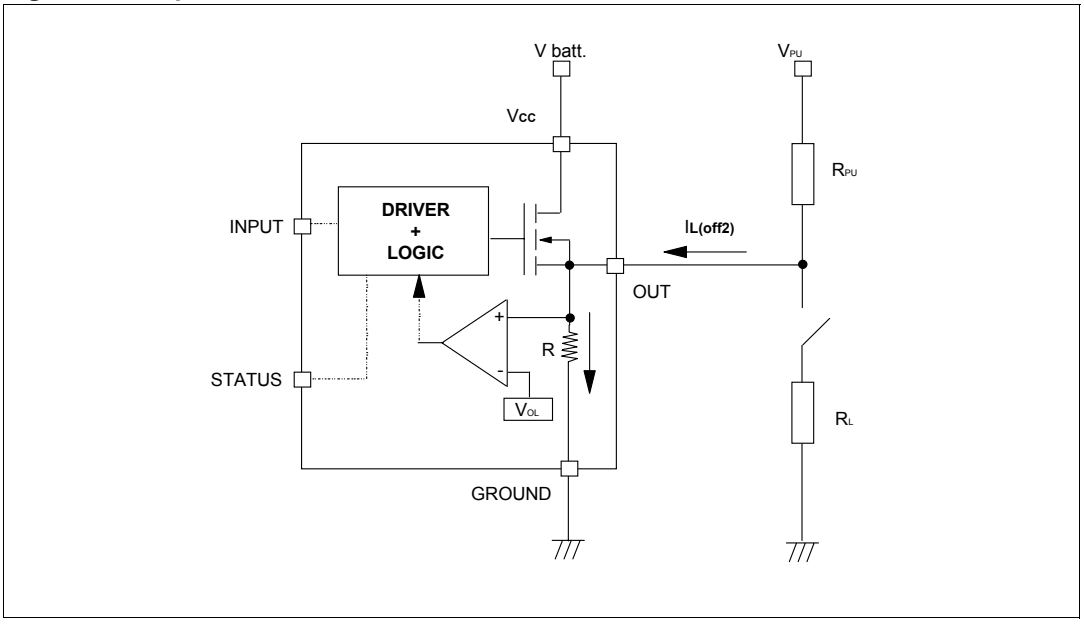
$V_{OUT} = (V_{PU} / (R_L + R_{PU}))R_L < V_{Olmin}$.

2. No misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition:

$R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

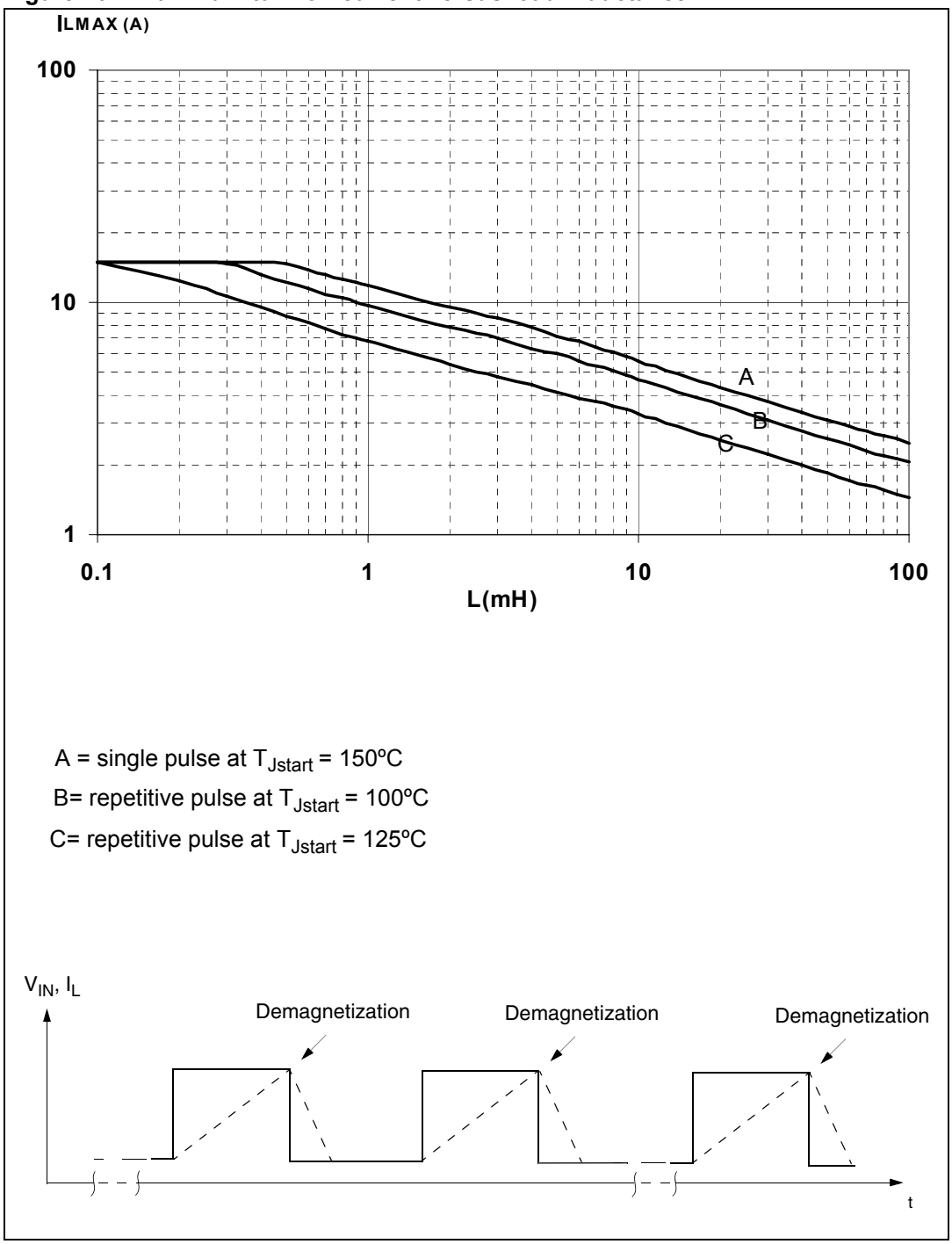
Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

Figure 25. Open-load detection in off-state



3.5 Maximum demagnetization energy (V_{CC} = 13.5 V)

Figure 26. Maximum turn-off current versus load inductance



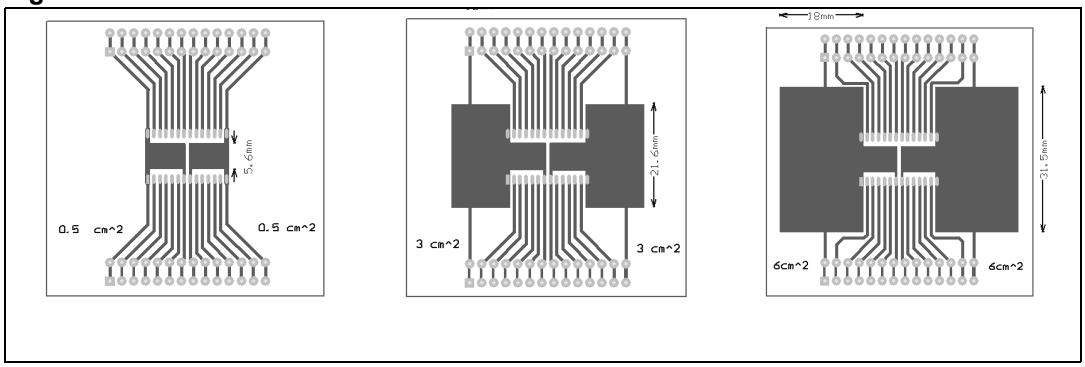
Note: Values are generated with R_L = 0 Ω.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PCB thermal data

4.1 SO-28 thermal data

Figure 27. SO-28 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 µm, Copper areas: 0.5 cm^2, 3 cm^2, 6 cm^2).

Table 14. Thermal calculation according to the PCB heatsink area

Chip 1	Chip 2	T_{jchip1}	T_{jchip2}	Note
ON	OFF	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
OFF	ON	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
ON	ON	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1} = P_{dchip2}$
ON	ON	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

R_{thA} = thermal resistance junction to ambient with one chip ON

R_{thB} = thermal resistance junction to ambient with both chips ON and $P_{dchip1} = P_{dchip2}$

R_{thC} = mutual thermal resistance

Figure 28. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

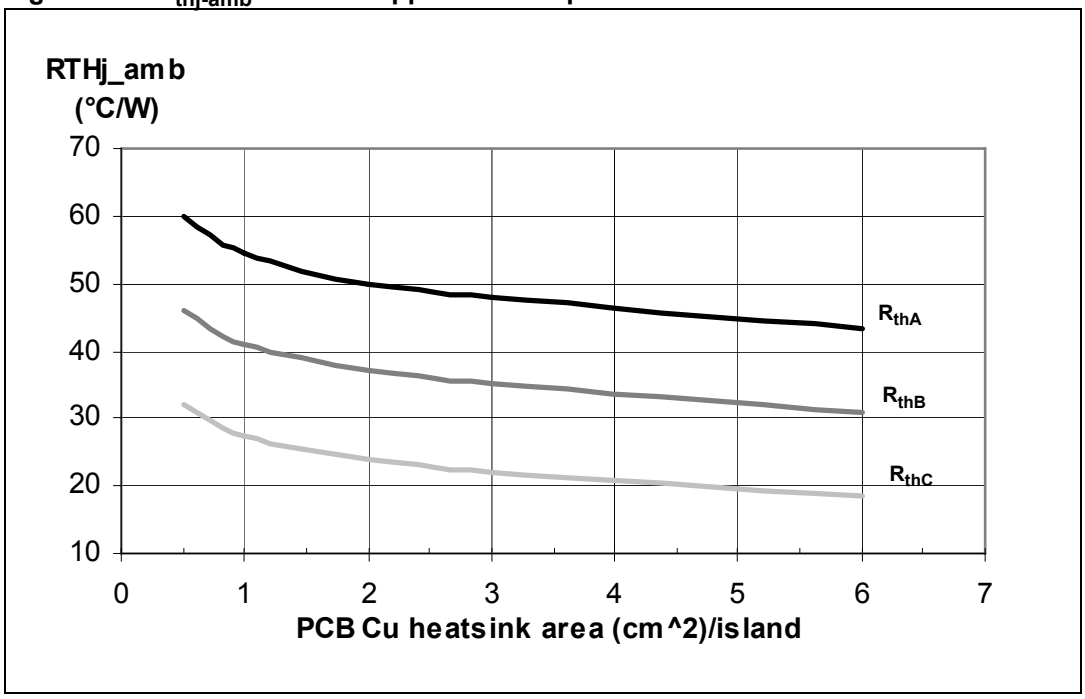
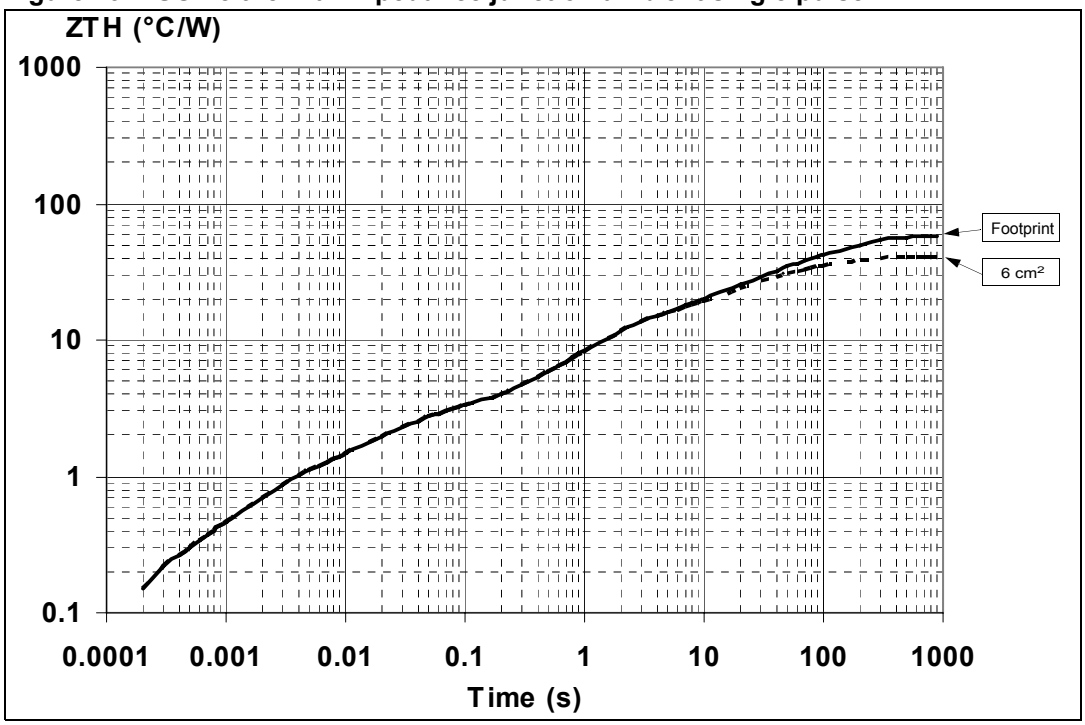


Figure 29. SO-28 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 30. Thermal fitting model of a quad channel HSD in SO-28

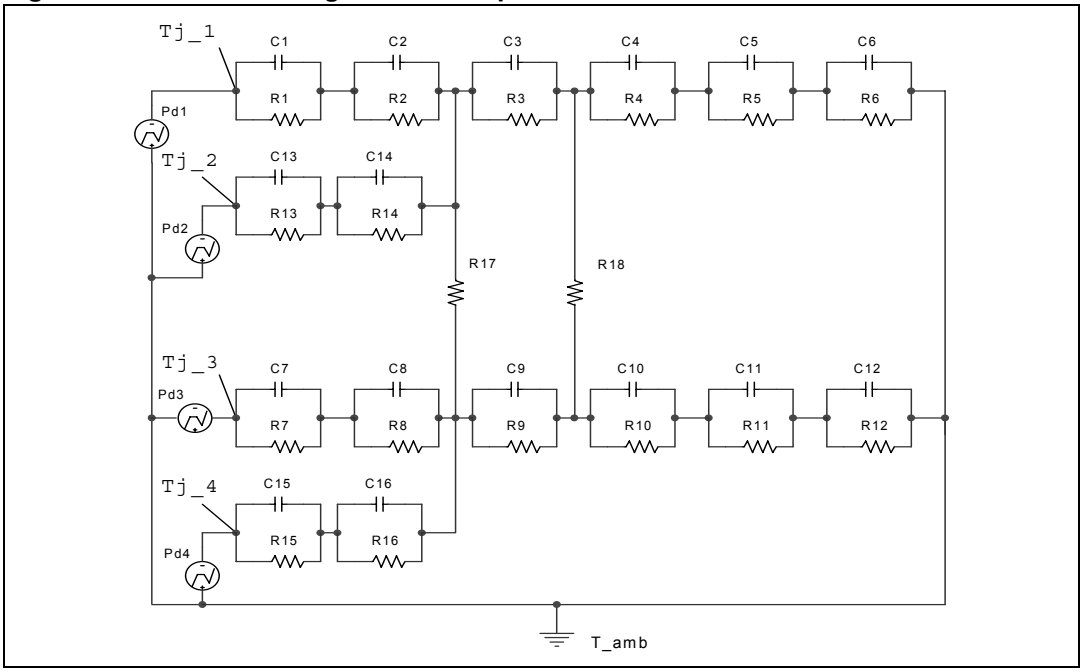


Table 15. Thermal parameters

Area / island (cm^2)	Footprint	6
R1 = R7 = R13 = R15 (°C/W)	0.15	
R2 = R8 = R14 = R16 (°C/W)	0.8	
R3 = R9 (°C/W)	4.5	
R4 = R10 (°C/W)	11	
R5 = R11 (°C/W)	15	
R6 = R12 (°C/W)	5	13
C1 = C7 = C13 = C15 (W.s/°C)	0.0006	
C2 = C8 = C14 = C16 (W.s/°C)	2.10 E-03	
C3 = C9 (W.s/°C)	6 E-03	
C4 = C10 (W.s/°C)	0.2	
C5 = C11 (W.s/°C)	1.5	
C6 = C12 (W.s/°C)	5	8
R17 = R18 (°C/W)	150	

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 31. SO-28 package dimensions

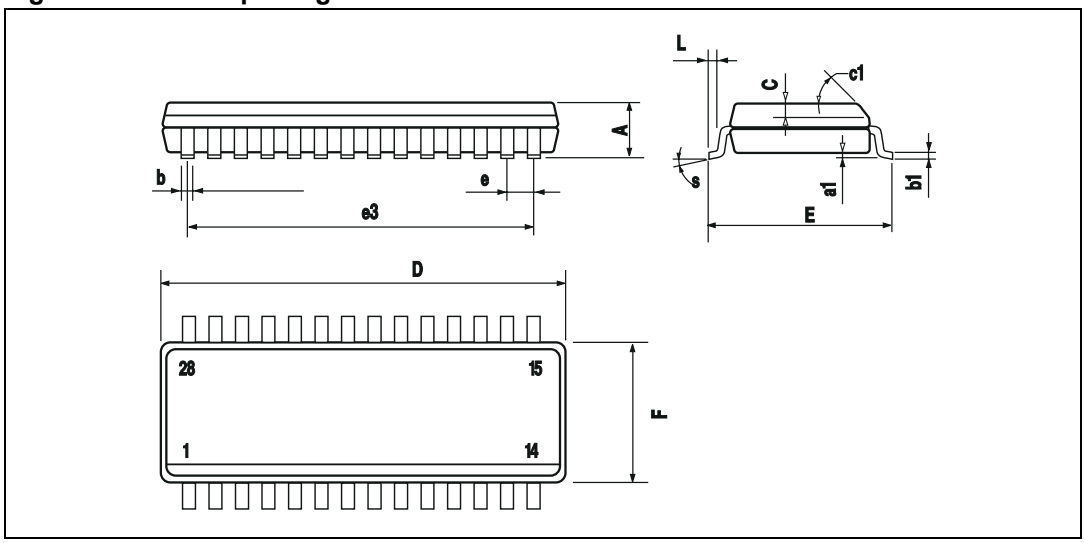
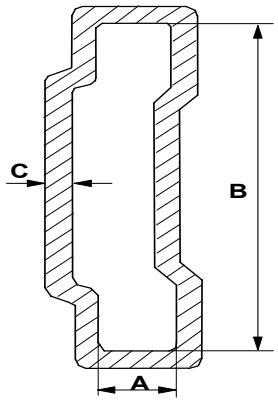


Table 16. SO-28 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.65
a1	0.10		0.30
b	0.35		0.49
b1	0.23		0.32
C		0.50	
c1		45° (typ.)	
D	17.7		18.1
E	10.00		10.65
e		1.27	
e3		16.51	
F	7.40		7.60
L	0.40		1.27
S		8° (max.)	

5.2 SO-28 packing information

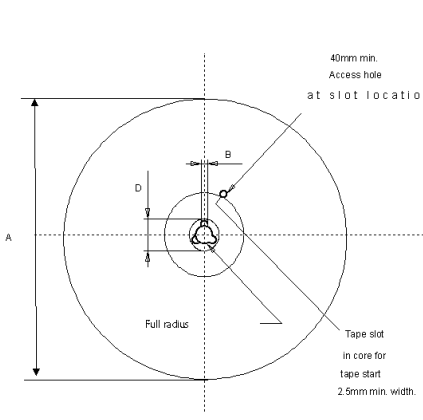
Figure 32. SO-28 tube shipment (no suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 33. SO-28 tape and reel shipment (suffix "TR")



Reel dimensions

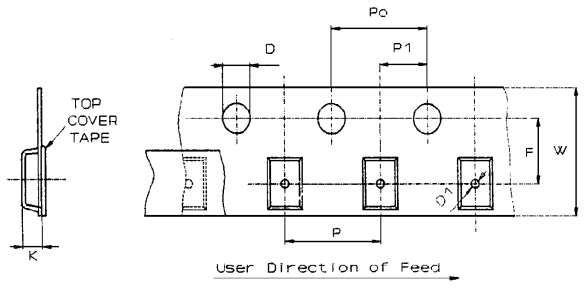
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

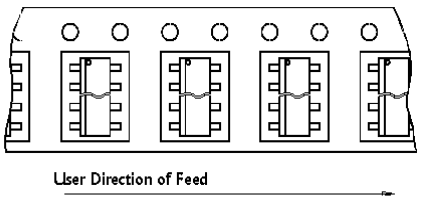
Tape dimensions

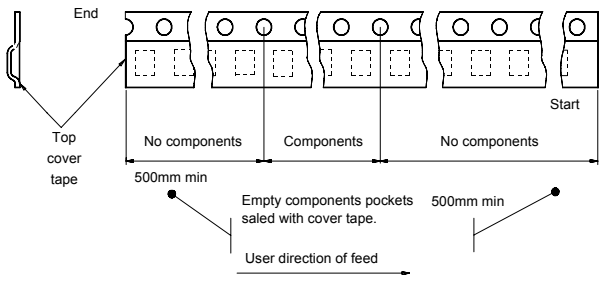
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Revision history

Table 17. Document revision history

Date	Revision	Changes
03-May-2006	1	Initial release.
18-Dec-2008	2	Document reformatted and restructured. Added contents, list of tables and figures. Added *ECOPACK® packages* information.
03-May-2010	3	Changed *Features* list. Replaced VND830P-E to VND830-E.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2010 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com