



Integrated Device Technology, Inc.

## HIGH-SPEED 4K x 8 DUAL-PORT STATIC RAM

IDT7134SA/LA

### FEATURES:

- High-speed access
  - Military: 25/35/45/55/70ns (max.)
  - Commercial: 20/25/35/45/55/70ns (max.)
- Low-power operation
  - IDT7134SA
    - Active: 500mW (typ.)
    - Standby: 5mW (typ.)
  - IDT7134LA
    - Active: 500mW (typ.)
    - Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible; single 5V ( $\pm 10\%$ ) power supply
- Available in several popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) is available, tested to military electrical specifications

### DESCRIPTION:

The IDT7134 is a high-speed 4K x 8 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those

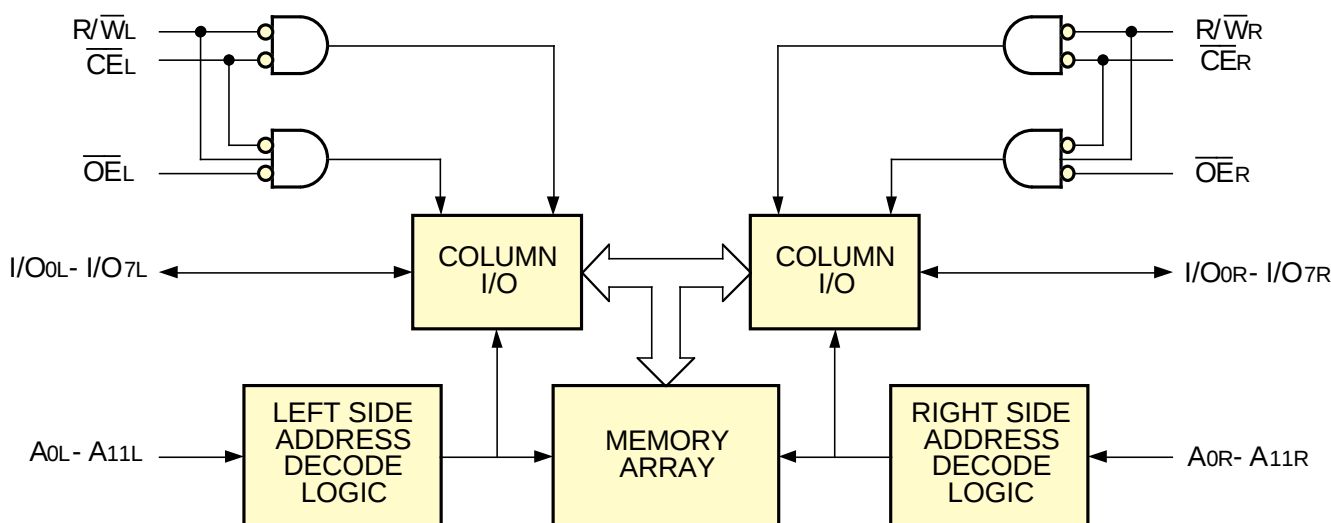
systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same Dual-Port RAM location.

The IDT7134 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by  $\overline{\text{CE}}$ , permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these Dual-Port typically on only 500mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200 $\mu\text{W}$  from a 2V battery.

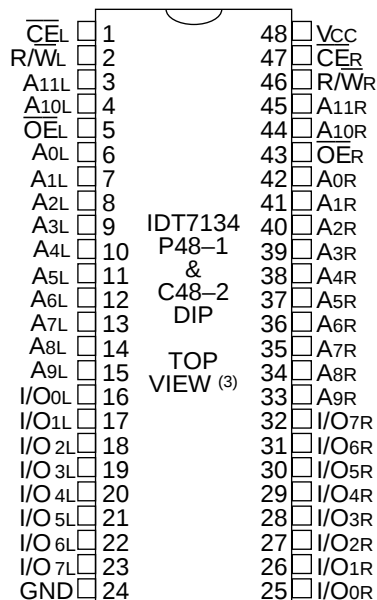
The IDT7134 is packaged on either a sidebrazed or plastic 48-pin DIP, 48-pin LCC, 52-pin PLCC and 48-pin Ceramic Flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

### FUNCTIONAL BLOCK DIAGRAM

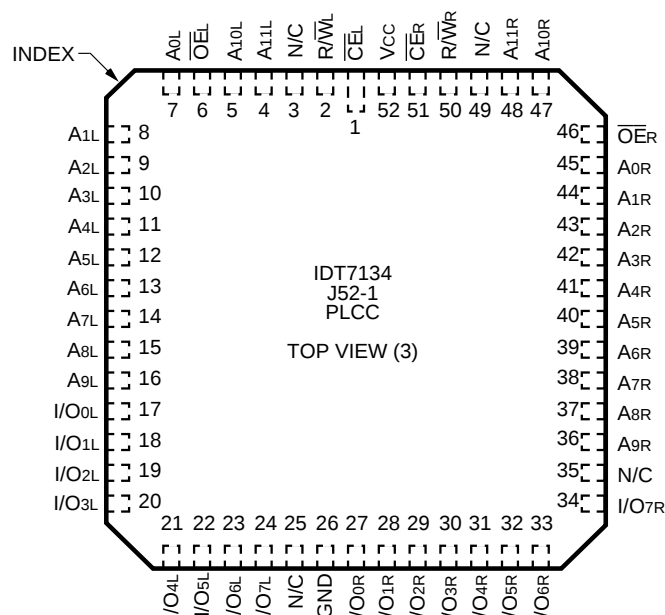


2720 drw 01

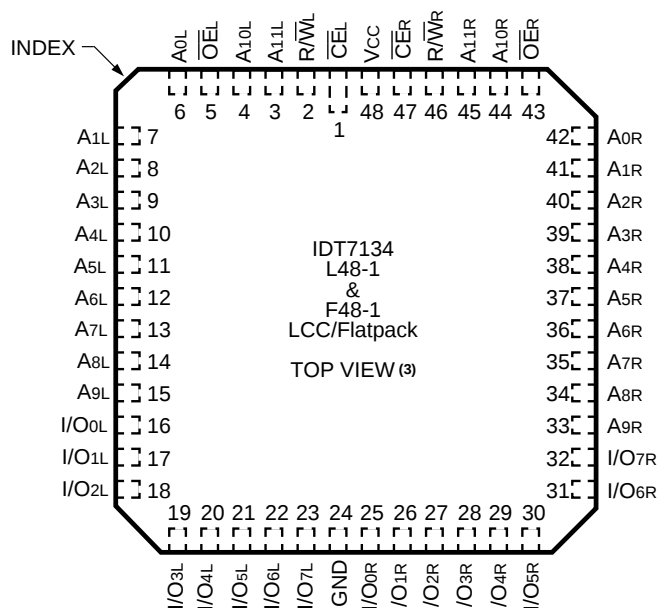
## PIN CONFIGURATIONS<sup>(1,2)</sup>



2720 drw 02



2720 drw 03



2720 drw 04

### NOTES:

1. All V<sub>CC</sub> pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. This text does not indicate orientation of actual part-marking.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol                           | Rating                                  | Com'l.       | Mil.         | Unit |
|----------------------------------|-----------------------------------------|--------------|--------------|------|
| V <sub>TERM</sub> <sup>(2)</sup> | Terminal Voltage with Respect to Ground | -0.5 to +7.0 | -0.5 to +7.0 | V    |
| T <sub>A</sub>                   | Operating Temperature                   | 0 to +70     | -55 to +125  | °C   |
| T <sub>BIAS</sub>                | Temperature Under Bias                  | -55 to +125  | -65 to +135  | °C   |
| T <sub>STG</sub>                 | Storage Temperature                     | -55 to +125  | -65 to +150  | °C   |
| P <sub>T</sub> <sup>(3)</sup>    | Power Dissipation                       | 1.5          | 1.5          | W    |
| I <sub>OUT</sub>                 | DC Output Current                       | 50           | 50           | mA   |

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### NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 0.5V for more than 25% of the cycle time or 10 ns maximum, and is limited to ≤ 20mA for the period of V<sub>TERM</sub> ≥ V<sub>CC</sub> + 0.5V.

## CAPACITANCE<sup>(1)</sup> (T<sub>A</sub> = +25°C, f = 1.0MHz)

| Symbol           | Parameter          | Conditions <sup>(2)</sup> | Max. | Unit |
|------------------|--------------------|---------------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> = 3dv     | 11   | pF   |
| C <sub>OUT</sub> | Output Capacitance | V <sub>OUT</sub> = 3dv    | 11   | pF   |

2720 tbl 02

### NOTES:

1. This parameter is determined by device characterization but is not production tested.
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V and from 3V to 0V.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade      | Ambient Temperature | GND | V <sub>CC</sub> |
|------------|---------------------|-----|-----------------|
| Military   | −55°C to +125°C     | 0V  | 5.0V ± 10%      |
| Commercial | 0°C to +70°C        | 0V  | 5.0V ± 10%      |

2720 tbl 03

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol          | Parameter          | Min.                | Typ. | Max.               | Unit |
|-----------------|--------------------|---------------------|------|--------------------|------|
| V <sub>CC</sub> | Supply Voltage     | 4.5                 | 5.0  | 5.5                | V    |
| GND             | Ground             | 0                   | 0    | 0                  | V    |
| V <sub>IH</sub> | Input High Voltage | 2.2                 | —    | 6.0 <sup>(2)</sup> | V    |
| V <sub>IL</sub> | Input Low Voltage  | −0.5 <sup>(1)</sup> | —    | 0.8                | V    |

### NOTES:

- V<sub>IL</sub> (min.) ≥ −1.5V for pulse width less than 10ns.
- V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 0.5V.

2720 tbl 04

## DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V<sub>CC</sub> = 5V ± 10%)

| Symbol          | Parameter                            | Test Conditions                                                     | IDT7134SA |      | IDT7134LA |      | Unit |
|-----------------|--------------------------------------|---------------------------------------------------------------------|-----------|------|-----------|------|------|
|                 |                                      |                                                                     | Min.      | Max. | Min.      | Max. |      |
| I <sub>LI</sub> | Input Leakage Current <sup>(1)</sup> | V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = 0V to V <sub>CC</sub>     | —         | 10   | —         | 5    | μA   |
| I <sub>LO</sub> | Output Leakage Current               | $\overline{CE} = V_{IH}$ , V <sub>OUT</sub> = 0V to V <sub>CC</sub> | —         | 10   | —         | 5    | μA   |
| V <sub>OL</sub> | Output Low Voltage                   | I <sub>OL</sub> = 6mA                                               | —         | 0.4  | —         | 0.4  | V    |
|                 |                                      | I <sub>OL</sub> = 8mA                                               | —         | 0.5  | —         | 0.5  | V    |
| V <sub>OH</sub> | Output High Voltage                  | I <sub>OH</sub> = −4mA                                              | 2.4       | —    | 2.4       | —    | V    |

### NOTE:

- At V<sub>CC</sub> ≤ 2.0V input leakages are undefined.

2720 tbl 05

## DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE<sup>(1)</sup> (V<sub>CC</sub> = 5.0V ± 10%)

| Symbol           | Parameter                                                  | Test Conditions                                                                                                                                                                                                       | Version  | 7134X20 <sup>(4)</sup> |      | 7134X25             |      | 7134X35             |      | 7134X45             |      | 7134X55             |      | 7134X70             |      | Unit |
|------------------|------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|------------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|------|
|                  |                                                            |                                                                                                                                                                                                                       |          | Typ. <sup>(2)</sup>    | Max. | Typ. <sup>(2)</sup> | Max. | Typ. <sup>(2)</sup> | Max. | Typ. <sup>(2)</sup> | Max. | Typ. <sup>(2)</sup> | Max. | Typ. <sup>(2)</sup> | Max. |      |
| I <sub>CC</sub>  | Dynamic Operating Current<br>(Both Ports Active)           | $\overline{CE} = V_{IL}$<br>Outputs Open<br>f = f <sub>MAX</sub> <sup>(3)</sup>                                                                                                                                       | MIL. S   | —                      | —    | 160                 | 310  | 150                 | 300  | 140                 | 280  | 140                 | 270  | 140                 | 270  | mA   |
|                  |                                                            |                                                                                                                                                                                                                       | L        | —                      | —    | 160                 | 260  | 150                 | 250  | 140                 | 240  | 140                 | 220  | 140                 | 220  |      |
|                  |                                                            |                                                                                                                                                                                                                       | COM'L. S | 170                    | 280  | 160                 | 280  | 150                 | 260  | 140                 | 240  | 140                 | 240  | 140                 | 240  |      |
|                  |                                                            |                                                                                                                                                                                                                       | L        | 170                    | 240  | 160                 | 220  | 150                 | 210  | 140                 | 200  | 140                 | 200  | 140                 | 200  |      |
| I <sub>SB1</sub> | Standby Current<br>(Both Ports—TTL Level Inputs)           | $\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$<br>f = f <sub>MAX</sub> <sup>(3)</sup>                                                                                                                               | MIL. S   | —                      | —    | 25                  | 100  | 25                  | 75   | 25                  | 70   | 25                  | 70   | 25                  | 70   | mA   |
|                  |                                                            |                                                                                                                                                                                                                       | L        | —                      | —    | 25                  | 80   | 25                  | 55   | 25                  | 50   | 25                  | 50   | 25                  | 50   |      |
|                  |                                                            |                                                                                                                                                                                                                       | COM'L. S | 25                     | 110  | 25                  | 80   | 25                  | 75   | 25                  | 70   | 25                  | 70   | 25                  | 70   |      |
|                  |                                                            |                                                                                                                                                                                                                       | L        | 25                     | 80   | 25                  | 50   | 25                  | 45   | 25                  | 40   | 25                  | 40   | 25                  | 40   |      |
| I <sub>SB2</sub> | Standby Current<br>(One Port—TTL Level Inputs)             | $\overline{CE}_{A-} = V_{IL}$ and<br>$\overline{CE}_{B-} = V_{IH}$<br>Active Port Outputs Open, f = f <sub>MAX</sub> <sup>(3)</sup>                                                                                   | MIL. S   | —                      | —    | 95                  | 210  | 85                  | 200  | 75                  | 190  | 75                  | 180  | 75                  | 180  | mA   |
|                  |                                                            |                                                                                                                                                                                                                       | L        | —                      | —    | 95                  | 170  | 85                  | 160  | 75                  | 150  | 75                  | 150  | 75                  | 150  |      |
|                  |                                                            |                                                                                                                                                                                                                       | COM'L. S | 105                    | 180  | 95                  | 180  | 85                  | 170  | 75                  | 160  | 75                  | 160  | 75                  | 160  |      |
|                  |                                                            |                                                                                                                                                                                                                       | L        | 105                    | 150  | 95                  | 140  | 85                  | 130  | 75                  | 130  | 75                  | 130  | 75                  | 130  |      |
| I <sub>SB3</sub> | Full Standby Current<br>(Both Ports—All CMOS Level Inputs) | Both Ports $\overline{CE}_L$ and<br>$\overline{CE}_R \geq V_{CC} - 0.2V$<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or<br>V <sub>IN</sub> ≤ 0.2V, f = 0 <sup>(3)</sup>                                               | MIL. S   | —                      | —    | 1.0                 | 30   | 1.0                 | 30   | 1.0                 | 30   | 1.0                 | 30   | 1.0                 | 30   | mA   |
|                  |                                                            |                                                                                                                                                                                                                       | L        | —                      | —    | 0.2                 | 10   | 0.2                 | 10   | 0.2                 | 10   | 0.2                 | 10   | 0.2                 | 10   |      |
|                  |                                                            |                                                                                                                                                                                                                       | COM'L. S | 1.0                    | 15   | 1.0                 | 15   | 1.0                 | 15   | 1.0                 | 15   | 1.0                 | 15   | 1.0                 | 15   |      |
|                  |                                                            |                                                                                                                                                                                                                       | L        | 0.2                    | 4.5  | 0.2                 | 4.0  | 0.2                 | 4.0  | 0.2                 | 4.0  | 0.2                 | 4.0  | 0.2                 | 4.0  |      |
| I <sub>SB4</sub> | Full Standby Current<br>(One Port—All CMOS Level Inputs)   | One Port $\overline{CE}_{A-}$ or<br>$\overline{CE}_{B-} \geq V_{CC} - 0.2V$<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or<br>V <sub>IN</sub> ≤ 0.2V<br>Active Port Outputs Open, f = f <sub>MAX</sub> <sup>(3)</sup> | MIL. S   | —                      | —    | 95                  | 210  | 85                  | 190  | 75                  | 180  | 75                  | 170  | 75                  | 170  | mA   |
|                  |                                                            |                                                                                                                                                                                                                       | L        | —                      | —    | 95                  | 150  | 85                  | 130  | 75                  | 120  | 75                  | 120  | 75                  | 120  |      |
|                  |                                                            |                                                                                                                                                                                                                       | COM'L. S | 105                    | 170  | 95                  | 170  | 85                  | 160  | 75                  | 150  | 75                  | 150  | 75                  | 150  |      |
|                  |                                                            |                                                                                                                                                                                                                       | L        | 105                    | 130  | 95                  | 120  | 85                  | 110  | 75                  | 100  | 75                  | 100  | 75                  | 100  |      |

### NOTES:

- "X" in part number indicates power rating (SA or LA).
- V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C for typical, and parameters are not production tested.
- f<sub>MAX</sub> = 1/trc = All inputs cycling at f = 1/trc (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby I<sub>SB3</sub>.
- (Commercial only) 0°C to +70°C temperature range.

2720 tbl 06

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

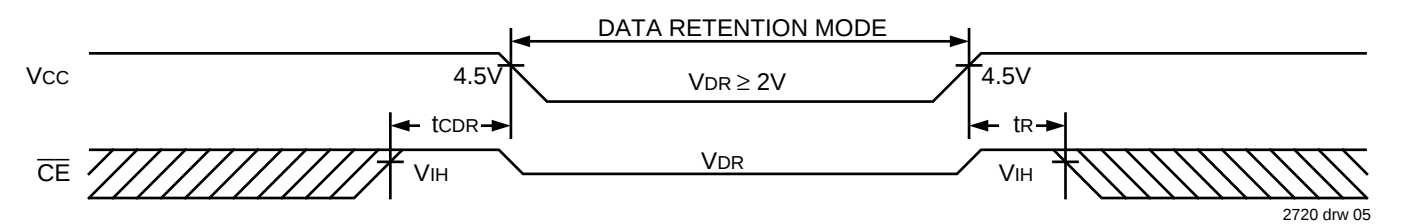
(LA Version Only)  $V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$

| Symbol                          | Parameter                            | Test Condition                                                       | Min.                           | Typ. <sup>(1)</sup> | Max.         | Unit    |
|---------------------------------|--------------------------------------|----------------------------------------------------------------------|--------------------------------|---------------------|--------------|---------|
| VDR                             | VCC for Data Retention               | $V_{CC} = 2V$                                                        | 2.0                            | —                   | —            | V       |
| I <sub>CCDR</sub>               | Data Retention Current               | $\overline{CE} \geq V_{HC}$<br>$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ | MIL. —<br>COM'L. —             | 100                 | 4000<br>1500 | $\mu A$ |
| t <sub>CDR</sub> <sup>(3)</sup> | Chip Deselect to Data Retention Time |                                                                      | 0                              | —                   | —            | ns      |
| t <sub>R</sub> <sup>(3)</sup>   | Operation Recovery Time              |                                                                      | t <sub>RC</sub> <sup>(2)</sup> | —                   | —            | ns      |

- NOTES:**
- $V_{CC} = 2V$ ,  $T_A = +25^{\circ}C$ , and are not production tested.
  - t<sub>RC</sub> = Read Cycle Time.
  - This parameter is guaranteed by device characterization, but not production tested.

2720 tbl 07

DATA RETENTION WAVEFORM

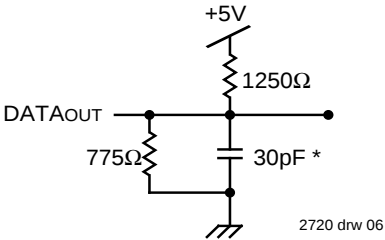


2720 drw 05

AC TEST CONDITIONS

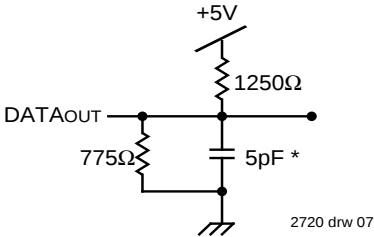
|                               |                 |
|-------------------------------|-----------------|
| Input Pulse Levels            | GND to 3.0V     |
| Input Rise/Fall Times         | 5ns             |
| Input Timing Reference Levels | 1.5V            |
| Output Reference Levels       | 1.5V            |
| Output Load                   | Figures 1 and 2 |

2720 tbl 08



2720 drw 06

Figure 1. AC Output Test Load



2720 drw 07

Figure 2. Output Test Load  
(for tLZ, tHZ, twz, tow)  
\*Including scope and jig

## AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE<sup>(4)</sup>

| Symbol     | Parameter                                      | 7134X20 <sup>(3)</sup> |      | 7134X25 |      | 7134X35 |      | Unit |
|------------|------------------------------------------------|------------------------|------|---------|------|---------|------|------|
|            |                                                | Min.                   | Max. | Min.    | Max. | Min.    | Max. |      |
| READ CYCLE |                                                |                        |      |         |      |         |      |      |
| tRC        | Read Cycle Time                                | 20                     | —    | 25      | —    | 35      | —    | ns   |
| tAA        | Address Access Time                            | —                      | 20   | —       | 25   | —       | 35   | ns   |
| tACE       | Chip Enable Access Time                        | —                      | 20   | —       | 25   | —       | 35   | ns   |
| tAOE       | Output Enable Access Time                      | —                      | 15   | —       | 15   | —       | 20   | ns   |
| tOH        | Output Hold from Address Change                | 0                      | —    | 0       | —    | 0       | —    | ns   |
| tLZ        | Output Low-Z Time <sup>(1, 2)</sup>            | 0                      | —    | 0       | —    | 0       | —    | ns   |
| tHZ        | Output High-Z Time <sup>(1, 2)</sup>           | —                      | 15   | —       | 15   | —       | 20   | ns   |
| tPU        | Chip Enable to Power Up Time <sup>(2)</sup>    | 0                      | —    | 0       | —    | 0       | —    | ns   |
| tPD        | Chip Disable to Power Down Time <sup>(2)</sup> | —                      | 20   | —       | 25   | —       | 35   | ns   |

## AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE<sup>(4)</sup> (CONT'D)

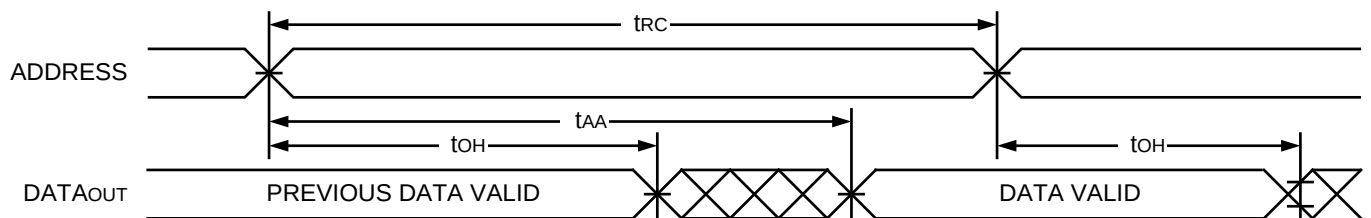
| Symbol     | Parameter                                      | 7134X45 |      | 7134X55 |      | 7134X70 |      | Unit |
|------------|------------------------------------------------|---------|------|---------|------|---------|------|------|
|            |                                                | Min.    | Max. | Min.    | Max. | Min.    | Max. |      |
| READ CYCLE |                                                |         |      |         |      |         |      |      |
| tRC        | Read Cycle Time                                | 45      | —    | 55      | —    | 70      | —    | ns   |
| tAA        | Address Access Time                            | —       | 45   | —       | 55   | —       | 70   | ns   |
| tACE       | Chip Enable Access Time                        | —       | 45   | —       | 55   | —       | 70   | ns   |
| tAOE       | Output Enable Access Time                      | —       | 25   | —       | 30   | —       | 40   | ns   |
| tOH        | Output Hold from Address Change                | 0       | —    | 0       | —    | 0       | —    | ns   |
| tLZ        | Output Low-Z Time <sup>(1, 2)</sup>            | 5       | —    | 5       | —    | 5       | —    | ns   |
| tHZ        | Output High-Z Time <sup>(1, 2)</sup>           | —       | 20   | —       | 25   | —       | 30   | ns   |
| tPU        | Chip Enable to Power Up Time <sup>(2)</sup>    | 0       | —    | 0       | —    | 0       | —    | ns   |
| tPD        | Chip Disable to Power Down Time <sup>(2)</sup> | —       | 45   | —       | 50   | —       | 50   | ns   |

### NOTES:

1. Transition is measured  $\pm 500\text{mV}$  from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. (Commercial only) 0°C to +70°C temperature range only.
4. "X" in part number indicates power rating (SA or LA).

2720 tbl 09

## TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE<sup>(1, 2, 3)</sup>

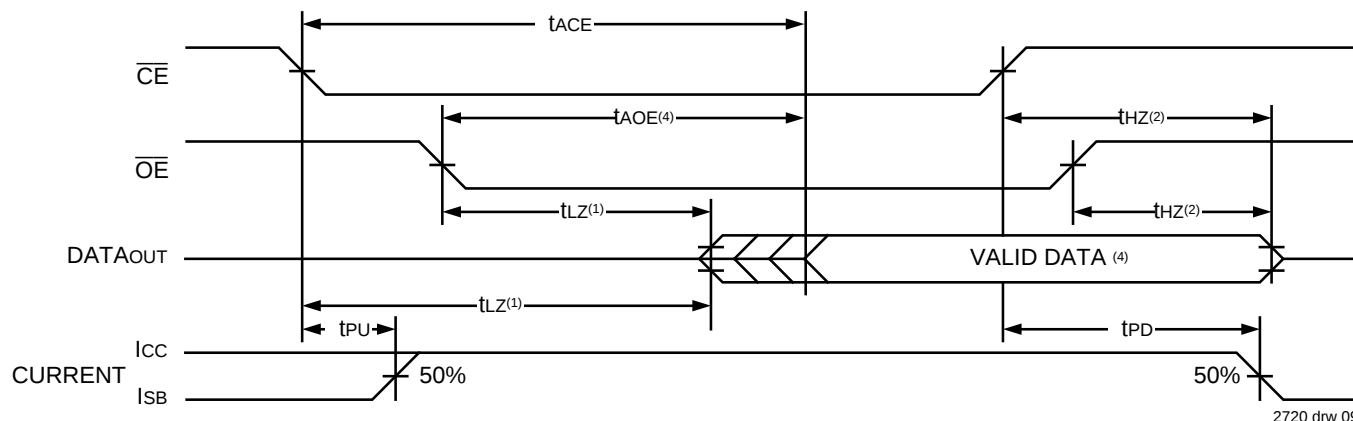


2720 drw 08

### NOTES:

1. Timing depends on which signal is asserted last,  $\overline{\text{OE}}$  or  $\overline{\text{CE}}$ .
2. Timing depends on which signal is de-asserted first,  $\overline{\text{OE}}$  or  $\overline{\text{CE}}$ .
3.  $R/\overline{W} = V_{IH}$ .

## TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE<sup>(1, 3)</sup>



### NOTES:

1. Timing depends on which signal is asserted last,  $\overline{OE}$  or  $\overline{CE}$ .
2. Timing depends on which signal is de-asserted first,  $\overline{OE}$  or  $\overline{CE}$ .
3.  $R/\overline{W} = V_{IH}$ .
4. Start of valid data depends on which timing becomes effective,  $t_{AOE}$ ,  $t_{ACE}$  or  $t_{AA}$ .
5.  $t_{AA}$  for RAM Address Access and  $t_{SAA}$  for Semaphore Address Access.

## AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE<sup>(6)</sup>

| Symbol      | Parameter                                             | 7134X20 <sup>(5)</sup> |      | 7134X25 |      | 7134X35 |      | Unit |
|-------------|-------------------------------------------------------|------------------------|------|---------|------|---------|------|------|
|             |                                                       | Min.                   | Max. | Min.    | Max. | Min.    | Max. |      |
| WRITE CYCLE |                                                       |                        |      |         |      |         |      |      |
| tWC         | Write Cycle Time                                      | 20                     | —    | 25      | —    | 35      | —    | ns   |
| tEW         | Chip Enable to End-of-Write                           | 15                     | —    | 20      | —    | 30      | —    | ns   |
| tAW         | Address Valid to End-of-Write                         | 15                     | —    | 20      | —    | 30      | —    | ns   |
| tAS         | Address Set-up Time                                   | 0                      | —    | 0       | —    | 0       | —    | ns   |
| tWP         | Write Pulse Width                                     | 15                     | —    | 20      | —    | 25      | —    | ns   |
| tWR         | Write RecoveryTime                                    | 0                      | —    | 0       | —    | 0       | —    | ns   |
| tdW         | Data Valid to End-of-Write                            | 15                     | —    | 15      | —    | 20      | —    | ns   |
| tHZ         | Output High-Z Time <sup>(1, 2)</sup>                  | —                      | 15   | —       | 15   | —       | 20   | ns   |
| tdH         | Data Hold Time <sup>(3)</sup>                         | 0                      | —    | 0       | —    | 3       | —    | ns   |
| twZ         | Write Enabled to Output in High-Z <sup>(1, 2)</sup>   | —                      | 15   | —       | 15   | —       | 20   | ns   |
| tOW         | Output Active from End-of-Write <sup>(1, 2, 3)</sup>  | 3                      | —    | 3       | —    | 3       | —    | ns   |
| twDD        | Write Pulse to Data Delay <sup>(4)</sup>              | —                      | 40   | —       | 50   | —       | 60   | ns   |
| tDDD        | Write Data Valid to Read Data Delay <sup>(4, 7)</sup> | —                      | 30   | —       | 30   | —       | 35   | ns   |

### NOTES:

1. Transition is measured  $\pm 500\text{mV}$  from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for  $t_{DH}$  must be met by the device supplying write data to the RAM under all operating conditions. Although  $t_{DH}$  and  $t_{OW}$  values will vary over voltage and temperature, the actual  $t_{DH}$  will always be smaller than the actual  $t_{OW}$ .
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
5. (Commercial only),  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  temperature range.
6. "X" in part number indicates power rating (SA or LA).
7.  $t_{DDD} = 35\text{ns}$  for military temperature range.

2720 tbl 10

## AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE<sup>(6)</sup> (CONT'D)

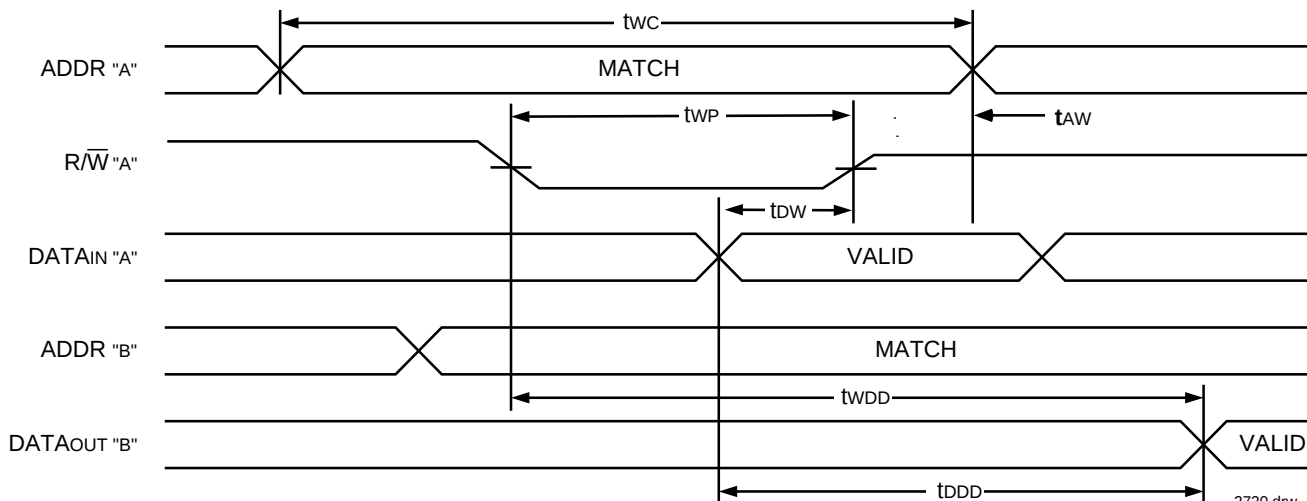
| Symbol      | Parameter                                            | 7134X45 |      | 7134X55 |      | 7134X70 |      | Unit |
|-------------|------------------------------------------------------|---------|------|---------|------|---------|------|------|
|             |                                                      | Min.    | Max. | Min.    | Max. | Min.    | Max. |      |
| WRITE CYCLE |                                                      |         |      |         |      |         |      |      |
| tWC         | Write Cycle Time                                     | 45      | —    | 55      | —    | 70      | —    | ns   |
| tEW         | Chip Enable to End-of-Write                          | 40      | —    | 50      | —    | 60      | —    | ns   |
| tAW         | Address Valid to End-of-Write                        | 40      | —    | 50      | —    | 60      | —    | ns   |
| tAS         | Address Set-up Time                                  | 0       | —    | 0       | —    | 0       | —    | ns   |
| tWP         | Write Pulse Width                                    | 40      | —    | 50      | —    | 60      | —    | ns   |
| tWR         | Write RecoveryTime                                   | 0       | —    | 0       | —    | 0       | —    | ns   |
| tdW         | Data Valid to End-of-Write                           | 20      | —    | 25      | —    | 30      | —    | ns   |
| thZ         | Output High-Z Time <sup>(1, 2)</sup>                 | —       | 20   | —       | 25   | —       | 30   | ns   |
| tdH         | Data Hold Time <sup>(3)</sup>                        | 3       | —    | 3       | —    | 3       | —    | ns   |
| twZ         | Write Enabled to Output in High-Z <sup>(1, 2)</sup>  | —       | 20   | —       | 25   | —       | 30   | ns   |
| tOW         | Output Active from End-of-Write <sup>(1, 2, 3)</sup> | 3       | —    | 3       | —    | 3       | —    | ns   |
| twDD        | Write Pulse to Data Delay <sup>(4)</sup>             | —       | 70   | —       | 80   | —       | 90   | ns   |
| tDDD        | Write Data Valid to Read Data Delay <sup>(4)</sup>   | —       | 45   | —       | 55   | —       | 70   | ns   |

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### NOTES:

1. Transition is measured  $\pm 500\text{mV}$  from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t<sub>DH</sub> must be met by the device supplying write data to the RAM under all operating conditions. Although t<sub>DH</sub> and t<sub>OW</sub> values will vary over voltage and temperature, the actual t<sub>DH</sub> will always be smaller than the actual t<sub>OW</sub>.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
5. (Commercial only), 0°C to +70°C temperature range.
6. "X" in part number indicates power rating (SA or LA).

## TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ<sup>(1)</sup>

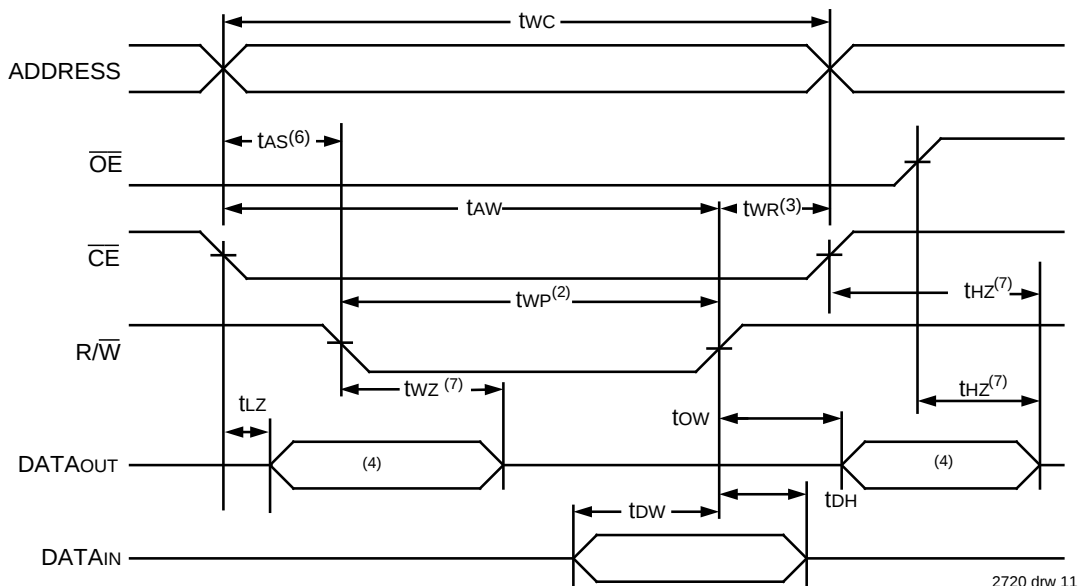


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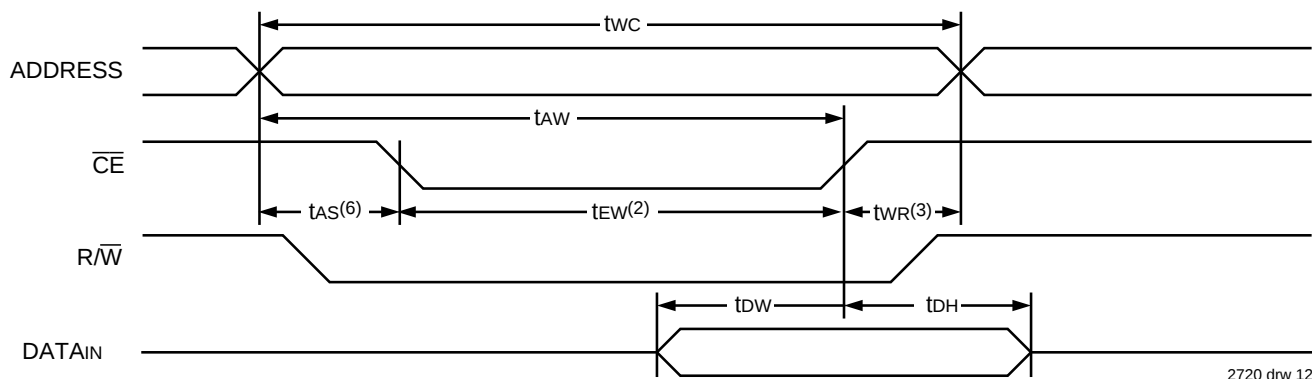
### NOTES:

1. Write cycle parameters should be adhered to, in order to ensure proper writing.
2.  $\overline{\text{CE}}_{\text{L}} = \overline{\text{CE}}_{\text{R}} = \text{V}_{\text{IL}}$ .  $\overline{\text{OE}}_{\text{B}} = \text{V}_{\text{IL}}$ .
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

## TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{R/\overline{W}}$ CONTROLLED TIMING<sup>(1, 5, 8)</sup>



## TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING<sup>(1, 5)</sup>



### NOTES:

1.  $\overline{R/\overline{W}}$  or  $\overline{CE}$  must be High during all address transitions.
2. A write occurs during the overlap ( $t_{EW}$  or  $t_{WP}$ ) of a  $\overline{CE} = V_{IL}$  and  $\overline{R/\overline{W}} = V_{IL}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{R/\overline{W}}$  going High to the end-of-write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE}$  Low transition occurs simultaneously with or after the  $\overline{R/\overline{W}}$  Low transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ( $\overline{CE}$  or  $\overline{R/\overline{W}}$ ) is asserted last.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured  $\pm 500\text{mV}$  from steady state with the Output Test Load (Figure 2).
8. If  $\overline{OE}$  is Low during a  $\overline{R/\overline{W}}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or ( $t_{WZ} + t_{OW}$ ) to allow the I/O drivers to turn off data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE}$  is High during an  $\overline{R/\overline{W}}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

FUNCTIONAL DESCRIPTION

The IDT7134 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by  $\overline{CE}$ . The  $\overline{CE}$  controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ( $\overline{CE}$  high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ( $\overline{OE}$ ). In the read mode, the port's  $\overline{OE}$  turns on the output drivers when set LOW. Non-contention READ/ WRITE conditions are illustrated in the table below.

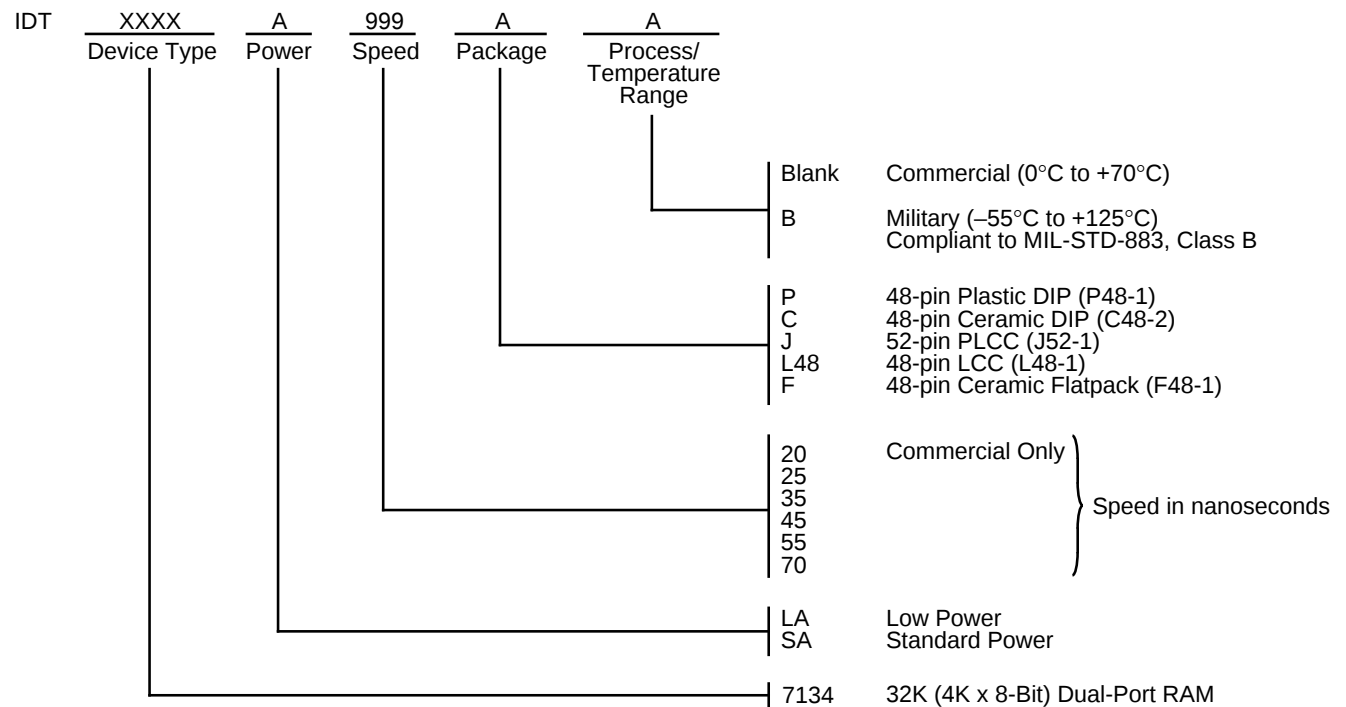
TRUTH TABLE I – READ/WRITE CONTROL<sup>(2)</sup>

| Left or Right Port <sup>(1)</sup> |                 |                 |         | Function                                                                |
|-----------------------------------|-----------------|-----------------|---------|-------------------------------------------------------------------------|
| R/W                               | $\overline{CE}$ | $\overline{OE}$ | D0-7    |                                                                         |
| X                                 | H               | X               | Z       | Port Disabled and in Power Down Mode, IsB2 or IsB4                      |
| X                                 | H               | X               | Z       | $\overline{CE_R} = \overline{CE_L} = H$ , Power Down Mode, IsB1 or IsB3 |
| L                                 | L               | X               | DATAin  | Data on port written into memory                                        |
| H                                 | L               | L               | DATAout | Data in memory output on port                                           |
| X                                 | X               | H               | Z       | High impedance outputs                                                  |

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- NOTES:
- AOL - A11L ≠ AOR - A11R
  - "H" = HIGH, "L" = LOW, "X" = Don't Care, and "Z" = High-impedance

ORDERING INFORMATION



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