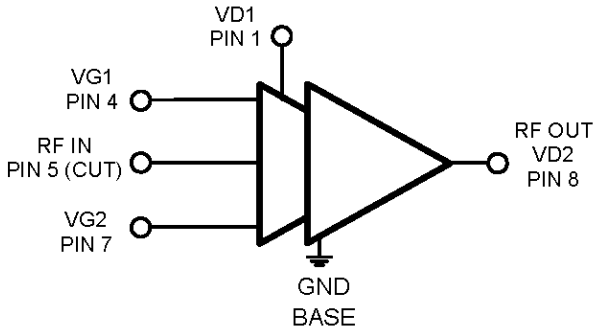
RFHA1021U

60W GaN Wide-Band Pulsed Power Amplifier



Package: Flanged Ceramic, 8 pin

The RFHA1021U is a 50V 60W high power amplifier designed for S-Band pulsed radar, air traffic control and surveillance and general purpose broadband amplifiers applications. Using an advanced high power density gallium nitride (GaN) semiconductor process, these high performance amplifiers achieve high output power, high efficiency and flat gain over a broad frequency range in a single package. The RFHA1021U is an input matched power GaN transistor with 26dB small signal gain packaged in a ceramic package. The package provides excellent thermal stability through the use of advanced heat sink and power dissipation technologies. Ease of integration is accomplished through the incorporation of single, optimized matching networks that provide wideband gain and power performance in a single amplifier.



Functional Block Diagram

Features

- Wideband Operation: 3.1GHz to 3.5GHz
- Advanced GaN HEMT Technology
- Input Optimized Evaluation Board Layout for 50Ω Operation
- Integrated Matching Components for High Terminal Impedances at Input
- 50V Operation Typical Performance
  - Output Pulsed Power 60W
  - Pulse Width 100µs, Duty Cycle 10%
  - Small Signal Gain 26dB
  - High Efficiency 49%
  - -40°C to 85°C Operation

Applications

- Radar
- Air Traffic Control and Surveillance
- General Purpose Broadband Amplifiers

Ordering Information

RFHA1021US2	Sample bag with 2 pieces
RFHA1021USB	Bag with 5 pieces
RFHA1021USQ	Bag with 25 pieces
RFHA1021USR	7” Short reel with 50 pieces
RFHA1021UTR13	13” Reel with 250 pieces
RFHA1021UPCBA-410	Fully Assembled Evaluation Board Optimized for 3.1-3.5GHz; 50V

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

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Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Voltage Output Stage (V_{D2})	150	V
Drain Voltage Input Stage (V_{D1})	54	V
Gate Voltage (V_G)	-6 to 2	V
Operating Voltage	50	V
Ruggedness (VSWR)	10:1	
Storage Temperature Range	-55 to +125	°C
Operating Temperature Range (T_C)	-40 to +85	°C
Operating Junction Temperature (T_J)	250	°C
Human Body Model	Class 1A	
MTTF (T_J < 200°C, 95% Confidence Limits)*	3E + 06	Hours
Thermal Resistance, R_{TH} (Junction to Case) Output Stage		
T_C =85°C, DC Bias Only	2.6**	°C/W
T_C =85°C, 100µs Pulse, 10% Duty Cycle	0.5**	

Caution! ESD sensitive device.

RoHS (Restriction of Hazardous Substances): Compliant per EU Directive 2011/65/EU.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

* MTTF – median time to failure for wear-out failure mode (30% I_{DSS} degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT(random) failure rate.

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table above.

Bias Conditions should also satisfy the following expression: $P_{DISS} < (T_J - TC) / R_{TH\ J\text{-}C}$ and $T_C = T_{CASE}$

** R_{TH} data estimates from RF3932 (equivalent output die size)

Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Recommended Operating Conditions					
Drain Voltage (V_{DSQ})		50		V	
Gate Voltage (V_{GSQ})	-5	-3	-2	V	
Drain Bias Current		264		mA	Stage 1 = 44mA, Stage 2 = 220mA
Frequency of Operation	3100		3500	MHz	
DC Functional Test					
V_{GSQ} Stage 1		-3.1		V	V_D = 50V, I_D Stage 1 = 42mA
V_{GSQ} Stage 2		-3.3		V	V_D = 50V, I_D Stage 2 = 220mA
$V_{DS(ON)}$ – Stage 2		0.45		V	V_G = 0V, I_D = 1.0A, Wafer level test

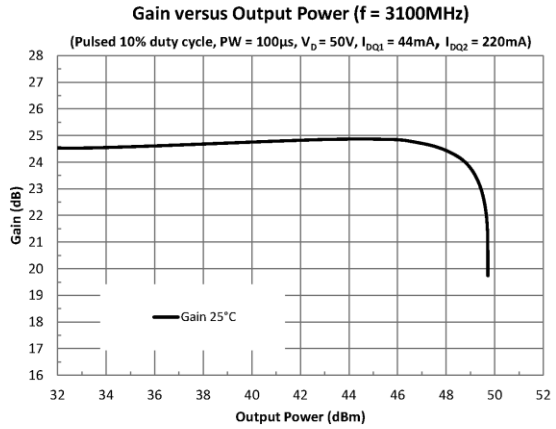
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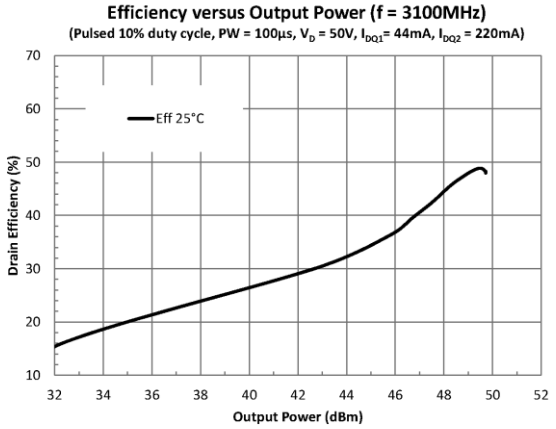
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
RF Functional Test					
Input Return Loss		-13.5	-6.2	dB	f = 3.1GHz, P_{IN} = 25dBm [1,2]
Output Power	47.5	48.45		dBm	
Efficiency	40	42.0		%	
Input Return Loss		-13.5	-6.2	dB	f = 3.5GHz, P_{IN} = 28dBm [1,2]
Output Power	47.5	48.45		dBm	
Efficiency	40	42.0		%	
RF Typical Performance					
Small Signal Gain		26		dB	f = 3.3GHz, P_{IN} = 0dBm [1,2]
Gain Variation with Temperature			TBD	dB/°C	At peak output power [1,2]
Output Power (P_{SAT})		48.45		dBm	f = 3.5GHz [1,2]
		70		W	
Drain Efficiency		50		%	At peak output power (P3dB, 3500MHz) [1,2]
Power Gain		24.5		dB	f = 3.1GHz, P_{OUT} = 60W [1,2]
Efficiency		43		%	
Input Return Loss		-7.2	-6.2	dB	
Power Gain		23.1		dB	f = 3.5GHz, P_{OUT} = 60W [1,2]
Efficiency		49		%	
Input Return Loss		-10.7	-6.2	dB	

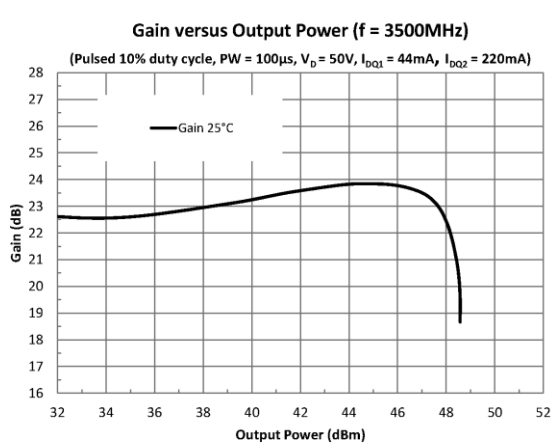
[1] Test Conditions: PW = 100µs, DC = 10%, V_{DSQ} = 50V, I_{DQ} = 264mA, T = 25ºC.
[2] Performance in a standard tuned test fixture.

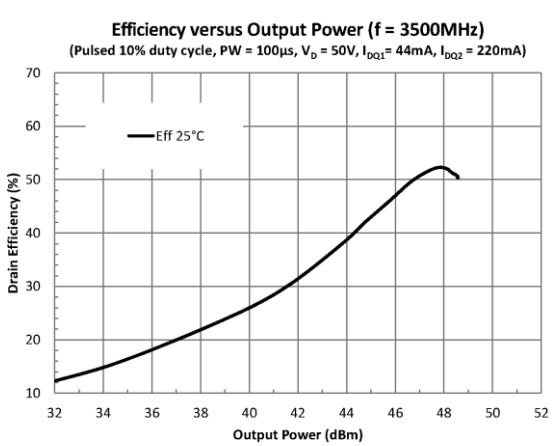
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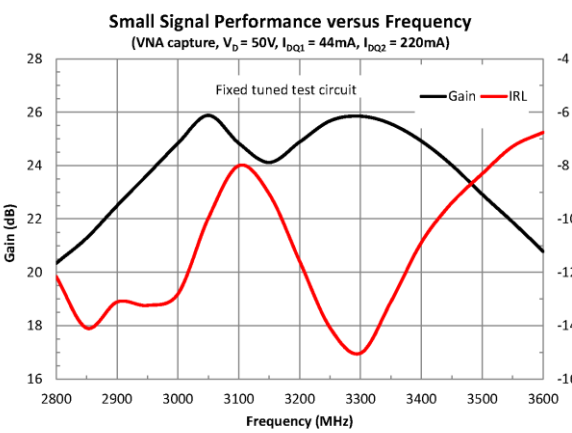
Typical Performance in Standard Fixed Tuned Test Fixture: (T = 25°C unless noted)

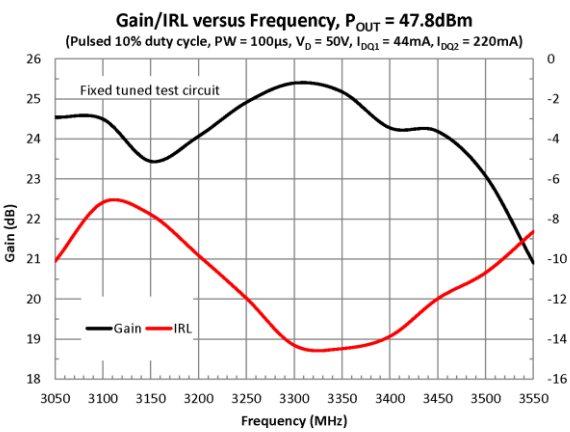






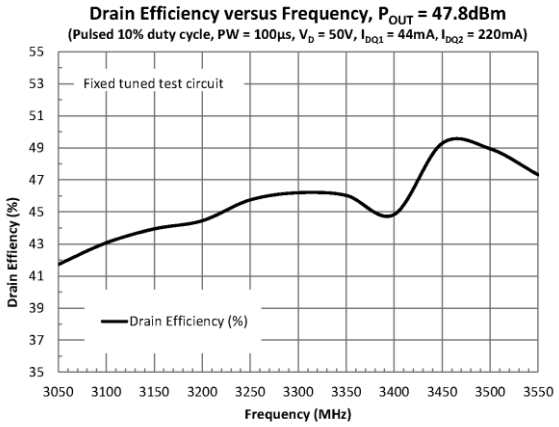


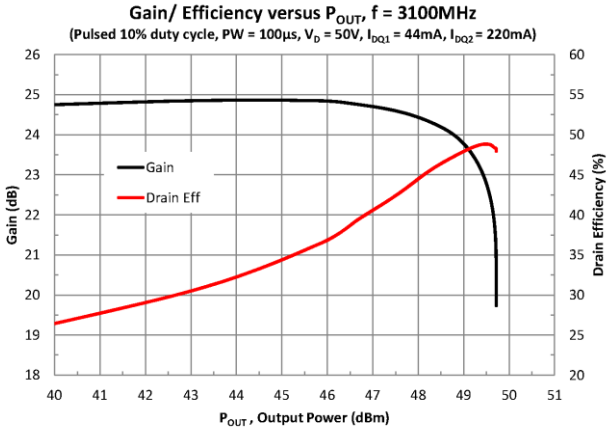


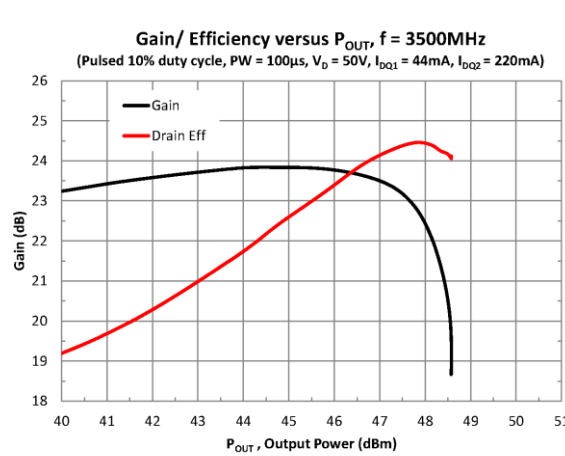


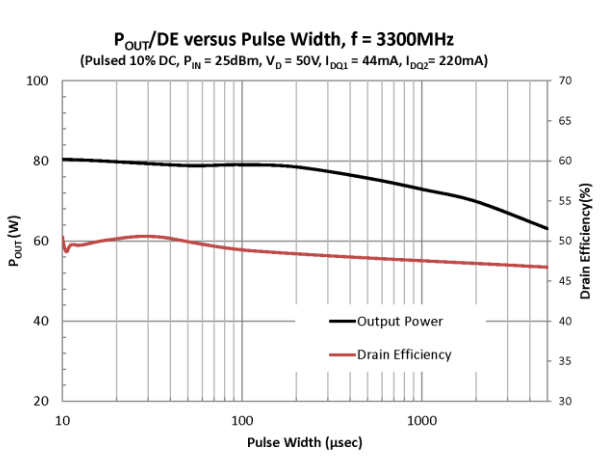
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Typical Performance in Standard Fixed Tuned Test Fixture: (T = 25°C unless noted) (continued)



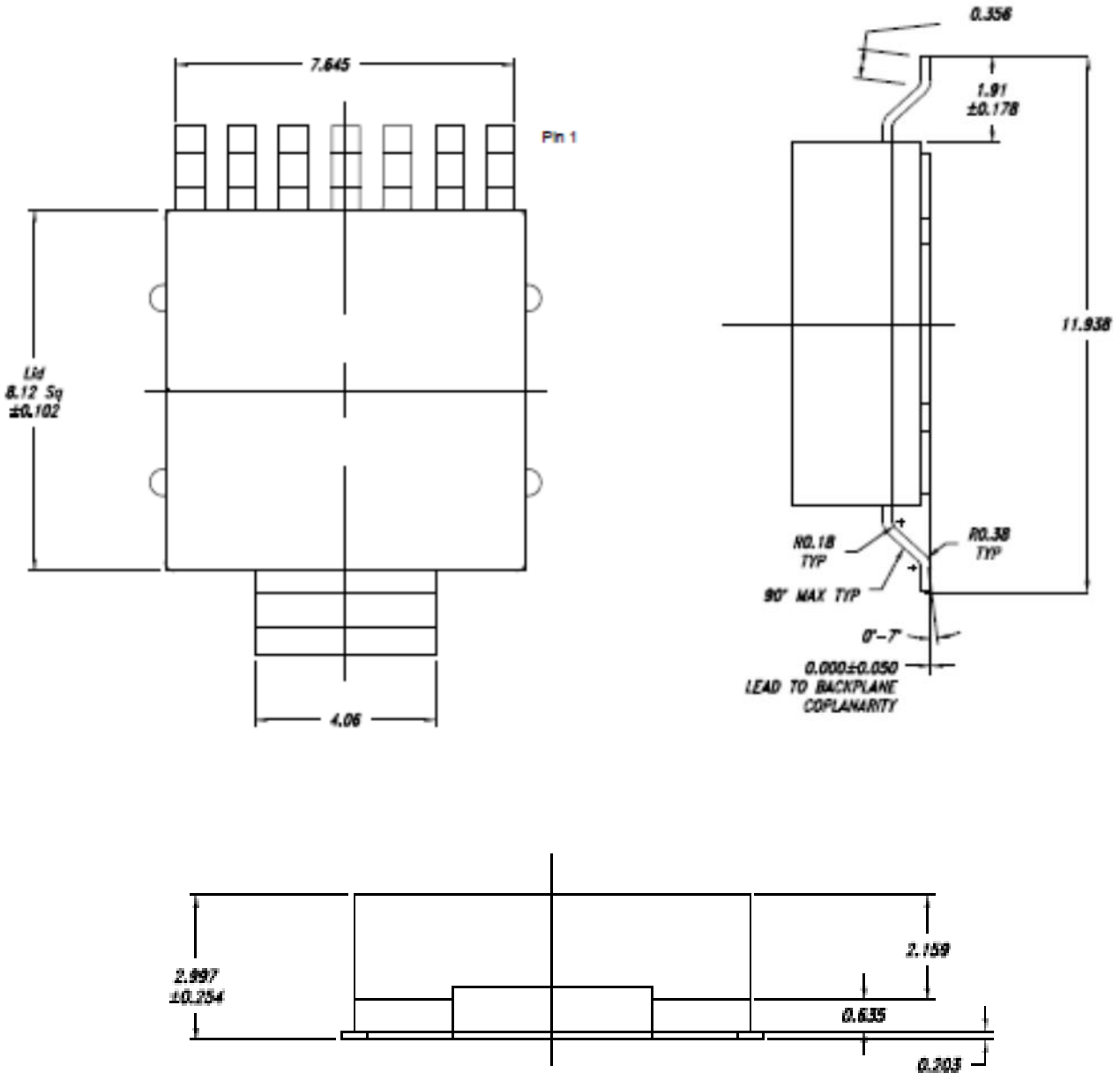






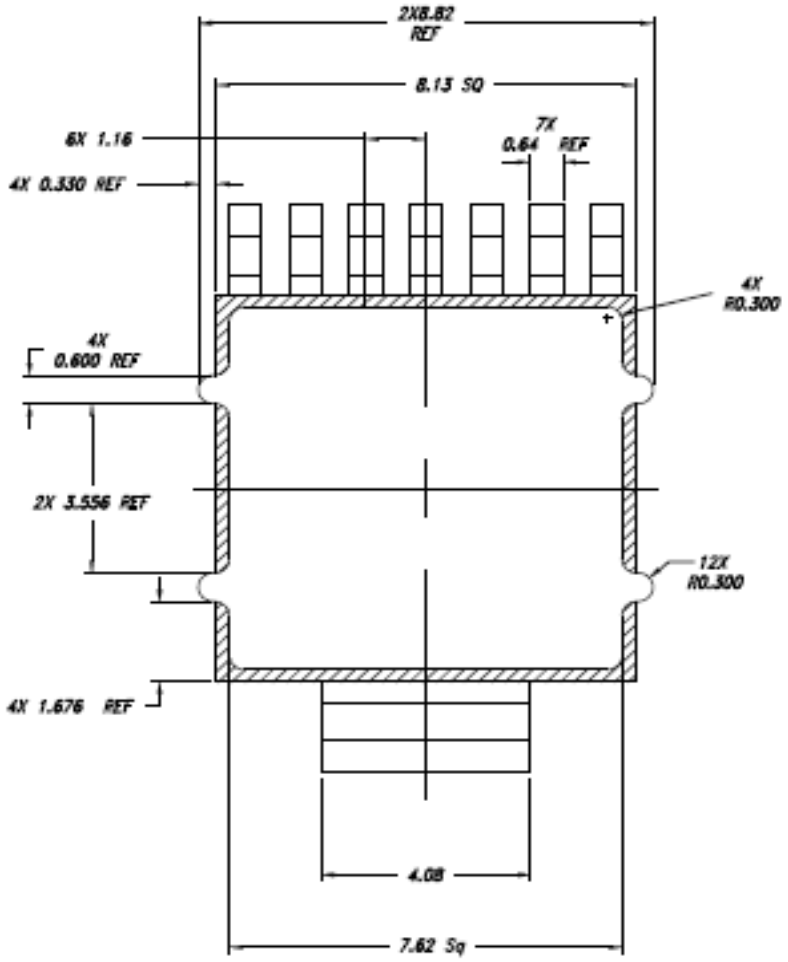
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Package Drawing (Dimensions in millimeters [+/- 0.127])



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Package Drawing (Dimensions in millimeters [+/- 0.127]) (continued)



Pin Names and Descriptions

Pin	Name	Description
1	DRAIN 1	DC Drain Feed Input Stage
2	NC	No Connect
3	NC	No Connect
4	GATE 1	DC Gate Feed Input Stage
5	RF IN	RF in input Stage
6	NC	No Connect
7	GATE 2	DC Gate Feed Output Stage
8	DRAIN 2	V_{DQ2} RF Output
9	SOURCE	Source – Ground Base

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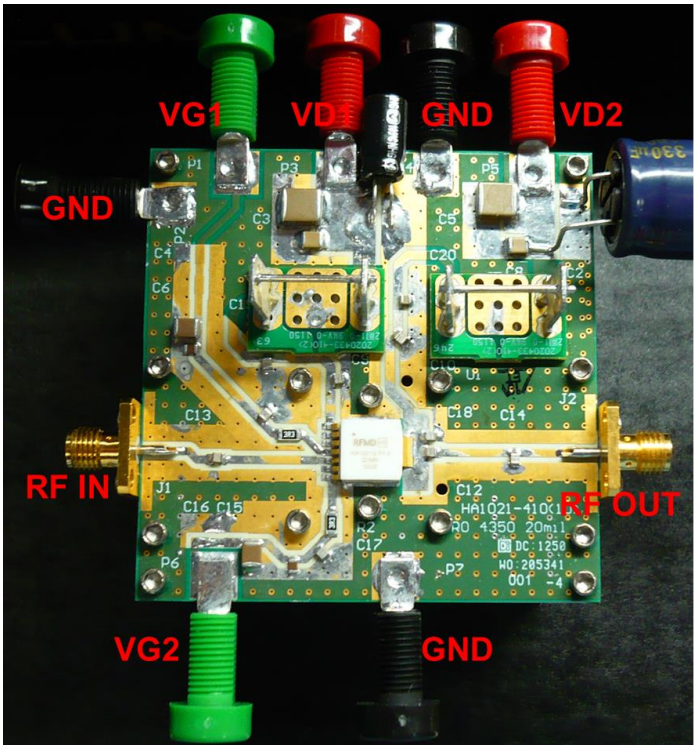
Bias Instruction for RFHA1021U 3.1GHz to 3.5GHz Evaluation Board

ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board.
Evaluation board requires additional external fan cooling.
Connect all supplies before powering evaluation board.

1. Connect RF cables at RFIN and RFOUT.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -5V to VG1 and VG2.
4. Apply 50V to VD1 and VD2.
5. Increase VG1 until drain current for VD1 reaches 44mA or desired bias point.
6. Increase VG2 until drain current for VD2 reaches 220mA or desired bias point.
7. Turn on the RF input.

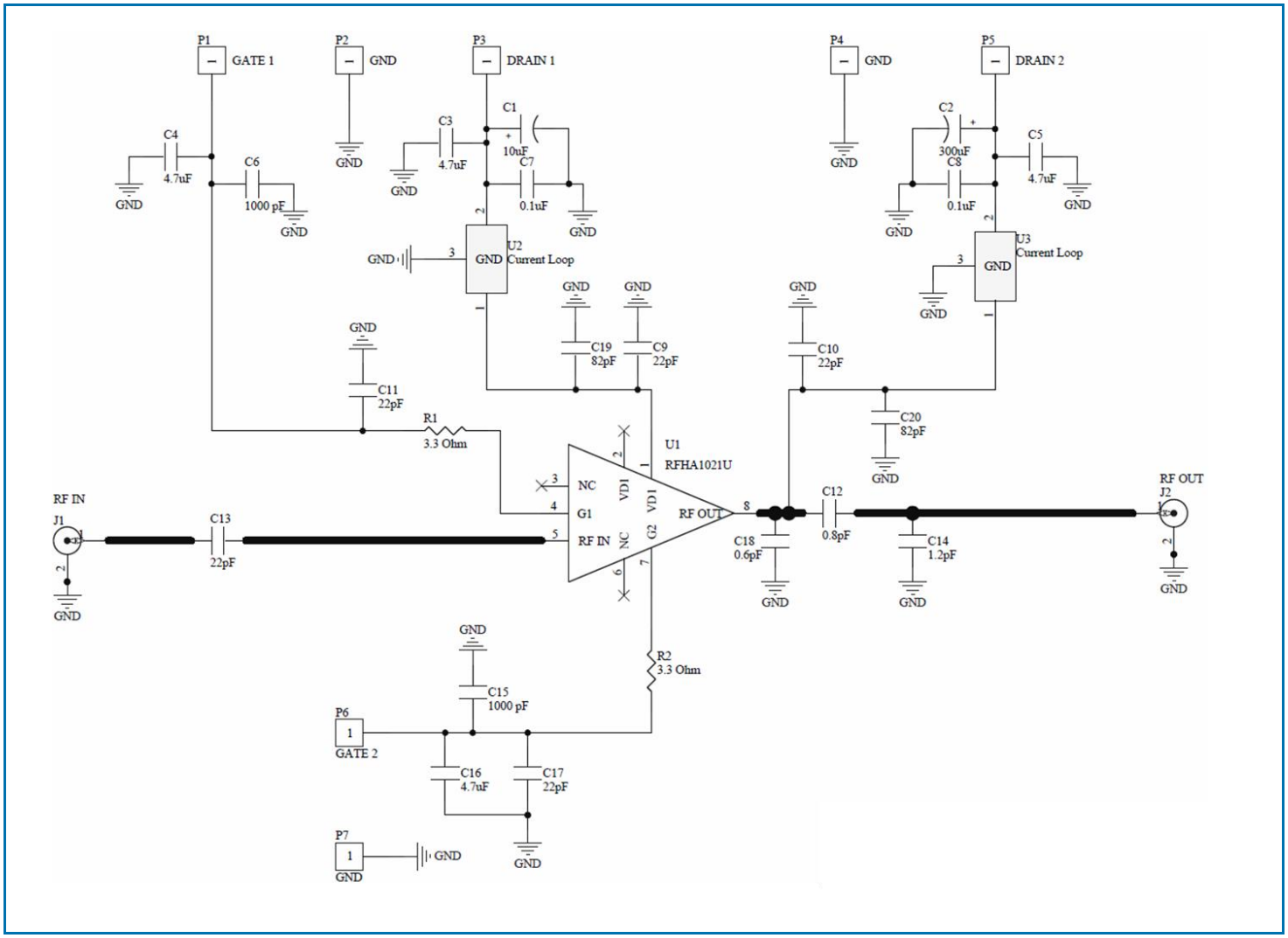
IMPORTANT NOTE: Depletion mode device - when biasing the device V_G must be applied BEFORE V_D. When removing bias V_D must be removed BEFORE V_G is removed. Failure to follow sequencing will cause the device to fail.

Note: For optimal RF performance, consistent and optimal heat removal from the base of the package is required. A thin layer of thermal grease should be applied to the interface between the base of the package and the equipment chassis. It is recommended a small amount of thermal grease is applied to the underside of the device package. Even application and removal of excess thermal grease can be achieved by spreading the thermal grease using a razor blade. The package should then be bolted to the chassis and input and output leads soldered to the circuit board.



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Proposed Evaluation Board Schematic



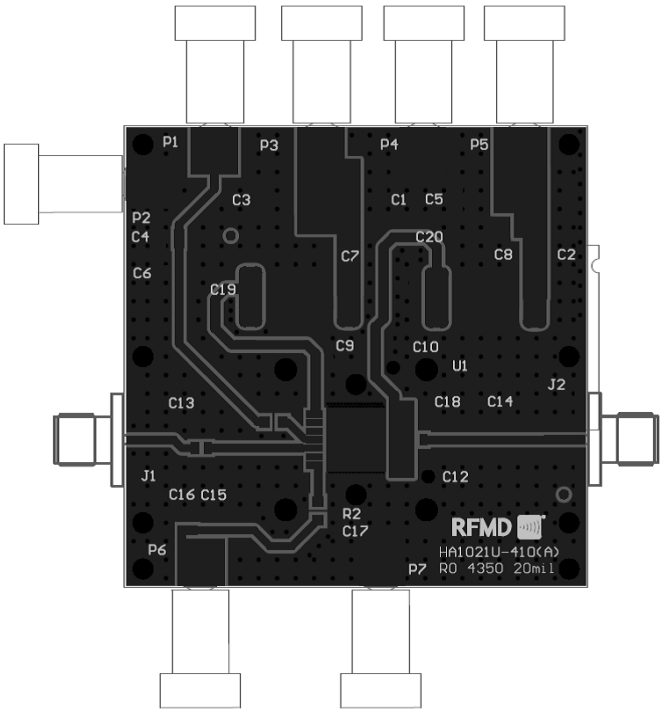
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Proposed Evaluation Board Bill of Materials

Component	Value	Manufacturer	Part Number
C2	CAP, 330µF, 20%, 100V, AL ELEC, RAD T/H	Illinois Capacitor, Inc.	337CKE100M
C1	CAP, 10µF, 20%, 100V, AL ELC, RAD	Panasonic Industrial Devices Sales	EEU-FC2A100
C3, C5	CAP, 4.7µF, 10%, 100V, X7R, 2220	Murata Electronics	GRM55ER72A475KA01L
C4, C16	CAP, 4.7µF, 10%, 50V, X7R, 1206	Murata Electronics	GRM31CR71H475KA12L
C7, C8	CAP, 0.1µF, 10%, 100V, X7R, 1206	AVX Corporation	12061C104K4T2A
C6, C15	CAP, 1000pF, 5%, 50V, C0G, 0805	Kemet	C0805C102J5GACTU
C18	CAP, 0.6pF, +/-0.1pF, 250V, C0G, ATC-A	American Technical Ceramics	800A0R6BT250XT
C12	CAP, 0.8pF, +/-0.1pF, 250V, C0G, ATC-A	American Technical Ceramics	ATC800A0R8BT250X
C14	CAP, 1.2pF, +/-0.1pF, 250V, C0G, ATC-A	American Technical Ceramics	800A1R2BT250X
C9, C10, C11, C13, C17	CAP, 22pF, +/-0.1pF, 250V, C0G, ATC-A	American Technical Ceramics	800A220BT250X
C19, C20	CAP, 82pF, 5%, 500V, C0G, ATC-B	American Technical Ceramics	ATC800B820JT500XT
R1, R2	RES, 3.3Ω, 5%, 1/4W, 1206	Panasonic Industrial Devices Sales	ERJ-8GEYJ3R3V
P1, P6	CONN, BANANA JACK, GREEN	Kamaya, Inc	RMC1/10JPTP
P3, P5	CONN, BANANA JACK, RED	JOHNSON CO	108-0902-001
P2, P4, P7	CONN, BANANA JACK, BLACK	JOHNSON CO	108-0903-001
J1, J2	CONN, SMA, ST JACK REC, FLNG MT, T/H	Emerson Network Power	142-0701-631

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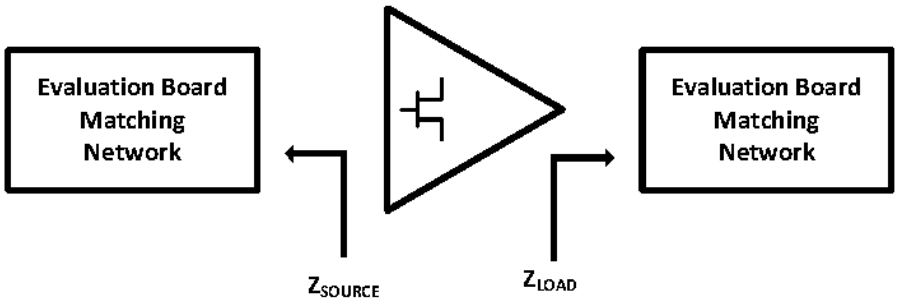
Evaluation Board Layout



Simulated Evaluation Board Impedances

Frequency	Z Source (Ω)	Z Load (Ω)
3100MHz	50	TBD
3300MHz	50	TBD
3500MHz	50	TBD

Device impedances reported are the simulated evaluation board impedances chosen for a tradeoff of efficiency, peak power, and linearity performance across the entire frequency bandwidth.



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Device Handling/Environmental Conditions

RFMD does not recommend operating this device with typical drain voltage applied and the gate pinched off in a high humidity, high temperature environment.

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance tradeoffs.

Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.

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