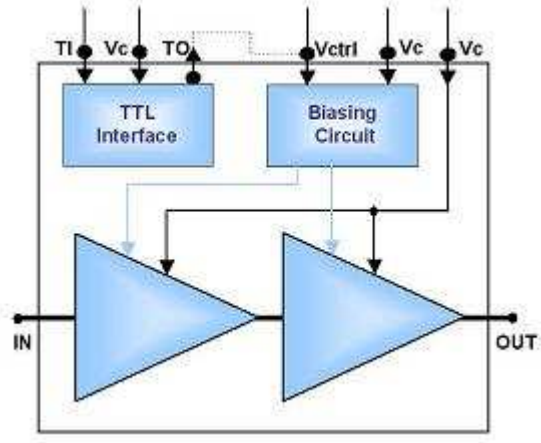
X Band Driver Amplifier

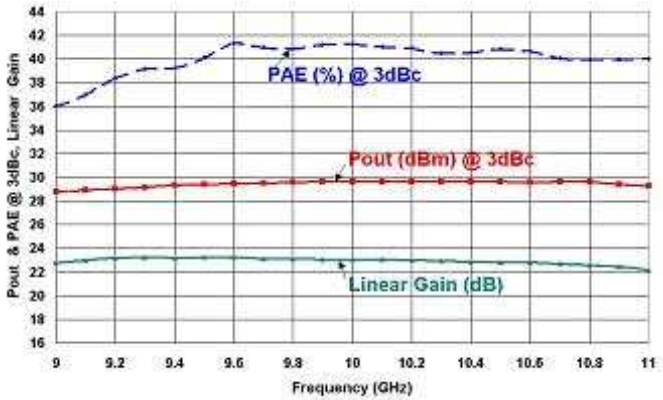
GaAs Monolithic Microwave IC

Description

The CHA5012 chip is a monolithic two-stage medium power amplifier designed for X band applications.
This device is manufactured using a GaInP HBT process, including via holes through the substrate and air bridges. A nitride layer protects the transistors and the passive components. Special heat removal techniques are implemented to guarantee high reliability.
To simplify the assembly process:

- the backside of the chip is both RF and DC grounded
- bond pads and back side are gold plated for compatibility with eutectic die attach method and thermosonic or thermocompression bonding process.





Pout & PAE @ 3dB gain compression and Linear Gain (Temperature 25°C)

Main Features

■ Frequency band : 9.2-10.8 GHz
■ Pout @3dB Gain compression : 29.5 dBm
■ P.A.E @3dB Gain Compression : 40 %
■ Two biasing modes:

- Digital control thanks to TTL interface
- Analog control thanks to biasing circuit

■ Chip size: 2.87 x 1.47 x 0.1 mm^3

Main Characteristics

Tamb = +25°C, Vc = +7.5V (Pulse 100µs 20%)

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	9.2		10.8	GHz
G	Small signal gain	21	23		dB
P3dB	Output power at 3dB compression		29.5		dBm
Icq	Power supply quiescent current		200		mA

ESD Protections : Electrostatic discharge sensitive device observe handling precautions

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Electrical Characteristics

Vc= +7.5V (Pulse 100µs 20%)

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	9.2		10.8	GHz
G	Small signal gain at 25℃	21	22.5		dB
ΔG	Small signal gain flatness at 25℃		±0.5		dB
ΔG_T	Linear gain variation vs temperature		-0.025		dB/℃
Pin	Input Power (1)			17	dBm
P1dB	Output power at 1dB gain compression at 25℃		28		dBm
P3dB	Output power at 3dB gain compression at 25℃ Output power at 3dB gain compression at 80℃	27.5 27	29.5 29		dBm
PAE_3dBc	PAE at 3dB gain compression at 25℃ PAE at 3dB gain compression at 80℃		40 37		%
dBS11	Input Return Loss		-12	-10	dB
dBS22	Output Return Loss		-10	-7	dB
Vc	Power supply voltage		7.5		V
Icq	Power supply quiescent current (2)		200		mA
Ic_3dBc	Consumption under 3dB compression		290		mA
Vctrl	Collector current control voltage		5		V
Ictrl	Biasing circuit consumption		5		mA
I_TI	TTL input consumption		1		mA
TI_Low	TTL input voltage low level		0	0.4	V
TI_High	TTL input voltage high level (2)	2.5	5		mA

(1) Output Load 50Ω

(2) For Vc=7.5V, TTL interface settles Icq to 200 mA when TI=TI_High . If needed, Icq can be tuned thanks to Vctrl if the analog biasing circuit is used

Absolute Maximum Ratings (3)

Tamb = 25℃

Symbol	Parameter	Values	Unit
Top	Operating temperature range	-40 to +80	℃
Vc	Power supply voltage (4)	10	V
Icq	Power supply quiescent current	320	mA
Ic_sat	Power supply current in saturation	350	mA
Vct	Collector current control voltage	6.5	V
Tj	Maximum Junction temperature	175	℃
Tstg	Storage temperature range	-55 to +125	℃

(3) Operation of this device above anyone of these parameters may cause permanent damage.

(4) Without RF input power

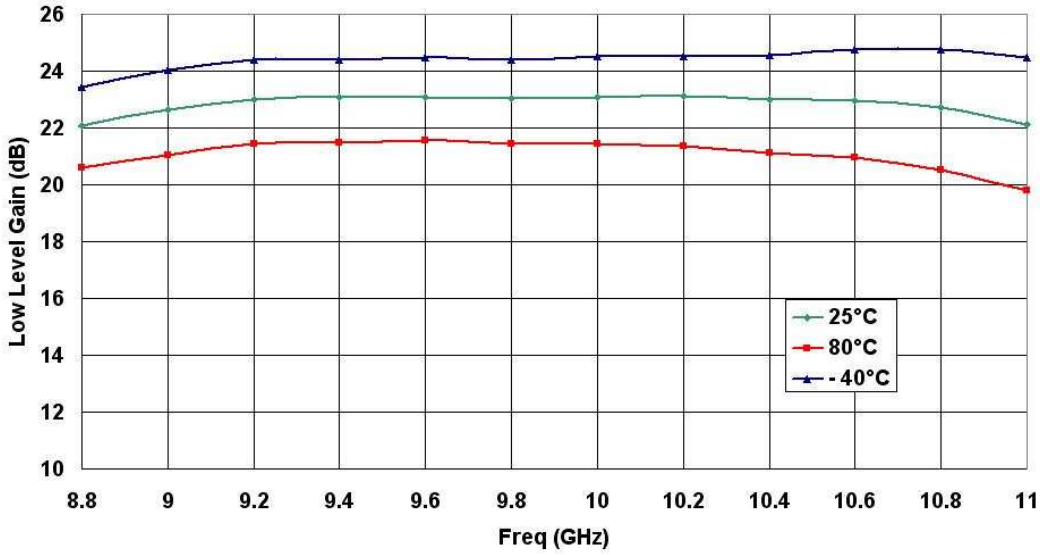
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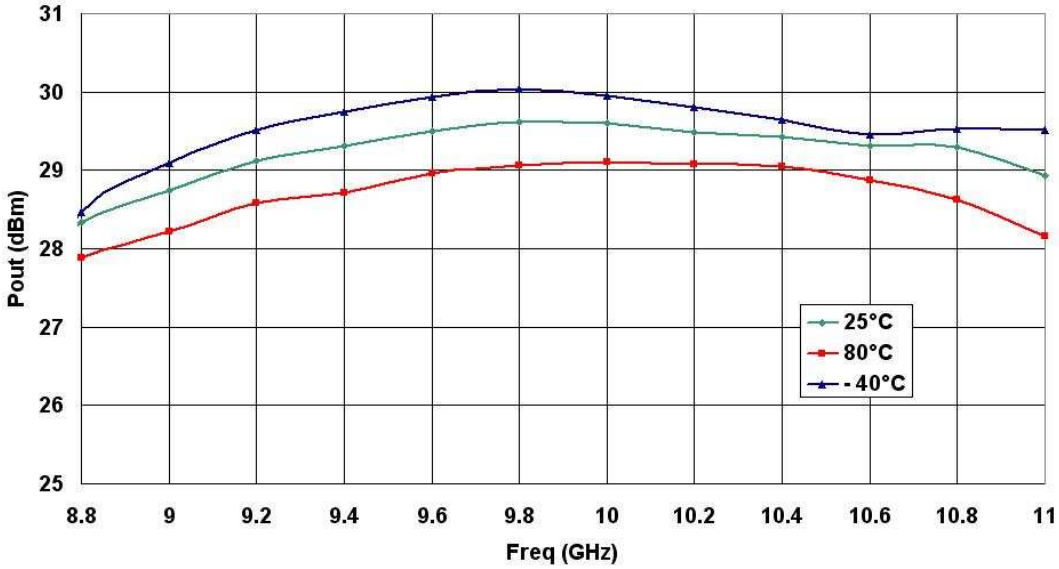
Typical measurement characteristics

Measurement conditions :

Vc=7.5V
TTL interface used for biasing. TI_High=5V and TI_Low=0V (Ic Quiescient=200mA)
Pulse width=100µs, Duty cycle= 20%

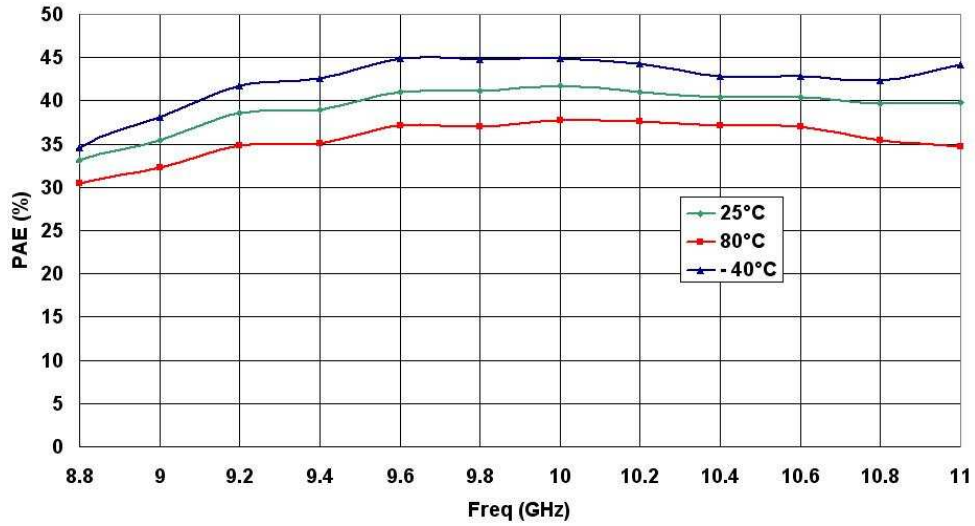


Linear gain versus frequency and temperature

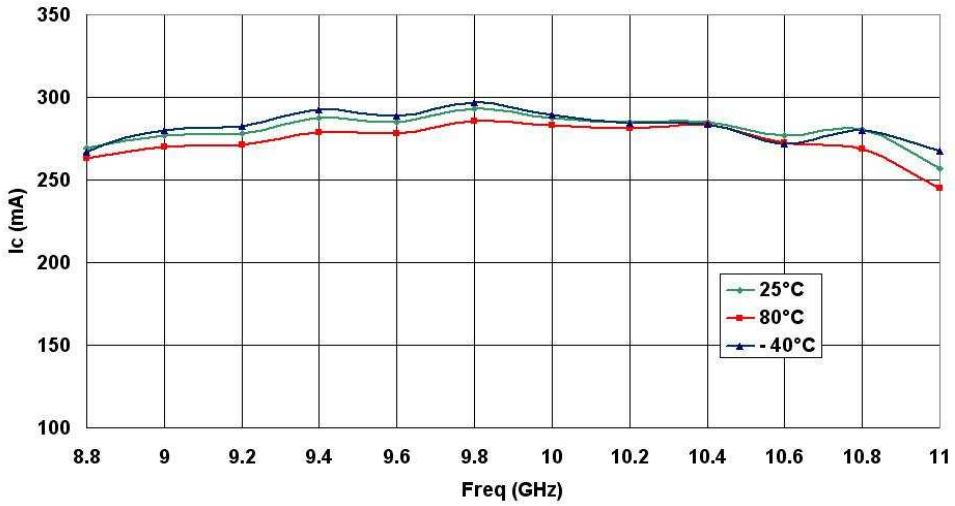


Output power @3dB gain compression versus frequency and temperature

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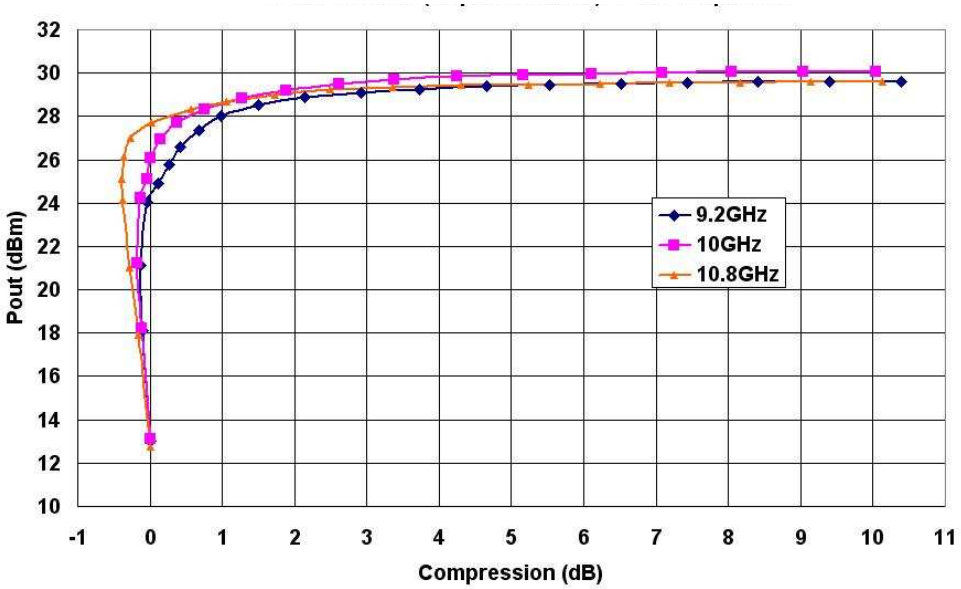


Power added efficiency @3dB gain compression versus frequency and temperature

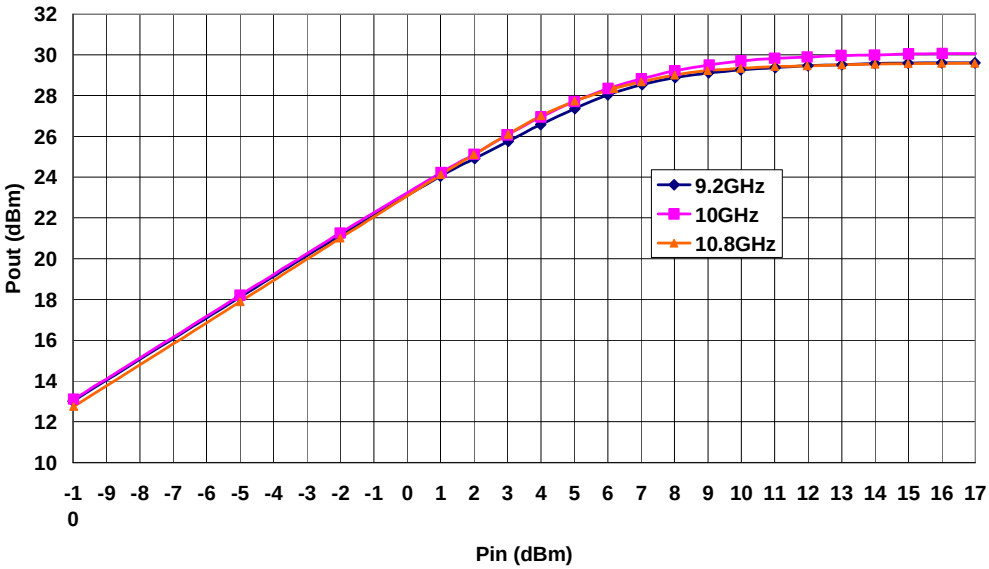


Collector current @3dB gain compression versus frequency and temperature

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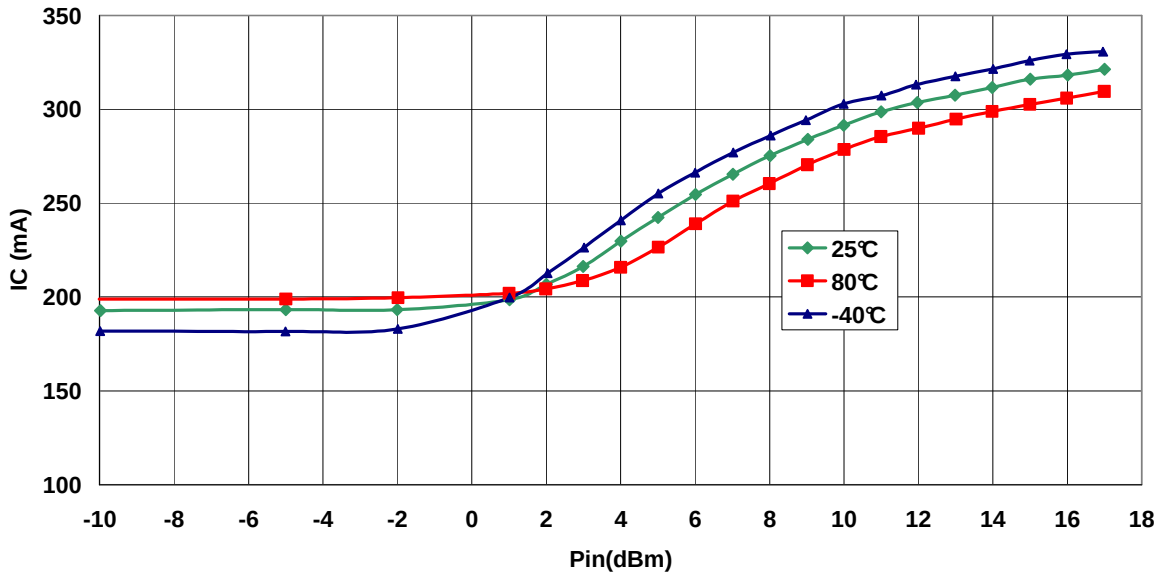


Output power versus gain compression and frequency (Temp.=25°C)

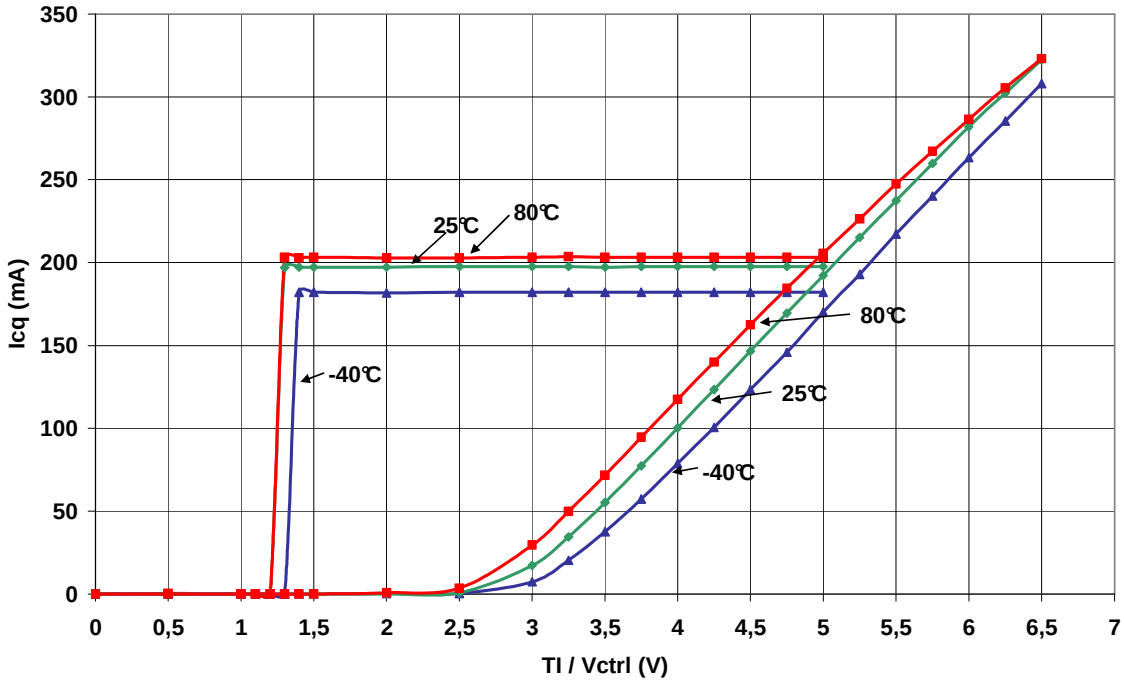


Output power versus Pin and frequency (Temp.=25°C)

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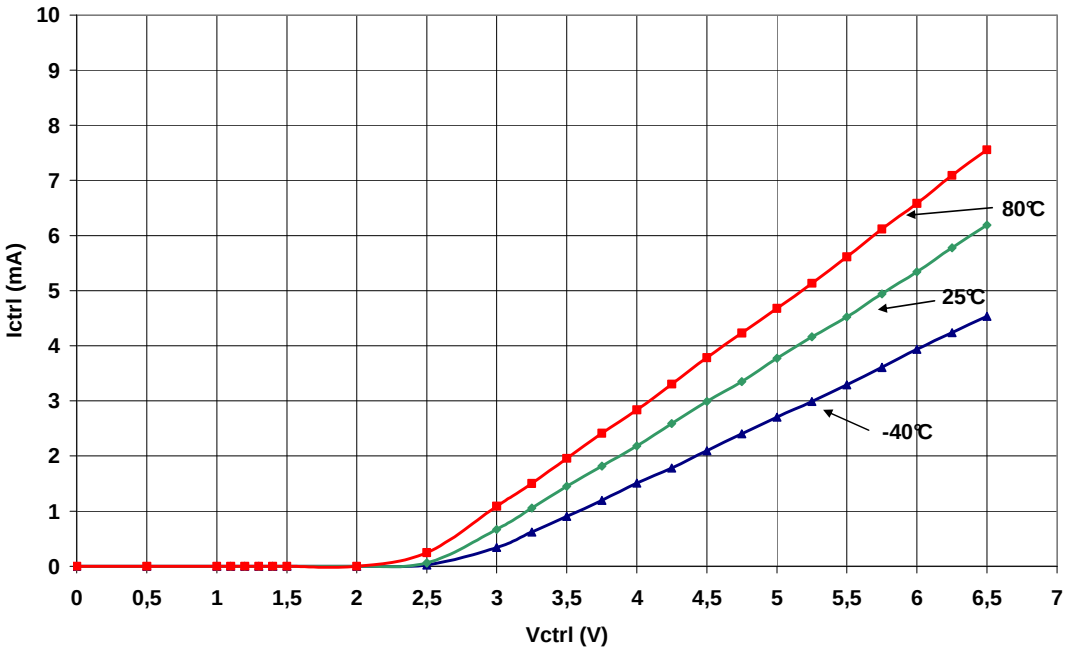
Collector current versus input power and temperature @10GHz



Collector quiescent current versus TI, Vctrl and temperature

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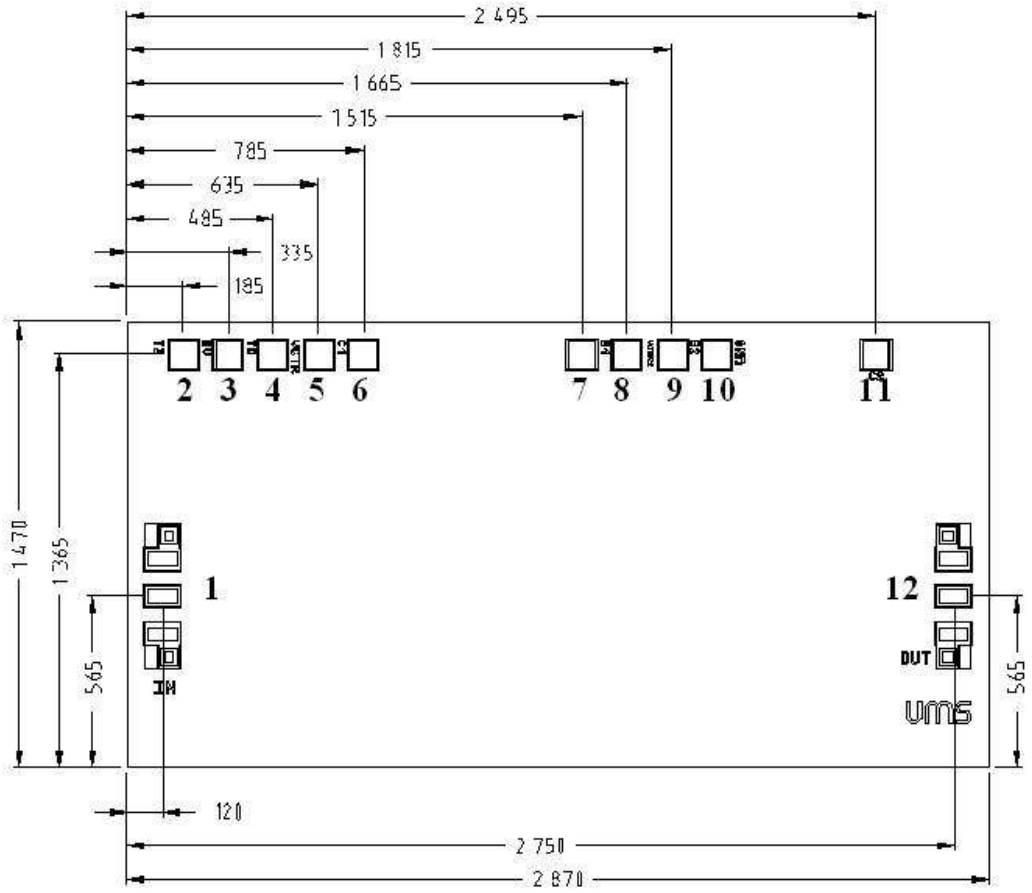
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Control current versus Vctrl and temperature

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Chip Mechanical Data and Pin references



Chip thickness = 100 +/- 10 µm
RF pads (1, 12) = 118 x 68 µm²
DC pads (2, 3, 4, 5, 9,6, 7, 8, 9, 10, 11) = 96 x 96 µm²

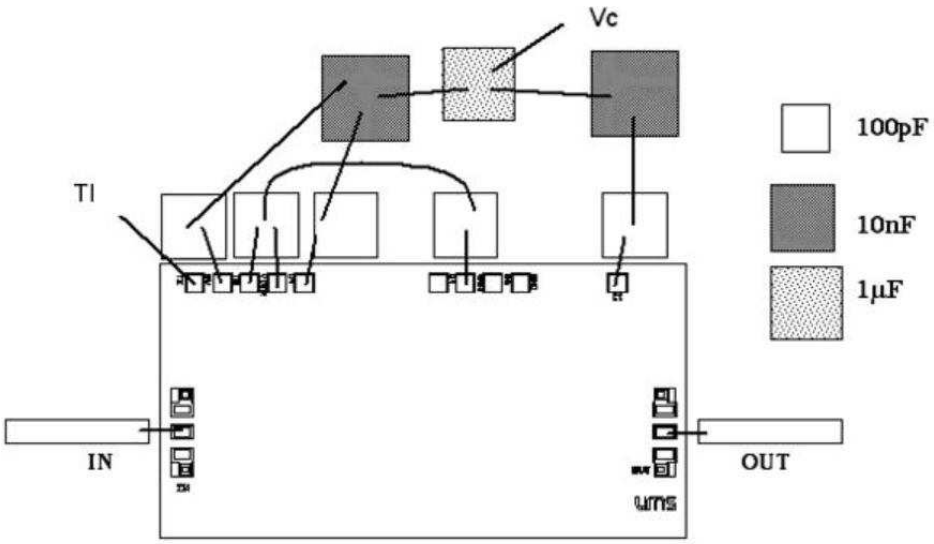
Pin number	Pin name	Description
1	IN	Input RF port
7, 9		NC
5, 8	Vctrl	Collector current control voltage
2	TI	TTL input
4	TO	TTL output
10	GND	Ground (NC)
3, 6, 11	Vc	Power supply voltage
12	OUT	Output RF port

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Bonding recommendations

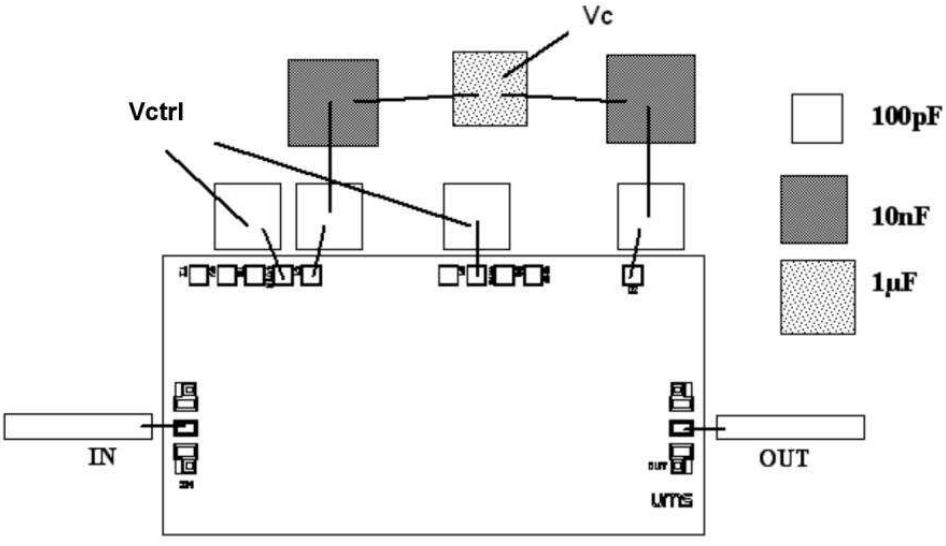
Port	Connection
IN (1)	Inductance (Lbonding) = 0.3nH 400µm length with wire diameter of 25 µm
OUT (12)	Inductance (Lbonding) = 0.3nH 400µm length with wire diameter of 25 µm

Assembly recommendations in test fixture using TTL interface



Note: when the TTL interface is used for biasing, the pin TO (pin number 4) must be connected to the pins Vctrl (pins number 5 and 8).

Assembly recommendations in test fixture using analog biasing circuits



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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form : CHA5012-99F/00

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