Plug-in Signal Conditioners M-UNIT

A/D CONVERTER

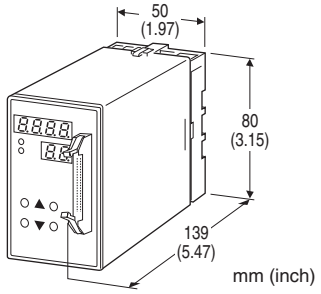
(16-bit resolution)

Functions & Features

• Converts a DC input into parallel digital signals with parity check
• BCD, binary, reflected binary, two's complement outputs selectable
• Open collector or CMOS for output levels
• Output can be scaled and displayed in convenient engineering unit
• Loop test output
• Response time adjustable within 0.15 and 60 sec.

Typical Applications

• Interface of analog signal to computers and PLC
• Input to a digital panel meter



MODEL: AD3V–[1][2]–[3][4]

ORDERING INFORMATION

• Code number: AD3V-[1][2]-[3][4]
Specify a code from below for each of [1] through [4].
(e.g. AD3V-S1C-M2/Q)
• Specify the specification for option code /Q
(e.g. /C01/S01)
• Use Ordering Information Sheet (No. ESU-1389) for settings.
Default setting will be used if not otherwise specified.

[1] INPUT

Current

Z1: Range 0 – 50 mA DC (Input resistance 100 Ω)

Voltage

S1: Range -1 – + 1 V DC (Input resistance 100 kΩ min.)
S2: Range -10 – +10 V DC (Input resistance 1 MΩ min.)
S3: Range -30 – +30 V DC (Input resistance 1 MΩ min.)

[2] OUTPUT LEVEL

A: Open collector (NPN)
B: Open collector (PNP)
C: CMOS level

[3] POWER INPUT

AC Power

M2: 100 – 240 V AC (Operational voltage range 85 – 264 V, 47 – 66 Hz)

DC Power

R3: 12 – 24 V DC
(Operational voltage range 10.8 - 26.4 V, ripple 10 %p-p max.)
P: 110 V DC
(Operational voltage range 85 – 150 V, ripple 10 %p-p max.)

[4] OPTIONS

blank: none
/Q: With options (specify the specification)

SPECIFICATIONS OF OPTION: Q (multiple selections)

COATING (For the detail, refer to M-System's web site.)

/C01: Silicone coating
/C02: Polyurethane coating
/C03: Rubber coating

TERMINAL SCREW MATERIAL

/S01: Stainless steel

RELATED PRODUCTS

• Connector terminal block (model: CNT)
• Special cable (model: MCN26)

GENERAL SPECIFICATIONS

Construction: Plug-in
Connection
Input & power: M3.5 screw terminals
Output: 26-pin connector (OMRON XG4A-2634)
Paired connector: OMRON XG4M-2630-T, XG5M-263x-N
Cover: OMRON XG5S-2612
Screw terminal: Chromated steel (standard) or stainless steel
Housing material: Flame-resistant resin (black)
Isolation: Input to output to power
Zero adjustment: -99.99 – 99.99 % (front)
Span adjustment-99.99 – 99.99 % (front)
Setting: (Front key pad)
• Scaled range
• Moving average
• Output code
• Available number of bits
• POL/OVF output logic

• Data output logic
• HOLD input logic
• DAV output logic
• DAV output time
• Output rate 'n' ratio
• Parity check
• etc.
For detailed information, refer to the instruction manual.

■DISPLAY
LED: 7 mm (.28") 7 segment, red
Number of display digits: 4 digits for DATA display; 2 digits for ITEM display
PV indication: Output signal in engineering unit
Overrange indication: LEDs blinking
Power saving mode: Displays turn off if the keys are untouched for a preset time period
PL1 (POL) LED: Red LED turns on at negative polarity.
PL2 (HOLD) LED: Red LED turns on at HOLD.

INPUT SPECIFICATIONS

■ **DC Current**: 0 – 50 mA DC; shunt resistor attached to input terminals (0.5 W)
Operational range: 0 – 70 mA DC (with 100 Ω/0.5 W)
Usable range:
• Max. range: 0 - 50 mA DC
• Min. step: 0.1 mA DC
• Input setting must: 100 % setting ≥ 0 % setting
• Input value is operational range or 15 to +115 %.

■ **DC Voltage**
Operation range:
S1: -1.15 to +1.15 V DC
S2: -11.5 to +11.5 V DC
S3: -34.5 to +34.5 V DC
Usable range:
• Max. range:
S1: -1 to +1 V DC
S2: -10 to +10 V DC
S3: -30 to +30 V DC
• Min. step:
S1: 10m V DC
S2: 100m V DC
S3: 100m V DC
• Input setting must: 100 % setting ≥ 0 % setting
• Input value is operational range or 15 to +115 %.

■ **Hold Input**: TTL level (5 V - CMOS level)
Commands to stop data renewal;
Choose from below:
Hold with low or short
Hold with high or open
(detecting voltage: approx. 5 V, saturation voltage: ≤ 1 V, sink current: 0.5 mA)

OUTPUT SPECIFICATIONS

■ **Output Code**: Code, logic and scaling are user-selectable.
BCD with polarity (Settable range: -9999 - 9999)
Binary with polarity (Settable range: -7FFF - 7FFF)
Offset binary (Settable range: 0000 - FFFF)
Two's complement (Settable range: 8000 - 7FFF)
Reflected binary (Settable range: 0000 - FFFF)
Output code, logic, scaling are settable.

■ **Available number of bits**
Selectable from 8, 10, 12, 14, 16 bits

■ **Output Level**
• **Open Collector**
Max. collector-emitter voltage: 30 V DC
Max. collector current: 30 mA
Saturation voltage:
NPN ≤ 1.1 V negative common
PNP ≤ 2.0 V positive common
• **CMOS Level**
H output: ≥ 4.5 V DC
L output: ≤ 0.5 V DC
Common: Negative

■ **POL output (Polarity)**: Same logic and level as for the output code; logic user-selectable

■ **OVF output (Overflow)**: Same logic and level as for the output code; logic user-selectable

■ **DAV output (Data available)**: Same level as for the output code; logic user-selectable

■ **Odd or even parity**: Same level as for the output code; logic user-selectable

INSTALLATION

Power consumption
•**AC**: Approx. 10 VA
•**DC**: Approx. 4 W (160 mA at 24 V)
Operating temperature: -5 to +55°C (23 to 131°F)
Operating humidity: 30 to 90 %RH (non-condensing)
Mounting: Surface or DIN rail
Weight: 260 g (0.57 lb)

PERFORMANCE in percentage of max. span

Accuracy: ±0.1 %
Min. span required to ensure the accuracy: 20 % of the nominal output range
Temp. coefficient: ±0.015 %/°C (±0.008 %/°F)
Resolution: 16 bits
Response time: 0.15 – 60 sec. (0 – 90 %) programmable at front key pad.
Line voltage effect: ±0.1 % over voltage range
Insulation resistance: ≥ 100 MΩ with 500 V DC
Dielectric strength: 2000 V AC @1 minute (input to output to power to ground)

STANDARDS & APPROVALS

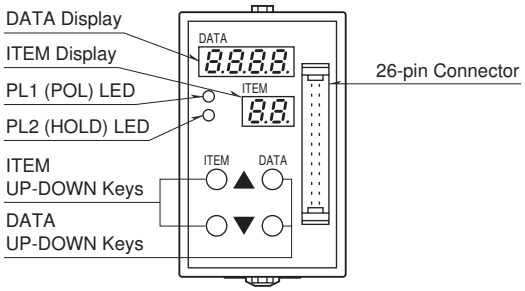
EU conformity:

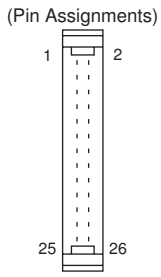
EMC Directive
- EMI EN 61000-6-4
- EMS EN 61000-6-2

Low Voltage Directive
- EN 61010-1
- Installation Category II
- Pollution Degree 2
- Input or output to power: Reinforced insulation (300 V)
- Input to output: Basic insulation (300 V)

RoHS Directive

EXTERNAL VIEW





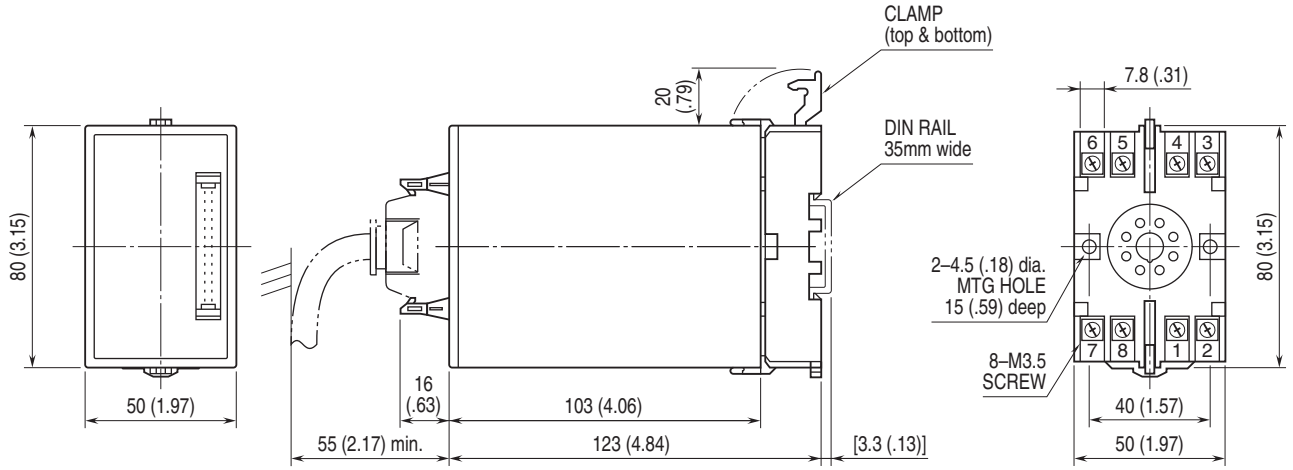
PARAMETER LIST

It is available to configure or confirm settings shown below by using front key pad.

ITEM	MDF. CODE	DATA	CONTENTS	DEFAULT
P/L	N/A	-9999 – 9999 (-FFFF – FFFF)	Output display in engineering unit with ITEM 01 DATA 1 (as set in ITEM 06/07) Loop test output with ITEM 01 DATA 2 ('L' is indicated as ITEM No.) BCD or binary (with polarity), offset binary, two's complement, reflected binary	----
01		1, 2, 3	Modification code 1 : Data indication only. 2 : All parameters are modifiable. 3 : Only ITEM 24 is modifiable.	1
02	N/A	0 – 99	Status indication ("0" is normally indicated.) 0: Normal 1: Memory error 10: Out of input range -15 – +115%	0
03	N/A	-15.0 – 115.0	Input indicated in % (of the range set in ITEM 22/23)	----
04	2	-99.99 – 99.99	Zero adjustment (%) (fine adj. of the value set in ITEM 22)	0.00
05	2	-99.99 – 99.99	Span adjustment (%) (fine adj. of the value set in ITEM 23)	0.00
06	2	-9999 – 9999	BCD Display range scaling 0% *1	-1000
07	2	-9999 – 9999	Display range scaling 100% *1	1000
06	2	-7FFF – 7FFF	Binary Display range scaling 0% *1	-7FFF
07	2	-7FFF – 7FFF	Display range scaling 100% *1	7FFF
06	2	0000 – FFFF	Offset binary Display range scaling 0% *1	0000
07	2	0000 – FFFF	Display range scaling 100% *1	FFFF
06	2	8000 – 7FFF	Two's complement Display range scaling 0% *1	8000
07	2	8000 – 7FFF	Display range scaling 100% *1	7FFF
06	2	0000 – FFFF	Reflected binary Display range scaling 0% *1	0000
07	2	0000 – FFFF	Display range scaling 100% *1	FFFF
08	2	0 – 99	Power ON-delay time (seconds)	5
09	2	0, 1, 2, 3, 4	Display code 0 : BCD with polarity (decimal) 1 : Binary with polarity 2 : Offset binary 3 : Two's complement 4 : Reflected binary	0
10	2	0, 1, 2, 3, 4	Available number of bits 0: 16 bits 1: 14 bits 2: 12 bits 3: 10 bits 4: 8 bits	0
11	2	0, 1, 2	Parity check 0: Disable 1: Enable Parity per each digit 2: Enable Parity for all digits	0
12	2	0, 1	Odd or even parity (Checking the number of High in the output) 0 : Odd (CMOS level, open collector (PNP)), Even (open collector (NPN)) 1 : Even (CMOS level, open collector (PNP)), Odd (open collector (NPN))	0
13	2	0, 1	POL, OVF output logic 0 : Data available at High (CMOS level) or ON (open collector) 1 : Data available at Low (CMOS level) or OFF (open collector)	0
14	2	0, 1	Data output logic *2 0 : Positive (CMOS level, open collector (PNP)), Negative (open collector (NPN)) 1 : Negative (CMOS level, open collector (PNP)), Positive (open collector (NPN))	0
15	2	0, 1	HOLD input logic 0 : HOLD at Low or shortcircuit 1 : HOLD at High or open circuit	0
16	2	0, 1	DAV output logic 0 : Data available at High (CMOS level) or ON (open collector) 1 : Data available at Low (CMOS level) or OFF (open collector)	0
17	2	1 – 50	DAV output time (msec.) selectable up to 50% of the Output Rate (ITEM 20)	1
18	2	0, 1, 2, 3, 4, 5	Moving average (10 msec./sampling) 0: No 1: 5 samples 2: 8 samples 3: 12 samples 4: 20 samples 5: 36 samples	1
19	2	0.0 – 60.0	Delay buffer (seconds, 0 – 90%) * When setting to less than or equal to 0.1, response time is 0.15 seconds.	0.5
20	2	1 – 20	Output rate 'n' ratio (n : 1 – 20 times)	1
21	2	0, 1 – 60	Power-saving mode 0 : Continuous display 1 – 60 : Time before display turned off (minutes)	10
22	2	-1.00 – 1.00	Input code S1 0% input voltage (V) *3	-1.00
23	2	-1.00 – 1.00	100% input voltage (V) *3	1.00
22	2	-10.0 – 10.0	Input code S2 0% input voltage (V) *3	-10.0
23	2	-10.0 – 10.0	100% input voltage (V) *3	10.0
22	2	-30.0 – 30.0	Input code S3 0% input voltage (V) *3	-30.0
23	2	-30.0 – 30.0	100% input voltage (V) *3	30.0
22	2	0.0 – 50.0	Input code Z1 0% input current (mA) *3	4.0
23	2	0.0 – 50.0	100% input current (mA) *3	20.0
24	3	0, 1	Reset all settings	0
25	N/A	----	ROM version	----

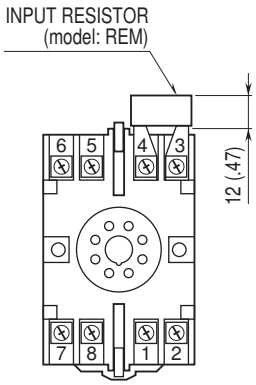
*1. Of the range set in ITEM 04/05. ITEM 06 < ITEM 07.
*2. ITEM 13, 15 or 16 is independent from ITEM 14.
*3. ITEM 22 < ITEM 23.

EXTERNAL DIMENSIONS unit: mm [inch]



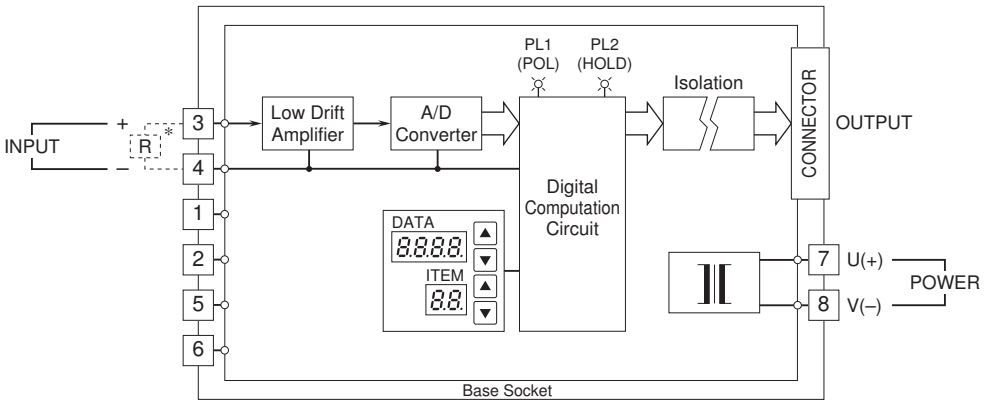
•When mounting, no extra space is needed between units.

TERMINAL ASSIGNMENTS unit: mm (inch)



Input shunt resistor attached
for current input.

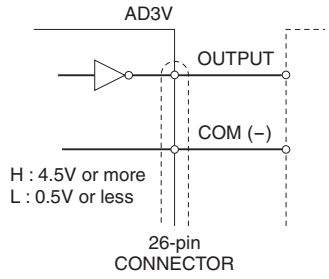
SCHEMATIC CIRCUITRY & CONNECTION DIAGRAM



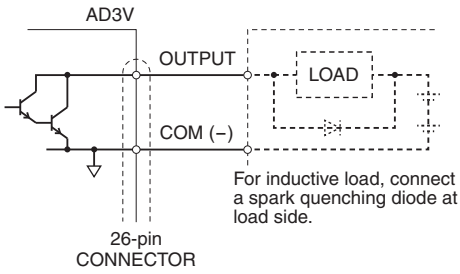
*Input shunt resistor attached for current input.

■ Connection Examples

• CMOS LEVEL (5V-CMOS)

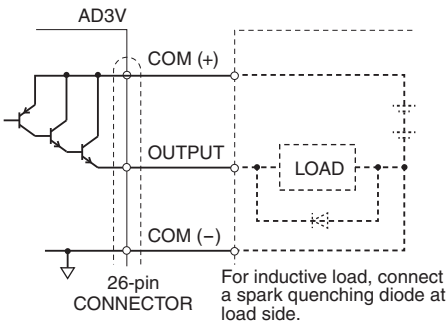


• OPEN COLLECTOR (NPN)



Max. collector-emitter voltage : 30V DC
Max. collector current : 30mA
Saturation voltage : ≤ 1.1V DC

• OPEN COLLECTOR (PNP)



Max. collector-emitter voltage : 30V DC
Max. collector current : 30mA
Saturation voltage : ≤ 2.0V DC

OUTPUT CONNECTOR (26-pin)

■ BCD OUTPUT

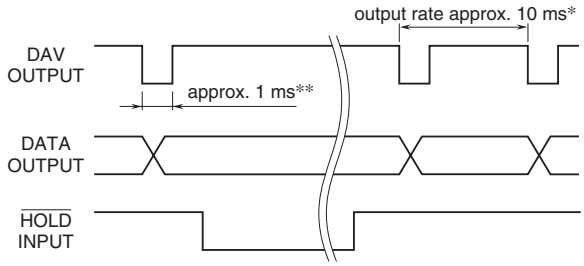
PIN NO.	ASSIGNMENT	PIN NO.	ASSIGNMENT
1	1 10^0	17	COM *1
2	2 10^0	18	COM (–)
3	4 10^0	19	OVF
4	8 10^0	20	POL
5	1 10^1	21	DAV
6	2 10^1	22	$\overline{\text{HOLD}}$ *2
7	4 10^1	23	P^0 *3
8	8 10^1	24	P^1
9	1 10^2	25	P^2
10	2 10^2	26	P^3
11	4 10^2		
12	8 10^2		
13	1 10^3		
14	2 10^3		
15	4 10^3		
16	8 10^3		

■ BINARY, TWO'S COMPLEMENT OUTPUTS

PIN NO.	ASSIGNMENT	PIN NO.	ASSIGNMENT
1	B^0	17	COM *1
2	B^1	18	COM (–)
3	B^2	19	OVF
4	B^3	20	POL
5	B^4	21	DAV
6	B^5	22	$\overline{\text{HOLD}}$ *2
7	B^6	23	P^0 *4
8	B^7	24	P^1
9	B^8	25	P^2
10	B^9	26	P^3
11	B^{10}		
12	B^{11}		
13	B^{12}		
14	B^{13}		
15	B^{14}		
16	B^{15}		

*1. For open collector (NPN) and CMOS level, COM (–). For open collector(PNP), COM (+).
*2. $\overline{\text{HOLD}}$ signal is for input, the others are for output.
*3. P^0 corresponds to n × 10^0, P^1 to n × 10^1, P^2 to n × 10^2, P^3 to n × 10^3. P^0 – P^3 are in sync when the parity for all digits are valid.
*4. P^0 corresponds to B^0 – B^3, P^1 to B^4 – B^7, P^2 to B^8 – B^{11}, P^3 to B^{12} – B^{15}. P^0 – P^3 are in sync when the parity for all digits are valid.
Note: With the number of bits set to 14 (or 12, 10, 8) with ITEM 10, Pin No. 1 – 14 (or 1 – 12, 1 – 10, 1 – 8) are valid.

TIMING CHART



Data output is halt during $\overline{\text{HOLD}}$ input.
DAV is output during DATA output.
* Varies by individual module. Set to 'n' times with ITEM 20.
**Selectable with ITEM 17.

INPUT-OUTPUT RELATION EXAMPLES

• FS

-FS stands for -15 % of the input range, which is configured by ITEM 22, 0 % input voltage/current and ITEM 23, 100 % input voltage/current. +FS stands for +115 % of the input range.

• OVF

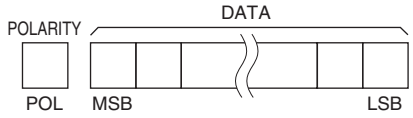
When one of the following conditions is true, the digital output overflows (OVF).

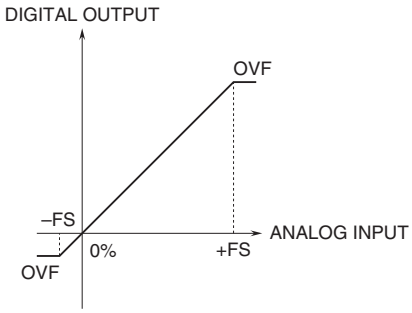
1) When the input signal is out of the range between -FS and +FS.

2) When the display value (= output signal) exceeds the display range.

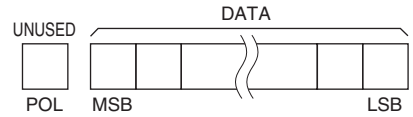
The display range differs according to output code. For example, in case of BCD with polarity, it is -9999 to 9999. Please refer to the instruction manual for detail.

■ BCD, BINARY (WITH POLARITY)





■ OFFSET BINARY & TWO'S COMPLEMENT



OUTPUT DATA & PARITY BIT RELATIONSHIP

Hi and Lo indicate the voltage level. Parity logic is unchanged. (ITEM 12 = I12; ITEM 14 = I14)

■ OPEN COLLECTOR (NPN)

• Positive Logic I14 : 1, Lo : False, Hi: True

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Lo	Lo	Lo	Lo	Lo	Hi
1	Lo	Lo	Lo	Hi	Hi	Lo
2	Lo	Lo	Hi	Lo	Hi	Lo
3	Lo	Lo	Hi	Hi	Lo	Hi
4	Lo	Hi	Lo	Lo	Hi	Lo
5	Lo	Hi	Lo	Hi	Lo	Hi
6	Lo	Hi	Hi	Lo	Lo	Hi
7	Lo	Hi	Hi	Hi	Hi	Lo
8	Hi	Lo	Lo	Lo	Hi	Lo
9	Hi	Lo	Lo	Hi	Lo	Hi
10	Hi	Lo	Hi	Lo	Lo	Hi
11	Hi	Lo	Hi	Hi	Hi	Lo
12	Hi	Hi	Lo	Lo	Lo	Hi
13	Hi	Hi	Lo	Hi	Hi	Lo
14	Hi	Hi	Hi	Lo	Hi	Lo
15	Hi	Hi	Hi	Hi	Lo	Hi

• Negative Logic I14 : 0, Lo : True, Hi: False

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Hi	Hi	Hi	Hi	Lo	Hi
1	Hi	Hi	Hi	Lo	Hi	Lo
2	Hi	Hi	Lo	Hi	Hi	Lo
3	Hi	Hi	Lo	Lo	Lo	Hi
4	Hi	Lo	Hi	Hi	Hi	Lo
5	Hi	Lo	Hi	Lo	Lo	Hi
6	Hi	Lo	Lo	Hi	Lo	Hi
7	Hi	Lo	Lo	Lo	Hi	Lo
8	Lo	Hi	Hi	Hi	Hi	Lo
9	Lo	Hi	Hi	Lo	Lo	Hi
10	Lo	Hi	Lo	Hi	Lo	Hi
11	Lo	Hi	Lo	Lo	Hi	Lo
12	Lo	Lo	Hi	Hi	Lo	Hi
13	Lo	Lo	Hi	Lo	Hi	Lo
14	Lo	Lo	Lo	Hi	Hi	Lo
15	Lo	Lo	Lo	Lo	Lo	Hi

■ CMOS LEVEL, OPEN COLLECTOR (PNP)

• Positive Logic I14 : 0, Lo : False, Hi: True

DATA	8	4	2	1	PARITY	
					Odd I12 : 0	Even I12 : 1
0	Lo	Lo	Lo	Lo	Hi	Lo
1	Lo	Lo	Lo	Hi	Lo	Hi
2	Lo	Lo	Hi	Lo	Lo	Hi
3	Lo	Lo	Hi	Hi	Hi	Lo
4	Lo	Hi	Lo	Lo	Lo	Hi
5	Lo	Hi	Lo	Hi	Hi	Lo
6	Lo	Hi	Hi	Lo	Hi	Lo
7	Lo	Hi	Hi	Hi	Lo	Hi
8	Hi	Lo	Lo	Lo	Lo	Hi
9	Hi	Lo	Lo	Hi	Hi	Lo
10	Hi	Lo	Hi	Lo	Hi	Lo
11	Hi	Lo	Hi	Hi	Lo	Hi
12	Hi	Hi	Lo	Lo	Hi	Lo
13	Hi	Hi	Lo	Hi	Lo	Hi
14	Hi	Hi	Hi	Lo	Lo	Hi
15	Hi	Hi	Hi	Hi	Hi	Lo

• Negative Logic I14 : 1, Lo : True, Hi: False

DATA	8	4	2	1	PARITY	
					Odd I12 : 0	Even I12 : 1
0	Hi	Hi	Hi	Hi	Hi	Lo
1	Hi	Hi	Hi	Lo	Lo	Hi
2	Hi	Hi	Lo	Hi	Lo	Hi
3	Hi	Hi	Lo	Lo	Hi	Lo
4	Hi	Lo	Hi	Hi	Lo	Hi
5	Hi	Lo	Hi	Lo	Hi	Lo
6	Hi	Lo	Lo	Hi	Hi	Lo
7	Hi	Lo	Lo	Lo	Lo	Hi
8	Lo	Hi	Hi	Hi	Lo	Hi
9	Lo	Hi	Hi	Lo	Hi	Lo
10	Lo	Hi	Lo	Hi	Hi	Lo
11	Lo	Hi	Lo	Lo	Lo	Hi
12	Lo	Lo	Hi	Hi	Hi	Lo
13	Lo	Lo	Hi	Lo	Lo	Hi
14	Lo	Lo	Lo	Hi	Lo	Hi
15	Lo	Lo	Lo	Lo	Hi	Lo

⚠ Specifications are subject to change without notice.