16-Bit, 250 kSPS PulSAR® ADC in MSOP

Data Sheet **AD7694**

FEATURES

16-bit resolution with no missing codes
Throughput: 250 kSPS at 5 V
INL: ±4 LSB max
S/(N + D): 92 dB at 20 kHz
THD: −106 dB at 20 kHz
Pseudo-differential analog input range:
0 V to V_{REF} with V_{REF} up to VDD
No pipeline delay
Single-supply operation: 2.7 V or 5 V
Proprietary serial interface
SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible[1]
Supply Current: 540 µA at 2.7 V/100 kSPS,
800 µA at 5 V/100 kSPS
Standby current: 1 nA
8-lead MSOP package
Improved second source to LTC1864 and LTC1864L

APPLICATIONS

Battery-powered equipment
Data acquisition
Instrumentation
Medical instruments
Process control

GENERAL DESCRIPTION

The AD7694 is a 16-bit, charge redistribution, successive approximation, PulSAR analog-to-digital converter (ADC) that operates from a single power supply, VDD, between 2.7 V to 5.25 V. It contains a low power, high speed, 16-bit sampling ADC with no missing codes (B grade), an internal conversion clock, and a serial, SPI-compatible interface port. The part also contains a low noise, wide bandwidth, short aperture delay track-and-hold circuit. On the CNV rising edge, it samples an analog input, IN+, between 0 V to REF with respect to a ground sense, IN−. The reference voltage, REF, is applied externally and can be set up to the supply voltage.

Its power scales linearly with throughput.

The AD7694 is housed in an 8-lead MSOP package with an operating temperature specified from −40°C to +85°C.

[1] Protected by U.S. Patent 6,703,961.

APPLICATION DIAGRAM

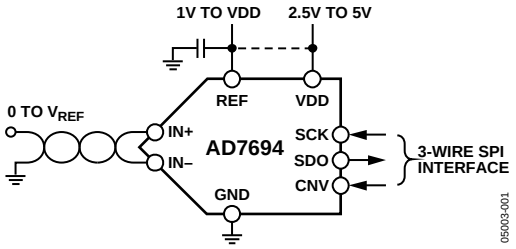


Figure 1.

Table 1. MSOP, LFCSP (QFN)/SOT-23, 16-Bit PulSAR ADC

Type	100 kSPS	250 kSPS	500 kSPS
True Differential	AD7684	AD7687	AD7688
Pseudo	AD7683	AD7685	AD7686
Differential/Unipolar		AD7694	
Unipolar	AD7680		

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AD7694* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7694 Evaluation Kit

DOCUMENTATION

Application Notes

- AN-931: Understanding PulSAR ADC Support Circuitry
- AN-932: Power Supply Sequencing

Data Sheet

- AD7694: 16-Bit, 250 kSPS PulSAR ADC in MSOP Data Sheet

User Guides

- UG-340: Evaluation Board for the 10-Lead Family 14-/16-/18-Bit PulSAR ADCs
- UG-682: 6-Lead SOT-23 ADC Driver for the 8-/10-Lead Family of 14-/16-/18-Bit PulSAR ADC Evaluation Boards

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7694 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7694 EngineerZone Discussions.

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REVISION HISTORY

6/14—Rev. A to Rev. B

Added Patent Footnote ... 1
Changes to Evaluating the AD7694 Performance Section ... 15
Changes to Ordering Guide ... 16

5/05—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Digital Interface Section ... 14
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7/04—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.7 V to 5.25 V; V_{REF} = VDD; T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

		A Grade			B Grade			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		16			16			Bits
ANALOG INPUT								
Voltage Range	IN+ − IN−	0		V_{REF}	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		VDD + 0.1	−0.1		VDD + 0.1	V
	IN−	−0.1		+0.1	−0.1		+0.1	V
Leakage Current at 25°C	Acquisition phase		1			1		nA
Input Impedance		See the Analog Input section						
ACCURACY								
No Missing Codes		15			16			Bits
Integral Linearity Error		−6		+6	−4		+4	LSB
Transition Noise	REF = VDD = 5 V		0.5			0.5		LSB
Gain Error[1], T_{MIN} to T_{MAX}			±2	±30		±2	±15	LSB
Gain Error Temperature Drift			±0.3			±0.3		ppm/°C
Offset Error[1], T_{MIN} to T_{MAX}			±0.7	±3.5		±0.7	±3.5	mV
Offset Temperature Drift			±0.3			±0.3		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±0.05			±0.05		LSB
THROUGHPUT								
Conversion Rate	VDD = 4.75 V to 5.25 V	0		250	0		250	kSPS
	VDD = 2.7 V to 4.75 V	0		150	0		150	kSPS
AC ACCURACY								
Signal-to-Noise	f_{IN} = 20 kHz, V_{REF} = 5 V		90		88	92		dB[2]
	f_{IN} = 20 kHz, V_{REF} = 2.5 V		86			87		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		−100			−106		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		−100			−106		dB
Signal-to-(Noise + Distortion)	f_{IN} = 20 kHz, V_{REF} = 5 V		89		88	92		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V		86			87		dB

[1] See the Terminology section. These specifications include full temperature range variation, but do not include the error contribution from the external reference.
[2] All specifications in dB refer to a full-scale input, FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

VDD = 2.7 V to 5.25 V; V_{REF} = VDD; T_A = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		1		VDD	V
Load Current	250 kSPS, $V_{IN+} - V_{IN-} = V_{REF}/2$ = 2.5 V		50		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			9		MHz
DIGITAL INPUTS					
Logic Levels					
V_{IL}	VDD = 4.75 V			0.8	V
	VDD = 2.7 V			0.45	V
V_{IH}	VDD = 5.25 V	3.15			V
	VDD = 3.3 V	1.9			V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial, 16 bits straight binary			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VDD − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	2.7		5.25	V
Operating Current					
VDD	VDD = 5 V, 100 kSPS throughput		0.8	1.2	mA
	VDD = 2.7 V, 100 kSPS throughput		540	960	µA
Standby Current[1, 2]	VDD = 5 V, 25°C		1	50	nA
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] With all digital inputs forced to VDD or GND, as required.
[2] During acquisition phase.

TIMING SPECIFICATIONS

VDD = 4.75 V to 5.25 V; T_A = −40°C to +85°C, unless otherwise stated.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}			3.2	µs
Time Between Conversions	t_{CYC}	4			µs
SCK Period	t_{SCK}	50			ns
SCK Low Time	t_{SCKL}	20			ns
SCK High Time	t_{SCKH}	20			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}			20	ns
CNV Low to SDO, D15 MSB Valid	t_{EN}			60	ns
CNV High to SDO High Impedance	t_{DIS}			60	ns

VDD = 2.7 V to 4.75 V; T_A = −40°C to +85°C, unless otherwise stated.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}			4.66	µs
Time Between Conversions	t_{CYC}	6.66			µs
SCK Period	t_{SCK}	125			ns
SCK Low Time	t_{SCKL}	50			ns
SCK High Time	t_{SCKH}	50			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}			50	ns
CNV Low to SDO, D15 MSB Valid	t_{EN}			120	ns
CNV High to SDO High Impedance	t_{DIS}			120	ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs	
IN+[1], IN−[1]	GND − 0.3 V to VDD + 0.3 V or ±130 mA
REF	GND − 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD to GND	−0.3 V to +7 V
Digital Inputs to GND	−0.3 V to VDD + 0.3 V
Digital Outputs to GND	−0.3 V to VDD + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	200°C/W (MSOP-8)
θ_{JC} Thermal Impedance	44°C/W (MSOP-8)
Lead Temperature Range	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] See the Analog Input section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

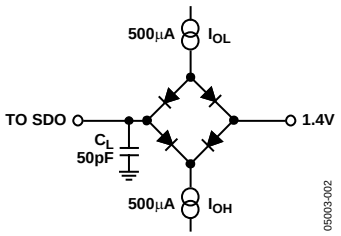


Figure 2. Load Circuit for Digital Interface Timing

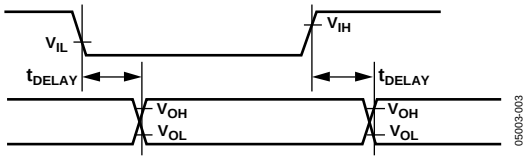


Figure 3. Voltage Reference Levels for Timing

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

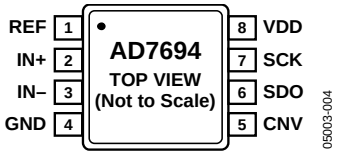


Figure 4. 8-Lead MSOP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Function
1	REF	AI	Reference Input Voltage. The REF range is from 1 V to VDD. It is referred to the GND pin. This pin should be decoupled closely to the pin with a ceramic capacitor of a few µF.
2	IN+	AI	Analog Input. It is referred to in IN–. The voltage range, that is, the difference between IN+ and IN–, which is 0 V to V_{REF}.
3	IN–	AI	Analog Input Ground Sense. To be connected to the analog ground plane or to a remote sense ground.
4	GND	P	Power Supply Ground.
5	CNV	DI	Convert Input. On its leading edge, it initiates the conversions. It enables the SDO pin when low.
6	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
7	SCK	DI	Serial Data Clock Input. When CNV is low, the conversion result is shifted out by this clock.
8	VDD	P	Power Supply.

[1]AI = analog input; DI = digital input; DO = digital output; and P = power.

TERMINOLOGY

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale to positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1 ½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 19).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
The first transition should occur at a level ½ LSB above analog ground (38.1 µV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111...10 to 111...11) should occur for an analog voltage 1 ½ LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset has been adjusted out.

Spurious-Free Dynamic Range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N + D) by

$$ENOB = (S/[N + D]_{dB} - 1.76)/6.02$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

Signal-to-(Noise + Distortion) Ratio (S/[N + D])
S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in dB.

Aperture Delay
Aperture delay is a measure of the acquisition performance and the time between the rising edge of the CNV input and the time the input signal is held for conversion.

Transient Response
The time required for the ADC to accurately acquire its input after a full-scale step function is applied.

TYPICAL PERFORMANCE CHARACTERISTICS

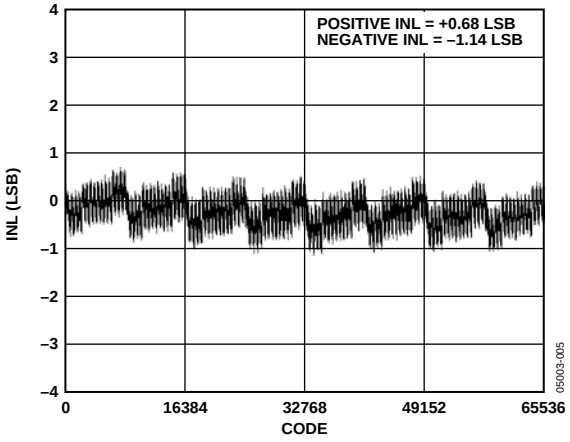


Figure 5. Integral Nonlinearity vs. Code

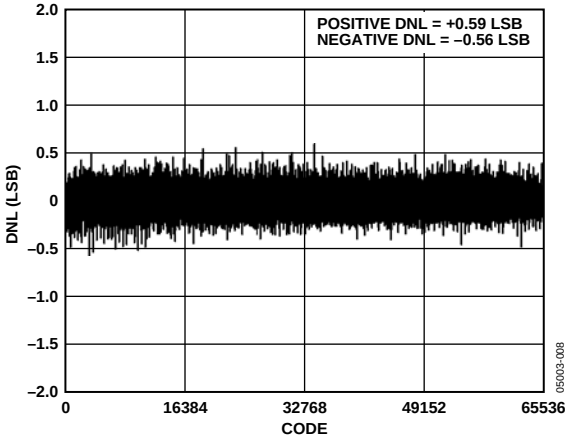


Figure 8. Differential Nonlinearity vs. Code

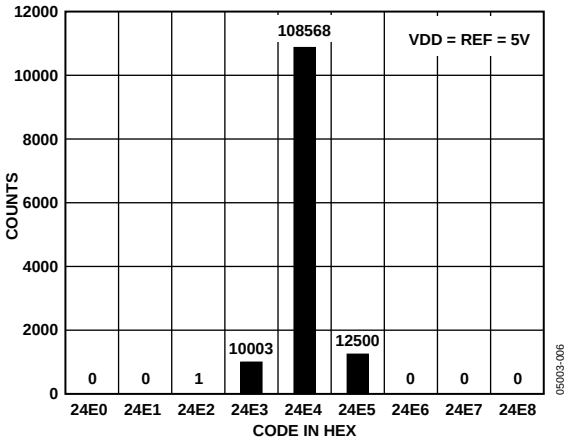


Figure 6. Histogram of a DC Input at the Code Center

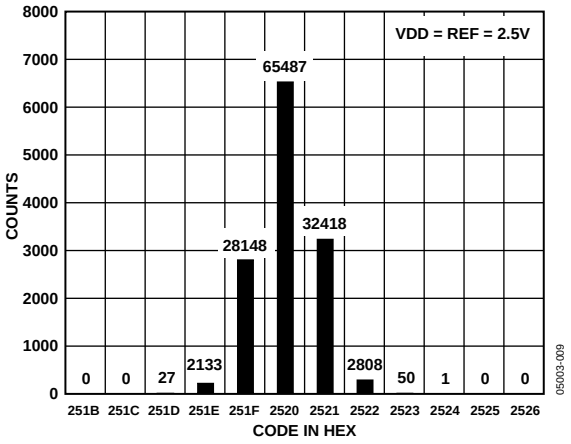


Figure 9. Histogram of a DC Input at the Code Center

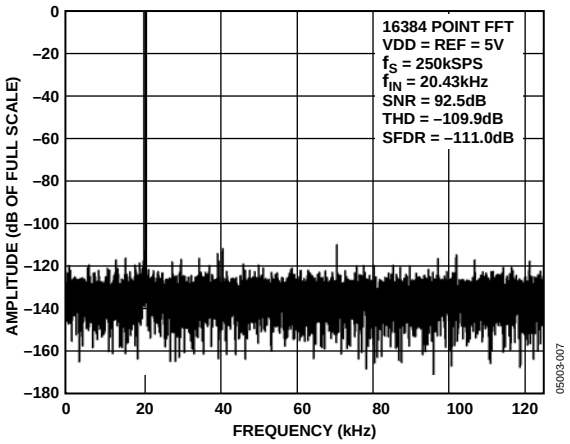


Figure 7. FFT Plot

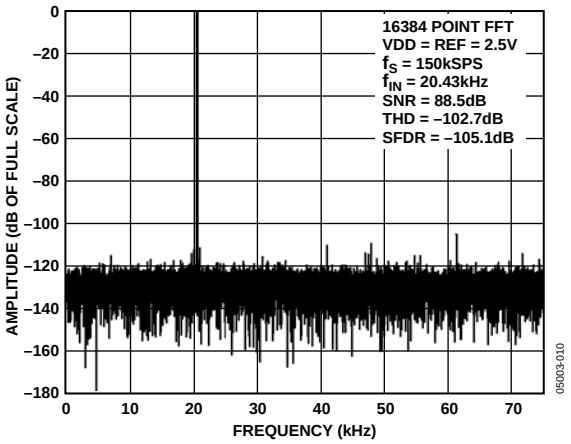


Figure 10. FFT Plot

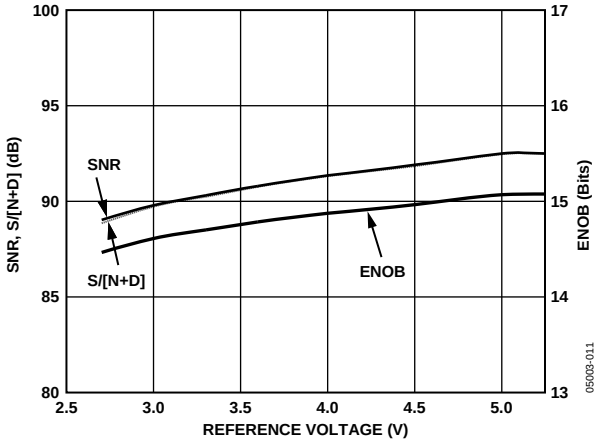


Figure 11. SNR, S/(N + D), and ENOB vs. Reference Voltage

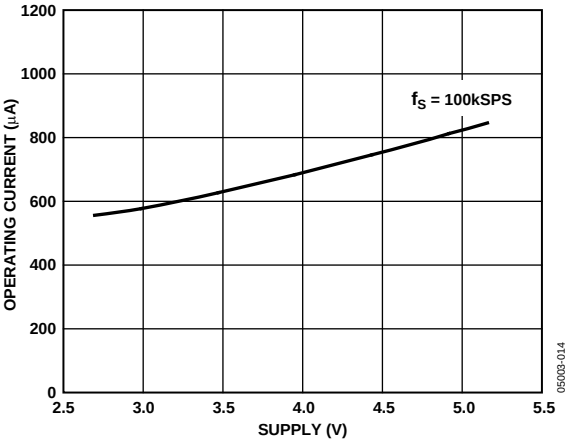


Figure 14. Operating Current vs. Supply

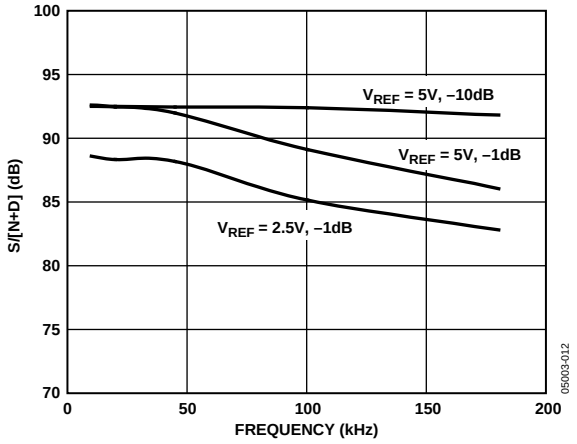


Figure 12. S/[N + D] vs. Frequency

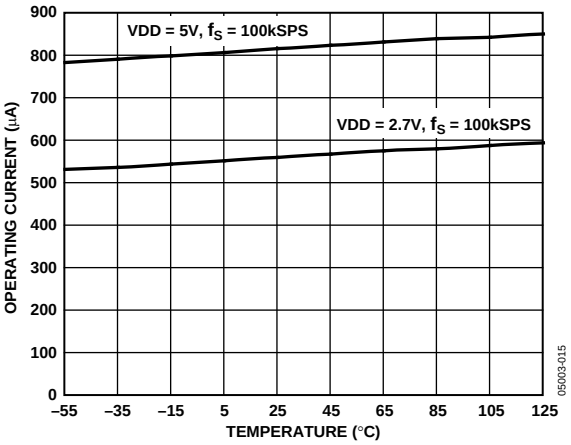


Figure 15. Operating Current vs. Temperature

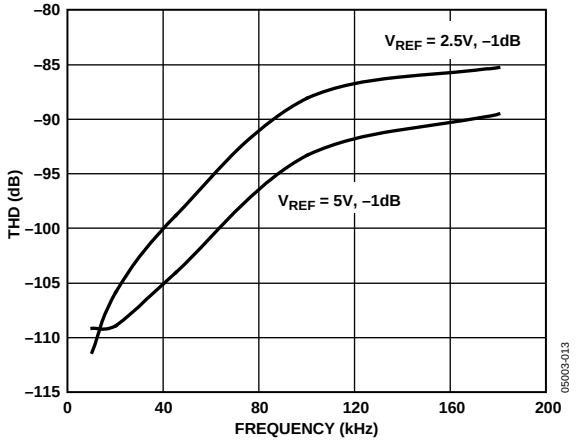


Figure 13. THD vs. Frequency

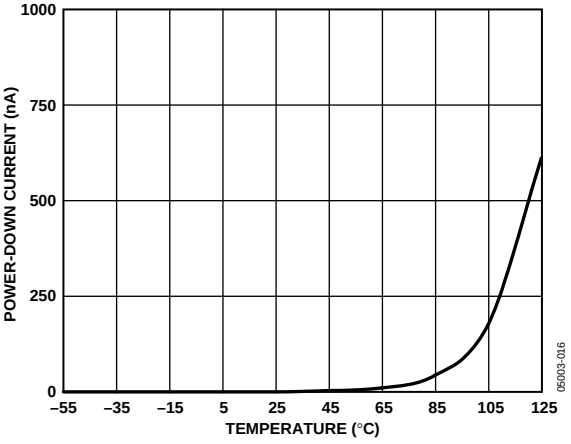


Figure 16. Power-Down Current vs. Temperature

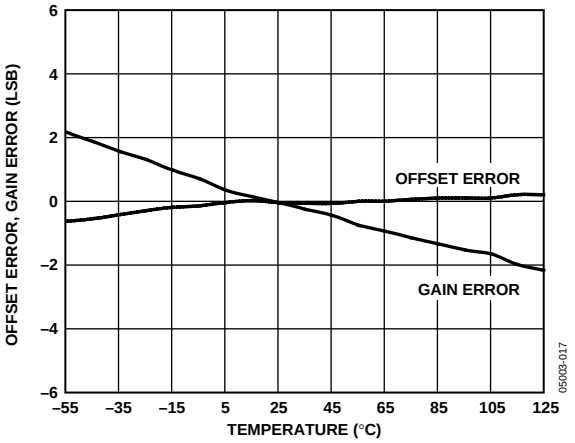


Figure 17. Offset and Gain Error vs. Temperature

APPLICATION INFORMATION

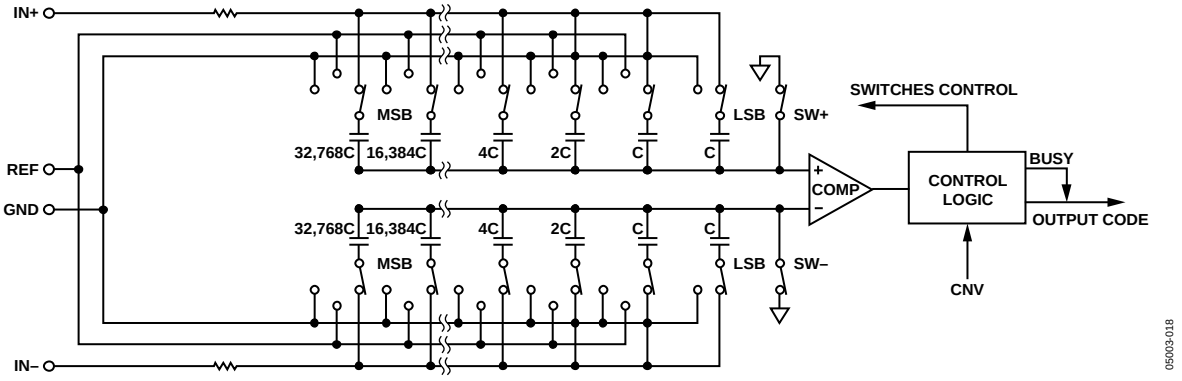


Figure 18. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7694 is a low power, single-supply, 16-bit ADC using a successive approximation architecture. It is capable of converting 250,000 samples per second (250 kSPS) and powers down between conversions. When operating at 100 SPS, for example, it typically consumes 4 μW, ideal for battery-powered applications.

The AD7694 provides the user with on-chip, track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple, multiplexed channel applications.

The AD7694 is specified from 2.7 V to 5.25 V. It is housed in an 8-lead MSOP. The AD7694 is an improved second source to LTC1864 and LTC1864L. For even better performance, the AD7685 should be considered.

CONVERTER OPERATION

The AD7694 is a successive approximation ADC based on a charge redistribution DAC. Figure 18 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase begins. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Thus, the differential voltage between the inputs, IN+ and IN−, captured at the end of the acquisition phase applies to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB, in order to bring the comparator back into a balanced condition.

After the completion of this process, the part returns to the acquisition phase and the control logic generates the ADC output code.

Because the AD7694 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

TRANSFER FUNCTIONS

The ideal transfer function for the AD7694 is shown in Figure 19 and Table 8.

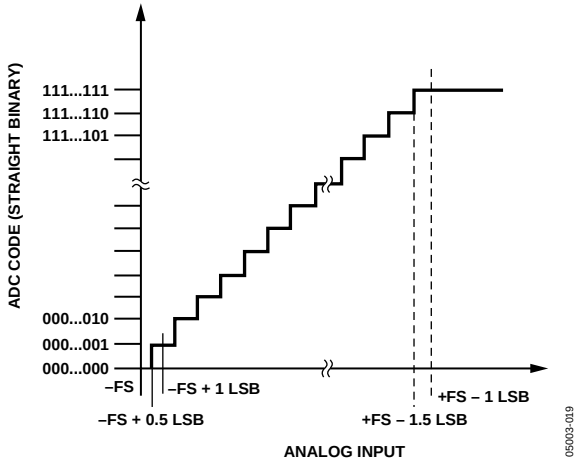


Figure 19. ADC Ideal Transfer Function

Table 8. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output Code Hexadecimal
FSR – 1 LSB	4.999924 V	FFFF[1]
Midscale + 1 LSB	2.500076 V	8001
Midscale	2.5 V	8000
Midscale – 1 LSB	2.499924 V	7FFF
–FSR + 1 LSB	76.3 μV	0001
–FSR	0 V	0000[2]

[1] This is also the code for an overranged analog input ($V_{IN+} – V_{IN-}$ above $V_{REF} – V_{GND}$).
[2] This is also the code for an underranged analog input ($V_{IN+} – V_{IN-}$ below V_{GND}).

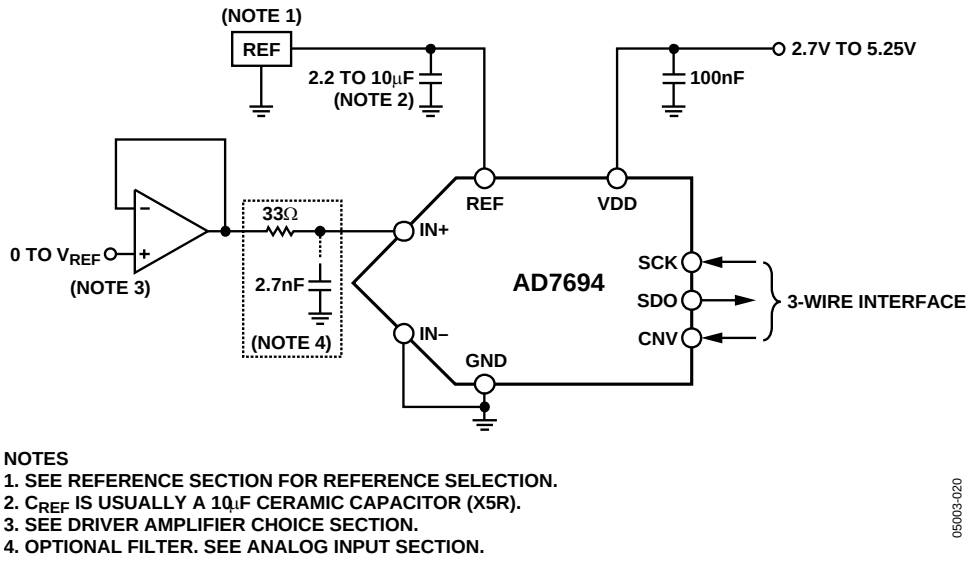


Figure 20. Typical Application Diagram

TYPICAL CONNECTION DIAGRAM

Figure 20 shows an example of the recommended application diagram for the AD7694.

ANALOG INPUT

Figure 21 shows an equivalent circuit of the AD7694 input structure. The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN+ and IN−. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V, because this will cause these diodes to become forward-biased and start conducting current. However, these diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from VDD. In such a case, an input buffer with a short-circuit, current limitation can be used to protect the part.

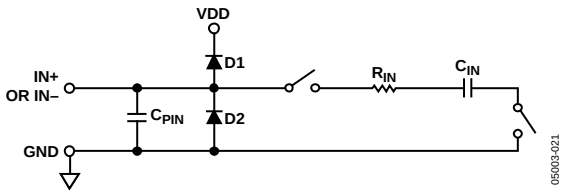


Figure 21. Equivalent Analog Input Circuit

This analog input structure allows the sampling of the differential signal between IN+ and IN−. By using this differential input, small signals common to both inputs are rejected. For instance, by using IN− to sense a remote signal ground, ground potential differences between the sensor and the local ADC ground are eliminated. During the acquisition phase, the impedance of the analog input IN+ can be modeled as a parallel combination of the capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 600 Ω and is a lumped component made up of some serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the AD7694 can be driven directly. Large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The dc performances are less sensitive to the input impedance.

DRIVER AMPLIFIER CHOICE

Although the AD7694 is easy to drive, the driver amplifier needs to meet the following requirements:

- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7694. Note that the AD7694 has a noise much lower than most of the other 16-bit ADCs and, therefore, can be driven by a noisier op amp while preserving the same or better system performance. The noise coming from the driver is filtered by the AD7694 analog input circuit 1-pole, low-pass filter made by R1 and C2 or by the external filter, if one is used.
- For ac applications, the driver needs to have a THD performance suitable to that of the AD7694. Figure 13 gives the THD vs. frequency that the driver should exceed.
- For multichannel, multiplexed applications, the driver amplifier and the AD7694 analog input circuit must be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection.

Table 9. Recommended Driver Amplifiers

Amplifier	Typical Application
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
OP184	Low power, low noise, and low frequency
AD8605, AD8615	5 V single-supply and low power
AD8519	Small, low power, and low frequency
AD8031	High frequency and low power

VOLTAGE REFERENCE INPUT

The AD7694 voltage reference input, REF, has a dynamic input impedance and should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source (for example, an unbuffered reference voltage like the low temperature drift ADR43x reference or a reference buffer using the AD8031 or the AD8605), a 10 µF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with a minimal impact on performance, especially DNL.

POWER SUPPLY

The AD7694 powers down automatically at the end of each conversion phase and, therefore, the power scales linearly with the sampling rate, as shown in Figure 22. This makes the part ideal for a low sampling rate (even a few Hz) and low battery-powered applications.

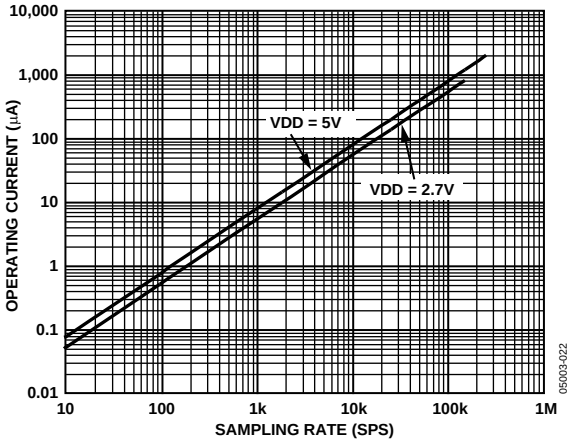
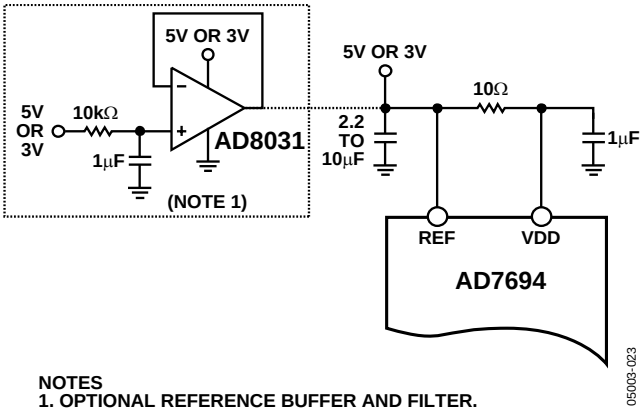


Figure 22. Operating Current vs. Sampling Rate

SUPPLYING THE ADC FROM THE REFERENCE

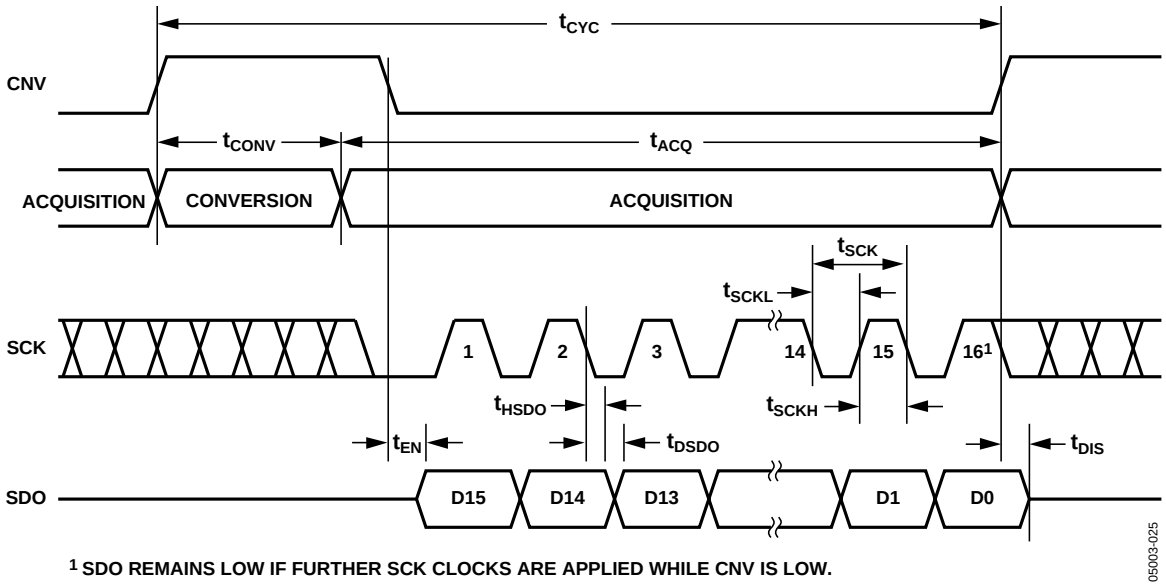
For simplified applications, the AD7694, with its low operating current, can be supplied directly using the reference circuit, as shown in Figure 23. The reference line can be driven by either

- The system power supply directly
- A reference voltage with enough current output capability, such as the ADR43x
- A reference buffer, such as the AD8031, that can also filter the system power supply, as shown in Figure 23



NOTES
1. OPTIONAL REFERENCE BUFFER AND FILTER.

Figure 23. Example of an Application Circuit



1 SDO REMAINS LOW IF FURTHER SCK CLOCKS ARE APPLIED WHILE CNV IS LOW.

Figure 24. Serial Interface Timing

DIGITAL INTERFACE

The AD7694 is compatible with SPI, QSPI, digital hosts, and DSPs, for example, Blackfin® ADSP-BF53x or ADSP-219x. The connection diagram is shown in Figure 25 and the corresponding timing diagram is shown in Figure 24.

A rising edge on CNV initiates a conversion and forces SDO to high impedance. When the conversion is complete, the AD7694 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are clocked by SCK falling edges. The data is valid on both SCK edges.

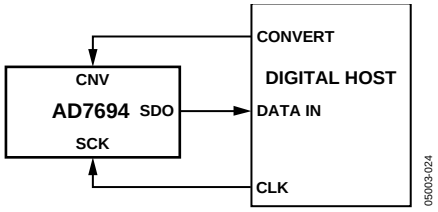


Figure 25. Connection Diagram

LAYOUT

The printed circuit board that houses the AD7694 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7694 with all its analog signals on the left side and all its digital signals on the right side eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7694 is used as a shield. Fast switching signals, such as CNV or clocks, should never run near analog signal paths. Crossover of digital and analog signals should be avoided.

At least one ground plane should be used. It could be common or split between the digital and analog section. In such a case, it should be joined underneath the AD7694s.

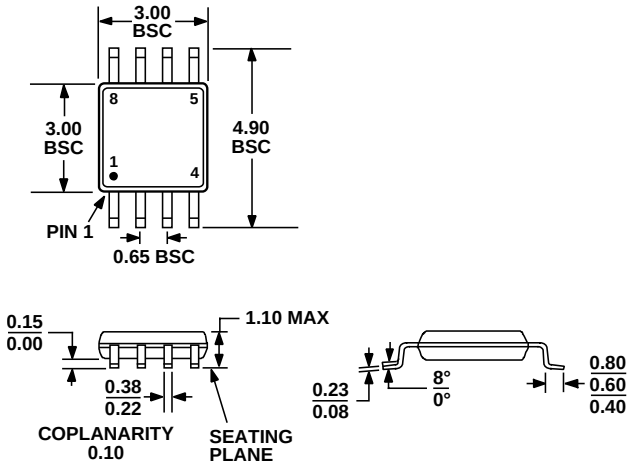
The AD7694 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. That is done by placing the reference decoupling ceramic capacitor close to, and ideally right up against, the REF and GND pins and by connecting these pins with wide, low impedance traces.

Finally, the power supply, VDD, of the AD7694 should be decoupled with a ceramic capacitor, typically 100 nF. This capacitor should be placed close to the AD7694 and connected using short and large traces to provide low impedance paths and reduce the effect of glitches on the power supply lines.

EVALUATING THE AD7694 PERFORMANCE

Other recommended layouts for the AD7694 are outlined in the evaluation board for the AD7694 (EVAL-AD7694SDZ). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-SDP-CB1Z.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 26. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions Shown in Millimeters

ORDERING GUIDE

Model[1, 2, 3]	Integral Nonlinearity	Temperature Range	Package Description	Package Option	Transport Media, Quantity	Branding
AD7694ARMZ	±6 LSB max	–40°C to +85°C	8-Lead MSOP	RM-8	Tube, 50	C4K
AD7694ARMZRL7	±6 LSB max	–40°C to +85°C	8-Lead MSOP	RM-8	Reel, 1,000	C4K
AD7694BRMZ	±4 LSB max	–40°C to +85°C	8-Lead MSOP	RM-8	Tube, 50	C4L
AD7694BRMZRL7	±4 LSB max	–40°C to +85°C	8-Lead MSOP	RM-8	Reel, 1,000	C4L
EVAL-AD7694SDZ			Evaluation Board			
EVAL-SDP-CB1Z			Controller Board			

[1] Z = RoHS Compliance Part.
[2] The EVAL-AD7694SDZ can be used as a standalone evaluation board or in conjunction with the EVAL-SDP-CB1Z for evaluation/demonstration purposes.
[3] The EVAL-SDP-CB1Z allows a PC to control and communicate with all Analog Devices evaluation boards ending in SD designators.

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