CMOS QUAD BILATERAL SWITCH

Check for Samples: CD4066B-Q1

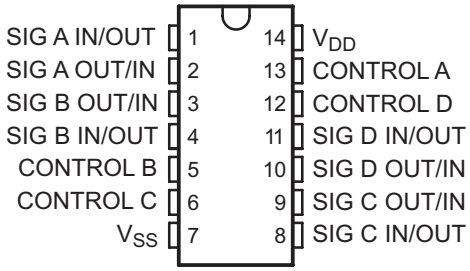
FEATURES

- **Qualified for Automotive Applications**
- **15-V Digital or ±7.5-V Peak-to-Peak Switching**
- **125-Ω Typical On-State Resistance for 15-V Operation**
- **Switch On-State Resistance Matched to Within 5 Ω Over 15-V Signal-Input Range**
- **On-State Resistance Flat Over Full Peak-to-Peak Signal Range**
- **High On/Off Output-Voltage Ratio: 80 dB Typical at f_{is} = 10 kHz, R_L = 1 kΩ**
- **High Degree of Linearity: <0.5% Distortion Typical at f_{is} = 1 kHz, V_{is} = 5 V p-p, $V_{DD} - V_{SS} \geq 10$ V, R_L = 10 kΩ**
- **Extremely Low Off-State Switch Leakage, Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10 pA Typical at $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely High Control Input Impedance (Control Circuit Isolated From Signal Circuit): 10^{12} Ω Typical**
- **Low Crosstalk Between Switches: –50 dB Typical at f_{is} = 8 MHz, R_L = 1 kΩ**
- **Matched Control-Input to Signal-Output Capacitance: Reduces Output Signal Transients**
- **Frequency Response, Switch On = 40 MHz Typical**
- **100% Tested for Quiescent Current at 20 V**
- **5-V, 10-V, and 15-V Parametric Ratings**
- **Latch-Up Exceeds 100mA per JESD78 - Class I**
- **Meets All Requirements of JEDEC Tentative Standard No. 13-B, *Standard Specifications for Description of "B" Series CMOS Devices***

APPLICATIONS

- **Analog Signal Switching/Multiplexing: Signal Gating, Modulator, Squelch Control, Demodulator, Chopper, Commutating Switch**
- **Digital Signal Switching/Multiplexing**
- **Transmission-Gate Logic Implementation**
- **Analog-to-Digital and Digital-to-Analog Conversion**
- **Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain**

E, F, M, NS, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The CD4066B-Q1 is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full signal-input range.

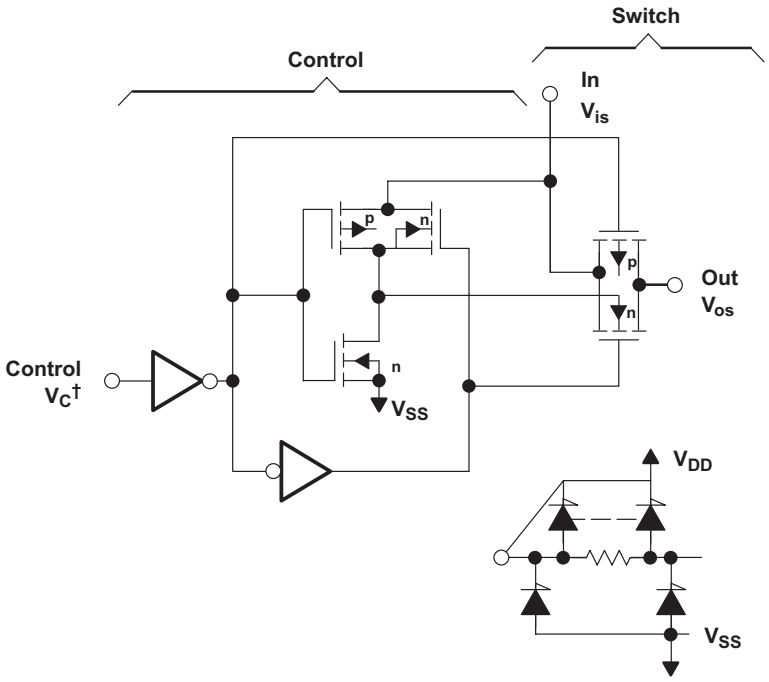
The CD4066B-Q1 consists of four bilateral switches, each with independent controls. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 1, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to VSS (when the switch is off). This configuration eliminates the variation of the switch-transistor threshold voltage with input signal and, thus, keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range. However, for sample-and-hold applications, the CD4016B is recommended.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	CD4066BQDRQ1	CD4066BQ



† All control inputs are protected by the CMOS protection network.

NOTES: A.All p substrates are connected to V_{DD}.
B. Normal operation control-line biasing: switch on (logic 1), $V_C = V_{DD}$; switch off (logic 0), $V_C = V_{SS}$
C. Signal-level range: $V_{SS} \leq V_{is} \leq V_{DD}$

Figure 1. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
DC supply-voltage range, V_{DD} (voltages referenced to V_{SS} terminal)		–0.5 to 20	V
Input voltage range, V_{is} (all inputs)		–0.5 to V_{DD} + 0.5	V
DC input current, IIN (any one input)		±10	mA
Package thermal impedance, θ_{JA} (2)	D package	86	°C/W
ESD Electrostatic discharge(3)	Human-Body Model (HBM)	500	V
	Machine Model (MM)	150	
	Field_Induced_Charged Device Model (CDM)	1000	
Lead temperature (during soldering): At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max		265	°C
Storage temperature range, T_{stg}		–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) Tested in accordance with AEC-Q100.

THERMAL INFORMATION

THERMAL METRIC(1)		CD4066B-Q1 D PACKAGE 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	92.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	52.5	
θ_{JB}	Junction-to-board thermal resistance	46.7	
ψ_{JT}	Junction-to-top characterization parameter	46.4	
ψ_{JB}	Junction-to-board characterization parameter	46.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	18	V
T_A	Operating free-air temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES				UNIT
					–40°C	125°C	25°C		
							TYP	MAX	
I_{DD}	Quiescent device current		0.5	5	0.25	7.5	0.01	0.25	µA
			0.10	10	0.5	15	0.01	0.5	
			0.15	15	1	30	0.01	1	
			0.20	20	5	150	0.02	5	
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})									
r_{on}	On-state resistance (max)	$V_C = V_{DD}$, R_L = 10 kΩ returned to $\frac{V_{DD} \quad V_{SS}}{2}$, $V_{is} = V_{SS}$ to V_{DD}		5	850	1300	470	1050	Ω
				10	330	550	180	400	
				15	210	320	125	240	
Δr_{on}	On-state resistance difference between any two switches	R_L = 10 kΩ, $V_C = V_{DD}$		5			15		Ω
				10			10		
				15			5		
THD	Total harmonic distortion	$V_C = V_{DD}$ = 5 V, V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 10 kΩ, f_{is} = 1-kHz sine wave					0.4%		
	3-dB cutoff frequency (switch on)	$V_C = V_{DD}$ = 5 V, V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ					40		MHz
	–50-dB feedthrough frequency (switch off)	$V_C = V_{SS}$ = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ					1		MHz
I_{is}	Input/output leakage current (switch off) (max)	V_C = 0 V, V_{is} = 18 V, V_{os} = 0 V; and V_C = 0 V, V_{is} = 0 V, V_{os} = 18 V		18	±0.1	±1	$\pm 10^{-5}$	±0.1	µA
	–50-dB crosstalk frequency	V_C(A) = V_{DD} = 5 V, V_C(B) = V_{SS} = -5 V, V_{is}(A) = 5 V_{p-p}, 50-Ω source, R_L = 1 kΩ					8		MHz
t_{pd}	Propagation delay (signal input to signal output)	R_L = 200 kΩ, $V_C = V_{DD}$, V_{SS} = GND, C_L = 50 pF, V_{is} = 10 V (square wave centered on 5 V), t_r, t_f = 20 ns		5			20	40	ns
				10			10	20	
				15			7	15	
C_{is}	Input capacitance	V_{DD} = 5 V, $V_C = V_{SS}$ = –5 V					8		pF
C_{os}	Output capacitance	V_{DD} = 5 V, $V_C = V_{SS}$ = –5 V					8		pF
C_{ios}	Feedthrough	V_{DD} = 5 V, $V_C = V_{SS}$ = –5 V					0.5		pF

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES				UNIT
					–40°C	125°C	25°C TYP	25°C MAX	
CONTROL (V_C)									
V_{ILC}	Control input, low voltage (max)	$\|I_{is}\|$ < 10 mA, $V_{is} = V_{SS}$, $V_{OS} = V_{DD}$, and $V_{is} = V_{DD}$, $V_{OS} = V_{SS}$		5	1	1		1	V
				10	2	2		2	
				15	2	2		2	
V_{IHC}	Control input, low voltage	See Figure 6		5	3.5 (MIN)				V
				10	7 (MIN)				
				15	11 (MIN)				
I_{IN}	Input current (max)	$V_{is} \le V_{DD}$, $V_{DD} - V_{SS}$ = 18 V, $V_{CC} \le V_{DD} - V_{SS}$		18	±0.1	±1	$\pm 10^{-5}$	±0.1	µA
	Crosstalk (control input to signal output)	V_C = 10 V (square wave), t_r, t_f = 20 ns, R_L = 10 kΩ		10			50		mW
	Turn-on and turn-off propagation delay	$V_{IN} = V_{DD}$, t_r, t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ		5			35	70	ns
				10			20	40	
				15			15	30	
	Maximum control input repetition rate	$V_{is} = V_{DD}$, V_{SS} = GND, R_L = 1 kΩ to GND, C_L = 50 pF, V_C = 10 V (square wave centered on 5 V), t_r, t_f = 20 ns, V_{os} = 1/2 V_{os} at 1 kHz		5			6		MHz
				10			9		
				15			9.5		
C_i	Input capacitance						5		pF

SWITCHING CHARACTERISTICS

V_{DD} (V)	SWITCH INPUT				SWITCH OUTPUT, V_{os} (V)	
	V_{is} (V)	I_{is} (mA)				
		–40°C	25°C	125°C	MIN	MAX
5	0	0.61	0.51	0.36		0.4
5	5	–0.61	–0.51	–0.36	4.6	
10	0	1.5	1.3	0.9		
10	10	–1.6	–1.3	–0.9		
15	0	4	3.4	2.4		1.5
15	15	–4	–3.4	–2.4	13.5	

TYPICAL CHARACTERISTICS

TYPICAL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE (ALL TYPES)

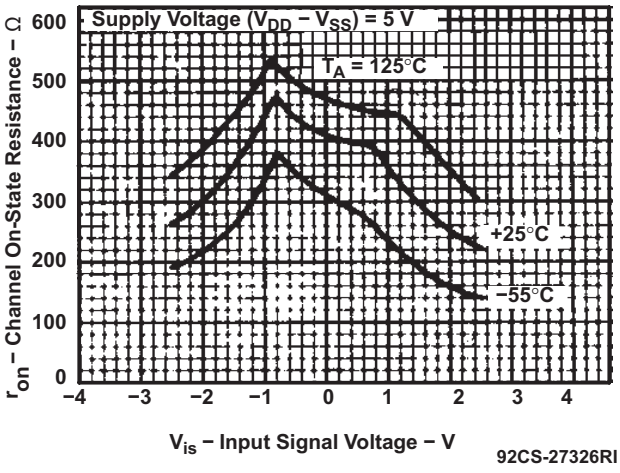


Figure 2.

TYPICAL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE (ALL TYPES)

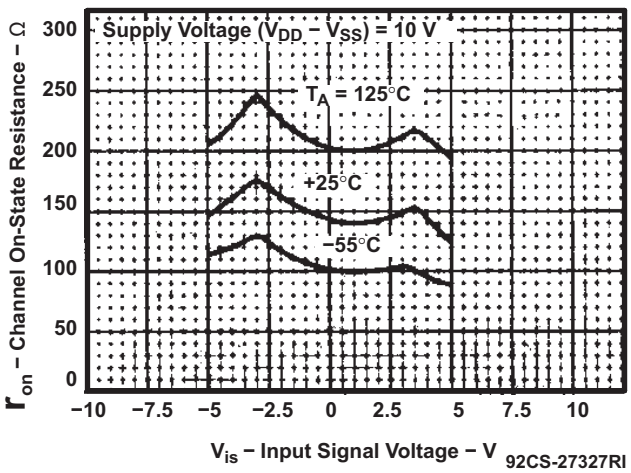


Figure 3.

TYPICAL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE (ALL TYPES)

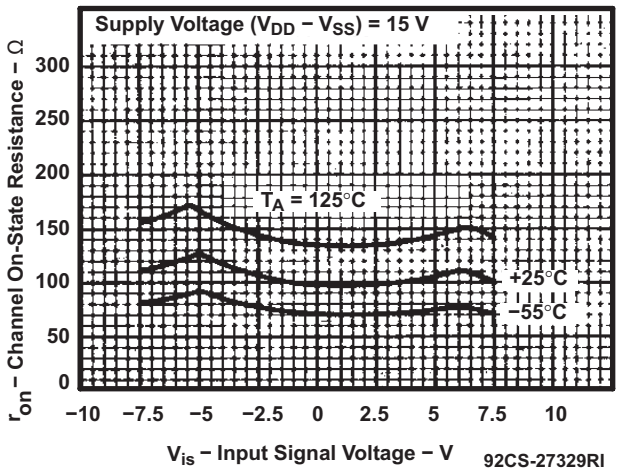


Figure 4.

TYPICAL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE (ALL TYPES)

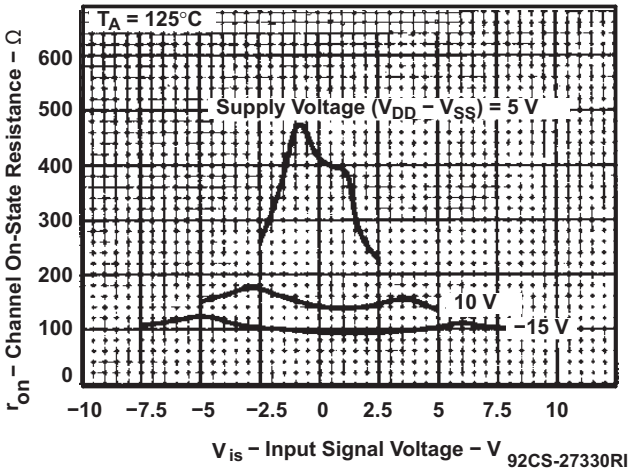


Figure 5.

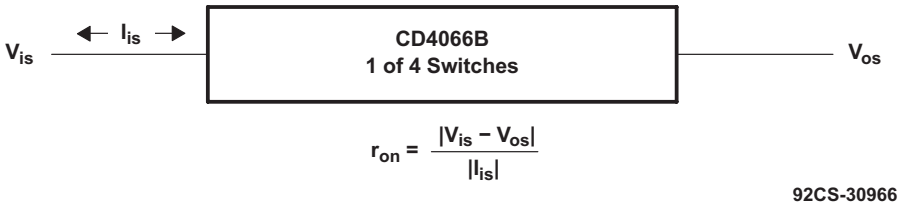


Figure 6. Determination of ron as a Test Condition for Control-Input High-Voltage (VIHC) Specification

TYPICAL CHARACTERISTICS (continued)

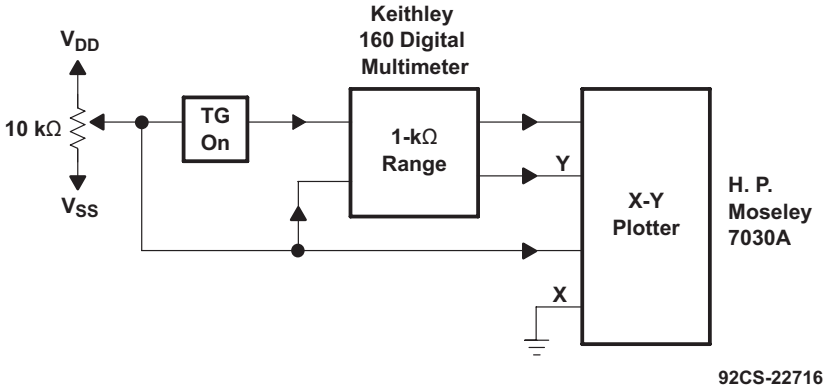


Figure 7. Channel On-State Resistance Measurement Circuit

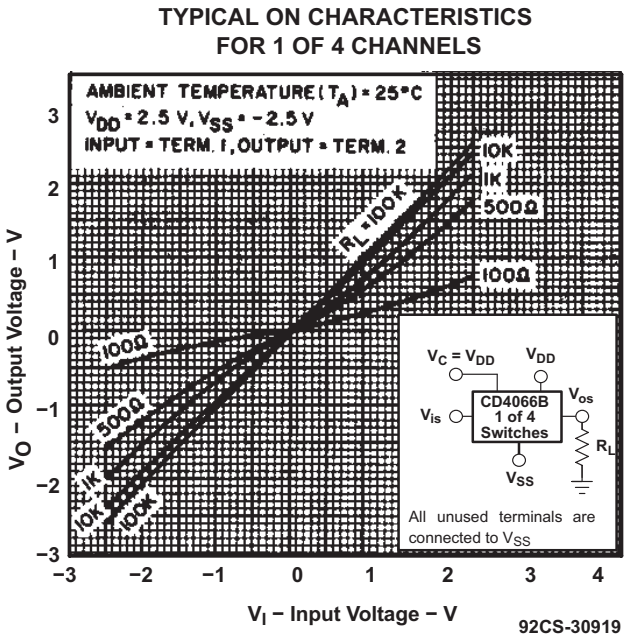


Figure 8.

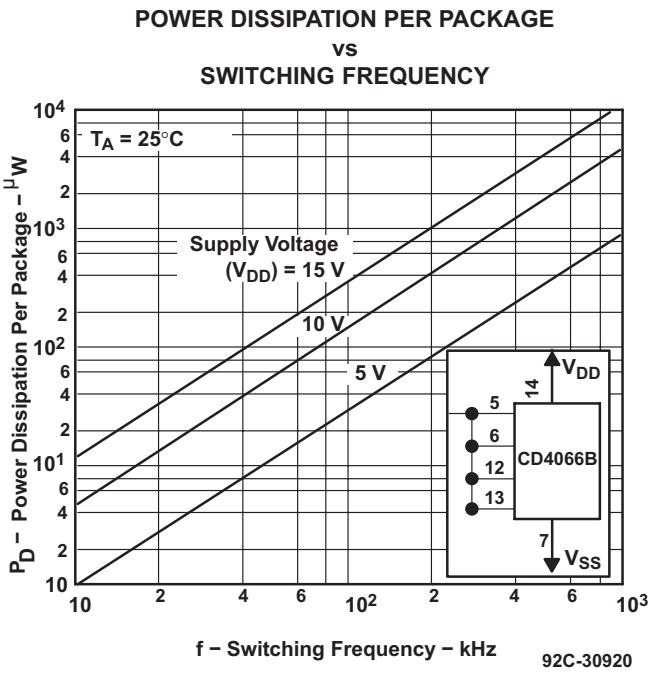
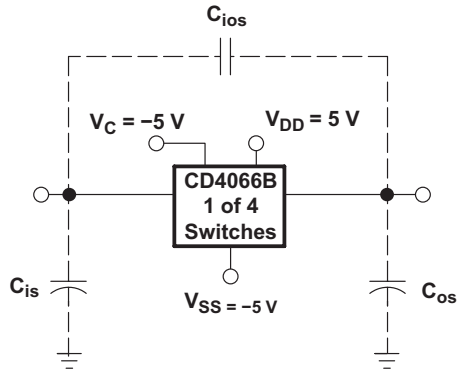


Figure 9.

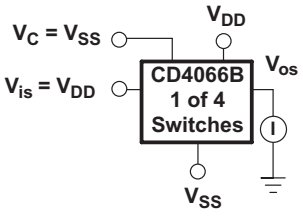
TYPICAL CHARACTERISTICS (continued)



92CS-30921

Measured on Boonton capacitance bridge, model 75a (1 MHz); test-fixture capacitance nulled out.

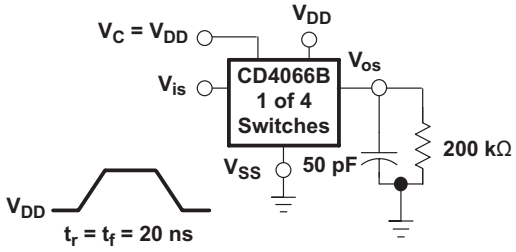
Figure 10. Typical On Characteristics for One of Four Channels



92CS-30922

All unused terminals are connected to V_{SS}.

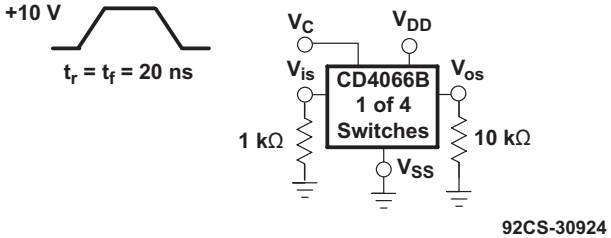
Figure 11. Off-Switch Input or Output Leakage



92CS-30923

All unused terminals are connected to V_{SS}.

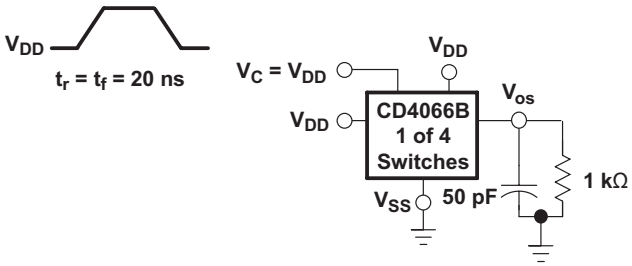
Figure 12. Propagation Delay Time Signal Input (V_{is}) to Signal Output (V_{os})



92CS-30924

All unused terminals are connected to V_{SS}.

Figure 13. Crosstalk-Control Input to Signal Output

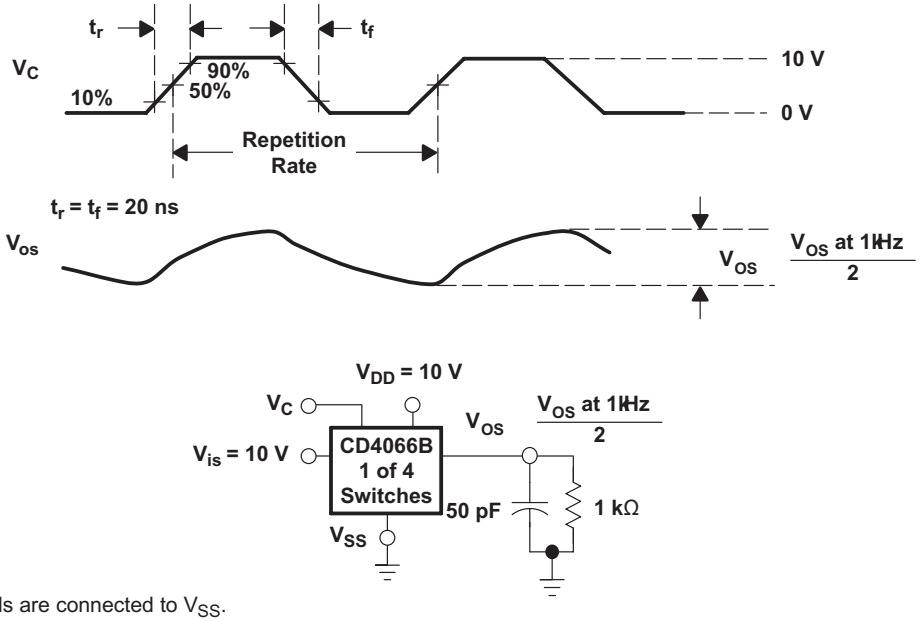


92CS-30925

NOTES: A.All unused terminals are connected to V_{SS}.
B. Delay is measured at V_{os} level of +10% from ground (turn-on) or on-state output level (turn-off).

Figure 14. Propagation Delay, t_{PLH}, t_{PHL} Control-Signal Output

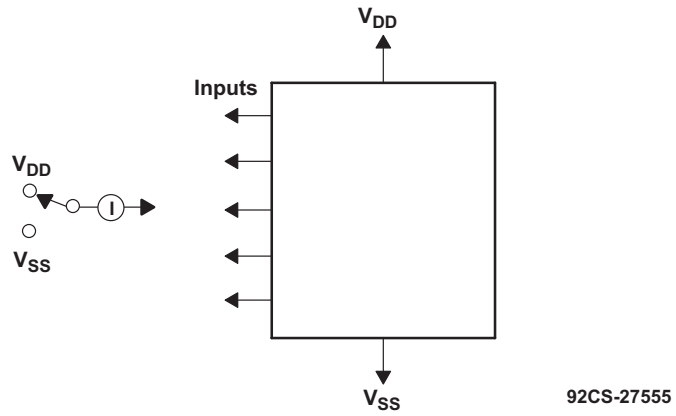
TYPICAL CHARACTERISTICS (continued)



All unused terminals are connected to V_{SS}.

92CS-30925

Figure 15. Maximum Allowable Control-Input Repetition Rate



92CS-27555

Measure inputs sequentially to both V_{DD} and V_{SS}. Connect all unused inputs to either V_{DD} or V_{SS}. Measure control inputs only.

Figure 16. Input Leakage-Current Test Circuit

TYPICAL CHARACTERISTICS (continued)

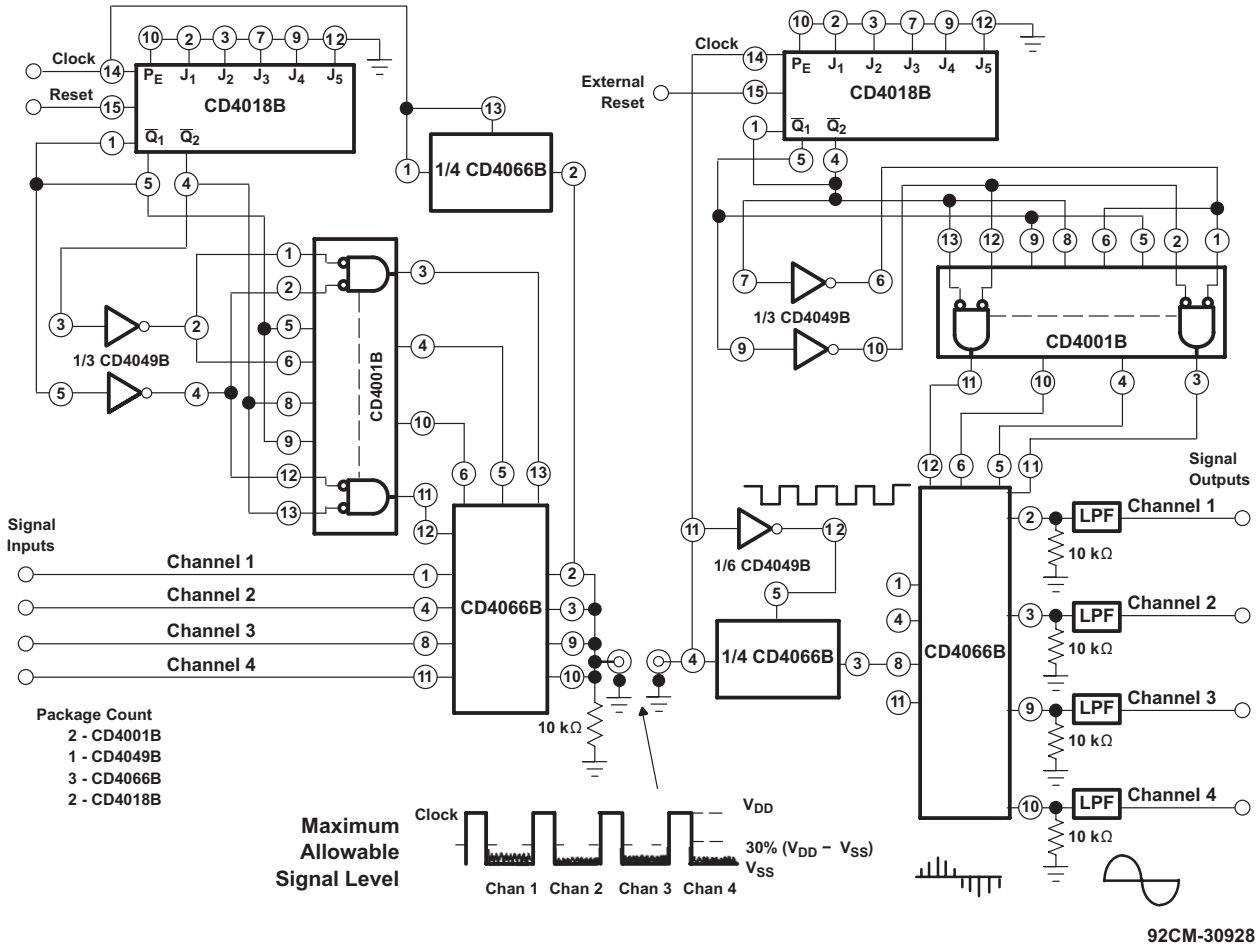


Figure 17. Four-Channel PAM Multiplex System Diagram

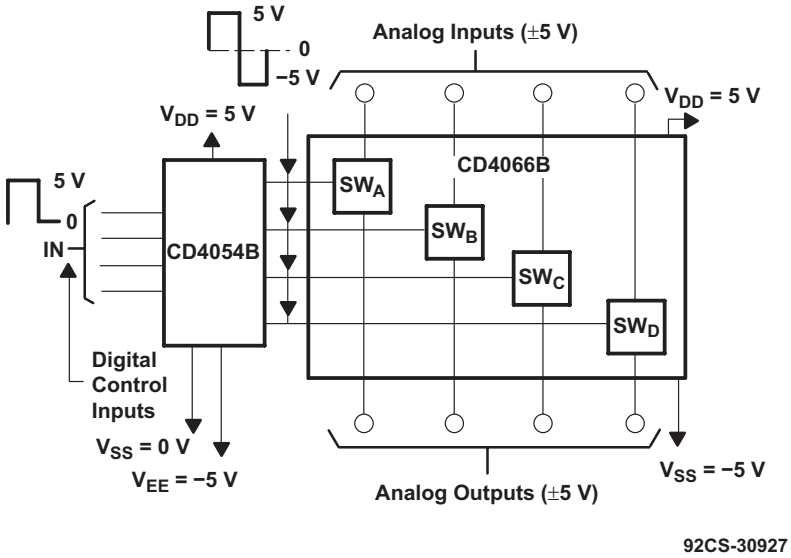


Figure 18. Bidirectional Signal Transmission Via Digital Control Logic

APPLICATION INFORMATION

In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B-Q1 bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B-Q1.

In certain applications, the external load-resistor current can include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from r_{on} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD4066BQDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4066BQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF CD4066B-Q1 :

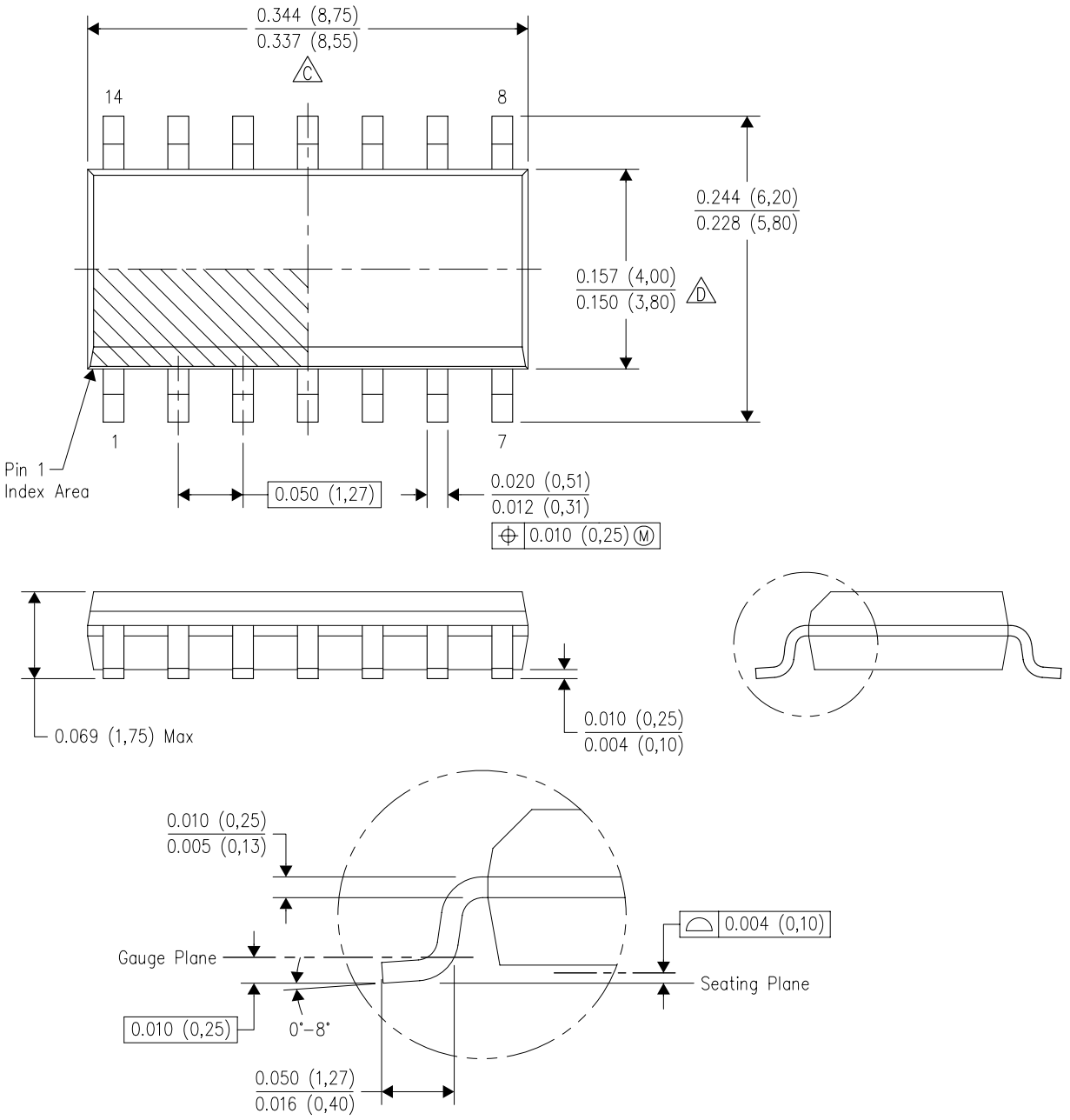
- Catalog: CD4066B

- Military: CD4066B-MIL

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

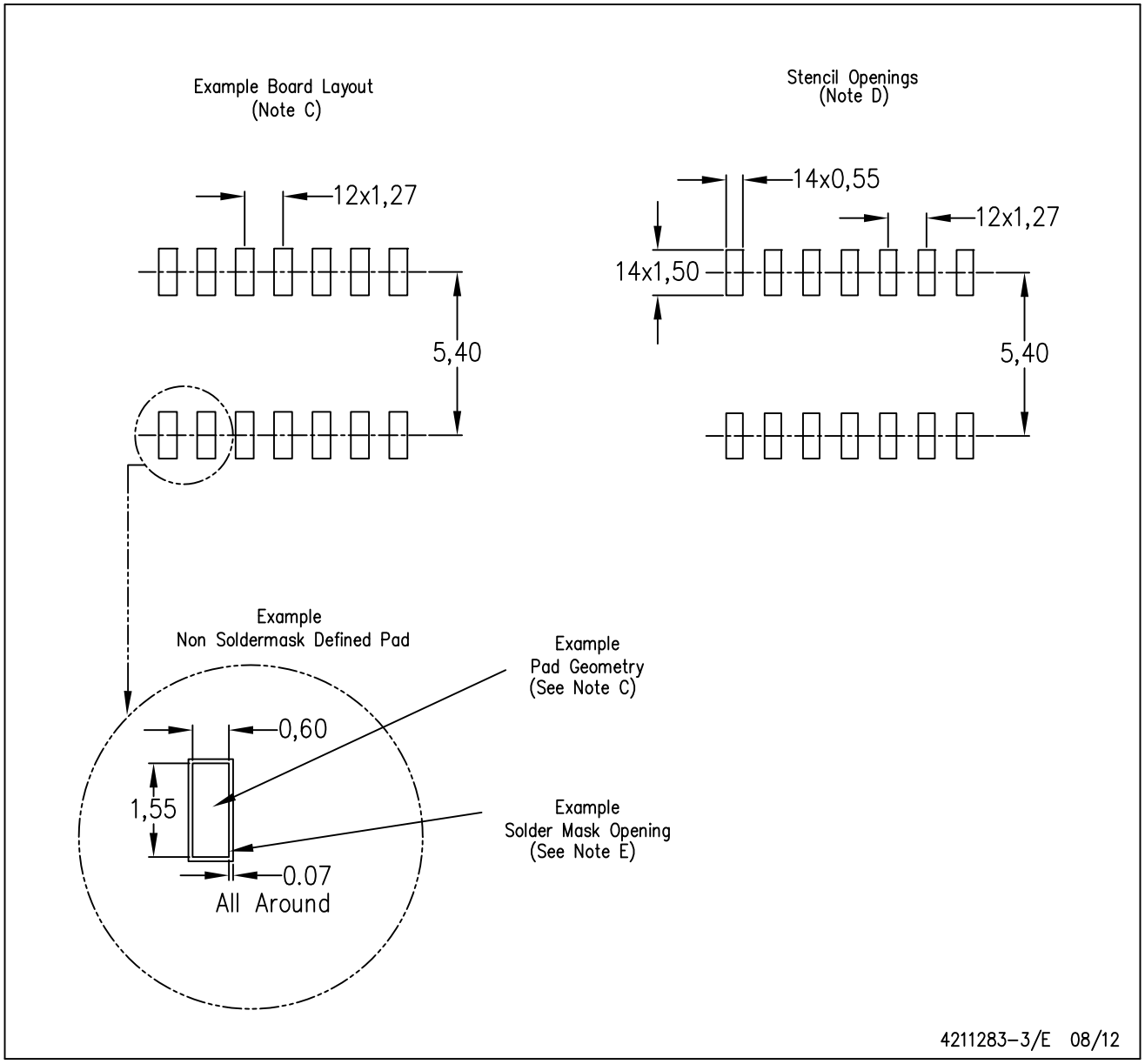
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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