

FEATURES

Output power for 1 dB compression (P1dB): 16 dBm typical

Saturated output power (P_{SAT}): 19.5 dBm typical

Gain: 15 dB typical

Noise figure: 2.0 dB typical

Output third-order intercept (IP3): 26 dBm typical

Supply voltage: 5 V at 64 mA

50 Ω matched input/output

APPLICATIONS

Test instrumentation

Military and space

FUNCTIONAL BLOCK DIAGRAM

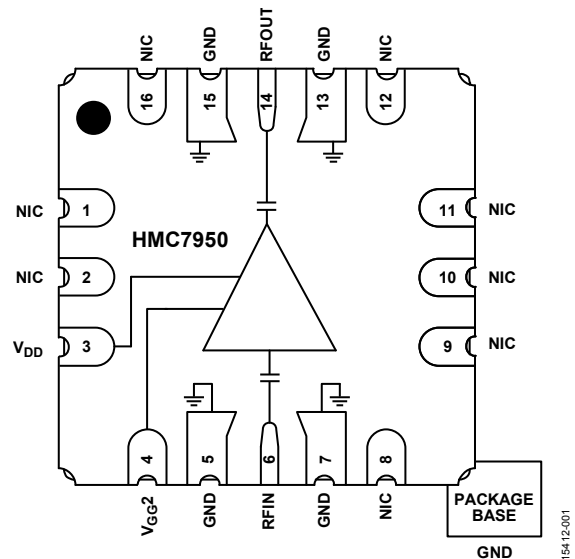


Figure 1.

GENERAL DESCRIPTION

The [HMC7950](#) is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC). The [HMC7950](#) is a wideband low noise amplifier that operates between 2 GHz and 28 GHz. The amplifier typically provides 15 dB of gain, 2.0 dB of noise figure, 26 dBm of output IP3, and 16 dBm of output power for 1 dB gain compression, requiring 64 mA from a 5 V supply. The [HMC7950](#)

is self biased with only a single positive supply needed to achieve a drain current, I_{DD}, of 64 mA. The [HMC7950](#) also has a gain control option, V_{GG2}. The [HMC7950](#) amplifier input/outputs are internally matched to 50 Ω and dc blocked. It comes in a 6 mm $\times$ 6 mm, 16-terminal LCC SMT ceramic package that is easy to handle and assemble.

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REVISION HISTORY

9/2017—Rev. 0 to Rev. A	
Added Figure 37; Renumbered Sequentially	11
1/2017—Revision 0: Initial Version	

SPECIFICATIONS

2 GHz TO 5 GHz FREQUENCY RANGE

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, $V_{GG2} = \text{open}$, unless otherwise stated. When using V_{GG2} , it is recommended to limit V_{GG2} from -2 V to $+2.6\text{ V}$. P_{OUT} is output power.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			2		5	GHz
GAIN			13.5	15.5		dB
Gain Variation Over Temperature				0.004		dB/ $^\circ\text{C}$
RETURN LOSS						
Input				12		dB
Output				13		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		13	16.5		dBm
Saturated Output Power	P_{SAT}			20.5		dBm
Output Third-Order Intercept	IP3	Measurement taken at $P_{OUT}/\text{tone} = 4\text{ dBm}$		26.5		dBm
NOISE FIGURE	NF			3.0	4.5	dB

5 GHz TO 18 GHz FREQUENCY RANGE

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, $V_{GG2} = \text{open}$, unless otherwise stated. When using V_{GG2} , it is recommended to limit V_{GG2} from -2 V to $+2.6\text{ V}$. P_{OUT} is output power.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			5		18	GHz
GAIN			13.3	15		dB
Gain Variation Over Temperature				0.007		dB/ $^\circ\text{C}$
RETURN LOSS						
Input				18		dB
Output				14		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		13	16		dBm
Saturated Output Power	P_{SAT}			19.5		dBm
Output Third-Order Intercept	IP3	Measurement taken at $P_{OUT}/\text{tone} = 4\text{ dBm}$		26		dBm
NOISE FIGURE	NF			2.0	3.5	dB

18 GHz TO 28 GHz FREQUENCY RANGE

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, $V_{GG2} = \text{open}$, unless otherwise stated. When using V_{GG2} , it is recommended to limit V_{GG2} from -2 V to $+2.6\text{ V}$. P_{OUT} is output power.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			18		28	GHz
GAIN			13	16.5		dB
Gain Variation over Temperature				0.012		dB/ $^\circ\text{C}$
RETURN LOSS						
Input				19		dB
Output				16		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		10	14.5		dBm
Saturated Output Power	P_{SAT}			17		dBm
Output Third-Order Intercept	IP3	Measurement taken at $P_{OUT}/\text{tone} = 4\text{ dBm}$		24		dBm
NOISE FIGURE	NF			2.8	5	dB

DC SPECIFICATIONS**Table 4.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY CURRENT						
Total Supply Current	I_{DD}			64	100	mA
Total Supply Current vs. V_{DD}						
$I_{DD} = 58\text{ mA}$				3		V
$I_{DD} = 61\text{ mA}$				4		V
$I_{DD} = 64\text{ mA}$				5		V
$I_{DD} = 66\text{ mA}$				6		V
$I_{DD} = 69\text{ mA}$				7		V
SUPPLY VOLTAGE	V_{DD}		3	5	7	V
V_{GG2} PIN	V_{GG2}	Normal condition is $V_{GG2} = \text{open}$	-2.0		2.6	V

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage (V_{DD})	8 V
Second Gate Bias Voltage (V_{GG2})	–2.5 V to +3 V
Radio Frequency Input Power (RFIN)	20 dBm
Channel Temperature	175°C
Continuous Power Dissipation (P_{DISS}), $T_A = 85^\circ\text{C}$ (Derate 17.2 mW/°C Above 85°C)	1.55 W
Maximum Peak Reflow Temperature (MSL3) ¹	260°C
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
ESD Sensitivity, Human Body Model (HBM)	250 V (Class 1A)

¹ See the Ordering Guide section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
EP-16-2 ¹	58	°C/W

¹ Channel to ground pad. See JEDEC Standard JESD51-2 for additional information on optimizing the thermal impedance

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

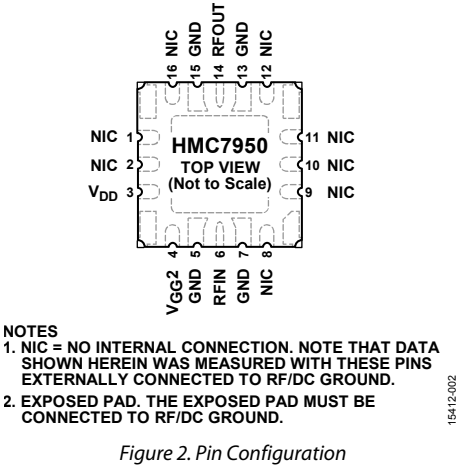
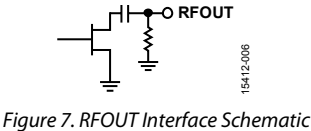
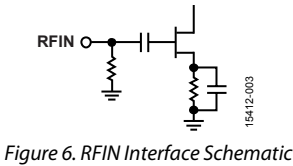
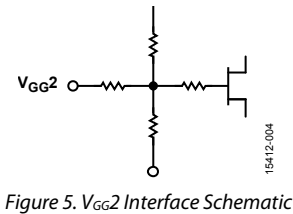
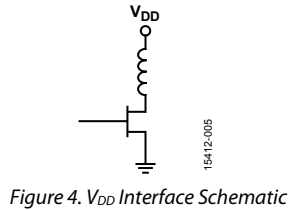
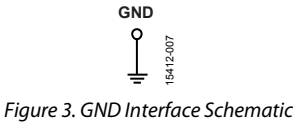


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin	Mnemonic	Description
1, 2, 8, 9, 10, 11, 12, 16	NIC	No Internal Connection. Note that data shown herein was measured with these pins externally connected to RF/dc ground. See Figure 3 for the interface schematic.
3	V _{DD}	Power Supply Voltage for the Amplifier. Connect a dc bias to provide drain current (I _{DD}). See Figure 4 for the interface schematic.
4	V _{GG2}	Gain Control. This pin is dc-coupled and accomplishes gain control by reducing the internal voltage and becoming more negative. See Figure 5 for the interface schematic.
5, 7, 13, 15	GND	These pins must be connected to RF/dc ground. See Figure 3 for the interface schematic.
6	RFIN	Radio Frequency (RF) Input. This pin is ac-coupled, but has a large resistor to GND for ESD protection, and matched to 50 Ω. See Figure 6 for the interface schematic.
14	RFOUT	RF Output. This pin is ac-coupled, but has a large resistor to GND for ESD protection, and matched to 50 Ω. See Figure 7 for the interface schematic.
	EPAD (GND)	Exposed Pad (Ground). The exposed pad must be connected to RF/dc ground. See Figure 3 for the interface schematic.

INTERFACE SCHEMATICS



TYPICAL PERFORMANCE CHARACTERISTICS

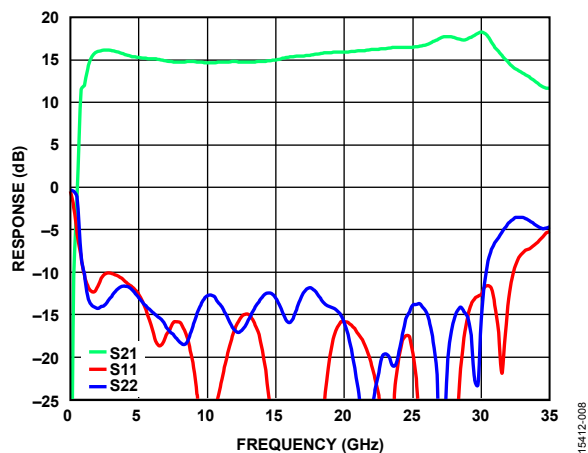


Figure 8. Response (Gain and Return Loss) vs. Frequency

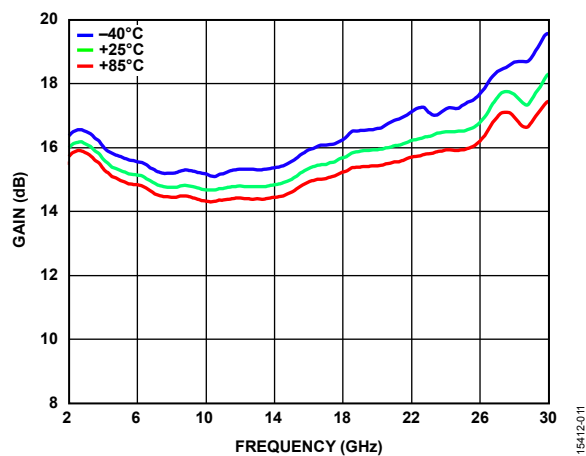


Figure 11. Gain vs. Frequency at Various Temperatures

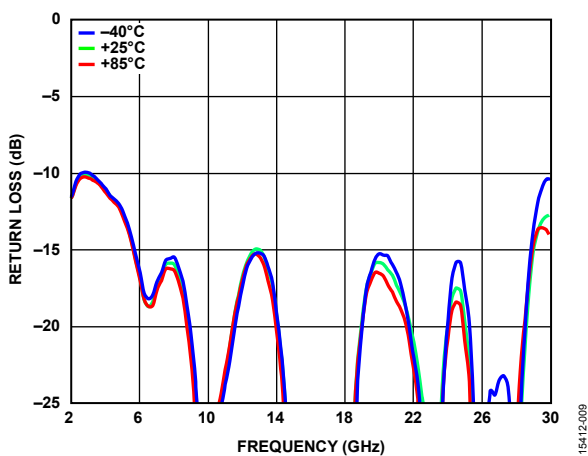


Figure 9. Input Return Loss vs. Frequency at Various Temperatures

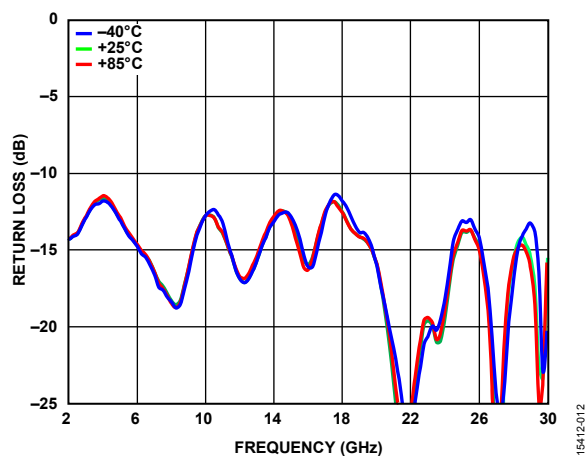


Figure 12. Output Return Loss vs. Frequency at Various Temperatures

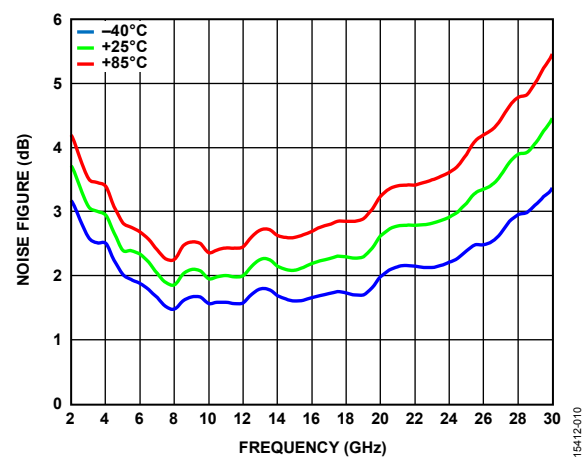


Figure 10. Noise Figure vs. Frequency at Various Temperatures

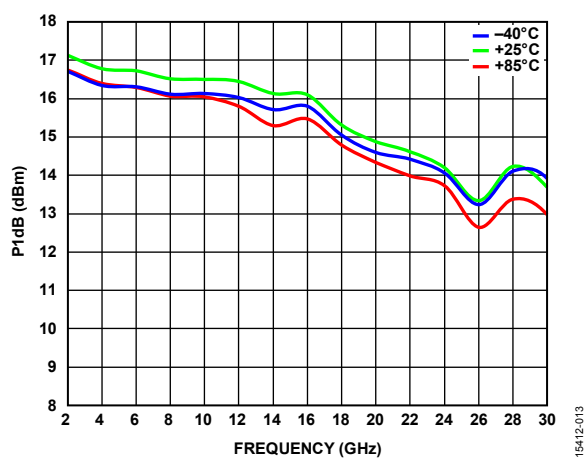


Figure 13. P1dB vs. Frequency at Various Temperatures

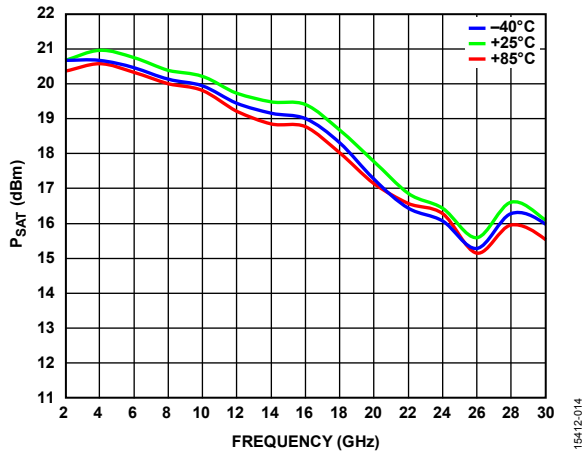


Figure 14. P_{SAT} vs. Frequency at Various Temperatures

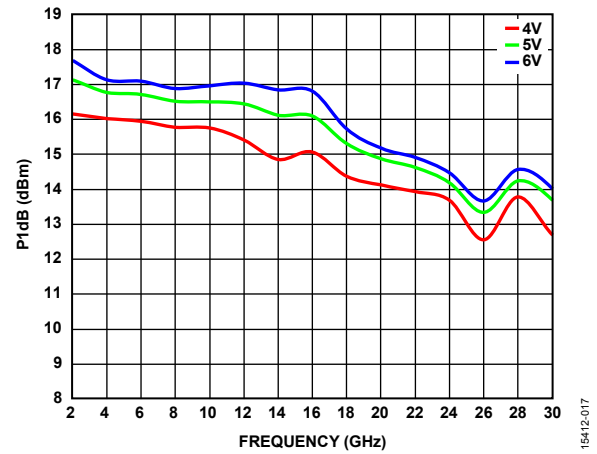


Figure 17. P_{1dB} vs. Frequency at Various Supply Voltages

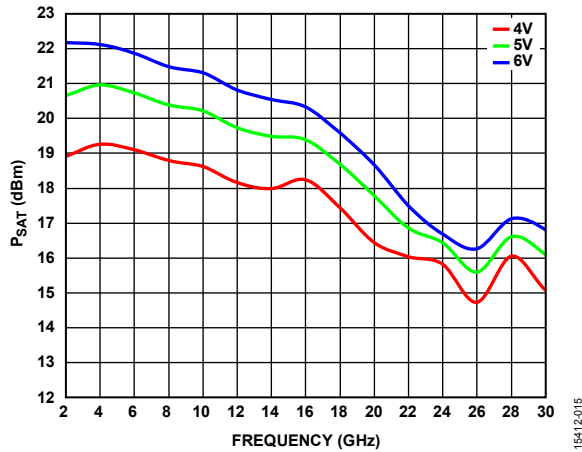


Figure 15. P_{SAT} vs. Frequency at Various Supply Voltages

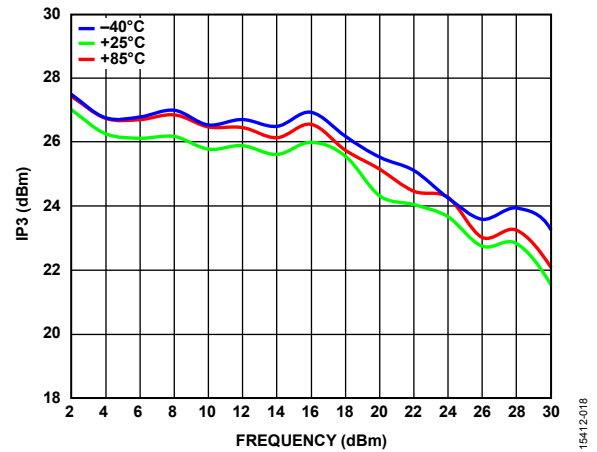


Figure 18. Output IP_3 vs. Frequency at Various Temperatures, $P_{OUT/Tone} = 4 \text{ dBm}$

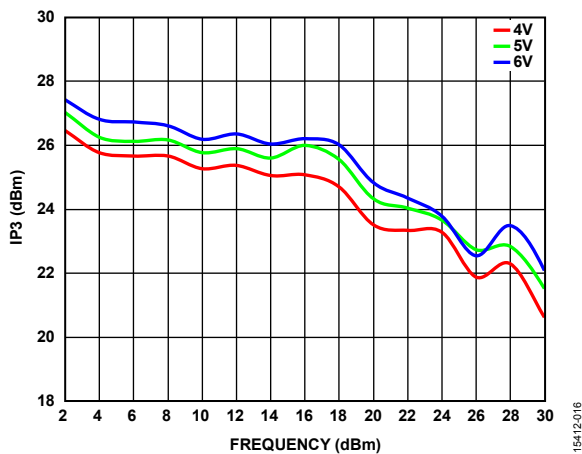


Figure 16. Output IP_3 vs. Frequency at Various Supply Voltages $P_{OUT/Tone} = 4 \text{ dBm}$

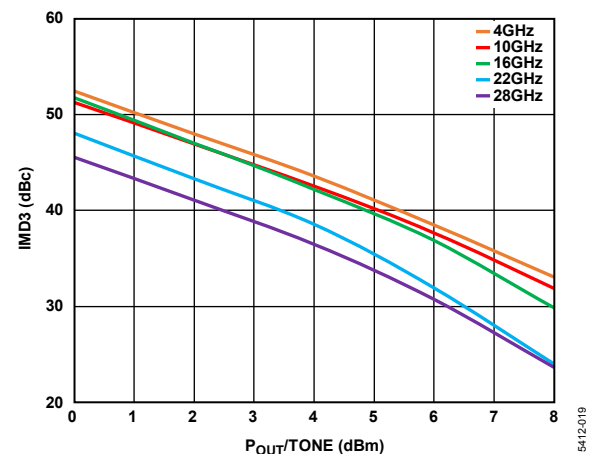


Figure 19. Output Third-Order Intermodulation Distortion (IMD_3) vs. $P_{OUT/TONE}$ at Various Frequencies, $V_{DD} = 4 \text{ V}$

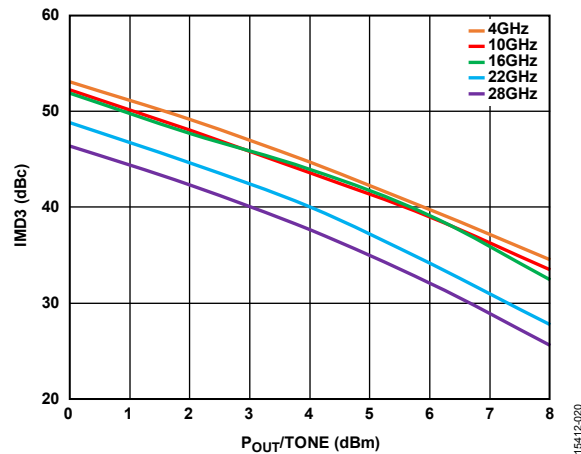
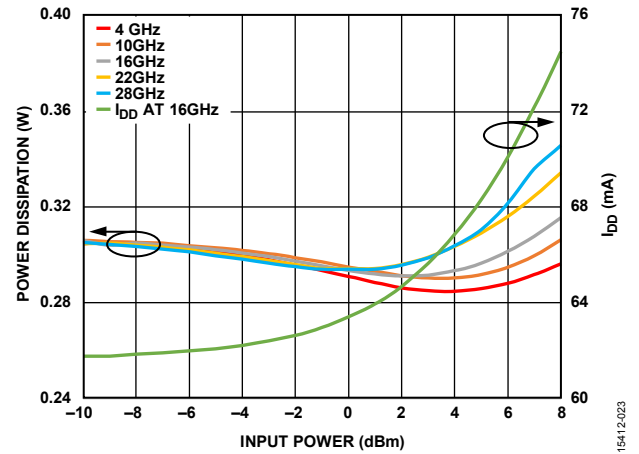
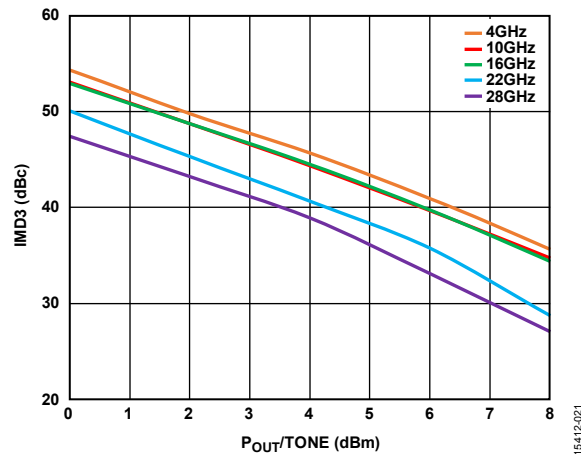
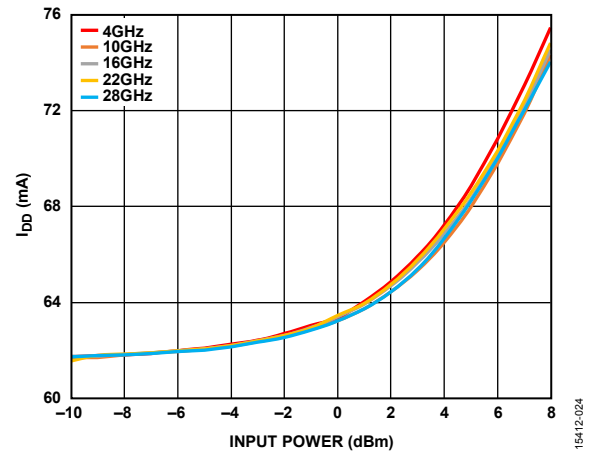
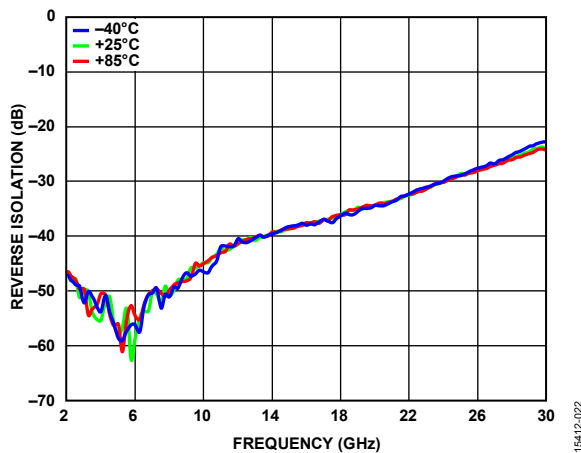
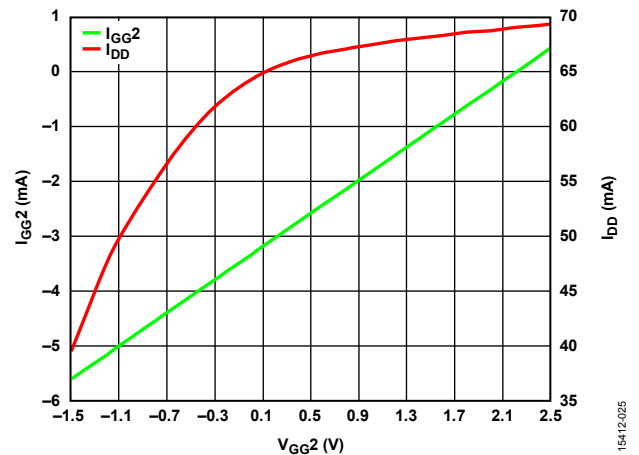
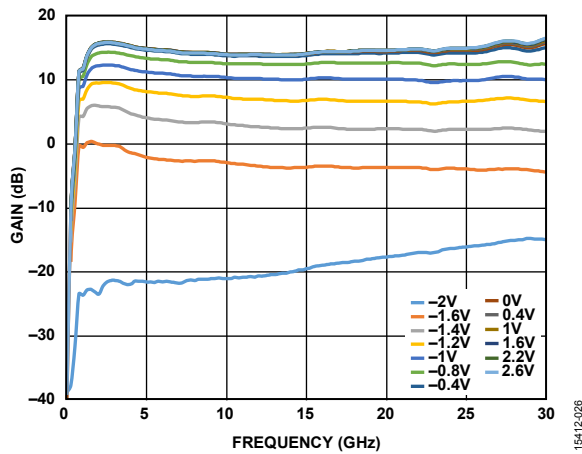
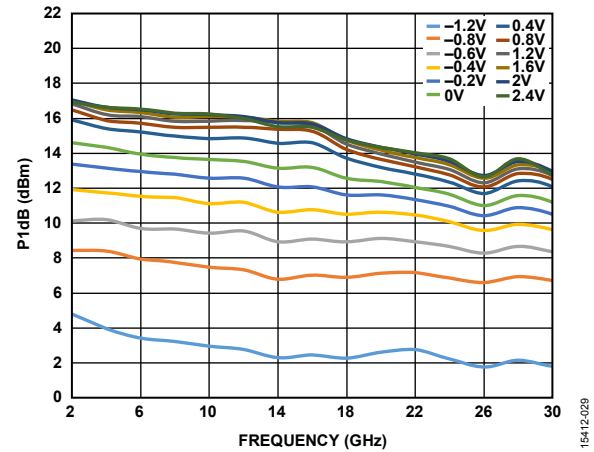
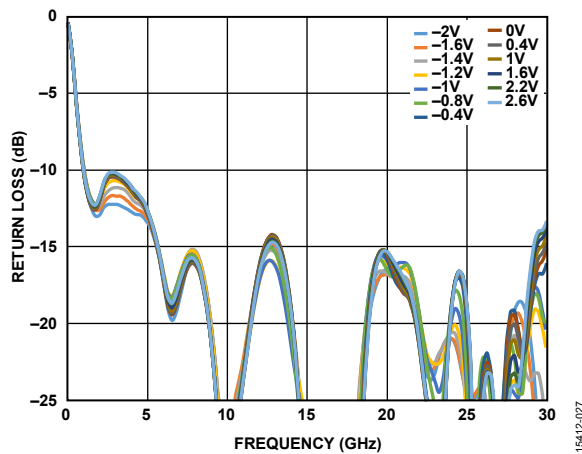
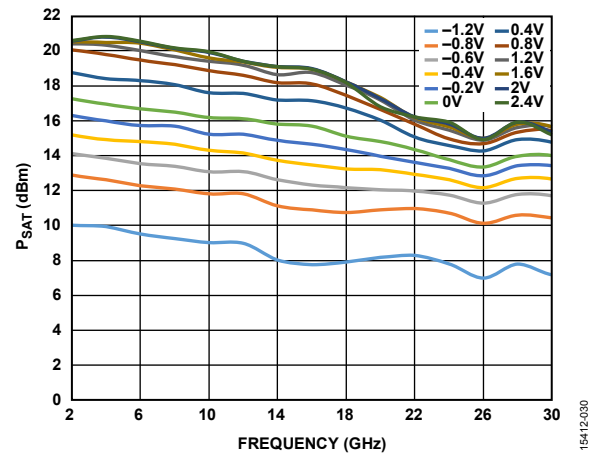
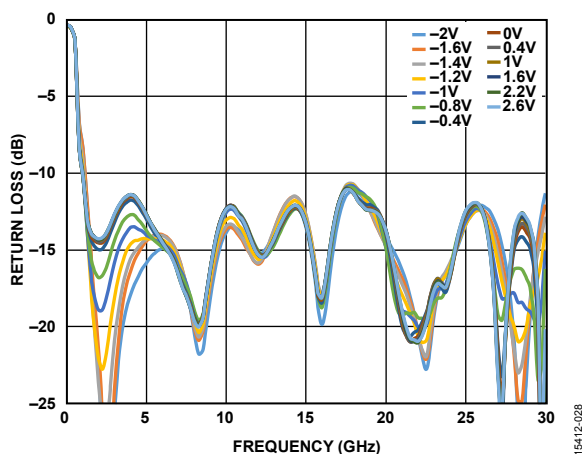
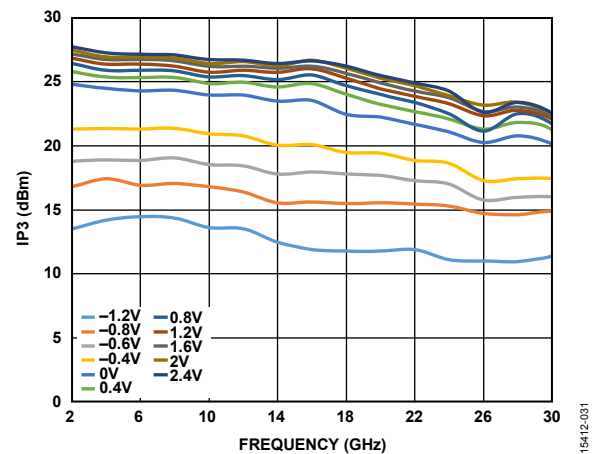
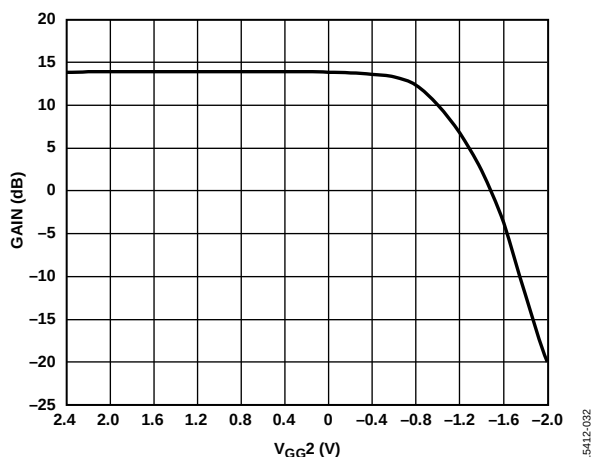
Figure 20. Output IMD3 vs. $P_{OUT}/Tone$ at Various Frequencies, $V_{DD} = 5 V$ Figure 23. Power Dissipation and I_{DD} vs. Input Power at Various Frequencies, 16 GHz, $T_A = 85^\circ C$ Figure 21. Output IMD3 vs. $P_{OUT}/Tone$ at Various Frequencies, $V_{DD} = 6 V$ Figure 24. I_{DD} vs. Input Power at Various Frequencies

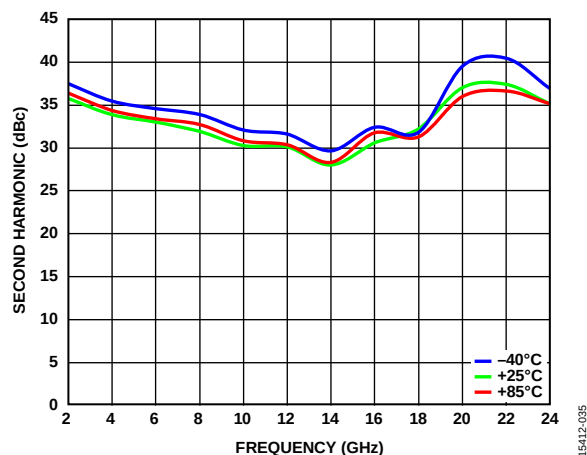
Figure 22. Reverse Isolation vs. Frequency at Various Temperatures

Figure 25. I_{GG2} and I_{DD} vs. V_{GG2} at 14 GHz, Input Power (P_{IN}) = 0 dBm

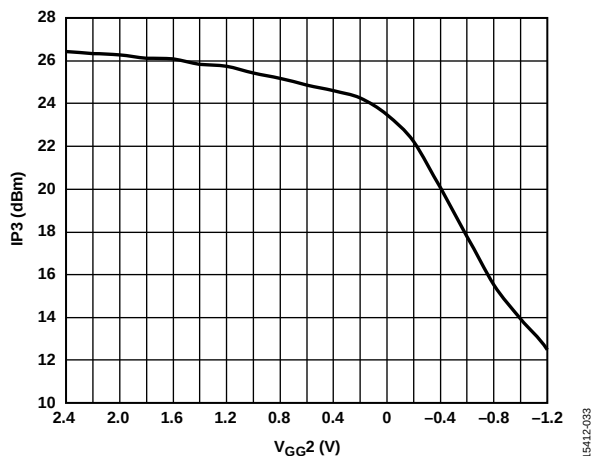
Figure 26. Gain vs. Frequency at Various V_{GG2} Voltage LevelsFigure 29. P1dB vs. Frequency at Various V_{GG2} Voltage LevelsFigure 27. Input Return Loss vs. Frequency at Various V_{GG2} Voltage LevelsFigure 30. P_{SAT} vs. Frequency at Various V_{GG2} Voltage LevelsFigure 28. Output Return Loss vs. Frequency at Various V_{GG2} Voltage LevelsFigure 31. Output IP3 vs. Frequency at Various V_{GG2} Voltage Levels, $P_{OUT}/Tone = 4$ dBm

Figure 32. Gain vs. V_{GG2} at 14 GHz

15412-032

Figure 35. Second Harmonic vs. Frequency at Various Temperatures, $P_{OUT} = 0$ dBm

15412-035

Figure 33. Output IP3 vs. V_{GG2} at 14 GHz

15412-033

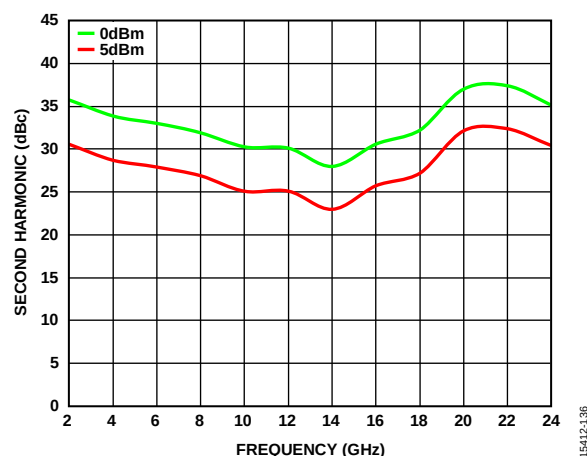
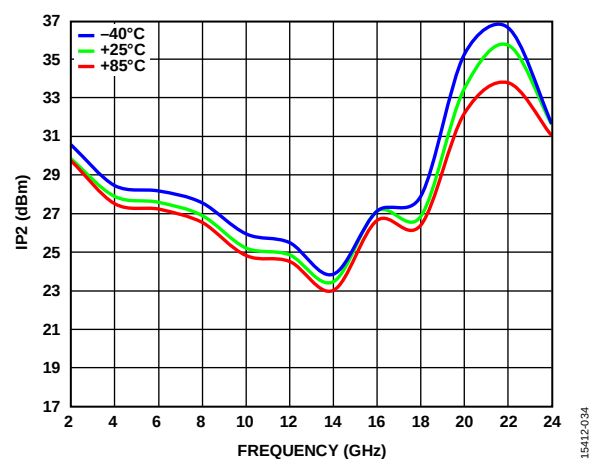
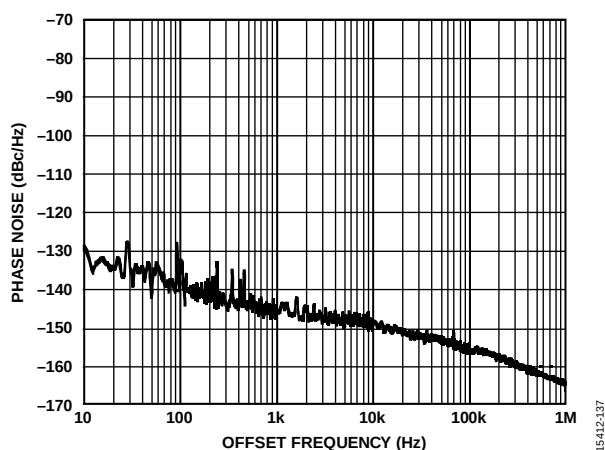


Figure 36. Second Harmonic vs. Frequency at Various Output Powers

15412-136

Figure 34. Output IP2 vs. Frequency at Various Temperatures, $P_{OUT}/Tone = 4$ dBm

15412-034

Figure 37. Additive Phase Noise vs. Offset Frequency, RF Frequency = 8 GHz, RF Input Power = 2.5 dBm (P_{1dB})

15412-137

THEORY OF OPERATION

The HMC7950 is a GaAs, pHEMT, MMIC low noise amplifier. Its basic architecture is that of a single-supply, biased cascode distributed amplifier with an integrated RF choke for the drain. The cascode distributed architecture uses a fundamental cell consisting of a stack of two field effect transistors (FETs) with the source of the upper FET connected to the drain of the lower FET. The fundamental cell is then duplicated several times, with a transmission line feeding the RFIN signal to the gates of the lower FETs and a separate transmission line interconnecting the drains of the upper FETs and routing the amplified signal to the RFOUT pin. Additional circuit design techniques around each cell optimize the overall performance for broadband operation. The major benefit of this architecture is that high performance is maintained across a bandwidth far greater than a single instance of the fundamental cell can provide. A simplified schematic of this architecture is shown in Figure 38.

Although the gate bias voltages of the upper FETs are set internally by a resistive voltage divider connected to V_{DD} , the V_{GG2} pin provides the user with an optional means of changing the gate bias of the upper FETs. Application of a voltage to V_{GG2} allows the user to change the voltage output by the resistive divider, altering the gate bias of the upper FETs and thus changing the gain. Application of V_{GG2} voltages across the range of -2.0 V to $+2.6$ V affects gain changes of approximately 30 dB, depending on the frequency. Increasing the voltage applied to V_{GG2} increases the gain, whereas decreasing the voltage decreases the gain. For $V_{DD} = 5.0$ V (nominal), the resulting V_{GG2} open circuit voltage is approximately 2.2 V.

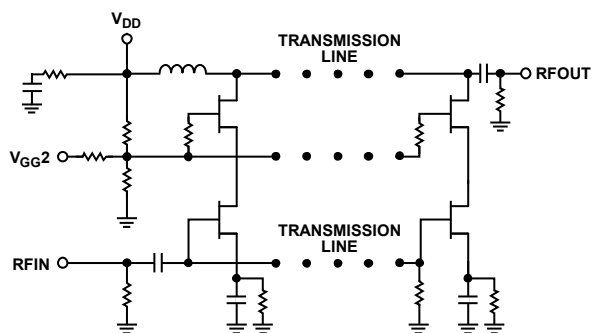


Figure 38. Architecture and Simplified Schematic

15412-036

APPLICATIONS INFORMATION

Capacitive bypassing is recommended for V_{DD} , as shown in the typical application circuit in Figure 39. Gain control is possible through the application of a dc voltage to V_{GG2} . If gain control is used, capacitive bypassing of V_{GG2} is recommended as shown in the typical application circuit. If gain control is not used, V_{GG2} can be either left open or capacitively bypassed as shown in Figure 39.

The recommended bias sequence during power-up is as follows:

1. Set V_{DD} to 5.0 V (this results in an I_{DD} near its specified typical value).
2. If the gain control function is to be used, apply a voltage within the range of -2.0 V to $+2.6$ V to V_{GG2} until the desired gain setting is achieved.
3. Apply the RF input signal.

The recommended bias sequence during power-down is as follows:

1. Turn off the RF input signal.
2. Remove the V_{GG2} voltage, or set it to 0 V.
3. Set V_{DD} to 0 V.

Power-up and power-down sequences can differ from the ones described, although care must always be taken to ensure adherence to the values shown in the Absolute Maximum Ratings section.

Unless otherwise noted, all measurements and data shown were taken using the typical application circuit as configured on the [HMC7950](#) evaluation board. The bias conditions shown in the Specifications section are recommended to optimize the overall performance. Operation using other bias conditions may result in performance that differs from the data shown in this data sheet.

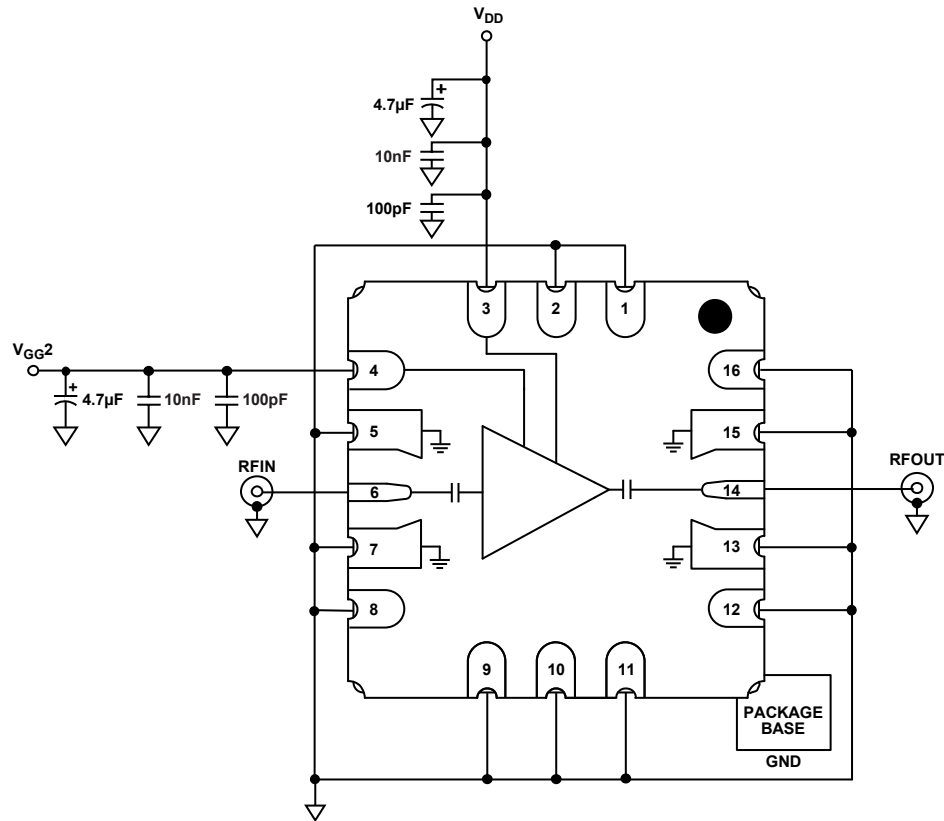


Figure 39. Typical Application Circuit

15412-037

EVALUATION BOARD

The [HMC7950](#) evaluation board is a 2-layer board fabricated using Rogers 4350 and using best practices for high frequency RF design. The RF input and RF output traces have a 50 Ω characteristic impedance.

The evaluation board and populated components are designed to operate over the ambient temperature range of -40°C to $+85^{\circ}\text{C}$. For the proper bias sequence, see the Applications Information section.

The evaluation board schematic is shown in Figure 41. A fully populated and tested evaluation board, shown in Figure 40, is available from Analog Devices, Inc., upon request.

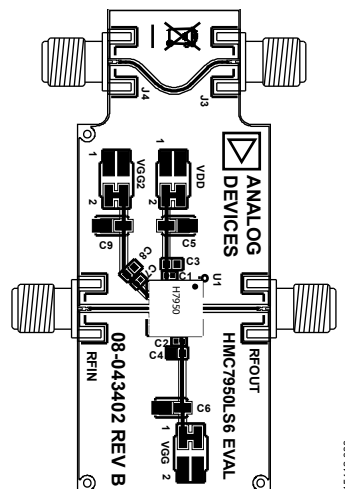


Figure 40. Evaluation PCB

Table 8. Bill of Materials for Evaluation PCB [EV1HMC7950LS6](#)

Item	Description
RFIN, RFOUT	PCB mount, K connector, SRI Part Number 21-146-1000-92
C1, C7	100 pF capacitor, 5%, 50 V, COG, 0402 package
C3, C8	10 nF capacitor, 10%, 16 V, X7R, 0402 package
C5, C9	4.7 μF tantalum capacitor, 10%, 20 V, 1206 package
U1	Amplifier, HMC7950LS6
PCB	Evaluation PCB; circuit board material: Rogers 4350
VDD, VGG2	DC pins, Molex Part Number 87759-0414
C2, C4, C6, J3, J4, VGG	Do not install (DNI)

EVALUATION BOARD SCHEMATIC

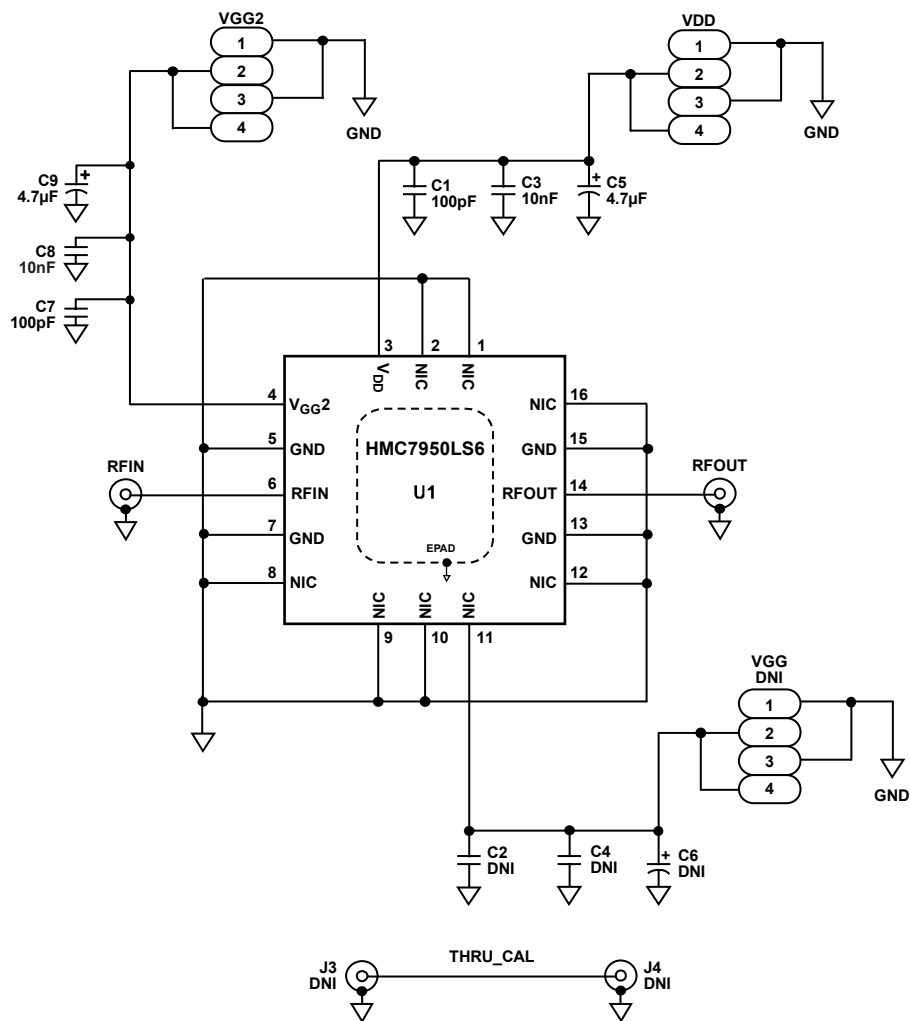
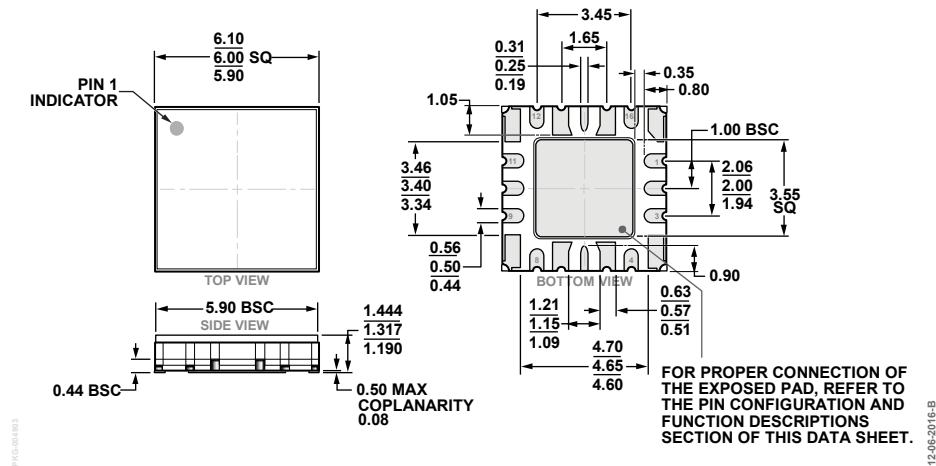


Figure 41. Evaluation Board Schematic

15412-039

OUTLINE DIMENSIONS



ORDERING GUIDE

Model ¹	Temperature Range	MSL Rating ²	Lead Finish	Package Description	Package Option	Branding ³
HMC7950LS6	−40°C to +85°C	MSL3	Au	16-Terminal LCC_HS	EP-16-2	H7950 XXXX
HMC7950LS6TR	−40°C to +85°C	MSL3	Au	16-Terminal LCC_HS	EP-16-2	H7950 XXXX
EV1HMC7950LS6				Evaluation PCB		

¹ The HMC7950LS6 and HMC7950LS6TR are RoHS compliant parts, made of low stress injection molded plastic.

² See the Absolute Maximum Ratings section for further information on the moisture sensitivity level (MSL) rating.

³ XXXX is the four-digit lot number.