MOTOROLA

MC33348

Lithium Battery Protection Circuit for One Cell Battery Packs

The MC33348 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of a one cell rechargeable battery pack. Cell protection features consist of internally trimmed charge and discharge voltage limits, discharge current limit detection with a delayed shutdown, and a virtually zero current sleepmode state when the cell is discharged. An additional feature includes an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. This MC33348 is available in standard SOIC 8 lead surface mount package.

- Internally Trimmed Charge and Discharge Voltage Limits
- Discharge Current Limit Detection with Delayed Shutdown
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Dedicated for One Cell Applications
- Minimum Components for Inclusion within the Battery Pack
- Available in a Low Profile Surface Mount Package

Ordering Information shown on following page.

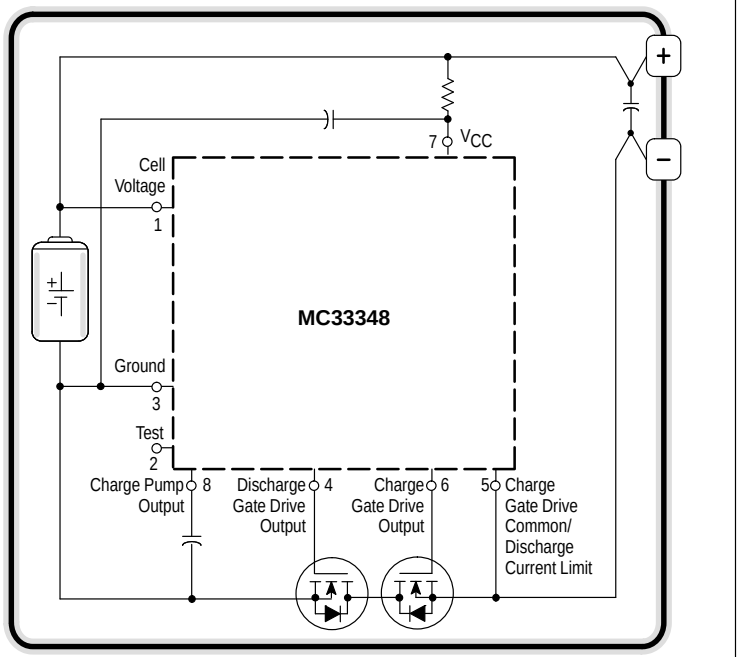
LITHIUM BATTERY PROTECTION CIRCUIT FOR ONE CELL SMART BATTERY PACKS

SEMICONDUCTOR TECHNICAL DATA



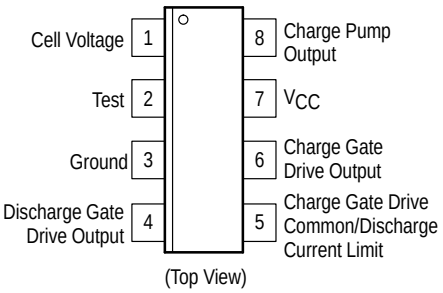
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Typical One Cell Smart Battery Pack



This device contains 1170 active transistors.

PIN CONNECTIONS



(Top View)

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ORDERING INFORMATION

Device	Charge Overvoltage Threshold (V)	Charge Overvoltage Hysteresis (mV)	Discharge Undervoltage Threshold (V)	Discharge Current Limit Threshold (mV)	Operating Temperature Range	Package
MC33348D–1	4.20	300	2.25	400	T_A = –25° to +85°C	SO–8
MC33348D–2				200		
MC33348D–3	4.25		2.28	400		
MC33348D–4				200		
MC33348D–5	4.35		2.30	400		
MC33348D–6				200		

NOTE: Additional threshold limit options can be made available. Consult factory for information.

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Measured with Respect to Ground, Pin 3) Cell Voltage (Pin 1) Test (Pin 2) Discharge Gate Drive Output (Pin 4) Charge Gate Drive Common/Discharge Current Limit (Pin 5) Charge Gate Drive Output (Pin 6) V_{CC} (Pin 7) Charge Pump Output (Pin 8)	V_{IR}	 7.5 7.5 18 ±11 ±11 7.5 10	V
Thermal Resistance, Junction–to–Air D Suffix, SO–8 Plastic Package, Case 751	$R_{\theta JA}$	 178	°C/W
Operating Junction Temperature (Note 1)	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTES: 1. Tested ambient temperature range for the MC33348:
T_{low} = –25°C T_{high} = +85°C
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Cell Charging Cutoff (Pin 1 to Pin 3)					
Overvoltage Threshold, V_{Cell} Increasing, T_A = 25°C	$V_{th(OV)}$				V
–1 Suffix		4.158	4.20	4.242	
–2 Suffix		4.158	4.20	4.242	
–3 Suffix		4.208	4.25	4.293	
–4 Suffix		4.208	4.25	4.293	
–5 Suffix		4.306	4.35	4.394	
–6 Suffix		4.306	4.35	4.394	
Overvoltage Hysteresis V_{Cell} Decreasing	V_H				mV
–1 Suffix		–	300	–	
–2 Suffix		–	300	–	
–3 Suffix		–	300	–	
–4 Suffix		–	300	–	
–5 Suffix		–	300	–	
–6 Suffix		–	300	–	
Cell Discharging Cutoff (Pin 1 to Pin 3, T_A = 25°C)					
Undervoltage Threshold, V_{Cell} Decreasing	$V_{th(UV)}$				V
–1 Suffix		2.205	2.25	2.295	
–2 Suffix		2.205	2.25	2.295	
–3 Suffix		2.234	2.28	2.326	
–4 Suffix		2.234	2.28	2.326	
–5 Suffix		2.254	2.30	2.346	
–6 Suffix		2.254	2.30	2.346	
Input Bias Current During Cell Voltage Sample (Pin 1)	I_{IB}	–	28	–	µA
Cell Voltage Sampling Rate	$t_{(smpl)}$	–	1.0	–	s
CURRENT SENSING					
Discharge Current Limit (Pin 3 to Pin 5, T_A = 25°C)					
Threshold Voltage	$V_{th(dschg)}$				mV
–1 Suffix		360	400	440	
–2 Suffix		180	200	220	
–3 Suffix		360	400	440	
–4 Suffix		180	200	220	
–5 Suffix		360	400	440	
–6 Suffix		180	200	220	
Delay	$I_{dly(dschg)}$	1.0	2.3	4.0	ms
CHARGE PUMP					
Output Voltage (Pin 8, $R_L \geq 10^{10}$, T_A = 25°C)	V_O	8.0	10.2	12	V
TOTAL DEVICE					
Average Cell Current (T_A = 25°C, Battery Pack Unloaded and without Current Limit Fault)	I_{CC}				
Operating (V_{CC} = 4.0 V)		–	17	20	µA
Sleepmode (V_{CC} = 2.0 V)		–	2.0	–	nA
Minimum Operating Cell Voltage for Logic and Gate Drivers	V_{CC}	–	1.5	–	V

NOTE: 1. Tested ambient temperature range for the MC33348:
T_{low} = –25°C T_{high} = +85°C

Figure 1. Charge and Discharge Threshold Voltage Change versus Temperature

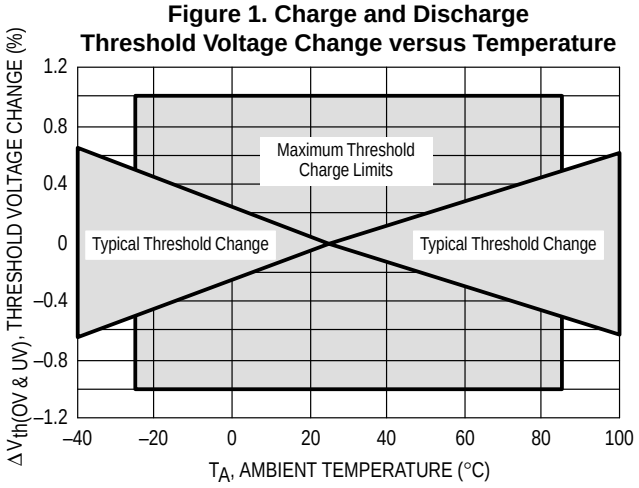


Figure 2. Discharge Current Limit Threshold Voltage Change versus Temperature

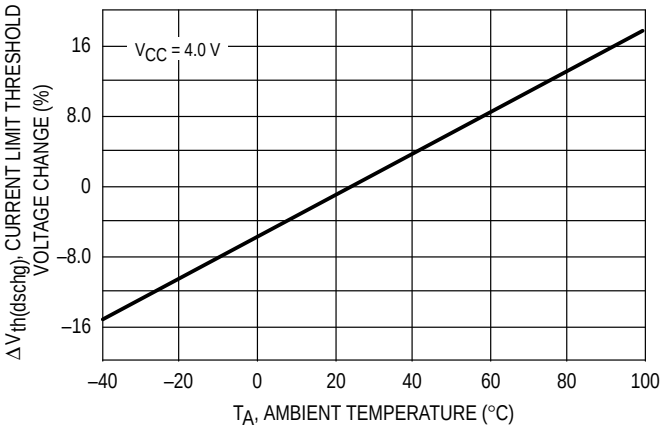


Figure 3. Gate Drive Output Voltage versus Load Current

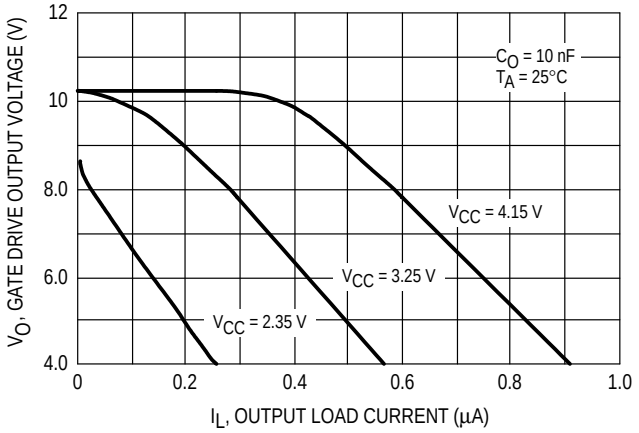


Figure 4. Gate Drive Output Voltage versus Supply Voltage

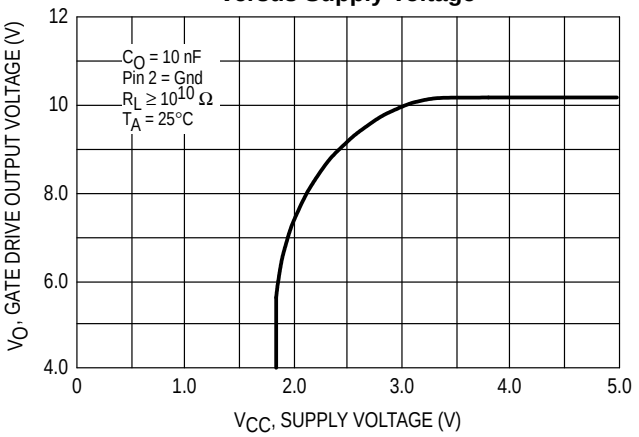


Figure 5. Charge Pump Output Voltage versus Temperature

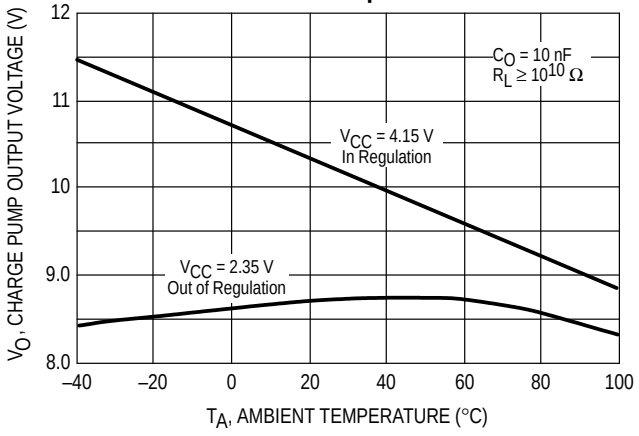
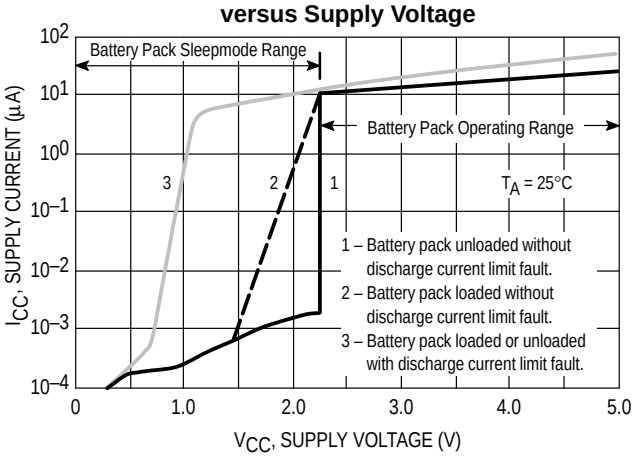


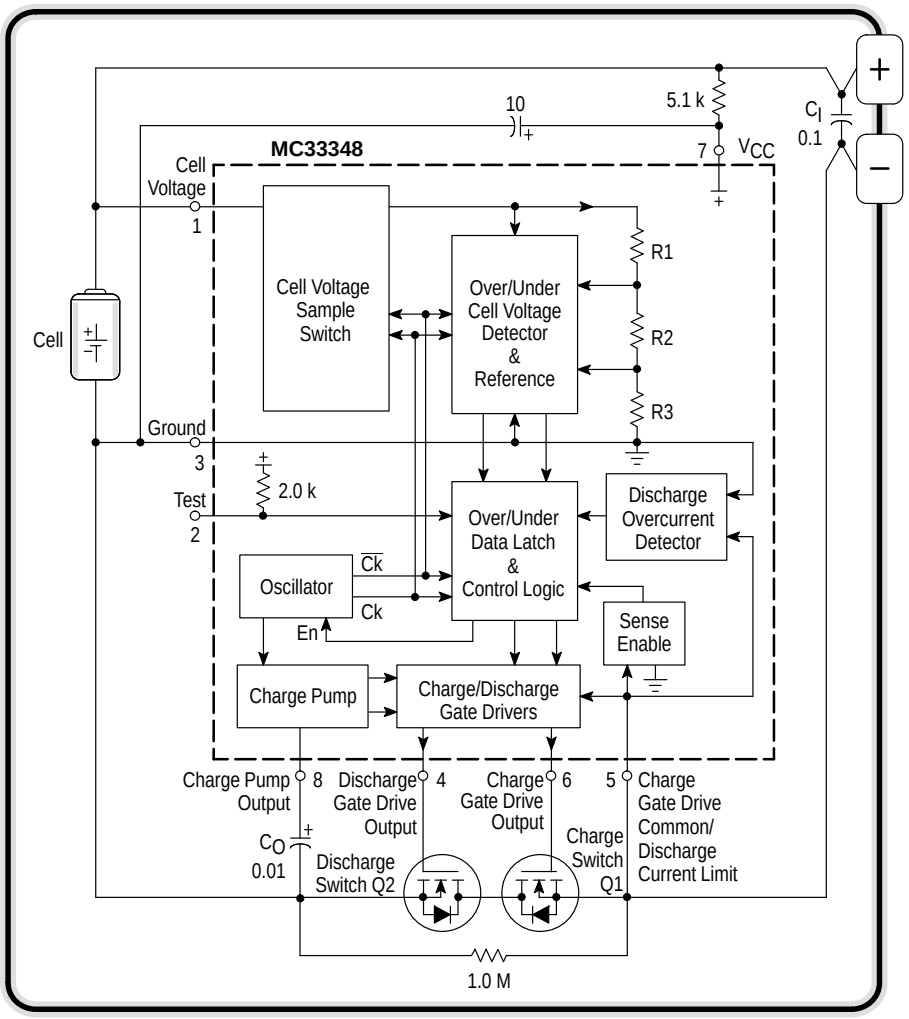
Figure 6. Supply Current versus Supply Voltage



PROTECTION CIRCUIT OPERATING MODE TABLE

Input Conditions Cell Status	Circuit Operation Battery Pack Status	Outputs		
		MOSFET Switches		Function
		Charge Q1	Discharge Q2	Charge Pump
CELL CHARGING/DISCHARGING				
Storage or Nominal Operation: No current or voltage faults	Both Charge MOSFET Q1 and Discharge MOSFET Q2 are on. The battery pack is available for charging or discharging.	On	On	Active
CELL CHARGING FAULT/RESET				
Charge Voltage Limit Fault: $V_{Pin\ 1} \geq V_{th(OV)}$ for 1.0 s	Charge MOSFET Q1 is latched off and the cell is disconnected from the charging source. An internal current source pull–up is applied to divider resistors R1 and R2 creating a hysteresis voltage of V_H. The battery pack is available for discharging. Discharge current limit protection is disabled.	On to Off	On	Active
Charge Voltage Limit Reset: $V_{Pin\ 1} < (V_{th(OV)} - V_H)$ for 1.0 s	Charge MOSFET Q1 will turn on when the voltage across the cell falls sufficiently to overcome hysteresis voltage V_H. This can be accomplished by applying a load to the battery pack. Discharge current limit protection is enabled.	Off to On	On	Active
CELL DISCHARGING FAULT/RESET				
Discharge Current Limit Fault: $V_{Pin\ 5} \geq (V_{Pin\ 3} + V_{th(dschg)})$ for 3.0 ms and $V_{Pin\ 1} < (V_{th(OV)} - V_H)$ for 1.0 ms	Discharge MOSFET Q2 is latched off and the cell is disconnected from the load. Q2 will remain in the off state as long as $V_{Pin\ 5}$ exceeds $V_{Pin\ 3}$ by $\approx V_{th(dschg)}$. The battery pack is available for charging.	On	On to Off	Active
Discharge Current Limit Reset: $V_{Pin\ 5} - V_{Pin\ 3} < V_{th(dschg)}$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 3}$ no longer exceeds $V_{Pin\ 5}$ by $\approx V_{th(dschg)}$. This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger.	On	Off to On	Active
Discharge Voltage Limit Fault: $V_{Pin\ 1} \leq V_{th(UV)}$ for three consecutive 1.0 s samples	Discharge MOSFET Q2 is latched off, the cells are disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging.	On	On to Off	Disabled
Discharge Voltage Limit Reset: $V_{Pin\ 3} > (V_{Pin\ 5} + 0.6\ V)$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 3}$ exceeds $V_{Pin\ 5}$ by 0.6 V. This can be accomplished by connecting the battery pack to the charger.	On	Off to On	Active
FAULTY CELL				
Discharge Voltage Limit Fault: $V_{Pin\ 1} \leq 1.5\ V$	This condition can happen if the cell is defective (<1.5 V). The protection circuit logic will not function and the battery pack cannot be charged.	Disabled	Disabled	Disabled

Figure 7. One Cell Smart Battery Pack



Components C_I is mandatory. Refer to the Battery Pack Application text.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Cell Voltage	This input is connected to the positive terminal of the cell for voltage monitoring. Internally, the Cell Voltage Sample Switch applies this voltage to a resistor divider where it is compared by the Cell Voltage Detector to an internal reference.
2	Test	This pin is normally not connected and is used in testing the protection IC. An active low at this input resets the internal logic and turns on both MOSFET switches. Upon release, the logic becomes active and the cell voltage is sampled within 1.0 ms.
3	Ground	This is the protection IC ground and all voltage ratings are with respect to this pin.
4	Discharge Gate Drive Output	This output connects to the gate of discharge switch Q2 allowing it to enable or disable battery pack discharging.
5	Charge Gate Drive Common/Discharge Current Limit	This is a multifunction pin that is used to monitor cell discharge current and to provide a gate turn–off path for charge switch Q1. A discharge current limit fault is set when the battery pack load causes the combined voltage drop of charge switch Q1 and discharge switch Q2 to exceed the discharge current limit threshold voltage, $V_{th(dschg)}$, with respect to Pin 3.
6	Charge Gate Drive Output	This output connects to the gate of charge switch Q1 allowing it to enable or disable battery pack charging.
7	V_{CC}	This pin is the positive supply voltage for the protection IC.
8	Charge Pump Output	This is the charge pump output. A reservoir capacitor is connected from this pin to ground.

INTRODUCTION

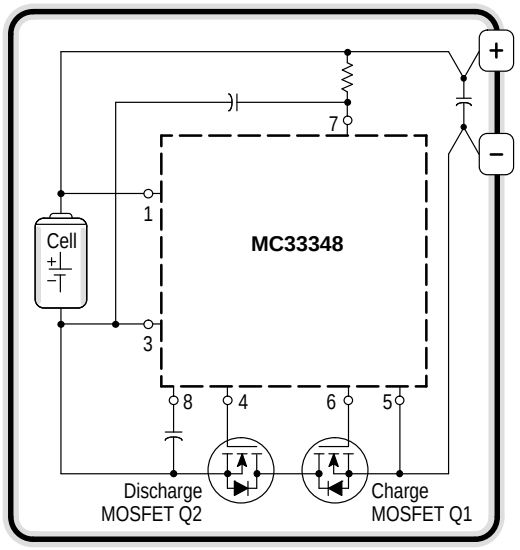
The insatiable demand for smaller lightweight portable electronic equipment has dramatically increased the requirements of battery performance. Batteries are expected to have higher energy densities, superior cycle life, be safe in operation and environmentally friendly. To address these high expectations, battery manufacturers have invested heavily in developing rechargeable lithium–based cells. Today's most attractive chemistries include lithium–polymer, lithium–ion, and lithium–metal. Each of these chemistries require electronic protection in order to constrain cell operation to within the manufacturers limits.

Rechargeable lithium–based cells require precise charge and discharge termination limits for both voltage and current in order to maximize cell capacity, cycle life, and to protect the end user from a catastrophic event. The termination limits are not as well defined as with older non–lithium chemistries. These limits are dependent upon a manufacturer's particular lithium chemistry, construction technique, and intended application. Battery pack assemblers may also choose to enhance cell capacity at the expense of cycle life. In order to address these requirements, six versions of the MC33348 protection circuit were developed. These devices feature charge overvoltage protection, discharge current limit protection with delayed shutdown, low operating current, a virtually zero current sleepmode state, and requires few external components to implement a complete one cell smart battery pack.

Operating Description

The MC33348 is specifically designed to be placed in the battery pack where it is continuously powered from a single lithium cell. In order to maintain cell operation within specified limits, the protection circuit senses both cell voltage and discharge current, and correspondingly controls the state of two N–channel MOSFET switches. These switches, Q1 and Q2, are placed in series with the negative terminal of the Cell and the negative terminal of the battery pack. This configuration allows the protection circuit to interrupt the appropriate charge or discharge path FET in the event that either a voltage threshold or the discharge current limit for the cell has been exceeded.

Figure 8. One Cell Smart Battery Pack



A functional description of the protection circuit blocks follows. Refer to the detailed block diagram shown in Figure 7.

Voltage Sensing

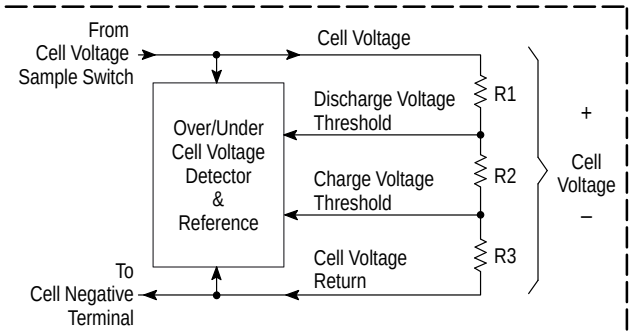
Voltage sensing is accomplished by the use of the Cell Voltage Sample Switch in conjunction with the Over/Under Voltage Detector and Reference block. The Sample Switch applies the cell voltage to the top resistor of an internal divider string. The voltage at each of the tap points is sequentially polled and compared to an internal reference. If a limit has been exceeded, the result is stored in the Over/Under Data Latch and Control Logic block. The Cell Voltage Sample Switch is gated on for a 1.0 ms period at a one second repetition rate. This low duty cycle sampling technique reduces the average load current that the divider presents across the cell, thus extending the useful battery pack capacity. The cell voltage limits are tested in the following sequence:

Figure 9. Cell Sensing Sequence

Polling Sequence	Time (ms)	Tested Limit
1	0.5	Overvoltage
2	0.5	Undervoltage

By incorporating this polling technique with a single comparator and voltage divider, a significant reduction of circuitry and trim elements is achieved. This results in a smaller die size, lower cost, and reduced operating current.

Figure 10. Cell Voltage Limit Sampling



The cell charge and discharge voltage limits are controlled by the values selected for the internal resistor divider string and the comparator input threshold. As the battery pack reaches full charge, the Cell Voltage Detector will sense an overvoltage fault condition when the cell exceeds the designed overvoltage limit. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. An internal current source pull–up is then applied to lower tap of the divider, creating a hysteresis voltage. As a result of an overvoltage fault, the battery pack is available for discharging only.

The overvoltage fault is reset by applying a load to the battery pack. As the voltage across the cell falls below the hysteresis level, charge MOSFET Q1 will turn on and the current source pull–up will turn off. The battery pack will now be available for charging or discharging.

As the load eventually depletes the battery pack charge, the Cell Voltage Detector will sense an undervoltage fault condition when the cell falls below the designed undervoltage limit. After three consecutive faults are detected, discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. The protection circuit will now enter a low current sleepmode state. Refer to Figure 6. As a result of the undervoltage fault, the battery pack is available for charging only. The typical cutoff thresholds and hysteresis voltage are shown in Figure 11.

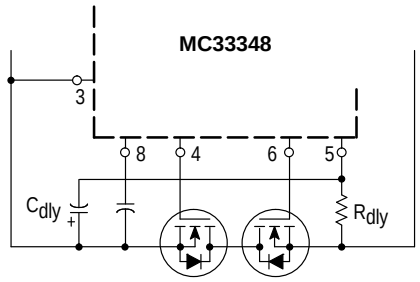
Figure 11. Cutoff and Hysteresis Limits

Device Suffix	Charging Cutoff (V)	Hysteresis (mV)	Disharging Cutoff (V)
–1, –2	4.20	300	2.25
–3, –4	4.25	300	2.28
–5, –6	4.35	300	2.30

The undervoltage logic is designed to automatically reset if less than three consecutive faults appear. This helps to prevent a premature disconnection of the load during high current pulses when the battery pack charge is close to being depleted.

The undervoltage fault is reset by applying charge current to the battery pack. When the voltage on Pin 3 exceeds Pin 5 by 0.6 V, discharge MOSFET Q2 will turn on. The battery pack will now be available for charging or discharging.

Figure 12. Additional Discharge Current Limit Delay



The discharge current limit shutdown delay time is typically 3.0 ms. This time can be extended with the addition of components R_{dly} and C_{dly}. With an R_{dly} of 5.1 k and C_{dly} of 10 μF, the current limit shutdown time is extended to 40 ms.

The additional discharge current limit delay circuitry must not be used if the anticipated open–circuit charger voltage will exceed 6.0 V. When the charger causes the battery pack input to exceed 6.0 V, additional current will flow out of Pin 5, creating a voltage drop across resistor R_{dly}. This voltage drop causes the source of MOSFET Q1 to fall below it's gate, allowing it to unexpectedly turn back on.

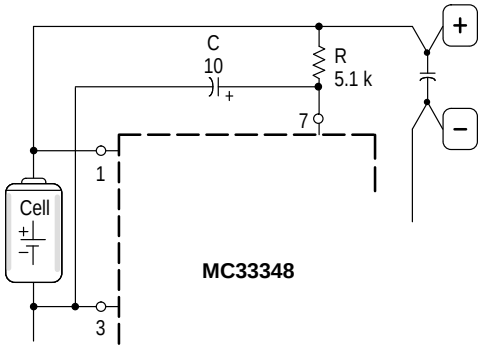
Current Sensing

Discharge current limit protection is internally provided by the MC33348. As the battery pack discharges, Pins 5 and 3 sense the voltage drop across MOSFETs Q1 and Q2. A discharge current limit fault is detected if the voltage at Pin 5 is greater than Pin 3 by 400 mV for –1, –3 and –5 suffix devices, or 200 mV for –2, –4 and –6 suffix devices. The fault information is stored in a data latch and discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. As a result of the discharge current fault, the battery pack is available for charging only. The discharge current limit is given by:

$$I_{Lim(dschg)} = \frac{V_{th(dschg)}}{R_{Lim(dschg)}} = \frac{V_{th(dschg)}}{R_{DS(on)Q1} + R_{DS(on)Q2}}$$

The discharge current fault is reset by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger. When the voltage on Pin 5 no longer exceeds Pin 3 by approximately $V_{th(dschg)}$, the Sense Enable circuit will turn on discharge MOSFET Q2.

Figure 13. Power Supply Decoupling



In order to guarantee proper discharge current limit operation when the battery pack output is shorted, power must be made available to the MC33348. This can be accomplished by decoupling the V_{CC} input with the R/C component values shown above. The capacitor value must be increased to 100 μF if the discharge current limit shutdown delay time is extended to 40 ms as shown in Figure 12. A small signal schottky diode can be used in place of R for enhanced short circuit operation. The diode cathode is connected to Pin 7 and C, and the anode is connected to the positive terminal of the cell. The schottky diode solution may be a better choice in applications that have a charger with a relatively high open circuit voltage. These components can be deleted if operation of the discharge current limit is not required when the battery pack output is shorted.

As previously stated in the voltage sensing operating description, charge MOSFET Q1 is held off during an overvoltage fault condition. When this condition is present, the discharge current limit protection function is internally disabled. This is required, since the voltage across Q1, in the off state, would exceed the current sense threshold. This would cause Q2 to turn off as well, preventing both charging and discharging of the cell. Discharge current limit protection is enabled whenever an overvoltage fault is not present.

The discharge current protection circuit contains a built in response delay of 3.0 ms. This helps to prevent fault activation when the battery pack is subjected to pulsed currents during discharging. An additional current sense delay can be added as shown in Figure 12. If the battery pack is subjected to extremely high discharge current pulses or is shorted, the V_{CC} pin must be decoupled from the cell. This is required so that the protection circuit will have sufficient operating voltage during the load transient, to ensure turn off of discharge MOSFET Q2. Figure 13 shows the placement of decoupling components.

Charge Pump and MOSFET Switches

The MC33348 contains an on chip Charge Pump to ensure that the MOSFET switches are fully enhanced for reduced power losses. An external reservoir capacitor normally connects from the Charge Pump output to ground, Pins 8 and 3. The capacitor value is not critical and is usually within the range of 10 nF to 100 nF. The Charge Pump output is regulated at 10.2 V allowing the use of the more economical logic level MOSFETs. The main requirement in selecting a particular type of MOSFET switch is to consider the desired on–resistance at the lowest anticipated operating voltage of the battery pack. A table of small outline surface mount devices is given in Figure 14. When using extremely low threshold MOSFETs, it may be desirable to disable the Charge Pump so that the maximum gate to source voltage is not exceeded. This can be accomplished by connecting Pin 6 to Pin 5, and will result in an additional cell drain current of approximately 8.0 μA.

Testing

A test pin is provided in order to speed up device and battery pack testing. By grounding Pin 2, the internal logic is held in a reset state and both MOSFET switches are turned on. Upon release, the logic becomes active and the cell voltage is polled within 1.0 ms.

Battery Pack Application

The one cell smart battery pack application shown in Figure 7 contains a capacitor labeled C_I that connects directly across the battery pack terminals. This component prevents excessive currents from flowing into the MC33348 when the battery pack terminals are shorted or arced, and is **mandatory**. Capacitor C_I is a 100 nF ±20% ceramic leaded or surface mount type. It must be placed directly across the battery pack plus and minus terminals with extremely short lead lengths (≤1/16″).

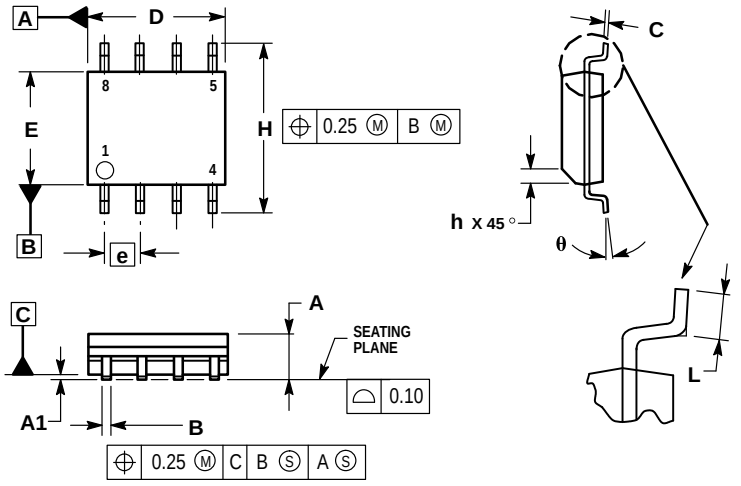
In applications where inordinately low leakage MOSFETs are used, the protection circuit may take a considerable amount of time to reset from an overcurrent fault after the load is removed. This situation can be remedied by providing a small leakage path for charging C_I, thus allowing Pin 5 to rapidly fall below the discharge current limit threshold. A 1.0 megohm resistor placed across the MOSFET switches accomplishes this task with a minimum increase in cell discharge current when the battery pack is connected to a load.

Figure 14. Small Outline Surface Mount MOSFET Switches

Device Type	On–Resistance (Ω) versus Gate to Source Voltage (V)						
	2.5 V	3.0 V	4.0 V	5.0 V	6.0 V	7.5 V	9.0 V
MMFT3055VL	–	–	–	0.120 Ω	0.115 Ω	0.108 Ω	0.100 Ω
MMDF3N03HD	–	0.525 Ω	0.080 Ω	0.065 Ω	0.063 Ω	0.062 Ω	0.060 Ω
MMDF4N01HD	0.047 Ω	0.042 Ω	0.037 Ω	0.035 Ω	0.034 Ω	0.033 Ω	0.033 Ω
MMSF5N02HD	–	0.065 Ω	0.023 Ω	0.021 Ω	0.020 Ω	0.018 Ω	0.018 Ω
MMDF6N02HD	0.043 Ω	0.035 Ω	0.029 Ω	0.028 Ω	0.026 Ω	0.025 Ω	0.023 Ω

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)
ISSUE S



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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