System PMIC for Battery Powered Systems

BD71805MWV

General Description

The BD71805MWV is a single chip power management IC for battery-powered portable devices. It integrates 4 Bucks, 3 LDOs, 2A single-cell linear charger, OVP, Coulomb counter, RTC, 32 kHz crystal circuitry and 3 GPOs.

Four highly efficient 2.5MHz step-down converters supply power to the application processor as well as system peripherals such as DDR memory, wireless modules, and touch controller. The regulator to the processor core supports DVS. The regulators maintain high efficiency over a wide range of current loads by supporting both PFM and PWM modes. High switching frequency allows the use of smaller and cheaper inductors and capacitors.

Features

- 4 Buck Converters:
  - 1-2000mA Buck
  - 3-1000mA Bucks
- 3 LDOs (General purpose)
  - 3-300mA LDOs
- LDO for DDR Reference Voltage
- LDO for Secure Non-Volatile Storage (SNVS)
- Single-cell Linear LIB Charger with 30V-OVP
  - Selectable Charging Voltage : 3.72 to 4.34 V
  - Programmable Charge Current : 100 to 2000mA
  - DCIN Over Voltage Protection
  - Battery Over Voltage Protection
  - Support Battery Supplement Mode
  - Battery Short Circuit Detection
- Voltage Measurement for Thermistor
  - Bias Voltage Output for External Thermistor
- Embedded Coulomb Counter for Battery Fuel Gauging
  - 15-bit ΔΣ-ADC with External Current Sense Resistor (10 mΩ, ±1%)
  - 1-sec cycle, 28-bit Accumulation
  - Coulomb Count while Charging/Discharging
- Battery Monitoring and Alarm Output
  - Under Voltage Alarm while Discharging
  - Over Discharge Current Alarm
  - Over/Under Temperature Alarm
  - Programmable Thresholds and Time Durations
  - Automatic Low Voltage Mode (Battery Protection)
    - 3.5V Detection : Interrupt to Processor to Ask User Plug-in
    - 3.3V Detection : Interrupt to Processor to Indicate Battery Critically Low Condition
- Real Time Clock with 32.768kHz Crystal Oscillator
  - 32.768kHz Clock Output (Open Drain or CMOS Output Selectable)
- 3 GPOs (Open Drain or CMOS Output Selectable)
- Power Control I/O
  - Power On/Off Control Input
  - Standby Input for Switching ON / STANDBY Mode
  - Reset Input to Reset Hung PMIC
  - Power On Reset Output
- I2C Interface

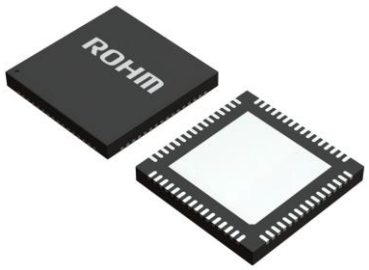
Applications

- E-Book Reader
- Portable Media Players
- Portable Navigation Devices

Key Specifications

- Input Voltage Range (DCIN): 3.5V to 28V
- Input Voltage Range (VIN,VSYS): 3.3V to 5.5V
- Input Voltage Range (DVDD): 1.5V to 3.4V
- Off Current : 25 μA (Typ)
  [RTC+ Coulomb counter+ LDO_SNVS+ 32kOSC only]
- Operating temperature range: -40°C to +85°C

Package	W(Typ)	D(Typ)	H(Max)
UQFN64MV8080	8.0mm x 8.0mm x 1.0mm		



Status of this document
The English version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document formal version takes priority.

○Product structure：Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays

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Typical Applications

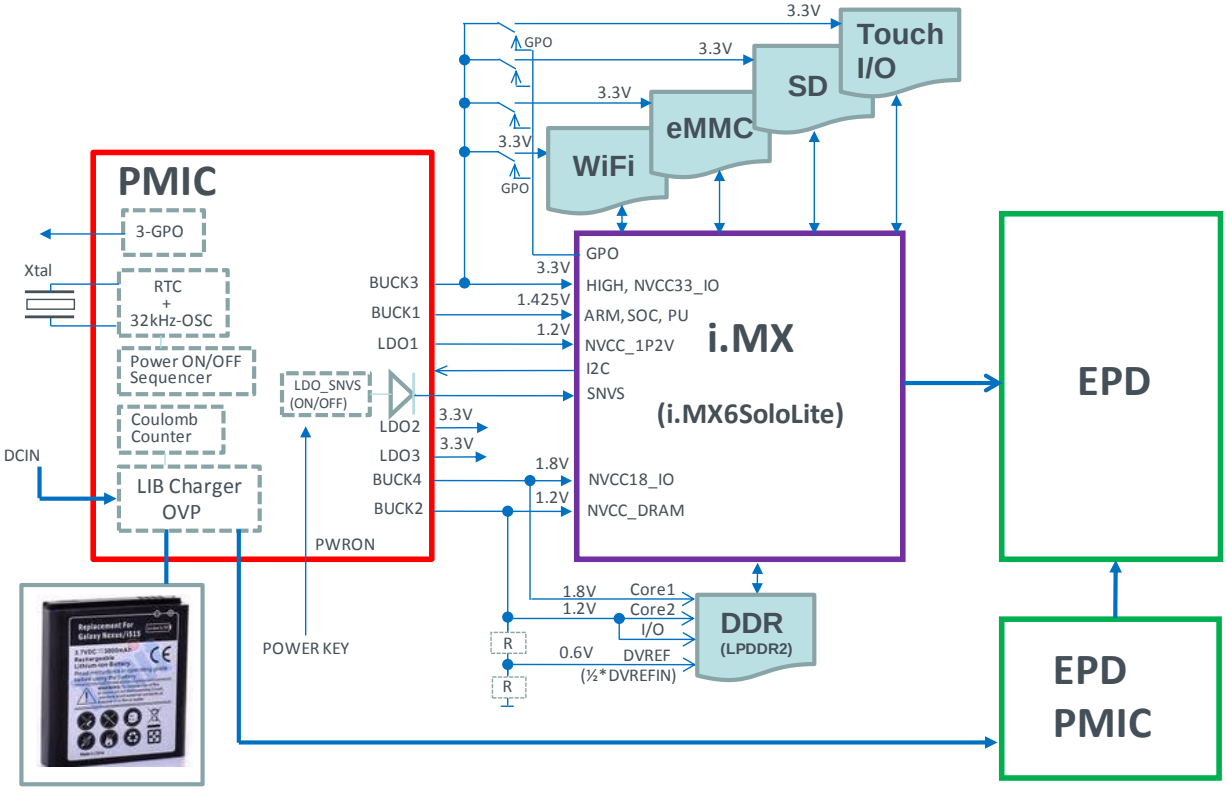

Figure 1. Typical Applications 1 (Master Control Mode)

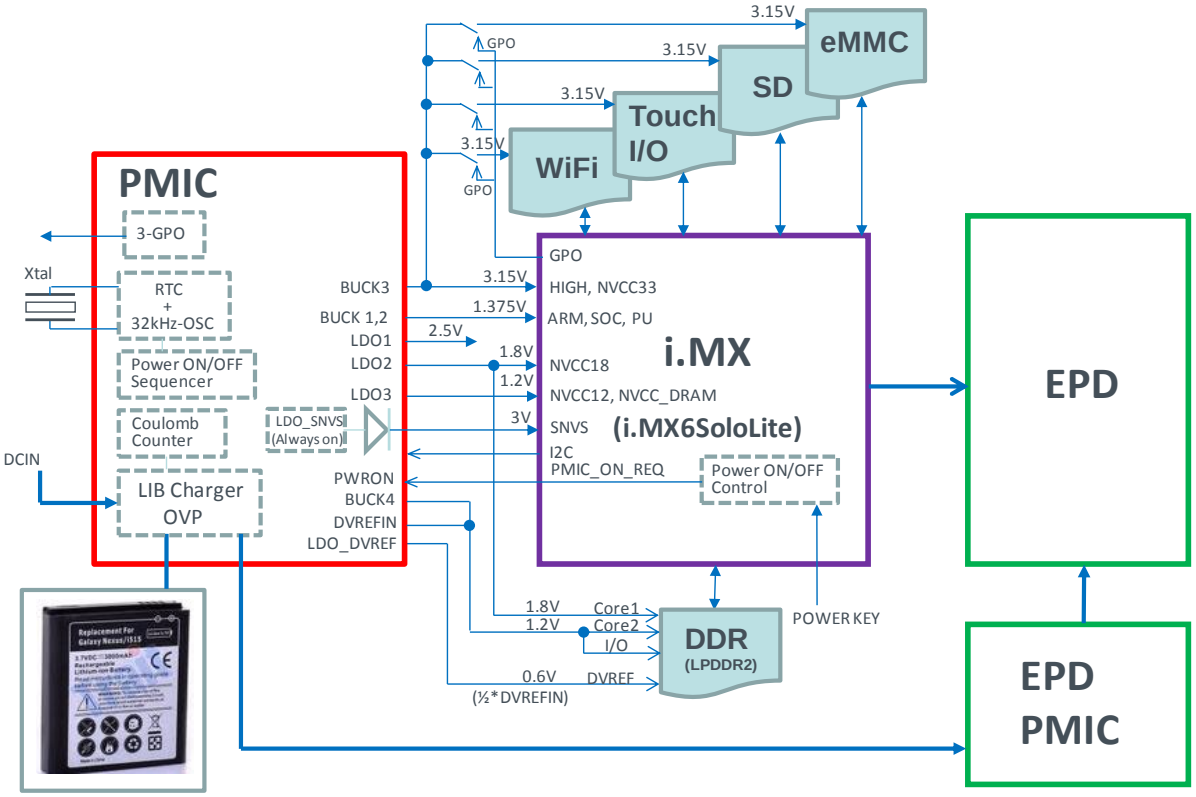

Figure 2. Typical Applications 2 (Slave Control Mode)

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Block Diagram

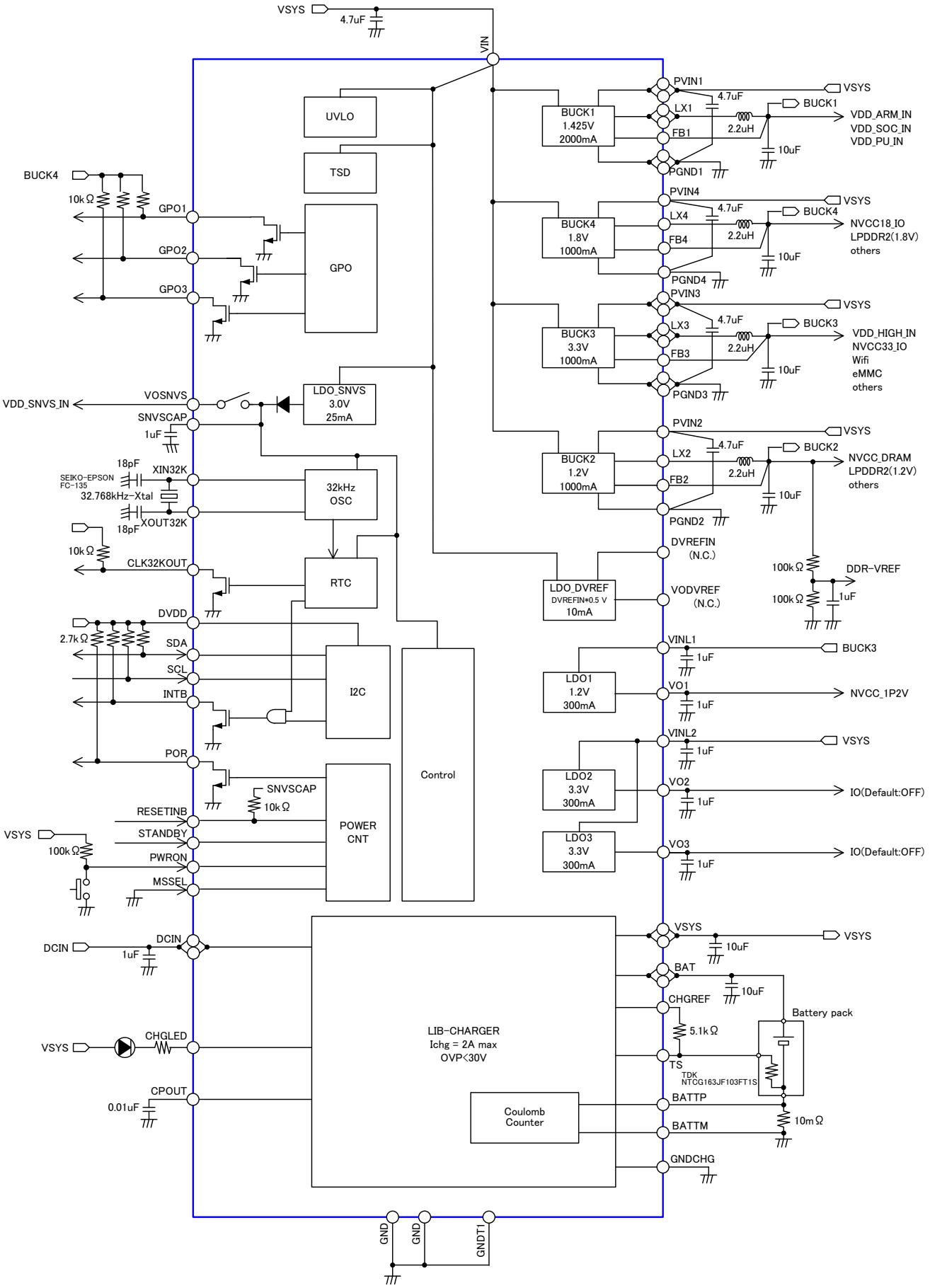

Figure 3. IC Block Diagram (Master Control Mode)

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Block Diagram - continued

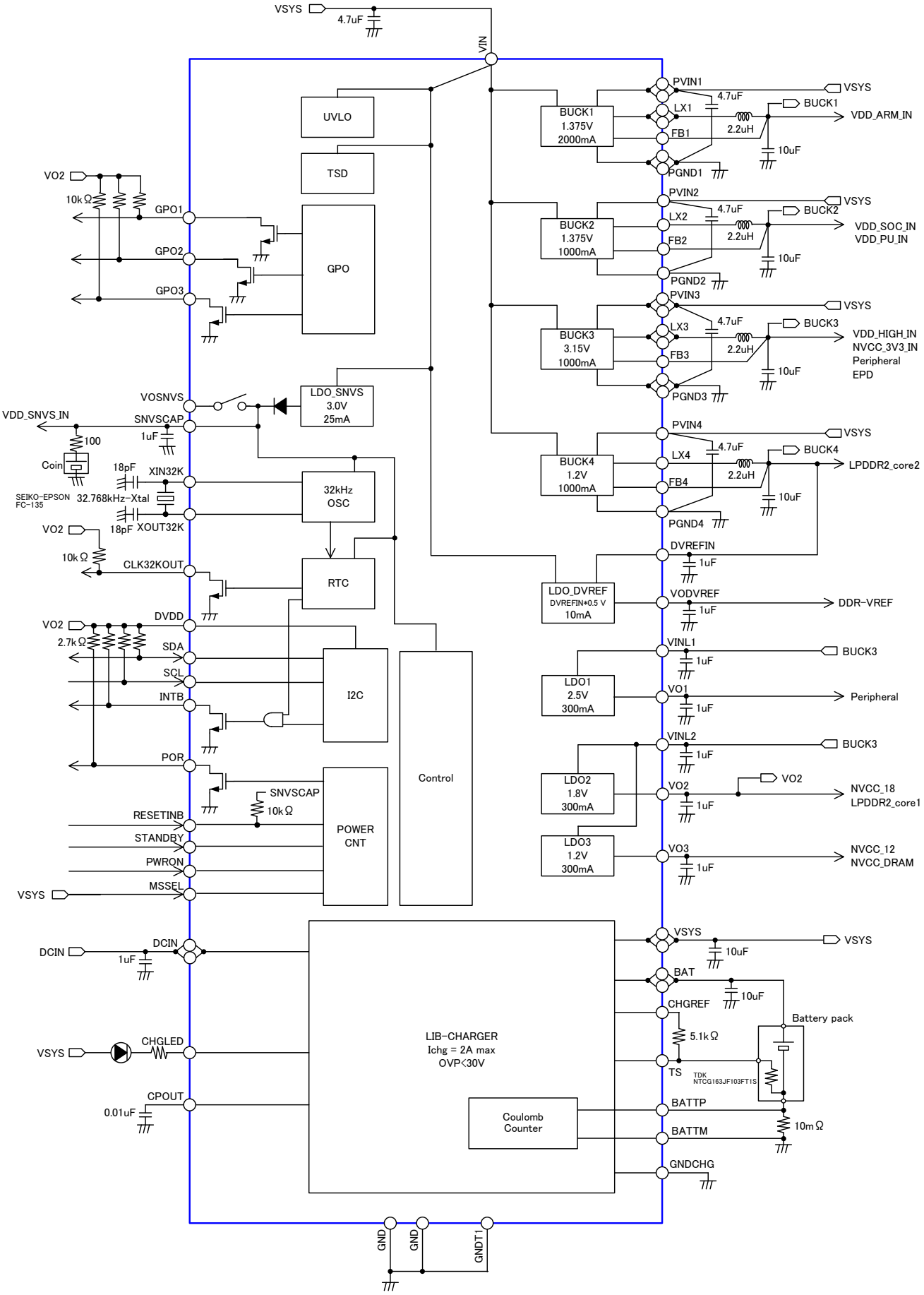

Figure 4. IC Block Diagram (Slave Control Mode)

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Pin Configuration

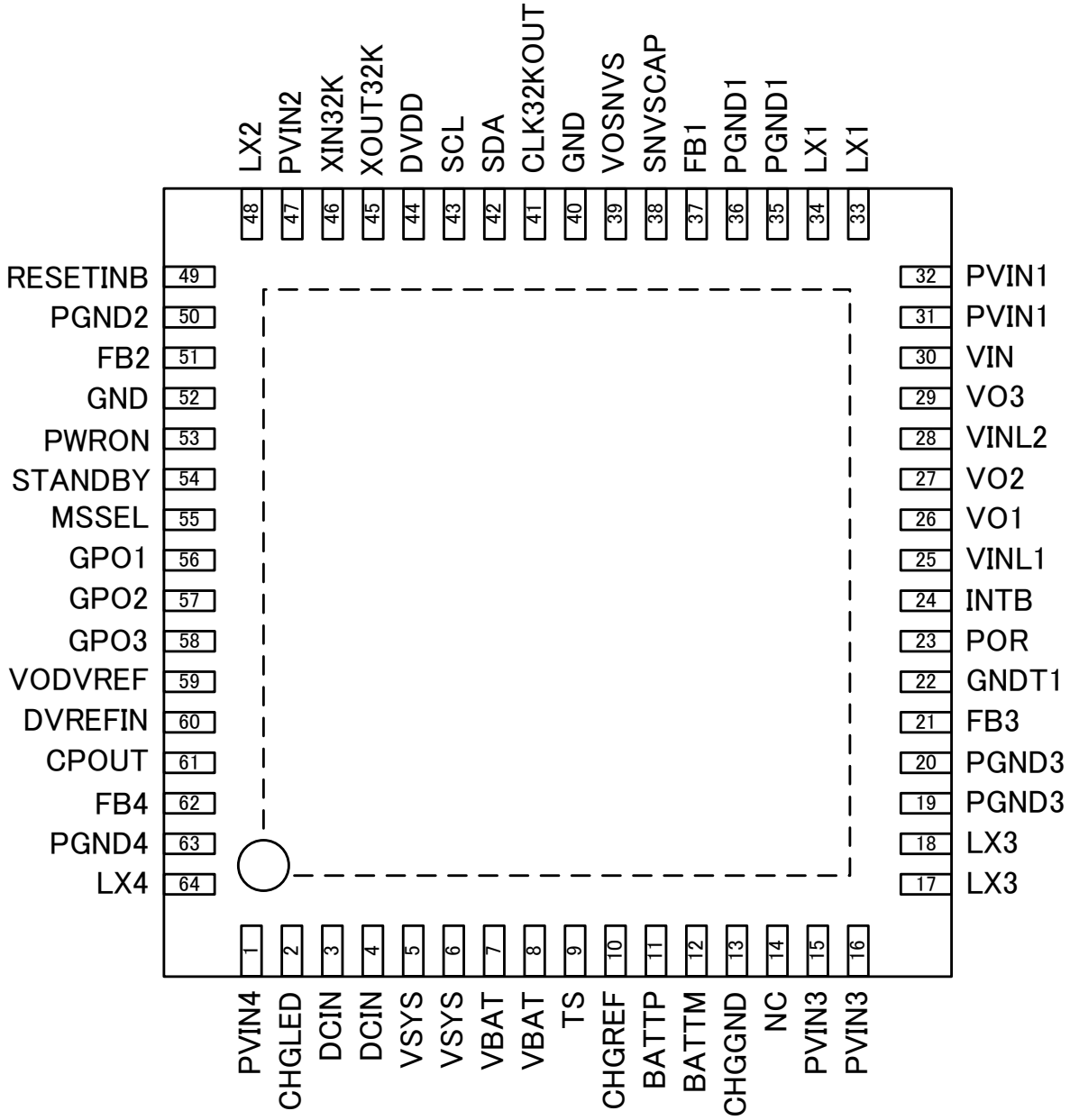

Figure 5. Pin Configuration (Top View)

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Pin Descriptions

Table 1. BD71805MWV Pin Description

Pin No.	Pin Name.	I/O	Function
1	PVIN4	I	Input power supply for BUCK4
2	CHGLED	O	Open-Drain Charging status Indication output
3	DCIN	I	DCIN power supply
4	DCIN	I	DCIN power supply
5	VSYS	O	System supply output
6	VSYS	O	System supply output
7	VBAT	I/O	Charger power stage output and battery voltage sense input
8	VBAT	I/O	Charger power stage output and battery voltage sense input
9	TS	I	Battery pack thermistor voltage sense
10	CHGREF	O	Internal reference for the LIB charger
11	BATTP	I	Current sense input (battery pack side)
12	BATTM	I	Current sense input (ground side)
13	CHGGND	-	Ground for Charger
14	NC	-	No Connection
15	PVIN3	I	Input power supply for BUCK3
16	PVIN3	I	Input power supply for BUCK3
17	LX3	O	Switch node connection for BUCK3
18	LX3	O	Switch node connection for BUCK3
19	PGND3	I	Power ground for BUCK3
20	PGND3	I	Power ground for BUCK3
21	FB3	I	Output voltage feedback for BUCK3
22	GNDT1	-	Ground for test
23	POR	O	Power on reset output
24	INTB	O	Open drain interrupt signal to processor
25	VINL1	I	LDO input for LDO1
26	VO1	O	LDO output for LDO1
27	VO2	O	LDO output for LDO2
28	VINL2	I	LDO input for LDO2, LDO3
29	VO3	O	LDO output for LDO3
30	VIN	I	Input power supply
31	PVIN1	I	Input power supply for BUCK1
32	PVIN1	I	Input power supply for BUCK1
33	LX1	O	Switch node connection for BUCK1
34	LX1	O	Switch node connection for BUCK1
35	PGND1	-	Power ground for BUCK1.
36	PGND1	-	Power ground for BUCK1.

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Pin Descriptions - continued

Table 2. BD71805MWV Pin Descriptions (continued)

Pin No.	Pin Name.	I/O	Function
37	FB1	I	Output voltage feedback for BUCK1
38	SNVSCAP	O	LDO output for secure non-volatile storage (requires capacitor)
39	VOSNVS	O	LDO output for secure non-volatile storage
40	GND	-	Signal ground
41	CLK32KOUT	O	32.768kHz clock output (Open drain or CMOS output selectable)
42	SDA	I/O	I2C data line (Open drain)
43	SCL	I	I2C clock
44	DVDD	I	Power supply for I2C Interface
45	XOUT32K	O	32.768kHz-Xtal output
46	XIN32K	I	32.768kHz-Xtal input
47	PVIN2	I	Input power supply for BUCK2
48	LX2	O	Switch node connection for BUCK2
49	RESETINB	I	Reset input to Shutdown BD71805MWV
50	PGND2	-	Power ground for BUCK2
51	FB2	I	Output voltage feedback for BUCK2
52	GND	-	Signal ground
53	PWRON	I	Power On/Off control input
54	STANDBY	I	Standby input signal for switching the ON and STANDBY modes
55	MSSEL	I	Master or Slave mode selector
56	GPO1	O	Output for general purpose (Open drain or CMOS output selectable)
57	GPO2	O	Output for general purpose (Open drain or CMOS output selectable)
58	GPO3	O	Output for general purpose (Open drain or CMOS output selectable)
59	VODVREF	O	LDO output for DDR-VREF
60	DVREFIN	I	LDO input for DDR-VREF
61	CPOUT	O	Charge Pump Output for OVP
62	FB4	I	Output voltage feedback for BUCK4
63	PGND4	-	Power ground for BUCK4
64	LX4	O	Switch node connection for BUCK4

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PCB Layout Recommendations

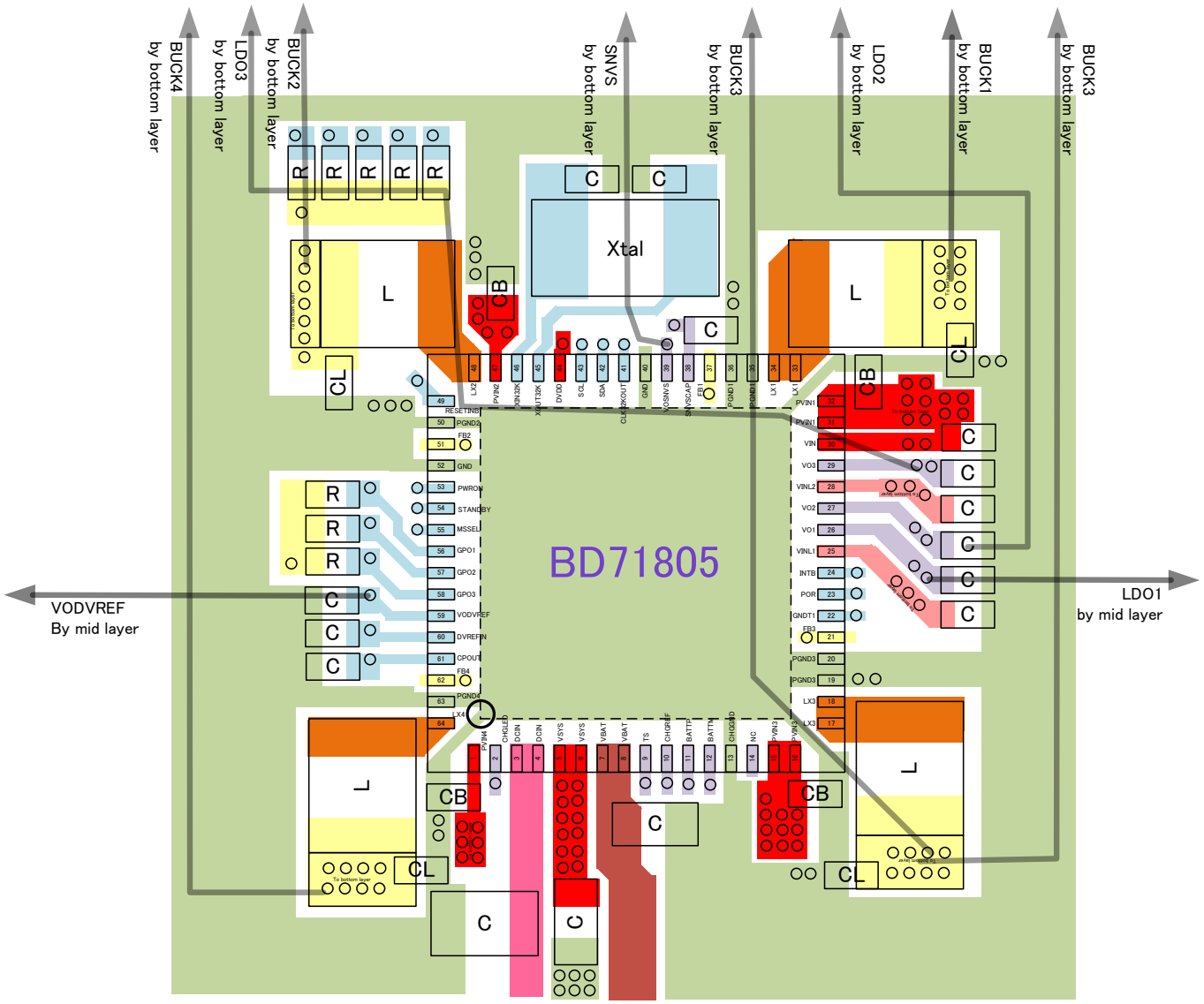

Figure 6. PCB Layout Recommendations (Top View)

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Description of Blocks

1. High Efficiency Buck Converters (BUCK1 – 4) and LDOs

BD71805MWV step down converters operate at fixed frequency of 2.5MHz and employ Pulse Width Modulation (PWM) at moderate to heavy load current. At light load current, a converter would automatically enter Power Save Mode and operate in Pulse Frequency Modulation (PFM).

During PWM operation, the converter uses a unique fast response voltage mode controller scheme with feed-forward input voltage to achieve good Line and Load Regulation, thus allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high side MOSFET switch is turned ON. The current flows from the input capacitor via the high side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trip causing the control logic to turn OFF the switch. The current limit comparator will also turn OFF the switch in case the current limit of the high side MOSFET switch is exceeded. The low side MOSFET rectifier is turned ON and the inductor current ramps down after a dead time preventing shoot-through current. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the low side MOSFET rectifier. The next cycle will again be initiated by the clock signal turning off the low side MOSFET rectifier and turning on the on the high side MOSFET switch.

Table 3. BD71805MWV Output Power Rails (Master Control Mode)

BD71805MWV Output	i.MX6 SoloLite Usage example	Power Supply	Initial Output Voltage	Load max	Adjustable range
BUCK1	ARM/SOC/PU	PVIN1	1.425V	2000mA	0.8 to 2.000V (25mV step) [DVS]
BUCK2	NVCC_DRAM / LPDDR2(1.2V) / Others	PVIN2	1.2V	1000mA	0.8 to 2.000V (25mV step) [DVS]
BUCK3	HIGH / NVCC33_IO/ Wifi / eMMC / Others	PVIN3	3.3V	1000mA	2.6 to 3.35V (50mV step)
BUCK4	NVCC18_IO / LPDDR2(1.8V) / Others	PVIN4	1.8V	1000mA	1.0 to 2.7V (50mV step)
VO1(LDO1)	NVCC_1P2V	VINL1	1.2V	300mA	0.8 to 3.3V (50mV step)
VO2(LDO2)	IO (Default:OFF)	VINL2	3.3V	300mA	0.8 to 3.3V (50mV step)
VO3(LDO3)	IO (Default:OFF)	VINL2	3.3V	300mA	0.8 to 3.3V (50mV step)
VODVREF	DDR_VREF (Default:OFF)	VIN	0.5*DVREFIN	10mA	0.4 to 1.00V (DVREFIN= BUCK2)(Note1)
VOSNVS	SNVS	VIN	3.0V	25mA	Fixed

(Note1) When VODVREF is not in use, please open DVREFIN and VODVREF.

Table 4. BD71805MWV Output Power Rails (Slave Control Mode)

BD71805MWV Output	i.MX6 SoloLite Usage example	Power Supply	Initial Output Voltage	Load max	Adjustable range
BUCK1	ARM	PVIN1	1.375V	2000mA	0.8 to 2.000V (25mV step) [DVS]
BUCK2	SOC/PU	PVIN2	1.375V	1000mA	0.8 to 2.000V (25mV step) [DVS]
BUCK3	HIGH / NVCC33_IO Peripheral, EPD	PVIN3	3.15V	1000mA	2.6 to 3.35V (50mV step)
BUCK4	LPDDR2(1.2V)	PVIN4	1.2V	1000mA	1.0 to 2.7V (50mV step)
VO1(LDO1)	Peripheral	VINL1	2.5V	300mA	0.8 to 3.3V (50mV step)
VO2(LDO2)	NVCC18_IO / LPDDR2(1.8V)	VINL2	1.8V	300mA	0.8 to 3.3V (50mV step)
VO3(LDO3)	NVCC_1P2V / NVCC_DRAM	VINL2	1.2V	300mA	0.8 to 3.3V (50mV step)
VODVREF	DDR_VREF	VIN	0.5*DVREFIN	10mA	0.5 to 1.35V (DVREFIN=BUCK4)
SNVSCAP	SNVS	VIN	3.0V	25mA	Fixed

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Table 5. BD71805MWV Output Power Rails

#	BUCKx ON[5:0] STBY[5:0] OFF[5:0]	BUCK1 [V]	BUCK2 [V]	BUCK3 [V]	BUCK4 [V]	LDOx[5:0]	LDO1 [V]	LDO2 [V]	LDO3 [V]
0	00 0000	0.800	0.800	2.600	1.000	00 0000	0.800	0.800	0.800
1	00 0001	0.825	0.825	2.650	1.050	00 0001	0.850	0.850	0.850
2	00 0010	0.850	0.850	2.700	1.100	00 0010	0.900	0.900	0.900
3	00 0011	0.875	0.875	2.750	1.150	00 0011	0.950	0.950	0.950
4	00 0100	0.900	0.900	2.800	1.200	00 0100	1.000	1.000	1.000
5	00 0101	0.925	0.925	2.850	1.250	00 0101	1.050	1.050	1.050
6	00 0110	0.950	0.950	2.900	1.300	00 0110	1.100	1.100	1.100
7	00 0111	0.975	0.975	2.950	1.350	00 0111	1.150	1.150	1.150
8	00 1000	1.000	1.000	3.000	1.400	00 1000	1.200	1.200	1.200
9	00 1001	1.025	1.025	3.050	1.450	00 1001	1.250	1.250	1.250
10	00 1010	1.050	1.050	3.100	1.500	00 1010	1.300	1.300	1.300
11	00 1011	1.075	1.075	3.150	1.550	00 1011	1.350	1.350	1.350
12	00 1100	1.100	1.100	3.200	1.600	00 1100	1.400	1.400	1.400
13	00 1101	1.125	1.125	3.250	1.650	00 1101	1.450	1.450	1.450
14	00 1110	1.150	1.150	3.300	1.700	00 1110	1.500	1.500	1.500
15	00 1111	1.175	1.175	3.350	1.750	00 1111	1.550	1.550	1.550
16	01 0000	1.200	1.200		1.800	01 0000	1.600	1.600	1.600
17	01 0001	1.225	1.225		1.850	01 0001	1.650	1.650	1.650
18	01 0010	1.250	1.250		1.900	01 0010	1.700	1.700	1.700
19	01 0011	1.275	1.275		1.950	01 0011	1.750	1.750	1.750
20	01 0100	1.300	1.300		2.000	01 0100	1.800	1.800	1.800
21	01 0101	1.325	1.325		2.050	01 0101	1.850	1.850	1.850
22	01 0110	1.350	1.350		2.100	01 0110	1.900	1.900	1.900
23	01 0111	1.375	1.375		2.300	01 0111	1.950	1.950	1.950
24	01 1000	1.400	1.400		2.350	01 1000	2.000	2.000	2.000
25	01 1001	1.425	1.425		2.400	01 1001	2.050	2.050	2.050
26	01 1010	1.450	1.450		2.450	01 1010	2.100	2.100	2.100
27	01 1011	1.475	1.475		2.500	01 1011	2.150	2.150	2.150
28	01 1100	1.500	1.500		2.550	01 1100	2.200	2.200	2.200
29	01 1101	1.525	1.525		2.600	01 1101	2.250	2.250	2.250
30	01 1110	1.550	1.550		2.650	01 1110	2.300	2.300	2.300
31	01 1111	1.575	1.575		2.700	01 1111	2.350	2.350	2.350
32	10 0000	1.600	1.600			10 0000	2.400	2.400	2.400
33	10 0001	1.625	1.625			10 0001	2.450	2.450	2.450
34	10 0010	1.650	1.650			10 0010	2.500	2.500	2.500
35	10 0011	1.675	1.675			10 0011	2.550	2.550	2.550
36	10 0100	1.700	1.700			10 0100	2.600	2.600	2.600
37	10 0101	1.725	1.725			10 0101	2.650	2.650	2.650
38	10 0110	1.750	1.750			10 0110	2.700	2.700	2.700
39	10 0111	1.775	1.775			10 0111	2.750	2.750	2.750
40	10 1000	1.800	1.800			10 1000	2.800	2.800	2.800
41	10 1001	1.825	1.825			10 1001	2.850	2.850	2.850
42	10 1010	1.850	1.850			10 1010	2.900	2.900	2.900

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Table 6. BD71805MWV Output Power Rails (continued)

#	BUCKx ON[5:0] STBY[5:0] OFF[5:0]	BUCK1 [V]	BUCK2 [V]	BUCK3 [V]	BUCK4 [V]	LDOx[5:0]	LDO1 [V]	LDO2 [V]	LDO3 [V]
43	10 1011	1.875	1.875			10 1011	2.950	2.950	2.950
44	10 1100	1.900	1.900			10 1100	3.000	3.000	3.000
45	10 1101	1.925	1.925			10 1101	3.050	3.050	3.050
46	10 1110	1.950	1.950			10 1110	3.100	3.100	3.100
47	10 1111	1.975	1.975			10 1111	3.150	3.150	3.150
48	11 0000	2.000	2.000			11 0000	3.200	3.200	3.200
49	11 0001					11 0001	3.250	3.250	3.250
50	11 0010					11 0010	3.300	3.300	3.300
51	11 0011					11 0011			
52	11 0100					11 0100			
53	11 0101					11 0101			
54	11 0110					11 0110			
55	11 0111					11 0111			
56	11 1000					11 1000			
57	11 1001					11 1001			
58	11 1010					11 1010			
59	11 1011					11 1011			
60	11 1100					11 1100			
61	11 1101					11 1101			
62	11 1110					11 1110			
63	11 1111					11 1111			
Voltage step		25mV	25mV	50mV	50mV	-	50mV	50mV	50mV

Initial voltage of Master control mode
Initial voltage of Slave control mode

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2. Power ON/OFF Sequence

(1) Master Control Mode

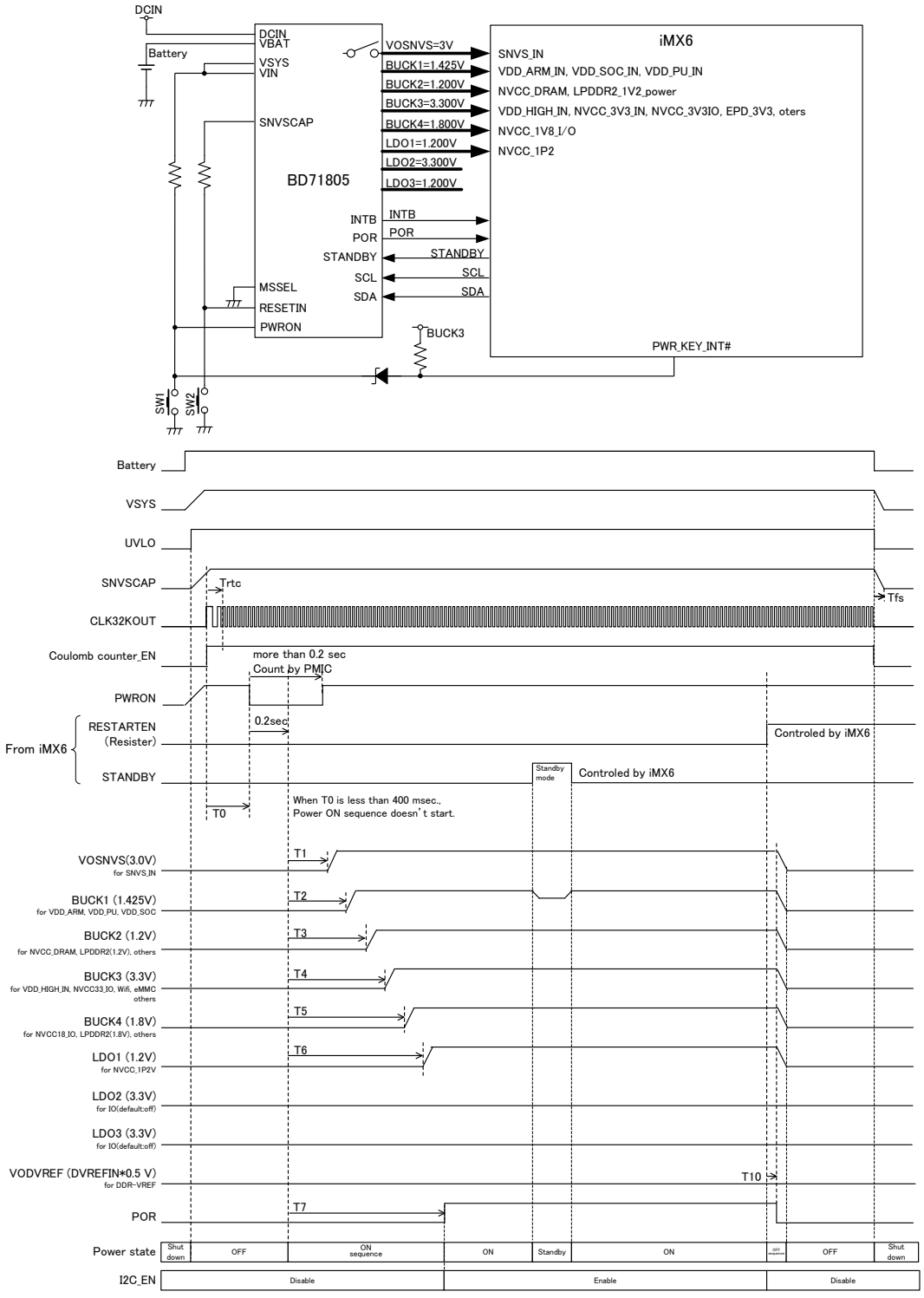

Figure 7. Power-ON/OFF Sequence (Master control mode)

Table 7. Power Rails Turn-ON/OFF Delays (Master control mode)

Parameter	symbol	spec			unit	condition
		min.	typ.	max.		
settling time of RTC clock	Trtc	–	100.0	–	ms	depend on crystal
PWRON valid time	T0	400.0	–	–	ms	
Turn on delay of VOSNVS	T1	–	0.24	–	ms	
Turn on delay of BUCK1	T2	–	0.49	–	ms	
Turn on delay of BUCK2	T3	–	0.73	–	ms	
Turn on delay of BUCK3	T4	–	0.98	–	ms	
Turn on delay of BUCK4	T5	–	1.22	–	ms	
Turn on delay of LDO1	T6	–	1.46	–	ms	
Turn on delay of POR	T7	–	2.44	–	ms	
Turn off delay	T10	–	0.49	–	ms	

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(2) Slave Control Mode

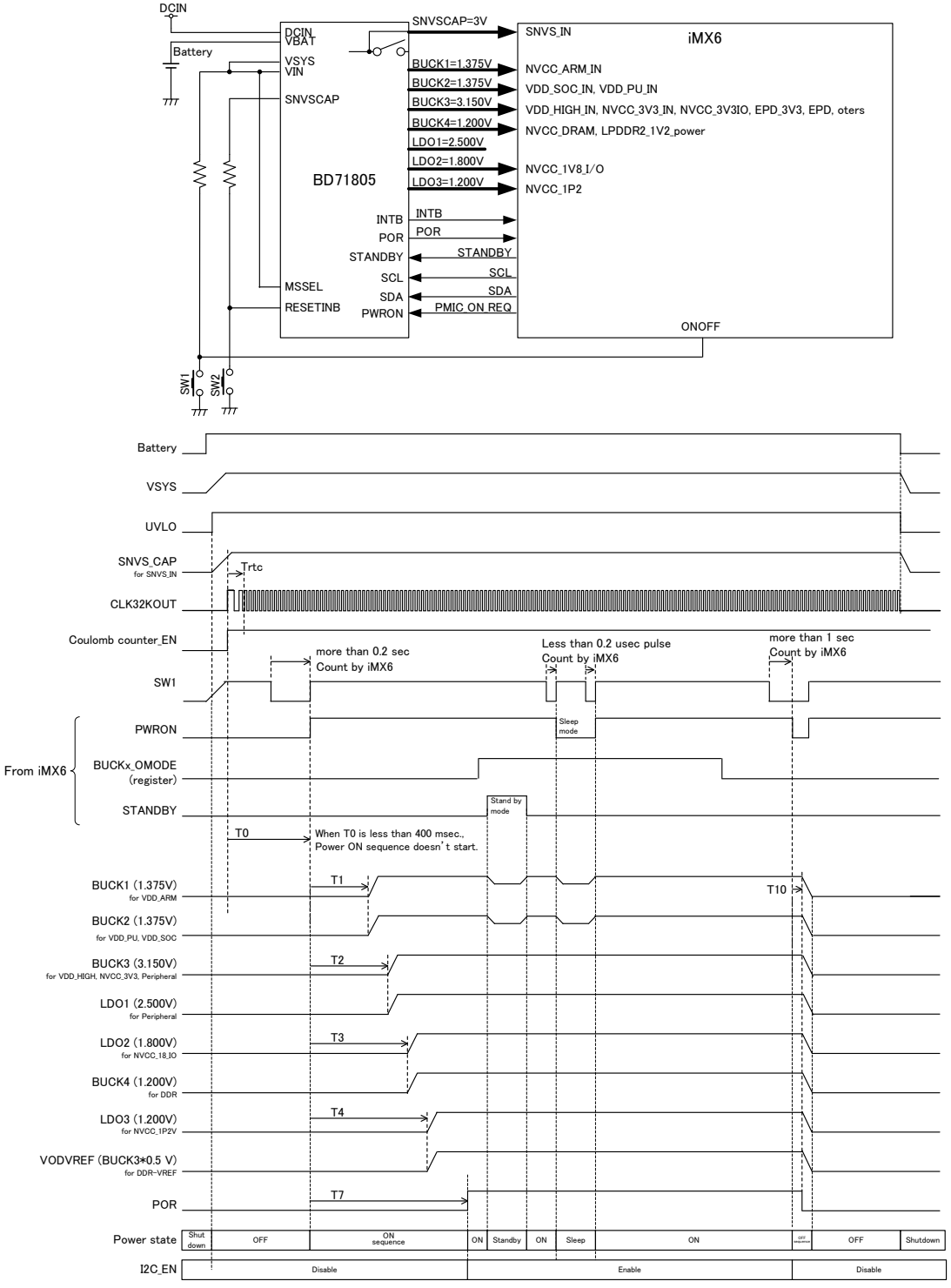

Figure 8. Power-ON/OFF Sequence (Slave control mode)

Table 8. Power Rails Turn-ON/OFF Delays (Slave control mode)

Parameter	symbol	spec			unit	condition
		min.	typ.	max.		
settling time of RTC clock	Trtc	–	100.0	–	ms	depend on crystal
PWRON valid time	T0	400.0	–	–	ms	
Turn on delay of BUCK1 and 2	T1	–	0.24	–	ms	
Turn on delay of BUCK3 and LDO1	T2	–	0.49	–	ms	
Turn on delay of BUCK4 and LDO4	T3	–	0.73	–	ms	
Turn on delay of LDO3 and VODVREF	T4	–	0.98	–	ms	
Turn on delay of POR	T7	–	2.44	–	ms	
Turn off delay	T10	–	0.49	–	ms	

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3. Master Control Modes Operation

BD71805MWV operates at Master control mode when MSSEL is set to LOW.
BD71805MWV Master mode has four power states or modes: ON, OFF, Standby, and Shutdown. Figure 9 shows the state transition diagram along with the conditions to enter and exit from each state.

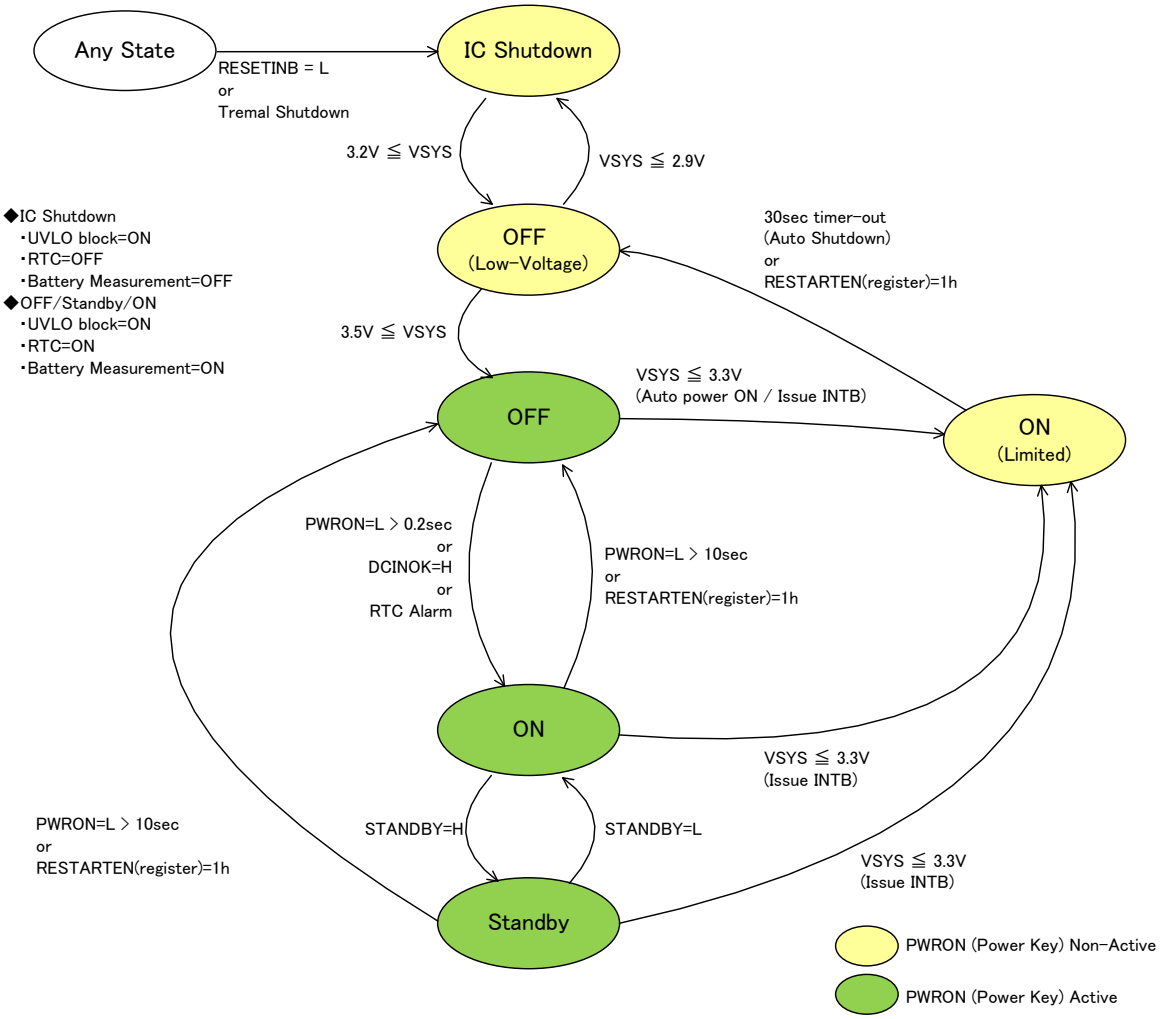

Figure 9. Power States Transitions (Master Control Mode)

Description of states is provided in the following section. Note that VSYS must exceed VSYSMAX (initial=3.5V) to power up. Additionally, I2C control is not possible in Shutdown mode, nonetheless, the interrupt signal, INTB, is active in Standby, and ON states.

Table 9. Voltage Rails ON/OFF for Respective Power States (Master Control Mode)

State	BUCK1	BUCK2	BUCK3	BUCK4	LDO1	LDO2	LDO3	DVREF	VOSNVS	I2C I/F
Shutdown	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Disable
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Disable
ON	ON (PWM fix)	ON (PWM fix)	ON (PWM fix)	ON (PWM fix)	ON	OFF	OFF	OFF	Output	Enable
STANDBY	ON (Auto)	ON (Auto)	ON (Auto)	ON (Auto)	ON	OFF	OFF	OFF	Output	Enable

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(1) Master Control Mode States

(a) Shutdown Mode

When VSYS falls below 2.9V, BD71805MWV enters Shutdown mode. A thermal shutdown event also forces BD71805MWV into Shutdown mode. In case of system hung up, setting RESETINB to LOW will cause the IC to shut down. Only the VSYS voltage measurement block (UVLO) is powered during Shutdown mode. All registers are cleared to initial data. To exit Shutdown mode, VSYS must exceed 3.2V.

(b) OFF (Low-Voltage) Mode

BD71805MWV enters OFF (Low-Voltage) mode when VSYS exceed 3.2V or after Auto Low Power ON event (Automatically turns ON when VSYS falls below VSYSMIN (initial=3.3V)). In this mode, UVLO, RTC and Battery measurement (Coulomb Counter) blocks are powered. No turn on event is accepted in this mode. To exit OFF (Low-Voltage) mode, VSYS must exceed VSYSMAX (initial=3.5V).

(c) OFF Mode

BD71805MWV enters OFF (Low-Voltage) mode after a turn-off event, wherein VSYS exceeds VSYSMAX (initial=3.5V). In this mode, UVLO, RTC and Battery measurement (Coulomb Counter) blocks are powered. POR is asserted LOW in this mode. To exit OFF mode, a valid turn-on event is required.

(d) ON Mode

BD71805MWV enters ON mode after a turn-on event. POR is de-asserted HIGH in this mode of operation.

(e) ON (Limited) Mode

BD71805MWV enters ON (Limited) mode after Auto Low Power ON event. To exit ON (Limited) Mode, set RESTARTEN to HIGH. RESTARTEN register is inaccessible for more than 30 seconds while forced to exit this mode until it enters OFF (Low-Voltage) Mode.

(f) STANDBY Mode

BD71805MWV enters STANDBY mode when STANDBY pin is asserted. This mode is typically used for low-power mode of operation. When in STANDBY mode, power consumption is reduced by lowering regulators' output voltages, or disabling some regulators, etc. Such configuration is pre-programmed through the I2C interface. To exit STANDBY mode, STANDBY pin is de-asserted.

(2) Master Control Mode Events

(a) Turn On Events

From OFF mode, BD71805MWV is powered on by turn on events. BD71805MWV Master mode has three turn on events. See Power Stage Transitions diagram (Figure 9). Following are more detailed descriptions of turn on events.

- If PWRON signal is low (pulse width is 0.2 seconds or more), BD71805MWV will turn on.
- If DCINOK signal is High (DCIN is supplied with appropriate voltage), BD71805MWV will turn on.
- If the alarm that is set in ALM0 register is interrupted, BD71805MWV will turn on.
- If VSYS falls below VSYSMIN (initial:3.3V), BD71805MWV will turn on (Auto Low Power ON event). When this event occurs, INTB is asserted LOW, and the IC enters ON (Limited) Mode.

(b) Turn Off Events

From ON or STANDBY mode, BD71805MWV is powered off by turn off events. BD71805MWV has three turn off events. See Power Stage Transitions diagram (Figure 9). Following are more detailed descriptions of turn on events.

- If PWRON signal is low (pulse width is 10 seconds or more), BD71805MWV will turn off.
- If RESTARTEN register is set to HIGH, BD71805MWV will turn off.
- If 30 seconds elapse after entering ON (Limited) mode, BD71805MWV will turn off.

(c) Thermal Shutdown event (Thermal protection)

If the die temperature surpasses a given threshold, the thermal protection circuit will shut down BD71805MWV to avoid damage. A turn-on event will not power on the PMIC while it is in thermal protection. The part will remain in Shutdown mode until the die temperature decreases below a given threshold. There are no specific interrupts related to this other than the warning interrupt. See Power Dissipation section for more detailed information.

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4. Slave Control Modes Operation

BD71805MWV operates at Slave control mode when MSSEL is set to HIGH.
BD71805MWV has five power states or modes: ON, OFF, Sleep, Standby, and Shutdown. Figure 10 shows the state transition diagram along with conditions to enter and exit from each state.

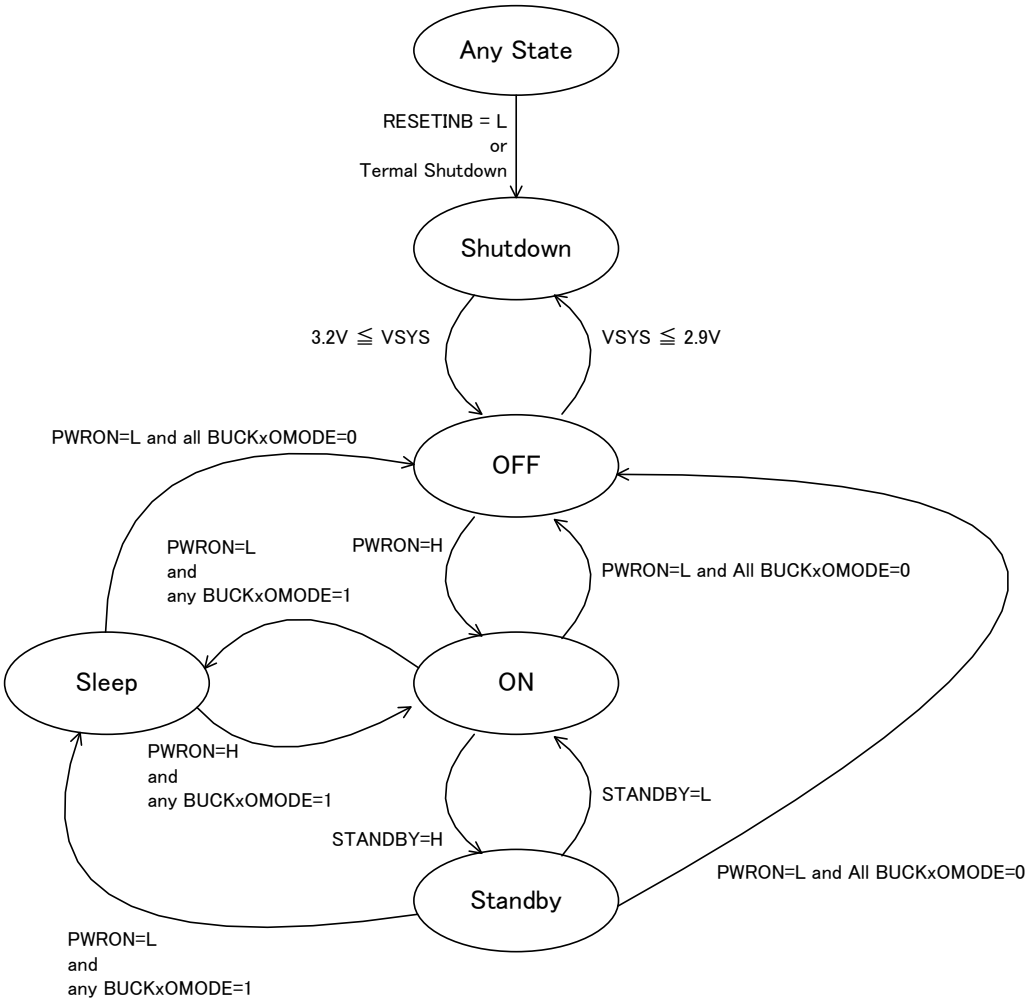

Figure 10. Power States Transitions (Slave Control Mode)

Description of states is provided in the following section. Note that VSYS must exceed 3.2V to allow power up. Additionally, I2C control is not possible in Shutdown mode, nonetheless, the interrupt signal, INTB, is active in Sleep, Standby, and ON states.

Table 10. Voltage Rails ON/OFF for Respective Power States (Slave Control Mode)

State	BUCK1	BUCK2	BUCK3	BUCK4	LDO1	LDO2	LDO3	DVREF	SNVSCAP	I2C I/F
Shutdown	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Disable
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Output	Disable
ON	ON (PWM fix)	ON (PWM fix)	ON (PWM fix)	ON (PWM fix)	ON	ON	ON	ON	Output	Enable
STANDBY	ON (Auto)	ON (Auto)	ON (Auto)	ON (Auto)	ON	ON	ON	ON	Output	Enable
SLEEP	ON (PFMfix)	ON (PFMfix)	ON (PFMfix)	ON (PFMfix)	ON	ON	ON	ON	Output	Enable

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(1) Slave Control Mode States

(a) Shutdown Mode

When VSYS falls below 2.9V, BD71805MWV enters Shutdown mode. A thermal shutdown event also forces BD71805MWV into Shutdown mode. To reset the hung up system, assert RESETINB to LOW causing the IC to shut down. Only VSYS voltage measurement block (UVLO) is powered in this mode. All registers are cleared to initial data. To exit Shutdown mode, VSYS must exceed 3.2V.

(b) OFF Mode

BD71805MWV enters OFF mode after a turn-off event. In this mode, SNVS, UVLO, RTC and Battery measurement (Coulomb Counter) blocks are powered. POR is asserted LOW in this mode. To exit OFF mode, a valid turn-on event is required.

(c) ON Mode

BD71805MWV enters ON mode after a turn-on event. POR is deasserted HIGH in this mode of operation.

(d) STANDBY Mode

BD71805MWV enters STANDBY mode when STANDBY pin is asserted. This mode is typically used for low-power mode of operation. When in STANDBY mode, power consumption is reduced by lowering regulators' output voltages, or disabling some regulators, etc. Such configuration is pre-programmed through the I2C interface. To exit STANDBY mode, STANDBY pin is de-asserted.

(e) SLEEP Mode

BD71805MWV enters SLEEP mode when PWRON pin is de-asserted and any BUCKxOMODE bit is set to HIGH. In SLEEP mode, each regulator will use the settings programmed to its sleep mode registers, e.g., BUCKxOMODE for BUCKx. Activated regulators will maintain the settings for this mode until the next turn-on event.

When in SLEEP mode, power consumption is reduced by lowering regulators' output voltages, shifting regulators to PFM fixed mode, or disabling some regulators, etc. Such configuration is pre-programmed through the I2C interface. To exit SLEEP mode, PWRON pin is asserted.

(2) Slave Control Mode Events

(a) Turn On Events

From OFF mode, BD71805MWV is powered on by turn on events. BD71805MWV Slave mode has two turn on events. See Power Stage Transitions diagram (Figure 10). Following are more detailed descriptions of turn on events.

- If PWRON signal is HIGH, BD71805MWV will turn on.
- If DCINOK signal is High (DCIN is supplied with appropriate voltage), BD71805MWV will turn on.

(b) Turn Off Events

From ON, STANDBY or SLEEP mode, BD71805MWV is powered off by turn off events. BD71805MWV has two turn off events. See Power Stage Transitions diagram (Figure 10). Following are more detailed descriptions of turn on events.

- If PWRON signal is LOW when all BUCKxOMODE bits are set to LOW, BD71805MWV will turn off.
- If VSYS falls below 3.1V, BD71805MWV will turn off.

(c) Thermal Shutdown event (Thermal protection)

If the die temperature surpasses a given threshold, the thermal protection circuit will shut down BD71805MWV to avoid damage. A turn-on event will not power on the PMIC while it is in thermal protection. The part will remain in Shutdown mode until the die temperature decreases below a given threshold. There are no specific interrupts related to this other than the warning interrupt. See Power Dissipation section for more detailed information.

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5. Dynamic Voltage Scaling (DVS) Control

BUCK1 and BUCK2 are support Dynamic Voltage Scaling (DVS). During change in operation mode, BUCK1 and BUCK2 voltages vary accordingly. Output voltage is set by I2C registers as follows.

(1) ON mode : Output voltage is set by BUCK1_ON[5:0] for BUCK1 and BUCK2_ON[5:0] for BUCK2.
(2) STANDBY mode : Output voltage is set by BUCK1_STBY[5:0] for BUCK1 and BUCK2_STBY[5:0] for BUCK2.
(3) SLEEP mode : Output voltage is set by BUCK1_SLP[5:0] for BUCK1 and BUCK2_SLP[5:0] for BUCK2.

Slope speed is also set via I2C register by BUCK1_RAMPRATE[1:0] for BUCK1 and BUCK_RAMPRATE[1:0] for BUCK2.

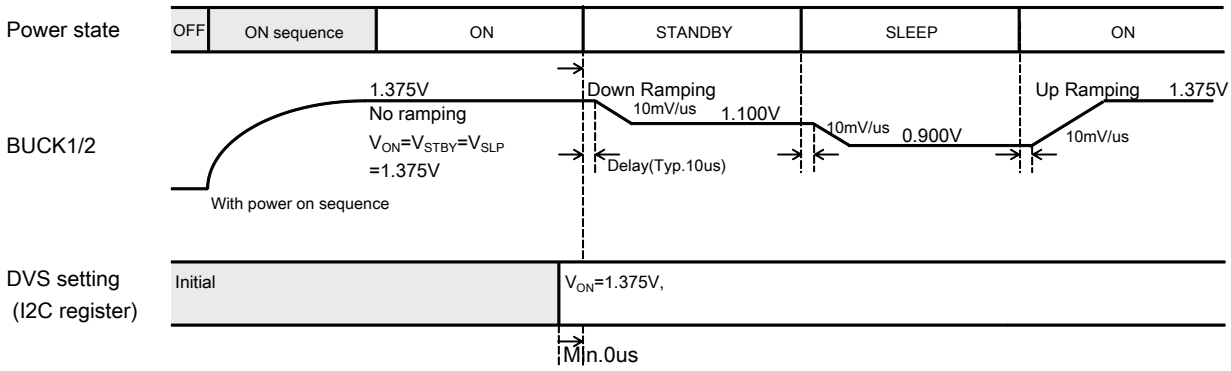

Figure 11. DVS Control image

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6. Over Voltage Protection (OVP) Block

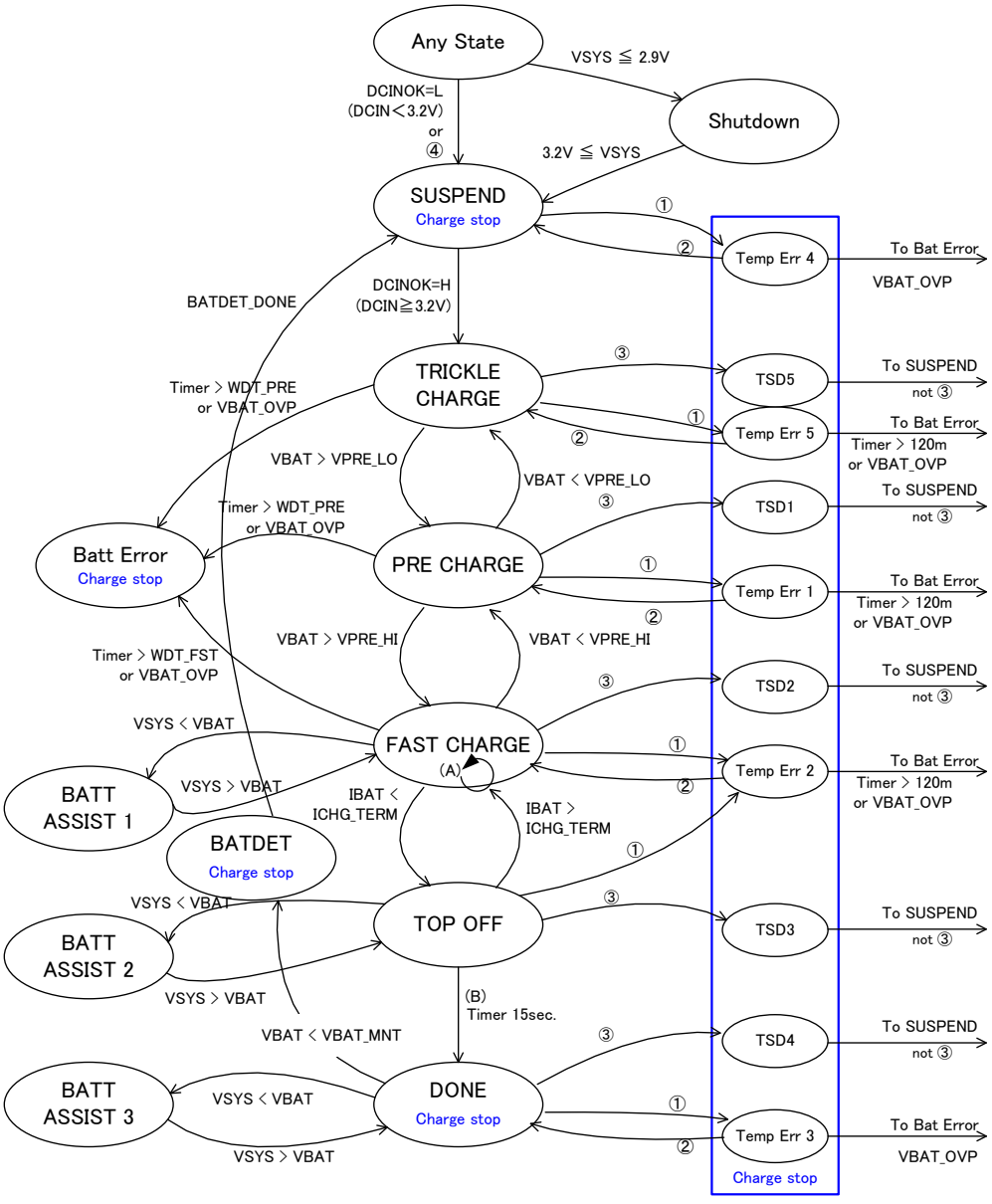
Features

- Single-input for the battery charger source: DCIN
- 30V over voltage protection for DCIN input.

7. Battery Charger Block

Features

- Supports battery insertion and removal detection
- JEITA compliant Battery Charging Profile with thermal control of charging current and voltage settings. This is achieved by measuring the temperature from the external thermistor (The Initial setting of BD71805MWV is adjusted to TDK NTCG163JF103FT1S).
- Supports battery supplement mode
- Automatic or manual (software) control of Watch Dog Timer while Pre–charging and Fast-charging
- Charger statuses or Error conditions are indicated on CHGLED output (for LED lighting)



(Note) When a battery is removed and is connected, please use 3-terminal battery including the thermistor.

Figure 12. Power State of Battery Charger

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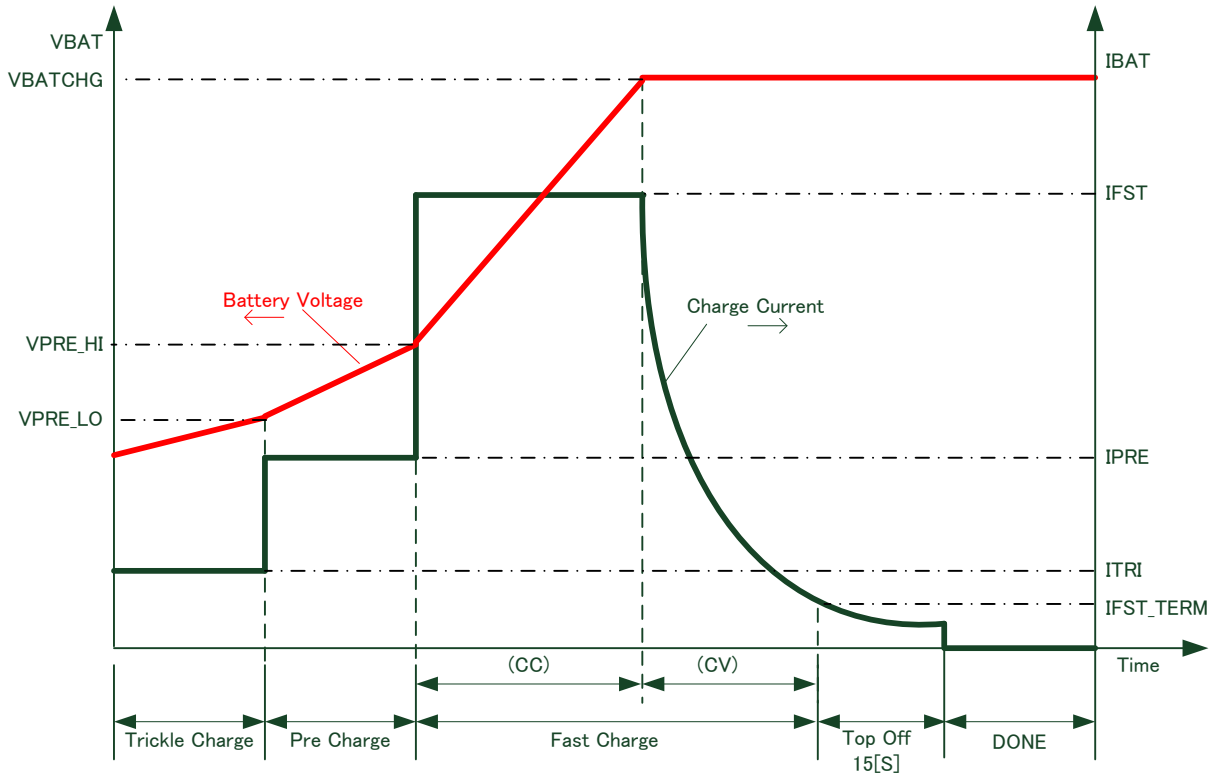

Figure 13. Battery Charger Output Control

There are four Watch Dog Timers to this IC.

A) High temperature protection timer
The High temperature protection timer is a timer to count when BAT_TEMP[2:0]=3h and state of the Temp_err1 or Temp_err2 or Temp_err5. This timer counts 1 in approximately 64 seconds and shifts to BTER state after 121 counts.

B) Low temperature protection timer
The Low temperature protection timer is a timer to count when BAT_TEMP[2:0]=5h and state of the Temp_err1 or Temp_err2 or Temp_err5. This timer counts 1 in approximately 64 seconds and shifts to BTER state after 121 counts.

C) Watch Dog Timer while Pre-charging and Trickle-charging
When Trickle-charge or Pre-charge needs a charge state machine, this timer counts 1 for approximately 64 seconds and shifts to BTER state after 121 counts. But the number of the counts is modifiable by changing register setting.
(Address44h WDT_PRE)

34h:CHG_STATE	3Bh:BAT_TEMP[2:0]	42h:CHG_SET1	WDT_DIS	WDT_AUTO	COLD_ERR_EN	CHG_EN	Initial set value	countdown value	threshold to BTER
TCHG or PCHG	0h or 1h or 2h or 6h	00XXXX11	L	L	H	H	WDT_PRE	-1	1
TCHG or PCHG	0h or 1h or 2h or 6h	01XXXX11	L	H	H	H	122	-1	1

D) Watch Dog Timer while Fast-charging and TOPOFF
When Fast-charge or TOPOFF needs a charge state machine, this timer counts 1 for approximately 64 seconds and shifts to BTER state after 601 counts. But the number of the counts is modifiable by changing register setting.(Address45h WDT_FST) This timer becomes the low temperature protection timer by changing register setting.(Address42h COLD_ERR_EN)

34h:CHG_STATE	3Bh:BAT_TEMP[2:0]	42h:CHG_SET1	WDT_DIS	WDT_AUTO	COLD_ERR_EN	CHG_EN	Initial set value	countdown value	threshold to BTER
FCHG or TOFF	4h	00XXXX11	L	L	H	H	1442	-1	3
FCHG or TOFF	4h	01XXXX11	L	H	H	H	1442	-1	3
FCHG or TOFF	4h	00XXXX01	L	L	L	H	WDT_FST * 8	-2	3
FCHG or TOFF	4h	01XXXX01	L	H	L	H	1442	-2	3
FCHG or TOFF	0h or 1h or 2h or 6h	00XXXX11	L	L	H	H	WDT_FST * 8	-2	240
FCHG or TOFF	0h or 1h or 2h or 6h	01XXXX11	L	H	H	H	1442	-2	240
FCHG or TOFF	0h or 1h or 2h or 6h	00XXXX01	L	L	L	H	WDT_FST * 8	-2	240
FCHG or TOFF	0h or 1h or 2h or 6h	01XXXX01	L	H	L	H	1442	-2	240

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(1) Thermal Control for Charging

Charging current is controlled by the battery temperature measured from the external thermistor.
In low-temperature condition, charging current is reduced to half of the setting value (ICHG).

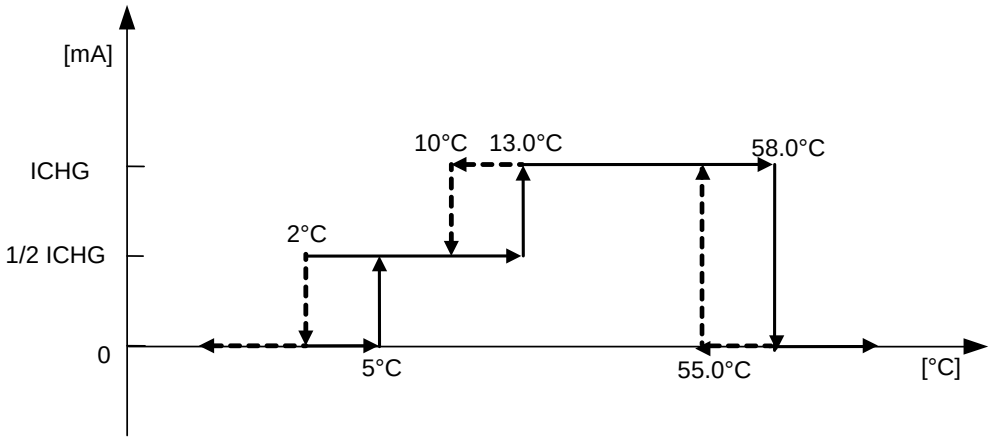

Figure 14. Charging Current vs. Battery Temperature

Charging voltage is also reduced by temperature and set by control registers.

Table 11. Charging Voltage vs. Battery Temperature

JEITA Temperature Range		Voltage Setting Register
T2 – T3	2 to 45°C, (typ)	VBAT_CHG1
T3 – T5	45 to 50°C, (typ)	VBAT_CHG2
T5 – T4	50 to 58°C, (typ)	VBAT_CHG3

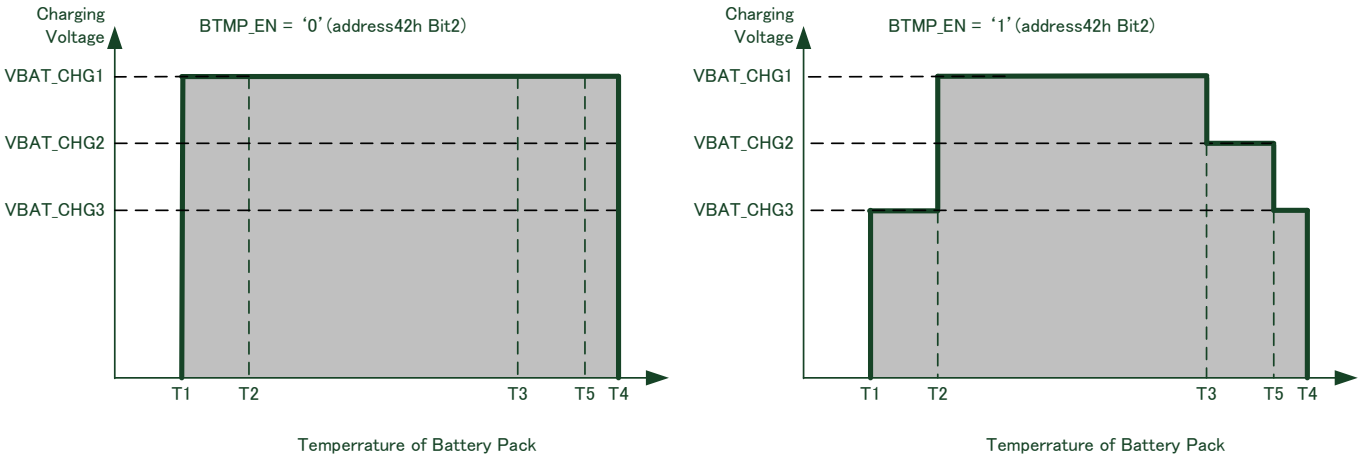

Figure 15. Charging Voltage vs. Battery Temperature

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8. Coulomb Counter Block

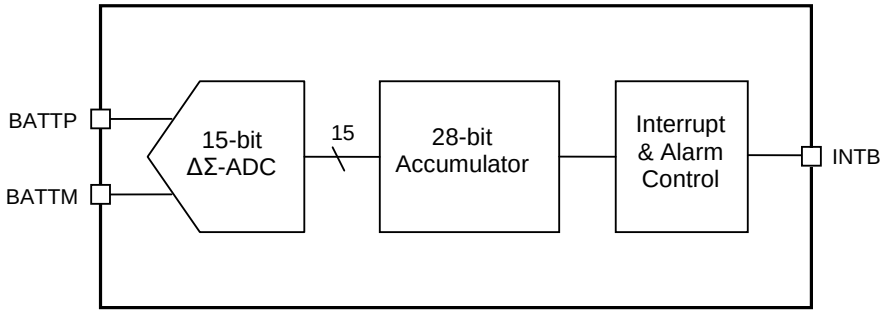

Figure 16. Coulomb Counter Block Diagram

Features

- 28-bit Coulomb Counter for battery fuel gauging
- 15-bit ΔΣ-ADC measures the battery's charge and discharge current by means of an external current sense resistor (10mΩ, ±1%).
- Charging/Discharging amount integration period : 1sec
- Coulomb Counter value approaches the battery capacity when finished charging.
- While discharging, a Half-capacity alarm and a Near-empty alarm can be output from INTB terminal

(1) Functions and Programmabilites

(a) 28-bit accumulator Charge / discharge integration
- Current measurement range is 0 to 3A for charging and discharging
- Current sampling rate is 1, 4, 8, or 16 Hz.
- The time base is from the external 32.768kHz RTC clock.
- Upper 16 bits of 27-bit Coulomb Counter can be read from Host, max 11380mAh.
- Coulomb Counter can be cleared by software command.
- Full charge capacity register can be either set by the Coulomb Counter when charging stops or set from Host.

(b) Two programmable Event Alarm output from INTB pin
- Half-capacity discharge alarm
- Near-empty discharge alarm

(c) Alarm output control settings and status for appropriate event
- Threshold: 16 bits, automatically calculated or set from Host
- Event Status: "1" when the discharge amount exceeds the threshold,
  "0" when the discharge amount is less than the threshold
- Alarm Output Enable: "1" for enabling alarm output / "0" for disabling it.
- Alarm Output Status: "1" indicates the alarm asserted / "0" indicates the alarm not asserted,
  and write to the bits to clear the status.

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9. 12-bit ADC (SAR) Block

Features

- 12-bit Successive Approximation Register A/D Converter
- Conversion period: 40µs
- Input Voltage range: 0.6 to 5.4V (VBAT for Battery voltage monitor)
- Input Voltage range: 0.6 to 5.4V (VSYS for System input voltage monitor)
- Input Voltage range: 0.2 to 1.3V (Vf for BD71805MWV die temperature monitor)
- Input Voltage range: 0.2 to 1.3V (TS for Battery temperature monitor)
- Input Voltage range: -30m to 30mV (BATTP for Battery current monitor)
- Input Voltage range : 2 to 16V (DCIN for DCIN voltage monitor)

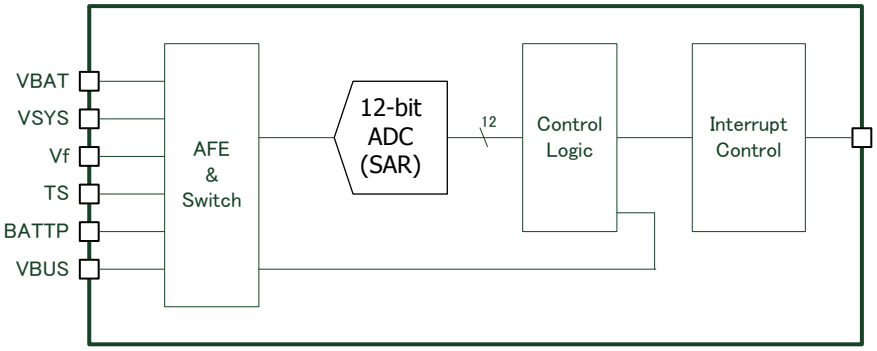

Figure 17. 12-bit ADC Block Diagram

10. Battery Monitor Block

Features

- Monitoring the battery condition and performance
- 12-bit SAR-ADC measures the battery output voltage, battery charge/discharge current with an external current sense resistor (higher rate than the ΔΣ-ADC), and battery temperature with an external thermistor (The Initial setting of BD71805MWV is adjusted to TDK NTCG163JF103FT1S),.
- The battery temperature information is provided for the battery charger.
- Dedicated output pin for alarm/interrupt with several programmable events
- Bias voltage output for the external thermistor
- Automatic low voltage mode (Battery protection)
  - 3.5V detection : interrupt to processor to ask user plug in
  - 3.3V detection : Interrupt to processor to indicate battery critically low condition.
    After 30sec, processor initiates power down. Power key is locked out.

(1) Functions and Programmabilites

(a) Battery Voltage Monitoring to detect over discharging
- Voltage measurement range is 0.6 to 5.4V
- Under voltage threshold is programmable
- Under voltage event can assert the alarm output
- Over Voltage is detected by the Battery Charger while charging

(b) Battery Temperature Monitoring to detect over/under temperature event
- Battery temperature is measured by the voltage of the external NTC thermistor with an external pull-up to bias voltage. (Common circuit with the Battery Charger)
- Over/under Temperature threshold is programmable
- Over/under Temperature event can assert the alarm output
- Software is able to enable/disable battery temperature monitoring

(c) Programmable Event Alarm with several events output from INTB pin
- Under voltage alarm while discharging
- Over/under temperature alarm while charging /discharging
- Over voltage alarm while charging.
- Battery maintenance voltage (VBATMENT) across below/over threshold

(d) Alarm output control settings and status for the appropriate event
- Threshold and Time duration
- Event Status : “1” when the value exceeds the threshold,/ “0” when the value is less than the threshold
- Alarm Output Enable: “1” for enabling alarm output / “0” for disabling it.
- Alarm Output Status: “1” indicates the alarm asserted / “0” indicates the alarm not asserted, and write to the bits to clear the status.

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11. Real Time Clock (RTC) Block

Features

- RTC is driven by 32.768 kHz oscillator and provides alarm and time keeping functions to the nearest second.
- Time information in seconds, minutes, and hours.
- Calendar information in day, month, year, and day of the week.
- Alarm interrupt sent at the time and day which are programmed into registers.
- Key status flags retained through reset and power cycle in RTC backup flags, e.g., reason for power-on or power-off
- Eight bit registers have values that are retained even after the main battery resets to zero when transitioning or until SHUTDOWN state.
- Eight bit registers have a lock control that once written will lock the resistor until SHUTDOWN state is entered.
- Leap year compensation up to 2099.
- Selectable 12-hour and 24-hour modes.
- RTC calibration support.
- Oscillator failure detection.
- 32.768 kHz crystal oscillator recommends SEIKO EPSON FC-135.
  When above-mentioned crystal FC-135 is used, input capacitance (Cin) value and output capacitance (Cout) value recommend 18pF. When different crystal is used, please set Cin and Cout capacitance value on enough matching validation.
- 32.768 kHz crystal oscillator is affected by PCB pattern, parasitic capacitance, the disturbance. To reduce the above-mentioned influence, please place 32.768 kHz crystal connected between XIN32K terminal and XOUT32K terminals and XIN32K input capacitance (Cin) and XOUT32K output capacitance (Cout) to the IC as close as possible. In PCB pattern design, please be careful about the interference with other signal lines.

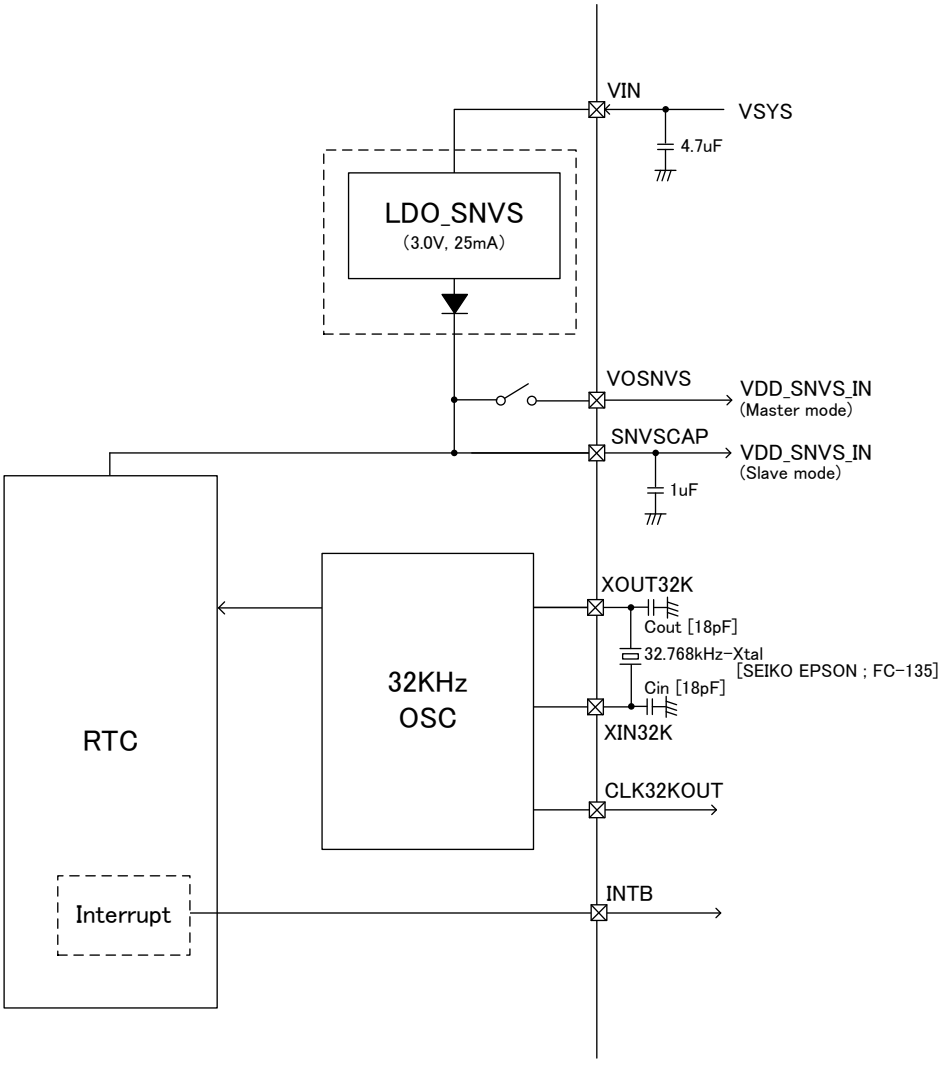

Figure 18. RTC Block Diagram

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(1) Oscillation adjustment

The oscillation adjustment circuit can be used to correct a time count gain or loss with high precision by varying the number of 1-second clock pulses once per 20 or 60 seconds.

When DEV bit in the TRIM Register is set to "0", Oscillation Adjustment Circuit varies the number of 1-second clock pulses once per 20 seconds. When DEV bit in the TRIM Register is set to "1", Oscillation Adjustment Circuit varies the number of 1-second clock pulses once per 60 seconds.

The Oscillation Adjustment Circuit can be disabled by writing the settings "*,0,0,0,0,0,*" ("*" represents "0" or "1") to the TRIM[6:0] in the TRIM Register. Conversely, when such oscillation adjustment is to be made, an appropriate oscillation adjustment value can be calculated using the equation below.

(a) When oscillation frequency is higher than target frequency.

When setting DEV bit to 0:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency} + 0.1)}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 10 + 1$$

When setting DEV bit to 1:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency} + 0.0333)}{\text{Oscillation frequency} \times 1.017 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 30 + 1$$

Oscillation frequency: Frequency of clock pulse output from CLK32KOUT pin.
Target frequency: Desired frequency to be set. Generally, a 32.768kHz quartz crystal unit has temperature characteristics that support the highest oscillation frequency at normal temperature. Consequently, the quartz crystal unit is recommended to have target frequency settings ranging from 32.768 to 32.76810 kHz (+3.05ppm relative to 32.768kHz).
Oscillation adjustment value: Value that is to be finally written to the TRIM[6:0] bits in the TRIM register and is represented in 7-bit coded decimal notation.

(b) When oscillation frequency is equal to target frequency.

Oscillation adjustment value = 0, +1, -64, or -63.

(c) When oscillation frequency is lower than target frequency.

When setting DEV bit to 0:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency})}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 10$$

When setting DEV bit to 1:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency})}{\text{Oscillation frequency} \times 1.017 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 30$$

Oscillation adjustment value calculations are exemplified below

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(ex.A) For an oscillation frequency = 32768.85Hz and a target frequency = 32768.05Hz

When setting DEV bit to 0:

$$\text{Oscillation adjustment value} = \frac{32768.85 - 32768.05 + 0.1}{32768.85 \times 3.051 \times 10^{-6}}$$
$$\approx (32768.85 - 32768.05) \times 10 + 1$$
$$= 9$$

In this instance, write the settings "00001001" in the TRIM register. Thus, an appropriate oscillation adjustment value in the presence of any time count gain represents a distance from 01h.

When setting DEV bit to 1:

$$\text{Oscillation adjustment value} = \frac{32768.85 - 32768.05 + 0.0333}{32768.85 \times 1.017 \times 10^{-6}}$$
$$\approx (32768.85 - 32768.05) \times 30 + 1$$
$$= 25$$

In this instance, write the settings "10011001" in the TRIM register.

(ex.B) For an oscillation frequency = 32762.22Hz and a target frequency = 32768.05Hz

When setting DEV bit to 0:

$$\text{Oscillation adjustment value} = \frac{32762.22 - 32768.05}{32762.22 \times 3.051 \times 10^{-6}}$$
$$\approx (32762.22 - 32768.05) \times 10$$
$$= -58$$

To represent an oscillation adjustment value of -58 in 7bit coded decimal notation, subtract 58 (3Ah) from 128 (80h) to obtain 46h. In this instance, write the settings of "01000110" in the TRIM register. Thus, an appropriate oscillation adjustment value in the presence of any time count loss represents a distance from 80h.

When setting DEV bit to 1:

$$\text{Oscillation adjustment value} = \frac{32762.22 - 32768.05}{32762.22 \times 1.017 \times 10^{-6}}$$
$$\approx (32762.22 - 32768.05) \times 30$$
$$= -175$$

Oscillation adjustment value can be set from -62 to 63. Then, in this case, Oscillation adjustment value is out of range.

(2) Difference between DEV=0 and DEV=1

Difference between DEV=0 and DEV=1 is the following,

Table 12. Difference between DEV=0 and DEV=1

	DEV=0	DEV=1
Maximum value range	-189.2ppm to 189.2ppm	-62ppm to 63ppm
Minimum resolution	3ppm	1ppm

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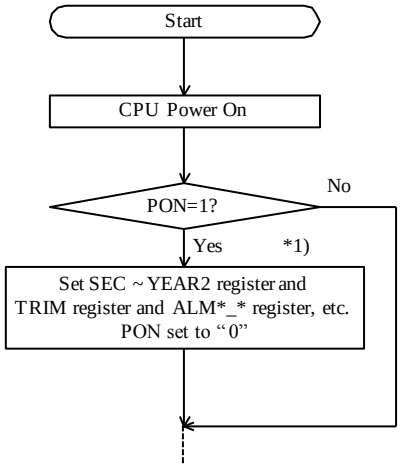
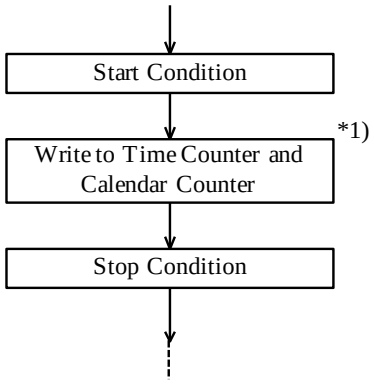
(3) Typical Software-based Operations

Initialization at Power-on



*1) This step involves ordinary initialization including the Oscillation Adjustment Register and interrupt cycle settings, etc.

Writing of Time and Calendar Data



*1) Writing on the min ~ year register is not recommended if the sec register is not also modified.
This is because when the seconds digit goes up while accessing I2C, the clock could assume an unpredictable value.
This can be prevented by writing on the sec register because less than 1Hz counter is cleared.

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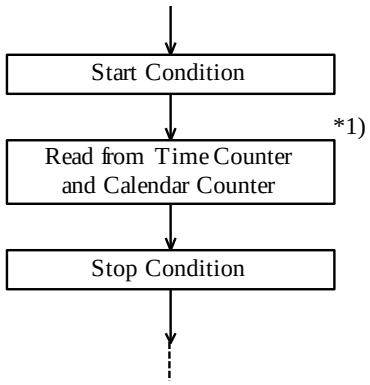
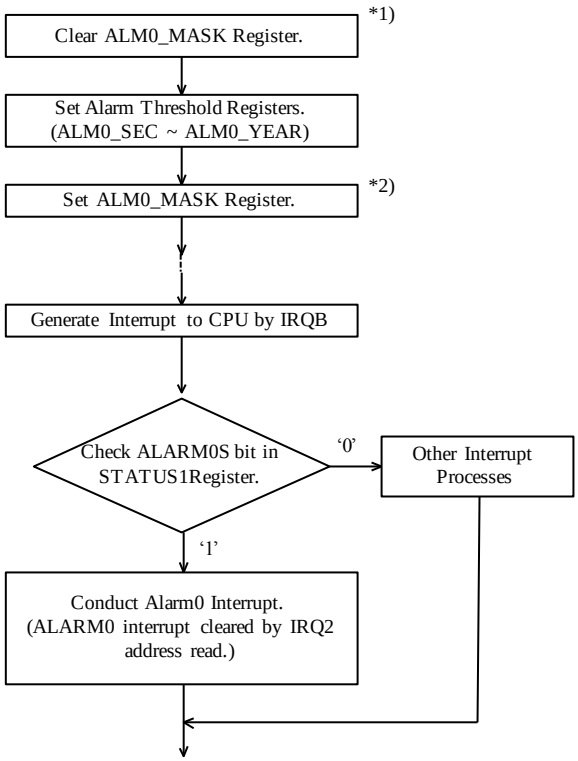
Reading Time and Calendar Data



*1) When reading clock and calendar counters, do not insert Stop Condition.

ALARM0 Interrupt Process



*1) This step is intended to disable the alarm interrupt circuit once by clearing ALM0_MASK register in anticipation of the coincidental occurrence of a match between current time and preset alarm time as the alarm interrupt function is set.

*2) This step is intended to enable the alarm interrupt function after completion of all alarm interrupt settings.

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12. I2C Bus Interface Block

The I2C compatible synchronous serial interface provides access to programmable functions and register on the device.

This protocol uses a two-wire interface for bi-directional communications between LSI's connected to the bus.

The two interface lines are Serial Data Line (SDA), and Serial Clock Line (SCL). These lines should be connected to the power supply DVDD by a pull-up resistor and remain high even when the bus is idle.

(1) Start and Stop Conditions

When SCL is high, pulling SDA low produces a start condition, while pulling SDA high produces a stop condition. Every instruction is started when a start condition occurs and terminated when a stop condition happens.

During read, a stop condition causes reading to terminate, then the chip enters the standby state.

During write, a stop condition causes the fetching of write data to terminate, after which writing starts automatically. Upon the completion of writing, the chip enters the standby state.

Two or more start conditions can not be entered consecutively.

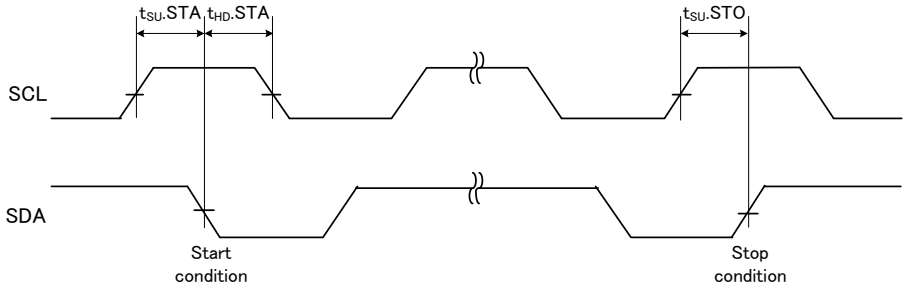

Figure 19. Start and Stop Conditions

(2) Modifying Data

Data on the SDA input can be modified while SCL is low. When SCL is high, modifying the SDA input means a start or stop condition.

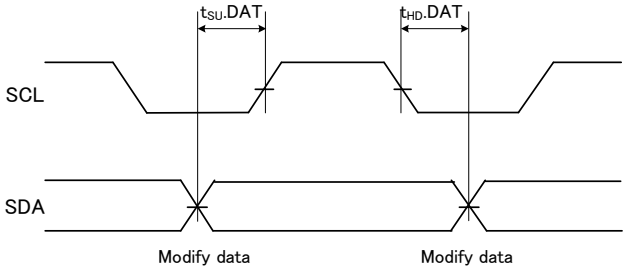

Figure 20. Modifying Data

(3) Acknowledge

Data is transmitted and received in 8-bit units. The receiver sends an acknowledge signal by outputting low on SDA in the 9th clock cycle, indicating that it has received data normally. The transmitter releases the bus in the 9th clock cycle to receive an acknowledge signal.

During write, the chip is always the receiver so that it outputs an acknowledge signal each time it has received eight bits of data.

During read, the chip outputs an acknowledge signal after it receives an address following a start condition. Then, it outputs read data and releases the bus to wait for an acknowledge signal from the master. When it detects an acknowledge signal, it outputs data at the next address if it does not detect a stop condition. If the chip does not detect an acknowledge signal, it stops read operation and enters the standby state wherein a stop condition occurs subsequently.

If the chip does not detect an acknowledge signal nor a stop condition, it keeps the bus released.

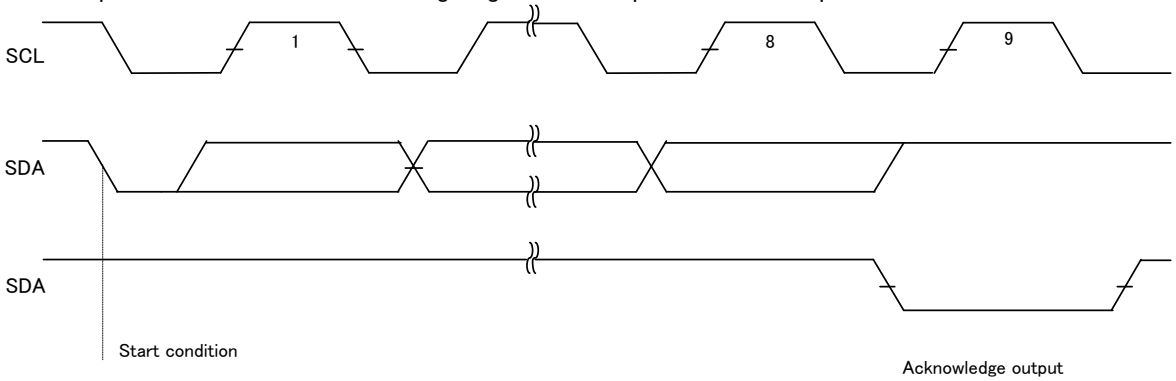

Figure 21. Acknowledge

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(4) Device Addressing

After a start condition occurs, a 7-bit device address and a 1-bit read/write instruction code are sent as input to the chip. The upper seven bits are called device address, which must always be “1001011”.

The least significant bit (R/W:READ/WRITE) indicates a read instruction when set to 1 and a write instruction when set to 0. An instruction is not executed if the device address does not match the specified value.

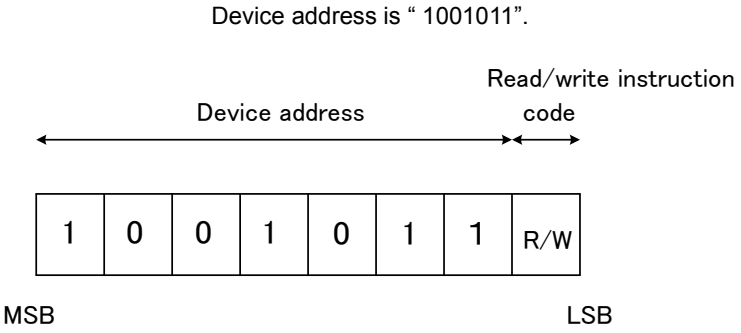

Figure 22. Device Addressing

(5) Write/Read operation

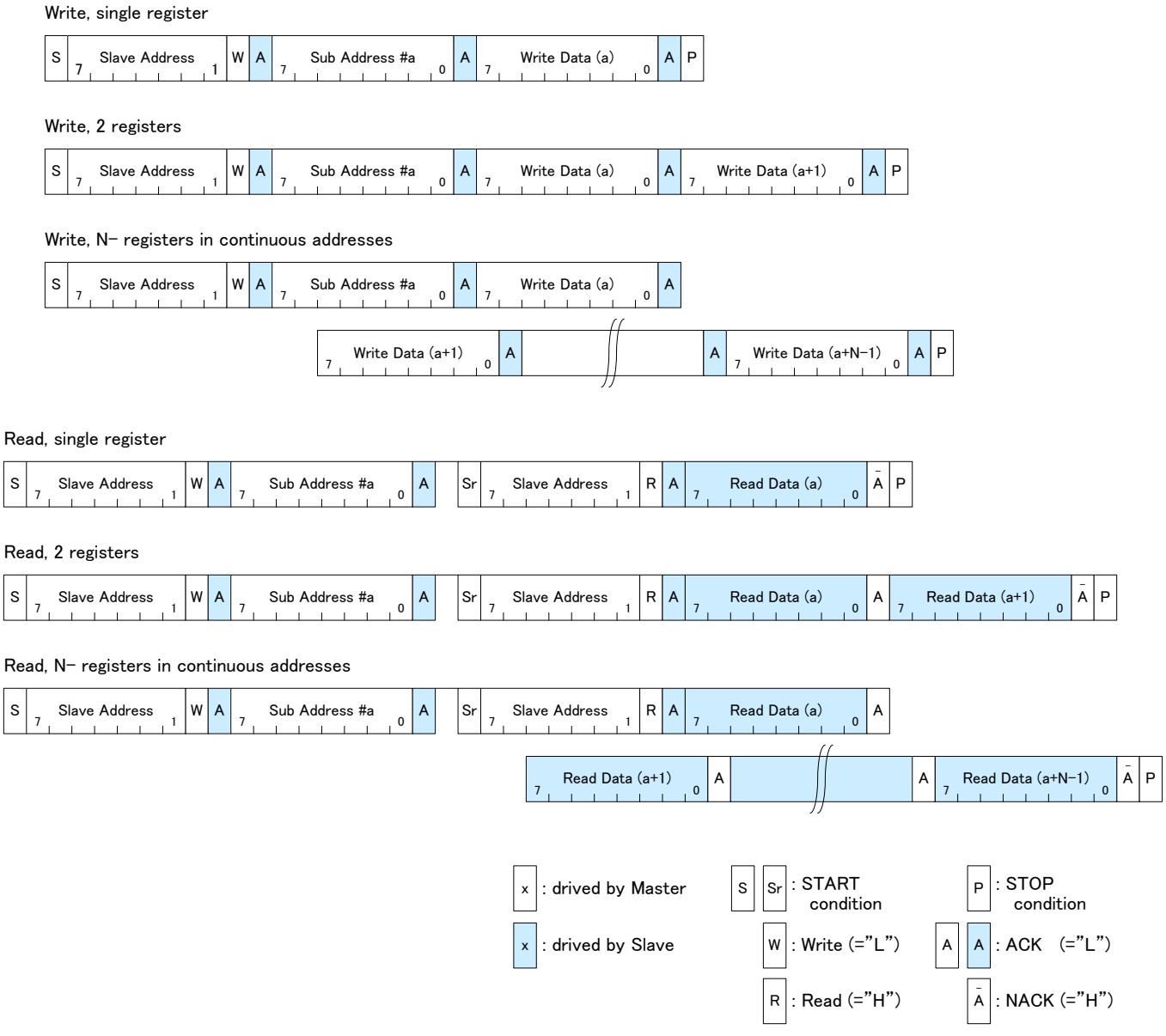

Figure 23. I2C Write / Read Operation

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(6) Pulling up the SDA and SCL pins

This IC requires SDA and SCL pins to be pulled up with an external resistor. The values of the pull-up resistors are determined by the capacitance of the bus. Exceedingly large resistance combined with a given bus capacitance will result to a rise time that would violate the maximum rise time specification. On the other hand, insufficiently small resistance will result in a contention with the pull-down transistor on either slave or master. The recommended pull-up resistance range is 1kohm to 5kohm.

Consider the DVDD related input threshold of VIH = 0.7xVDD and VIL = 0.3xVDD for the purposes of RC time constant calculation.

$V(t1) = 0.3 \times DVDD = DVDD\ (1 - e^{-t1\ /\ RC})$; then $t1 = 0.3566749 \times RC$

$V(t2) = 0.7 \times DVDD = DVDD\ (1 - e^{-t2\ /\ RC})$; then $t2 = 1.2039729 \times RC$

$T = t2 - t1 = 0.8473 \times RC$

To determine the value of the pull-up resistance, you can calculate it by using the equation R=t/(0.8473C).

t : SDA, SCL rise time to meet the I2C AC specification.

C : Total Bus capacitance on each SDA, SCL line.

(7) About limitation of I2C

Write data is synchronized with internal clock. If internal fifo is full, not generating an acknowledge for write data. For example, continuous addressing access with more than 294kHz in I2C.

13. Interrupt Handling

The system is informed about important events through interrupts. Enabled interrupt events are signaled to the processor by driving the INTB pin low.

Each interrupt can be disabled by setting the corresponding enable bit to 0.

Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain set until cleared. Each interrupt can be cleared by writing “1” to the appropriate bit in the Interrupt Status register; this will also cause the INTB pin to go high. If there are multiple interrupt bits, the INTB pin will remain low until all are cleared. If a new interrupt occurs while the processor clears an existing interrupt bit, the INTB pin will remain low.

The IC powers up with all interrupts disabled, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can enable the interrupt bits of interest.

Interrupts generated by external events are debounced; therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are documented in the Interrupt summary. Due to the asynchronous nature of the debounce timer, the effective debounce time can vary slightly.

Table 13. Interrupt summary

Interrupt Event	Register Map				Debounce Interval [Hz] (3 times match)	Interrupt Event	Register Map				Debounce Interval [Hz] (3 times match)
	Enable		Status/Clear				Enable		Status/Clear		
	Address	bit	Address	bit			Address	bit	Address	bit	
BUCK4FAULT	88	3	95	3	1kHz	VBAT_OV_DET	8E	7	9B	7	128Hz
BUCK3FAULT	88	2	95	2	1kHz	VBAT_OV_RES	8E	6	9B	6	128Hz
BUCK2FAULT	88	1	95	1	1kHz	VBAT_LO_DET	8E	5	9B	5	128Hz
BUCK1FAULT	88	0	95	0	1kHz	VBAT_LO_RES	8E	4	9B	4	128Hz
DCIN_OV_DET	89	5	96	5	1kHz	VBAT_SHT_DET	8E	3	9B	3	128Hz
DCIN_OV_RES	89	4	96	4	1kHz	VBAT_SHT_RES	8E	2	9B	2	128Hz
DCIN_CLPS_IN	89	3	96	3	4kHz	DBAT_DET	8E	1	9B	1	128Hz
DCIN_CLPS_OUT	89	2	96	2	4kHz	VBAT_MON_DET	8F	1	9C	1	128Hz
DCIN_RMV	89	1	96	1	1kHz	VBAT_MON_RES	8F	0	9C	0	128Hz
DCIN_MON_DET	8A	1	97	1	4kHz	BATCAP_MON3_DET	90	2	9D	2	1Hz
DCIN_MON_RES	8A	0	97	0	4kHz	BATCAP_MON2_DET	90	1	9D	1	1Hz
VSYS_MON_DET	8B	7	98	7	128Hz	BATCAP_MON1_DET	90	0	9D	0	1Hz
VSYS_MON_RES	8B	6	98	6	128Hz	OCUR3_DET	91	5	9E	5	4kHz
VSYS_LO_DET	8B	3	98	3	128Hz	OCUR3_RES	91	4	9E	4	4kHz
VSYS_LO_RES	8B	2	98	2	128Hz	OCUR2_DET	91	3	9E	3	4kHz
VSYS_UV_DET	8B	1	98	1	128Hz	OCUR2_RES	91	2	9E	2	4kHz
VSYS_UV_RES	8B	0	98	0	128Hz	OCUR1_DET	91	1	9E	1	4kHz
CHG_TRNS	8C	7	99	7	32.768kHz	OCUR1_RES	91	0	9E	0	4kHz
TMP_TRNS	8C	6	99	6	32.768kHz	VF_MON_DET	92	7	9F	7	1Hz
BAT_MNT_IN	8C	5	99	5	1kHz	VF_MON_RES	92	6	9F	6	1Hz
BAT_MNT_OUT	8C	4	99	4	1kHz	VF_F125_DET	92	5	9F	5	128Hz
CHG_WDT_EXP	8C	3	99	3	32.768kHz	VF_F125_RES	92	4	9F	4	128Hz
EXTEMP_TOUT	8C	2	99	2	32.768kHz	OVBTMP_DET	92	3	9F	3	1Hz
TH_DET	8D	7	9A	7	1Hz	OVBTMP_RES	92	2	9F	2	1Hz
TH_RMV	8D	6	9A	6	1Hz	LOBTMP_DET	92	1	9F	1	1Hz
BAT_DET	8D	5	9A	5	128Hz	LOBTMP_RES	92	0	9F	0	1Hz
BAT_RMV	8D	4	9A	4	128Hz	ALM2	93	2	A0	2	128Hz
TMP_OUT_DET	8D	1	9A	1	1Hz	ALM1	93	1	A0	1	128Hz
TMP_OUT_RES	8D	0	9A	0	1Hz	ALM0	93	0	A0	0	128Hz

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Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Maximum Supply Voltage 1 DCIN	$V_{DCINMAX}$	30	V
Maximum Supply Voltage 2 VIN, PVIN1,2,3,4, VINL1, VINL2	V_{INMAX} P_{VINMAX} $V_{INL1MAX}$ $V_{INL2MAX}$	6.0	V
Maximum Supply Voltage 3 DVDD	$V_{DVDDMAX}$	4.5	V
Power Dissipation (Note1)	Pd	4.16	W
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +125	°C

(Note 1) Derate by 41.6mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board 74.2x74.2x1.6tmm).
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
Input Voltage Range 1 DCIN	V_{DCIN}	3.5 to 28	V
Input Voltage Range 2(Note2) VIN, PVIN1,2,3,4	V_{IN} P_{VIN}	3.3 to 5.5	V
Input Voltage Range 3 VINL1, VINL2	V_{INL1} V_{INL2}	2.6 to 5.5	V
Input Voltage Range 4 DVDD	V_{DVDD}	1.5 to 3.4	V

(Note2) It is necessary to supply the same voltage to VIN, and PVIN1,2,3,4

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Electrical Characteristics

(Unless otherwise specified, Ta=+25°C, VIN=PVIN=4.0V, DVDD=1.8V, BUCK1=1.425V, BUCK2=1.2V, BUCK3=VINL1=VINL2=3.3V, BUCK4=1.8V, LDO1=1.2V, LDO2=LDO3=3.3V <Default of master control mode>)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Quiescent Circuit Current						
VBAT Circuit Current 1 (OFF)	I_{QVB1}	-	25	70	µA	RTC , Coulomb counter LDO_SNVS, 32kOSC are ON. DCINOK=L, DVDD=0V
VBAT Circuit Current 2 (STANDBY)	I_{QVB2}	-	180	300	µA	BUCKs, LDOs, are all on. (PWM/PFM Auto Mode) DCINOK=L
VBAT Circuit Current 3 (ON)	I_{QVB3}	-	16	36	mA	BUCKs, LDOs are all on. (PWM Mode)
DVDD Circuit Current	I_{QDVDD}	-	-	1	µA	
Voltage Detector – UVDET						
Detect Voltage1	V_{UVLO35}	3.4	3.5	3.6	V	VIN sweep down Interrupt to processor
Detect Voltage2	V_{UVLO33}	3.2	3.3	3.4	V	VIN sweep down Interrupt to processor 30sec Timer start
Detect Voltage3	V_{UVLO29}	2.81	2.9	2.99	V	VIN sweep down UVLO – IC shutdown
Release Voltage	$V_{UVLOR32}$	3.1	3.2	3.3	V	VIN sweep up UVLO – IC Active
GPO1, 2, 3						
Output L Level	V_{OL_GPO}	-	-	0.4	V	I_{OL}=1mA
Output Off Leak current	I_{OFF_GPO}	-	-	1	µA	V_{GPO}=5.5V,VIN=5.5V Open Drain output off mode
Digital pin characteristics - Input1 (PWRON, STANDBY)						
PWRON, STANDBY, Input "H" level	V_{IH1}	1.44	-	-	V	
PWRON, STANDBY, Input "L" level	V_{IL1}	-	-	0.4	V	
PWRON, STANDBY, Pull Up/ Down Resistance	R_{P1}	-	1.5	-	MΩ	PWRON Pull up(Master Mode) STANDBY Pull Down
Digital pin characteristics – Input2 (RESETINB, MSSEL)						
RESETINB, MSSEL Input "H" level	V_{IH2}	2.1	-	-	V	
RESETINB, MSSEL Input "L" level	V_{IL2}	-	-	0.9	V	
RESETINB Pull Up Resistance	R_{PU2}	-	10	-	kΩ	
Digital pin characteristics – Input3 (SCL, SDA)						
SCL,SDA Input "H" level	V_{IH3}	DVDD x0.7	-	DVDD +0.3	V	
SCL,SDA Input "L" level	V_{IL3}	-0.3	-	DVDD x0.3	V	
SCL,SDA Input leak current	I_{IC3}	-1	-	1	µA	
Digital pin characteristics - Output (SDA, POR, INTB)						
SDA Output "L" level voltage	V_{OL1}	-	-	0.4	V	I_{OL}=6mA
POR, INTB Output "L" level voltage	V_{OL2}	-	-	0.4	V	I_{OL}=1mA

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(Unless otherwise specified, Ta=+25°C, VIN=PVIN=4.0V, DVDD=1.8V, BUCK1=1.425V, BUCK2=1.2V, BUCK3=VINL1=VINL2=3.3V, BUCK4=1.8V, LDO1=1.2V, LDO2=LDO3=3.3V <Default of master control mode>)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
BUCK1 – ARM, SOC, PU						
Output Voltage	V_{OSW1}	1.404	1.425	1.446	V	Initial value, Io=200mA PWM Mode
Programmable Output Voltage Range	V_{ORSW1}	0.80	-	2.00	V	25mV step
Output Current	I_{OSW1}	-	-	2000	mA	PWM Mode
Load Stability	ΔV_{LSW1}	-	10	20	mV	Io=1mA to 2000mA, PWM Mode
Efficiency	η_{SW11}	-	85	-	%	Vo=1.425V, Io=1mA Inductor Rdc=84mΩ
	η_{SW12}	-	89	-	%	Vo=1.425V, Io=200mA Inductor Rdc=84mΩ
Oscillating Frequency	f_{SW1}	-	2.5	-	MHz	Vo=1.425V, Io=200mA PWM mode
Turn-on Time	t_{ONSW1}	-	-	500	usec	
Discharge Resistance	R_{DISSW1}	-	600	-	Ω	
Output Inductance	L_{SW1}	1.5	2.2	-	µH	Ta = -40°C to 85°C
Output Capacitance	C_{SW1}	4.7	10	-	µF	Ta = -40°C to 85°C with BUCK's DC bias
BUCK2 – NVCC_DRAM, LPDDR2(1.2V)						
Output Voltage	V_{OSW2}	1.182	1.200	1.218	V	Initial value, Io=200mA PWM Mode
Programmable Output Voltage Range	V_{ORSW2}	0.80	-	2.00	V	25mV step
Output Current	I_{OSW2}	-	-	1000	mA	PWM Mode
Load Stability	ΔV_{LSW2}	-	10	20	mV	Io=1mA to 1000mA, PWM Mode
Efficiency	η_{SW21}	-	80	-	%	Vo=1.2V, Io=1mA Inductor Rdc=84mΩ
	η_{SW22}	-	86	-	%	Vo=1.2V, Io=200mA Inductor Rdc=84mΩ
Oscillating Frequency	f_{SW2}	-	2.5	-	MHz	Vo=1.2V, Io=200mA PWM mode
Turn-on Time	t_{ONSW2}	-	-	500	usec	
Discharge Resistance	R_{DISSW2}	-	600	-	Ω	
Output Inductance	L_{SW2}	1.5	2.2	-	µH	Ta=-40°C to 85°C
Output Capacitance	C_{SW2}	4.7	10	-	µF	Ta=-40°C to 85°C with BUCK's DC bias

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(Unless otherwise specified, Ta=+25°C, VIN=PVIN=4.0V, DVDD=1.8V, BUCK1=1.425V, BUCK2=1.2V, BUCK3=VINL1=VINL2=3.3V, BUCK4=1.8V, LDO1=1.2V, LDO2=LDO3=3.3V <Default of master control mode>)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
BUCK3 – HIGH, NVCC33_IO, Wifi, eMMC, others						
Output Voltage	V_{OSW3}	3.250	3.300	3.350	V	Initial value, Io=200mA PWM Mode
Programmable Output Voltage Range	V_{ORSW3}	2.60	-	3.350	V	50mV step
Output Current	I_{OSW3}	-	-	1000	mA	PWM Mode
Load Stability	ΔV_{LSW3}	-	10	20	mV	Io=1mA to 1000mA, PWM Mode
Efficiency	η_{SW31}	-	92	-	%	Vo=3.3V, Io=1mA Inductor Rdc=84mΩ
	η_{SW32}	-	95	-	%	Vo=3.3V, Io=200mA Inductor Rdc=84mΩ
Oscillating Frequency	f_{SW3}	-	2.5	-	MHz	Vo=3.3V, Io=200mA PWM mode
Turn-on Time	t_{ONSW3}	-	-	500	usec	
Discharge Resistance	R_{DISSW3}	-	600	-	Ω	
Output Inductance	L_{BUCK3}	1.5	2.2	-	μH	Ta =-40°C to 85°C
Output Capacitance	C_{BUCK3}	4.7	10	-	μF	Ta=-40°C to 85°C with BUCK's DC bias
BUCK4 – NVCC18_IO, LPDDR(1.8V), others						
Output Voltage	V_{OSW4}	1.773	1.800	1.827	V	Initial value, Io=200mA PWM Mode
Programmable Output Voltage Range	V_{ORSW4}	1.00	-	2.70	V	50mV step
Output Current	I_{OSW4}	-	-	1000	mA	PWM Mode
Load Stability	ΔV_{LSW4}	-	10	20	mV	Io=1mA to 1000mA, PWM Mode
Efficiency	η_{SW41}	-	86	-	%	Vo=1.8V, Io=1mA Inductor Rdc=84mΩ
	η_{SW42}	-	90	-	%	Vo=1.8V, Io=200mA Inductor Rdc=84mΩ
Oscillating Frequency	f_{SW4}	-	2.5	-	MHz	Vo=1.8V, Io=200mA PWM mode
Turn-on Time	t_{ONSW4}	-	-	500	usec	
Discharge Resistance	R_{DISSW4}	-	600	-	Ω	
Output Inductance	L_{SW4}	1.5	2.2	-	μH	Ta =-40°C to 85°C
Output Capacitance	C_{SW4}	4.7	10	-	μF	Ta=-40°C to 85°C with BUCK's DC bias

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(Unless otherwise specified, Ta=+25°C, VIN=PVIN=4.0V, DVDD=1.8V, BUCK1=1.425V, BUCK2=1.2V, BUCK3=VINL1=VINL2=3.3V, BUCK4=1.8V, LDO1=1.2V, LDO2=LDO3=3.3V <Default of master control mode>)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO1						
Output Voltage	V_{OL1}	1.176	1.200	1.224	V	Initial value Io=50mA
Programmable Output Voltage Range	V_{ORL1}	0.80	-	3.30	V	50mV step
Output Current	I_{OL1}	-	-	300	mA	
Dropout Voltage	V_{ODPL1}	-	0.10	-	V	Io=50mA VINL1=3.2V (Vo=3.3V setting)
Input Voltage Stability	ΔV_{IL1}	-	2	5	mV	VIN =PVIN=3.5V to 4.5V, Io=50mA
Load Stability	ΔV_{LL1}	-	10	20	mV	Io=1mA to 150mA
Discharge Resistance	R_{DISL1}	-	600	-	Ω	
Ripple rejection ratio	RR_{L1}	-	60	-	dB	VIN=PVIN=4.2V, VR=0.4Vpp, fR=120Hz, Io=5mA, Vo=1.2V BW=20Hz to 20kHz
Output Capacitor	C_{OL1}	0.47	1.0	-	μF	Ta=-40°C to 85°C, with LDO's DC bias
LDO2						
Output Voltage	V_{OL2}	3.234	3.300	3.366	V	Initial value Io=50mA
Programmable Output Voltage Range	V_{ORL2}	0.80	-	3.30	V	50mV step
Output Current	I_{OL2}	-	-	300	mA	
Dropout Voltage	V_{ODPL2}	-	0.10	-	V	Io=50mA VINL2=3.2V (Vo=3.3V setting)
Input Voltage Stability	ΔV_{IL2}	-	2	5	mV	VIN=PVIN=3.5V to 4.5V, Io=50mA
Load Stability	ΔV_{LL2}	-	10	20	mV	Io=1mA to 150mA
Discharge Resistance	R_{DISL2}	-	600	-	Ω	
Ripple rejection ratio	RR_{L2}	-	60	-	dB	VIN= PVIN=4.2V, VR=0.4Vpp , fR=120Hz, Io=5mA, Vo=3.3V BW=20Hz to 20kHz
Output Capacitor	C_{OL2}	0.47	1.0	-	μF	Ta=-40 to 85°C, with LDO's DC bias

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(Unless otherwise specified, Ta=+25°C, VIN=PVIN=4.0V, DVDD=1.8V, BUCK1=1.425V, BUCK2=1.2V, BUCK3=VINL1=VINL2=3.3V, BUCK4=1.8V, LDO1=1.2V, LDO2=LDO3=3.3V <Default of master control mode>)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO3						
Output Voltage	V_{OL3}	3.234	3.300	3.366	V	Initial value Io=50mA
Programmable Output Voltage Range	V_{ORL3}	0.80	-	3.30	V	50mV step
Output Current	I_{OL3}	-	-	300	mA	
Dropout Voltage	V_{ODPL3}	-	0.10	-	V	Io=50mA VINL2=3.2V (Vo=3.3V setting)
Input Voltage Stability	ΔV_{IL3}	-	2	5	mV	VIN= PVIN=3.5V to 4.5V, Io=50mA
Load Stability	ΔV_{LL3}	-	10	20	mV	Io=1mA to 150mA
Discharge Resistance	R_{DISL3}	-	600	-	Ω	
Ripple rejection ratio	RR_{L3}	-	60	-	dB	VIN= PVIN=4.2V, VR=0.4Vpp , fR=120Hz, Io=5mA, Vo=3.3.V BW=20Hz to 20kHz
Output Capacitor	C_{OL3}	0.47	1.0	-	μF	Ta=-40 to 85°C, with LDO's DC bias
LDO_DVREF (DDR_VREF)						
Output Voltage	V_{OL4}	DVREFIN *0.49	DVREFIN *0.50	DVREFIN *0.51	V	Io=5mA
Output Current	I_{OL4}	-	-	10	mA	
Input Voltage Stability	ΔV_{IL4}	-	2	5	mV	VIN= PVIN=3.5V to 4.5V, Io=5mA
Load Stability	ΔV_{LL4}	-	10	20	mV	Io=1mA to 10mA
Discharge Resistance	R_{DISL4}	-	600	-	Ω	
Output Capacitor	C_{OL4}	0.47	1.0	-	μF	Ta=-40 to 85°C, with LDO's DC bias
LDO_SNVS						
Output Voltage	V_{OL5}	2.94	3.00	3.06	V	Io=10mA
Output Current	I_{OL5}	-	-	25	mA	
Input Voltage Stability	ΔV_{IL5}	-	2	5	mV	VIN= PVIN=3.5V to 4.5V, Io=10mA
Load Stability	ΔV_{LL5}	-	10	20	mV	Io=1mA to 10mA
Output Capacitor	C_{OL5}	0.47	1.0	-	μF	Ta=-40 to 85°C, with LDO's DC bias

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(Unless otherwise specified, Ta=+25°C, VIN=PVIN=4.0V, DVDD=1.8V, BUCK1=1.425V, BUCK2=1.2V, BUCK3=VINL1=VINL2=3.3V, BUCK4=1.8V, LDO1=1.2V, LDO2=LDO3=3.3V <Default of master control mode>)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Li-ion Battery Charger – OVP						
DCIN UVLO release voltage	V_{DCIN_UVLO}	3.7	3.8	3.9	V	DCIN rising
DCIN UVLO hysteresis range	$V_{DCIN\_UVLOhys}$	100	150	200	mV	
DCIN OVP detection voltage	V_{DCIN_OVP}	6.3	6.5	6.7	V	DCIN rising
DCIN OVP hysteresis range	V_{DCIN_OVPhys}	100	150	200	mV	
Voltage Output turn-on time	t_{DCIN_ON}	-	5	10	msec	
DCIN input current in OVP state	I_{DCIN_OVP}	-	-	3	mA	DCIN < 28V
Li-ion Battery Charger						
Fast Charging current range	I_{BATCHG_R}	100	-	2000	mA	100mA step
Fast Charging current accuracy	I_{BATCHG_AC}	-	±10	-	%	Ichg=500mA
Pre Charging current range	I_{BATPRE_R}	100	-	500	mA	
Trickle Charging current range	I_{TRI_R}	20	-	100	mA	10mA step
Pre Charging detection voltage Low	V_{PRE_L}	2.1	-	3.6	V	BAT rising, 100mV step
Pre Charging detection voltage High	V_{PRE_H}	2.1	-	3.6	V	BAT rising, 100mV step
Battery Charging voltage range	V_{CHG_R}	3.72	-	4.34	V	
BAT OVP detection	V_{BOVP}	4.4	-	4.8	V	50mV step
Charging termination current range	I_{CHG_TERM}	10	-	200	mA	50mA step
Charging termination current accuracy	$I_{CHG\_TERM\_AC}$	-	±20	-	%	Ichg_term=50mA setting
Enter Supplement mode voltage threshold	ΔV_{BS}	20	60	100	mV	VBAT-VSYS voltage
Exit supplement mode voltage threshold（Hysteresis）	ΔV_{BSTH}	-	40	-	mV	
ON-state resistance between SYSTEM and VBAT	R_{ON_VBAT}	40	80	160	mΩ	
Battery error detection time (Pre charging time)	t_{PRE}	116	129	142	min	
Battery error detection time (Fast charging time)	t_{FAST}	577	641	705	min	
Battery error detection time (High temperature protection)	t_{HTPRO}	116	129	142	min	Over 58°C
Charging termination delay time	t_{TOPOFF}	13	15	17	sec	
CHGLED output toggling frequency	f_{CHGLED}	0.48	0.6	0.72	Hz	At Temp Error1 or 2
Battery high voltage threshold	V_{BAT_H}	3.0	-	3.6	V	For VBAT rising detection
Battery low voltage threshold	V_{BAT_L}	2.5	-	3.1	V	For VBAT falling detection
Battery short-circuit detection voltage	V_{BAT_SHT}	1.4	1.5	1.6	V	
Battery short-circuit detection hysteresis range	V_{BAT_SHThys}	-	0.1	-	V	
Battery detection load current	I_{BAT_DET}	-	20	-	mA	
Battery temperature threshold HOT	T_{BTMP_HOT}	-	58	-	°C	

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(Unless otherwise specified, Ta=+25°C, VIN=PVIN=4.0V, DVDD=1.8V, BUCK1=1.425V, BUCK2=1.2V, BUCK3=VINL1=VINL2=3.3V, BUCK4=1.8V, LDO1=1.2V, LDO2=LDO3=3.3V <Default of master control mode>)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Li-ion Battery Charger (continued)						
Battery temperature threshold COLD	T_{BTMP_COLD}	-	2	-	°C	
Battery temperature measurement accuracy	T_{BAT}	-3	-	3	°C	
TS threshold disable voltage	V_{TS_DIS}	0.06	0.1	0.17	V	
Battery Open detection voltage	V_{TS_BATOPN}	1.25	1.39	1.53	V	Measure TS voltage
Coulomb counter						
Resolution	RES_{CC}	-	-	15	bit	Sign + 14-bits
Operating Clock Frequency	f_{CC}	-	32.768	-	kHz	Xtal
Integration Period	t_{CONVCC}	-	1	-	sec	
Analog Input Voltage Range	V_{AIN}	−30	-	30	mV	
Least Significant Bit	LSB	-	6.1	-	μV	
Current Measurement Range	I_{AIN}	−3.0	-	3.0	A	Sense resister 10mΩ
DC Offset	V_{DCO}	-0.5	-	+0.5	mV	
Linearity	LIN	-	±4	-	LSB	V_{AIN} range
12-bit SAR ADC						
Resolution	RES_{SAR}	-	-	12	bit	
Operating Clock Frequency	f_{SAR}	-	400	-	kHz	
Conversion Period	$t_{CONVSAR}$	-	40	-	μsec	16 clocks
Analog Input Voltage Range 1	V_{AIN1}	0.6	-	5.4	V	VBAT input
Analog Input Voltage Range 2	V_{AIN2}	0.2	-	1.3	V	TS input
Analog Input Voltage Range 3	V_{AIN3}	-30	-	30	mV	BATTP input
Differential Non-Linearity	DNL	-	±3	-	LSB	TS input
Integral Non-Linearity	INL	-	±6	-	LSB	TS input
RTC / Output Buffer (CLK32KOUT)						
Clock Frequency	f_{RTC}	-	32.768	-	kHz	With external crystal
Output Clock Frequency Drift	D_{RTCCLK}	−100	-	100	ppm	(Note1)
Oscillator Stabilization Time	t_{RTCSTB}	-	-	1000	msec	Within 3% of target frequency.
Oscillator Stop Detection	t_{STPDET}	-	-	150	μsec	
Supply Current	I_{RTC}	-	3	-	μA	C_L=20pF
Output Duty Cycle	$DUTY_{RTC}$	30	50	70	%	
Output L Level Voltage	V_{OL32K}	-	-	0.4	V	I_{OL} = 1mA
Output Off Leak current	I_{OFF32K}	-	-	1	μA	$V_{CLK32KOUT}$=5.5V,VIN=5.5V Open drain output OFF mode

(Note1) Frequency stability over temperature depends on the characteristics of the crystal unit which is expressed as a quadratic function.
Recommended crystal unit is FC-135(SEIKO EPSON).

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(Unless otherwise specified, Ta=+25°C, VIN=PVIN=4.0V, DVDD=1.8V, BUCK1=1.425V, BUCK2=1.2V, BUCK3=VINL1=VINL2=3.3V, BUCK4=1.8V, LDO1=1.2V, LDO2=LDO3=3.3V <Default of master control mode>)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
I2C Bus Interface						
I2C_CLK clock frequency	f_{SCL}	0	-	400	kHz	
Hold time START condition	$t_{HD;STA}$	160	-	-	nsec	
LOW period of I2C_CLK clock	t_{LOW}	160	-	-	nsec	
HIGH period of I2C_CLK clock	t_{HIGH}	60	-	-	nsec	
Set-up time for a repeated START condition	$t_{SU;STA}$	160	-	-	nsec	
Data hold time	$t_{HD;DAT}$	0	-	70	nsec	
Data set-up time	$t_{SU;DAT}$	10	-	-	nsec	
Set-up time for STOP condition	$t_{SU;STO}$	160	-	-	nsec	
Capacitive load for each bus line	C_b	-	-	100	pF	
Pulse width of spikes that are suppressed by the input filter *	t_{SP}	0	-	10	ns	
Bus Free Time	t_{BUFF}	1.3	-	-	us	

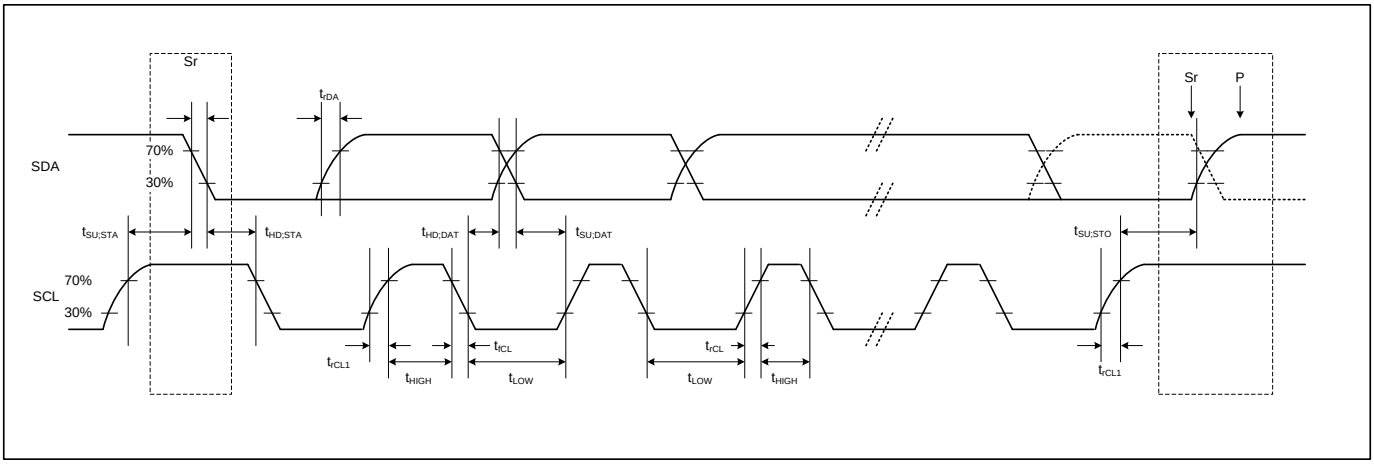

Figure 24. I2C AC Timing

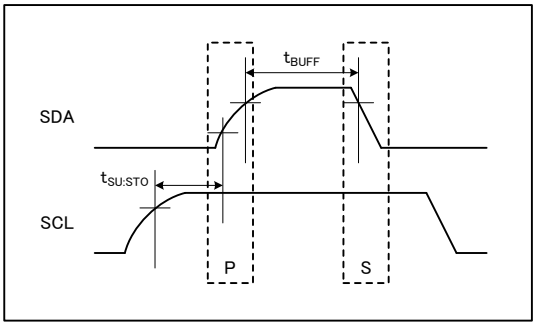

Figure 25. I2C AC Timing – Bus Free Time

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Register Map

ADRS.	Register Name	R/W	INIT MST	INIT SLV	D7	D6	D5	D4	D3	D2	D1	D0
00h	DEVICE	R, R/W	41h	41h	I2C_UNEMPTY	LSIVER [2:0]			DEVICEID[3:0]			
01h	PWRCTRL	R/W	00h	00h	-	STBY_INV	-	-	PWRON_DBNC[1:0]		-	RESTARTEN
02h	BUCK1_ON	R/W	19h	17h	-	-	BUCK1_ON[5:0]					
03h	BUCK1_STBY	R/W	19h	17h	-	-	BUCK1_STBY[5:0]					
04h	BUCK1_SLP	R/W	19h	17h	-	-	BUCK1_SLP[5:0]					
05h	BUCK1_MODE	R/W	06h	06h	-	-	BUCK1_OMODE	-	BUCK1_ONSTBYMODE[3:0]			
06h	BUCK1_CONF	R/W	00h	00h	-	-	-	-	-	-	BUCK1_RAMPRATE[1:0]	
07h	BUCK2_ON	R/W	10h	17h	-	-	BUCK2_ON[5:0]					
08h	BUCK2_STBY	R/W	10h	17h	-	-	BUCK2_STBY[5:0]					
09h	BUCK2_SLP	R/W	10h	17h	-	-	BUCK2_SLP[5:0]					
0Ah	BUCK2_MODE	R/W	06h	06h	-	-	BUCK2_OMODE	-	BUCK2_ONSTBYMODE[3:0]			
0Bh	BUCK2_CONF	R/W	00h	00h	-	-	-	-	-	-	BUCK2_RAMPRATE[1:0]	
0Ch	BUCK3_VOLT	R/W	0Eh	0Bh	-	-	-	-	BUCK3_ON[3:0]			
0Dh	BUCK3_MODE	R/W	06h	06h	-	-	BUCK3_OMODE	-	BUCK3_ONSTBYMODE[3:0]			
0Eh	BUCK4_VOLT	R/W	10h	04h	-	-	-	BUCK4_ON[4:0]				
0Fh	BUCK4_MODE	R/W	06h	06h	-	-	BUCK4_OMODE	-	BUCK4_ONSTBYMODE[3:0]			
10h	LDO1_CTRL	R/W	11h	0Fh	-	-	-	VOSNVS_SW_EN	DVREF_EN	LDO3_EN	LDO2_EN	LDO1_EN
11h	LDO2_CTRL	R/W	00h	00h	-	-	LDO3_LPWR	LDO3_STBY	LDO2_LPWR	LDO2_STBY	LDO1_LPWR	LDO1_STBY
12h	LDO1_VOLT	R/W	08h	22h	-	-	LDO1[5:0]					
13h	LDO2_VOLT	R/W	32h	14h	-	-	LDO2[5:0]					
14h	LDO3_VOLT	R/W	32h	08h	-	-	LDO3[5:0]					
15h	BUCK_PDEN	R/W	0Fh	0Fh	-	-	-	-	BUCK4_PDEN	BUCK3_PDEN	BUCK2_PDEN	BUCK1_PDEN
16h	LDO_PDEN	R/W	0Fh	0Fh	-	-	-	-	DVREF_PDEN	LDO3_PDEN	LDO2_PDEN	LDO1_PDEN
17h	GPO	R/W	07h	07h	-	GPO3_MODE	GPO2_MODE	GPO1_MODE	-	GPO3_OUT	GPO2_OUT	GPO1_OUT
18h	OUT32K	R/W	01h	01h	-	-	-	-	-	-	OUT32K_MODE	OUT32K_EN
19h	SEC	R/W	XXh	XXh	-	S40	S20	S10	S8	S4	S2	S1
1Ah	MIN	R/W	XXh	XXh	-	M40	M20	M10	M8	M4	M2	M1
1Bh	HOUR	R/W	XXh	XXh	12/24	-	H20/PA	H10	H8	H4	H2	H1
1Ch	WEEK	R/W	0Xh	0Xh	-	-	-	-	-	W4	W2	W1
1Dh	DAY	R/W	XXh	XXh	-	-	D20	D10	D8	D4	D2	D1
1Eh	MONTH	R/W	XXh	XXh	-	-	-	MO10	MO8	MO4	MO2	MO1
1Fh	YEAR	R/W	XXh	XXh	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
20h	ALM0_SEC	R/W	00h	00h	-	A0S40	A0S20	A0S10	A0S8	A0S4	A0S2	A0S1
21h	ALM0_MIN	R/W	00h	00h	-	A0M40	A0M20	A0M10	A0M8	A0M4	A0M2	A0M1
22h	ALM0_HOUR	R/W	00h	00h	A0_12/24	-	A0H20/PA	A0H10	A0H8	A0H4	A0H2	A0H1
23h	ALM0_WEEK	R/W	00h	00h	-	-	-	-	-	A0W4	A0W2	A0W1
24h	ALM0_DAY	R/W	00h	00h	-	-	A0D20	A0D10	A0D8	A0D4	A0D2	A0D1
25h	ALM0_MONTH	R/W	00h	00h	-	-	-	A0MO10	A0MO8	A0MO4	A0MO2	A0MO1
26h	ALM0_YEAR	R/W	00h	00h	A0Y80	A0Y40	A0Y20	A0Y10	A0Y8	A0Y4	A0Y2	A0Y1
27h	ALM1_SEC	R/W	00h	00h	-	A1S40	A1S20	A1S10	A1S8	A1S4	A1S2	A1S1
28h	ALM1_MIN	R/W	00h	00h	-	A1M40	A1M20	A1M10	A1M8	A1M4	A1M2	A1M1

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Register Map - continued

ADRS.	Register Name	R/W	INIT MST	INIT SLV	D7	D6	D5	D4	D3	D2	D1	D0
29h	ALM1_HOUR	R/W	00h	00h	A1_12/24	-	A1H20/PA	A1H10	A1H8	A1H4	A1H2	A1H1
2Ah	ALM1_WEEK	R/W	00h	00h	-	-	-	-	-	A1W4	A1W2	A1W1
2Bh	ALM1_DAY	R/W	00h	00h	-	-	A1D20	A1D10	A1D8	A1D4	A1D2	A1D1
2Ch	ALM1_MONTH	R/W	00h	00h	-	-	-	A1MO10	A1MO8	A1MO4	A1MO2	A1MO1
2Dh	ALM1_YEAR	R/W	00h	00h	A1Y80	A1Y40	A1Y20	A1Y10	A1Y8	A1Y4	A1Y2	A1Y1
2Eh	ALM0_MASK	R/W	00h	00h	A0_ONESEC	A0_YEAR	A0_MON	A0_DAY	A0_WEEK	A0_HOUR	A0_MIN	A0_SEC
2Fh	ALM1_MASK	R/W	00h	00h	A1_ONESEC	A1_YEAR	A1_MON	A1_DAY	A1_WEEK	A1_HOUR	A1_MIN	A1_SEC
30h	ALM2	R/W	00h	00h	-	-	-	-	-	-	ALM2[1:0]	
31h	TRIM	R/W	00h	00h	DEV	TRIM[6:0]						
32h	CONF	R/W	01h	01h	-	-	-	-	-	-	XSTB	PON
33h	SYS_INIT	R/W	00h	00h	-	-	-	-	-	-	CHGRST	-
34h	CHG_STATE	R	XXh	XXh	-	CHG_STATE[6:0]						
35h	CHG_LAST_STATE	R	XXh	XXh	-	CHG_LAST_STATE[6:0]						
36h	BAT_STAT	R	XXh	XXh	-	-	BAT_DET	BAT_DET_DONE	VBAT_OV	LOW_BAT	VBAT_SHORT	DBAT_DET
37h	DCIN_STAT	R	0Xh	0Xh	-	-	-	-	DCIN_OV	INHIBIT(Note1)	DCIN_CLPS	DCIN_DET
38h	VSYS_STAT	R	0Xh	0Xh	-	-	-	-	-	-	VSYS_LO	VSYS_UVN
39h	CHG_STAT	R	0Xh	0Xh	-	-	-	-	-	-	-	VRECHG_DET
3Ah	CHG_WDT_STAT	R	XXh	XXh	CHGWDTS[7:0]							
3Bh	BAT_TEMP	R	0Xh	0Xh	-	-	-	-	-	BAT_TEMP[2:0]		
3Eh	DCIN_CLPS	R/W	36h	36h	DCIN_CLPS[7:0]							
3Fh	VSYS_REG	R/W	09h	09h	-	-	-	INHIBIT(Note1)	VSYS_REG[3:0]			
40h	VSYS_MAX	R/W	23h	21h	-	VSYS_MAX[6:0]						
41h	VSYS_MIN	R/W	21h	1Fh	-	VSYS_MIN[6:0]						
42h	CHG_SET1	R/W	6Fh	6Fh	WDT_DIS	WDT_AUTO	AUTO_FST	FST_TRG	AUTO_RECHG	BTMP_EN	COLD_ERR_EN	CHG_EN
43h	CHG_SET2	R/W	90h	90h	VF_TREG_EN	-	REBATDET	BATDET_EN	-	-	TIM_CNT_SEL[1:0]	
44h	CHG_WDT_PRE	R/W	1Eh	1Eh	WDT_PRE[7:0]							
45h	CHG_WDT_FST	R/W	26h	26h	WDT_FST[7:0]							
46h	CHG_IPRE	R/W	52h	52h	ITRI[3:0]				IPRE[3:0]			
47h	CHG_IFST	R/W	04h	04h	-	-	-	IFST[4:0]				
48h	CHG_IFST_TERM	R/W	05h	05h	-	-	-	-	IFST_TERM[3:0]			
49h	CHG_VPRE	R/W	C9h	C9h	VPRE_HI[3:0]				VPRE_LO[3:0]			
4Ah	CHG_VBAT_1	R/W	18h	18h	-	-	-	VBAT_CHG1[4:0]				
4Bh	CHG_VBAT_2	R/W	13h	13h	-	-	-	VBAT_CHG2[4:0]				
4Ch	CHG_VBAT_3	R/W	10h	10h	-	-	-	VBAT_CHG3[4:0]				
4Dh	CHG_LED_1	R/W	03h	03h	-	-	-	-	-	TERR[2:0]		
4Eh	VF_TH	R/W	00h	00h	VF_TH[7:0]							
4Fh	BAT_SET_1	R/W	00h	00h	VBAT_HI[3:0]				VBAT_LO[3:0]			
50h	BAT_SET_2	R/W	30h	30h	VBAT_OVP[3:0]				-	VBAT_MNT[2:0]		
51h	BAT_SET_3	R/W	02h	02h	-	-	-	-	-	TIM_DBP[2:0]		

(Note1) Please always write "0" to the INHIBIT register when in use.

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Register Map - continued

ADRS.	Register Name	R/W	INIT MST	INIT SLV	D7	D6	D5	D4	D3	D2	D1	D0
52h	ALM_VBAT_TH_U	R/W	01h	01h	-	-	-	-	-	-	-	VBAT_TH[8]
53h	ALM_VBAT_TH_L	R/W	FFh	FFh	VBAT_TH[7:0]							
54h	ALM_DCIN_TH	R/W	0Fh	0Fh	DCIN_TH[7:0]							
55h	ALM_VSYS_TH	R/W	FFh	FFh	VSYS_TH[7:0]							
56h	VM_IBAT_U	R	00h	00h	-	-	-	-	IBAT[11:8]			
57h	VM_IBAT_L	R	00h	00h	IBAT[7:0]							
58h	VM_VBAT_U	R	00h	00h	-	-	-	VBAT[12:8]				
59h	VM_VBAT_L	R	00h	00h	VBAT[7:0]							
5Ah	VM_BTMP	R/W	00h	00h	BTMP[7:0]							
5Bh	VM_VTH	R/W	00h	00h	VTH[7:0]							
5Ch	VM_DCIN_U	R	00h	00h	-	-	-	-	DCIN[11:8]			
5Dh	VM_DCIN_L	R	00h	00h	DCIN[7:0]							
5Eh	VM_VSYS	R	00h	00h	VSYS[7:0]							
5Fh	VM_VF	R	00h	00h	VF[7:0]							
60h	VM_IBATLOAD_PRE_U	R	00h	00h	-	-	-	-	IBAT_BATLOAD_PRE[11:8]			
61h	VM_IBATLOAD_PRE_L	R	00h	00h	IBAT_BATLOAD_PRE[7:0]							
62h	VM_VBATLOAD_PRE_U	R	00h	00h	-	-	-	VBAT_BATLOAD_PRE[12:8]				
63h	VM_VBATLOAD_PRE_L	R	00h	00h	VBAT_BATLOAD_PRE[7:0]							
64h	VM_IBATLOAD_PST_U	R	00h	00h	-	-	-	-	IBAT_BATLOAD_PST[11:8]			
65h	VM_IBATLOAD_PST_L	R	00h	00h	IBAT_BATLOAD_PST[7:0]							
66h	VM_VBATLOAD_PST_U	R	00h	00h	-	-	-	VBAT_BATLOAD_PST[12:8]				
67h	VM_VBATLOAD_PST_L	R	00h	00h	VBAT_BATLOAD_PST[7:0]							
68h	VM_SMA_VBAT_U	R	00h	00h	-	-	-	VBAT_SMA[12:8]				
69h	VM_SMA_VBAT_L	R	00h	00h	VBAT_SMA[7:0]							
6Ah	VM_SMA_IBAT_U	R	00h	00h	-	-	-	-	IBAT_SMA[11:8]			
6Bh	VM_SMA_IBAT_L	R	00h	00h	IBAT_SMA[7:0]							
6Dh	CC_CTRL	R/W	40h	40h	CCNTRST	CCNTENB	CC_CALIB	-	-	-	-	-
6Eh	CC_BATCAP1_TH_U	R/W	00h	00h	-	-	-	-	CC_BATCAP1_TH[11:8]			
6Fh	CC_BATCAP1_TH_L	R/W	7Eh	7Eh	CC_BATCAP1_TH[7:0]							
70h	CC_BATCAP2_TH_U	R/W	00h	00h	-	-	-	-	CC_BATCAP2_TH[11:8]			
71h	CC_BATCAP2_TH_L	R/W	3Fh	3Fh	CC_BATCAP2_TH[7:0]							
72h	CC_BATCAP3_TH_U	R/W	00h	00h	-	-	-	-	CC_BATCAP3_TH[11:8]			
73h	CC_BATCAP3_TH_L	R/W	1Fh	1Fh	CC_BATCAP3_TH[7:0]							
74h	CC_STAT	R	00h	00h	-	-	-	-	-	CC_MON3	CC_MON2	CC_MON1
75h	CC_CCNTD_3	R/W	0Xh	00h	-	-	-	-	CCNTD[27:24]			
76h	CC_CCNTD_2	R/W	XXh	00h	CCNTD[23:16]							
77h	CC_CCNTD_1	R/W	XXh	00h	CCNTD[15:8]							
78h	CC_CCNTD_0	R/W	XXh	00h	CCNTD[7:0]							
79h	CC_CURCD_U	R	XXh	00h	CURDIR	-	CURCD[13:8]					
7Ah	CC_CURCD_L	R	XXh	00h	CURCD[7:0]							

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Register Map - continued

ADRS.	Register Name	R/W	INIT MST	INIT SLV	D7	D6	D5	D4	D3	D2	D1	D0
7Bh	VM_OCUR_THR_1	R/W	7Dh	7Dh	OCURTHR1[7:0]							
7Ch	VM_OCUR_DUR_1	R/W	64h	64h	OCURDUR1[7:0]							
7Dh	VM_OCUR_THR_2	R/W	5Eh	5Eh	OCURTHR2[7:0]							
7Eh	VM_OCUR_DUR_2	R/W	8Ch	8Ch	OCURDUR2[7:0]							
7Fh	VM_OCUR_THR_3	R/W	4Eh	4Eh	OCURTHR3[7:0]							
80h	VM_OCUR_DUR_3	R/W	A5h	A5h	OCURDUR3[7:0]							
81h	VM_OCUR_MON	R	0Xh	00h	-	-	-	-	-	OCUR3	OCUR2	OCUR1
82h	VM_BTMP_OV_THR	R/W	8Ch	8Ch	OVBTMPTHR[7:0]							
83h	VM_BTMP_OV_DUR	R/W	28h	28h	OVBTMPDUR[7:0]							
84h	VM_BTMP_LO_THR	R/W	C8h	C8h	LOBTMPTHR[7:0]							
85h	VM_BTMP_LO_DUR	R/W	28h	28h	LOBTMPDUR[7:0]							
86h	VM_BTMP_MON	R	0Xh	00h	-	-	-	-	-	-	OVBTMP	LOBTMP
88h	INT_EN_01	R/W	00h	00h	-	-	-	-	BUCK4FAULT	BUCK3FAULT	BUCK2FAULT	BUCK1FAULT
89h	INT_EN_02	R/W	00h	00h	-	-	DCIN_OV_DET	DCIN_OV_RES	DCIN_CLPS_IN	DCIN_CLPS_OUT	DCIN_RMV	-
8Ah	INT_EN_03	R/W	00h	00h	-	-	-	-	-	-	DCIN_MON_DET	DCIN_MON_RES
8Bh	INT_EN_04	R/W	08h	00h	VSYS_MON_DET	VSYS_MON_RES	-	-	VSYS_LO_DET	VSYS_LO_RES	VSYS_UV_DET	VSYS_UV_RES
8Ch	INT_EN_05	R/W	00h	00h	CHG_TRNS	TMP_TRNS	BAT_MNT_IN	BAT_MNT_OUT	CHG_WDT_EXP	EXTEMP_TOUT	-	-
8Dh	INT_EN_06	R/W	00h	00h	TH_DET	TH_RMV	BAT_DET	BAT_RMV	-	-	TMP_OUT_DET	TMP_OUT_RES
8Eh	INT_EN_07	R/W	00h	00h	VBAT_OV_DET	VBAT_OV_RES	VBAT_LO_DET	VBAT_LO_RES	VBAT_SHT_DET	VBAT_SHT_RES	DBAT_DET	-
8Fh	INT_EN_08	R/W	00h	00h	-	-	-	-	-	-	VBAT_MON_DET	VBAT_MON_RES
90h	INT_EN_09	R/W	00h	00h	-	-	-	-	-	CC8TH_DET	CC4TH_DET	CC2ND_DET
91h	INT_EN_10	R/W	00h	00h	-	-	OCUR3_DET	OCUR3_RES	OCUR2_DET	OCUR2_RES	OCUR1_DET	OCUR1_RES
92h	INT_EN_11	R/W	00h	00h	VF_DET	VF_RES	VF125_DET	VF125_RES	OVTMP_DET	OVTMP_RES	LOTMP_DET	LOTMP_RES
93h	INT_EN_12	R/W	00h	00h	-	-	-	-	-	ALM2	ALM1	ALM0
94h	INT_STAT	R	00h	00h	BUCK_AST	DCIN_AST	VSYS_AST	CHG_AST	BAT_AST	BMON_AST	TMP_AST	ALM_AST
95h	INT_STAT_01	R/WC	00h	00h	-	-	-	-	BUCK4FAULT	BUCK3FAULT	BUCK2FAULT	BUCK1FAULT
96h	INT_STAT_02	R/WC	00h	00h	-	-	DCIN_OV_DET	DCIN_OV_RES	DCIN_CLPS_IN	DCIN_CLPS_OUT	DCIN_RMV	-
97h	INT_STAT_03	R/WC	00h	00h	-	-	-	-	-	-	DCIN_MON_DET	DCIN_MON_RES
98h	INT_STAT_04	R/WC	00h	00h	VSYS_MON_DET	VSYS_MON_RES	-	-	VSYS_LO_DET	VSYS_LO_RES	VSYS_UVDET	VSYS_UV_RES
99h	INT_STAT_05	R/WC	00h	00h	CHG_TRNS	TMP_TRNS	BAT_MNT_IN	BAT_MNT_OUT	CHG_WDT_EXP	EXTEMP_TOUT	-	-
9Ah	INT_STAT_06	R/WC	00h	00h	TH_DET	TH_RMV	BAT_DET	BAT_RMV	-	-	TMP_OUT_DET	TMP_OUT_RES
9Bh	INT_STAT_07	R/WC	00h	00h	VBAT_OV_DET	VBAT_OV_RES	VBAT_LO_DET	VBAT_LO_RES	VBAT_SHT_DET	VBAT_SHT_RES	DBAT_DET	-
9Ch	INT_STAT_08	R/WC	00h	00h	-	-	-	-	-	-	VBAT_MON_DET	VBAT_MON_RES
9Dh	INT_STAT_09	R/WC	00h	00h	-	-	-	-	-	CC8TH_DET	CC4TH_DET	CC2ND_DET
9Eh	INT_STAT_10	R/WC	00h	00h	-	-	OCUR3_DET	OCUR3_RES	OCUR2_DET	OCUR2_RES	OCUR1_DET	OCUR1_RES
9Fh	INT_STAT_11	R/WC	00h	00h	VF_DET	VF_RES	VF125_DET	VF125_RES	OVTMP_DET	OVTMP_RES	LOTMP_DET	LOTMP_RES
A0h	INT_STAT_12	R/WC	00h	00h	-	-	-	-	-	ALM2	ALM1	ALM0
A1h	INT_UPDATE	R/WC	00h	00h	-	-	-	-	-	-	-	INT_UPDATE
A2h-FFh	-	-	00h	00h	-	-	-	-	-	-	-	-

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Address 00h: DEVICE Register (R,R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	DEVICE	R, R/W	I2C_UNEMPTY	LSIVER [2:0]			DEVICEID[3:0]			
	Initial Value (Master mode)	41h	0	1	0	0	0	0	0	1
	Initial Value (Slave mode)	41h	0	1	0	0	0	0	0	1

Bit 7 : I2C_UNEMPTY
0 : The buffer passed to RTC from I2C is empty.
1 : The buffer passed to RTC from I2C is not empty.

Bit 7-4 : LSIVER [3:0] LSI Version

Bit 3-0 : DEVICE ID[3:0] Device ID

Address 01h: PWRCTRL Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	PWRCTRL	R/W	-	STBY_INV	-	-	PWRON_DBNC[1:0]		-	RESTARTEN
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 6 : STBY_INV STANDBY pin polarity setting
0 : STANDBY pin HIGH active
1 : STANDBY pin LOW active

Bit 3-2 : PWRON_DBNC[1:0] PWRON hardware debounce time setting

PWRON_DBNC	Turn ON
00	0
01	31.25
10	125
11	750

Bit 0 : RESTARTEN Restart the IC
0 : Normal
1 : Restart the IC

Address 02h: BUCK1_ON Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	BUCK1_ON	R/W	-	-	BUCK1_ON[5:0]					
	Initial Value (Master mode)	19h	0	0	0	1	1	0	0	1
	Initial Value (Slave mode)	17h	0	0	0	1	0	1	1	1

Bit 5-0 : BUCK1_ON[5:0] Sets the BUCK1 output voltage during "ON" mode.
See Table 5 and Table 6 for all possible configurations.

Address 03h: BUCK1_STBY Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03h	BUCK1_STBY	R/W	-	-	BUCK1_STBY[5:0]					
	Initial Value (Master mode)	19h	0	0	0	1	1	0	0	1
	Initial Value (Slave mode)	17h	0	0	0	1	0	1	1	1

Bit 5-0 : BUCK1_STBY[5:0] Sets the BUCK1 output voltage during "STANDBY" mode.
See Table 5 and Table 6 for all possible configurations.

Address 04h: BUCK1_SLP Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04h	BUCK1_SLP	R/W	-	-	BUCK1_SLP[5:0]					
	Initial Value (Master mode)	19h	0	0	0	1	1	0	0	1
	Initial Value (Slave mode)	17h	0	0	0	1	0	1	1	1

Bit 5-0 : BUCK1_SLP[5:0] Sets the BUCK1 output voltage during "SLEEP" mode.
See Table 5 and Table 6 for all possible configurations.

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Address 05h: BUCK1_MODE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
05h	BUCK1_MODE	R/W	-	-	BUCK1_OMODE	-	BUCK1_ONSTBYMODE[3:0]			
	Initial Value (Master mode)	06h	0	0	0	0	0	1	1	0
	Initial Value (Slave mode)	06h	0	0	0	0	0	1	1	0

Bit 5 : BUCK1_OMODE BUCK1 Operational Mode control when "PWRON = H → L" (Slave Mode Only)
0 : OFF
1 : SLEEP Mode

Bit 3-0 : BUCK1_ONSTBYMODE[3:0] BUCK1 Operational Mode control when in "ON, STANDBY" mode

BUCK1 ONSTBYMODE[3:0]	ON Mode	STANDBY Mode
0000	OFF	OFF
0001	PWM	OFF
0010	Reserved	Reserved
0011	PFM	OFF
0100	PFM/PWM Auto	OFF
0101	PWM	PWM
0110	PWM	PFM/PWM Auto
0111	Reserved	Reserved
1000	PFM/PWM Auto	PFM/PWM Auto
1001	Reserved	Reserved
1010	Reserved	Reserved
1011	Reserved	Reserved
1100	PFM/PWM Auto	PFM
1101	PWM	PFM
1110	Reserved	Reserved
1111	Reserved	Reserved

BUCK Mode Control Description

Mode	Description
OFF	BUCK is switched off and the output voltage is discharged.
PFM	BUCK is always in PFM mode, which is useful at light loads for optimized efficiency.
PWM	BUCK is always in PWM mode operation regardless of load conditions.
PWM/PWM Auto	BUCK moves automatically between PFM mode and PWM mode depending on load conditions.

Address 06h: BUCK1_CONF Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h	BUCK1_CONF	R/W	-	-	-	-	-	-	BUCK1_RAMPRATE[1:0]	
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 1-0 : BUCK1_RAMPRATE[1:0] BUCK1 DVS ramp rate setting
00 : 10.0mV/usec
01 : 5.0mV/usec
10 : 2.5mV/usec
11 : 1.25mV/usec

Address 07h: BUCK2_ON Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
07h	BUCK2_ON	R/W	-	-	BUCK2_ON[5:0]					
	Initial Value (Master mode)	10h	0	0	0	1	0	0	0	0
	Initial Value (Slave mode)	17h	0	0	0	1	0	1	1	1

Bit 5-0 : BUCK2_ON[5:0] Sets the BUCK2 output voltage during "ON" mode.
See Table 5 and Table 6 for all possible configurations.

Address 08h: BUCK2_STBY Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08h	BUCK2_STBY	R/W	-	-	BUCK2_STBY[5:0]					
	Initial Value (Master mode)	10h	0	0	0	1	0	0	0	0
	Initial Value (Slave mode)	17h	0	0	0	1	0	1	1	1

Bit 5-0 : BUCK2_STBY[5:0] Sets the BUCK2 output voltage during "STANDBY" mode.
See Table 5 and Table 6 for all possible configurations.

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Address 09h: BUCK2_SLP Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
09h	BUCK2_SLP	R/W	-	-	BUCK2_SLP[5:0]					
	Initial Value (Master mode)	10h	0	0	0	1	0	0	0	0
	Initial Value (Slave mode)	17h	0	0	0	1	0	1	1	1

Bit 5-0 : BUCK2_SLP[5:0] Sets the BUCK2 output voltage during "SLEEP" mode.
See Table 5 and Table 6 for all possible configurations.

Address 0Ah: BUCK2_MODE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ah	BUCK2_MODE	R/W	-	-	BUCK2_OMODE	-	BUCK2_ONSTBYMODE[3:0]			
	Initial Value (Master mode)	06h	0	0	0	0	0	1	1	0
	Initial Value (Slave mode)	06h	0	0	0	0	0	1	1	0

Bit 5 : BUCK2_OMODE BUCK2 Operational Mode control when "PWRON = H → L"(Slave Mode Only)
0 : OFF Mode
1 : SLEEP Mode

Bit 3-0 : BUCK2_ONSTBYMODE[3:0] BUCK2 Operational Mode control when in "ON, STANDBY" mode

BUCK2 ONSTBYMODE[3:0]	ON Mode	STANDBY Mode
0000	OFF	OFF
0001	PWM	OFF
0010	Reserved	Reserved
0011	PFM	OFF
0100	PFM/PWM Auto	OFF
0101	PWM	PWM
0110	PWM	PFM/PWM Auto
0111	Reserved	Reserved
1000	PFM/PWM Auto	PFM/PWM Auto
1001	Reserved	Reserved
1010	Reserved	Reserved
1011	Reserved	Reserved
1100	PFM/PWM Auto	PFM
1101	PWM	PFM
1110	Reserved	Reserved
1111	Reserved	Reserved

Address 0Bh: BUCK2_CONF Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Bh	BUCK2_CONF	R/W	-	-	-	-	-	-	BUCK2_RAMPRATE[1:0]	
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 1-0 : BUCK2_RAMPRATE[1:0] BUCK2 DVS ramp rate setting
00 : 10.0mV/usec
01 : 5.0mV/usec
10 : 2.5mV/usec
11 : 1.25mV/usec

Address 0Ch: BUCK3_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	BUCK3_VOLT	R/W	-	-	-	-	BUCK3_ON[3:0]			
	Initial Value (Master mode)	0Eh	0	0	0	0	1	1	1	0
	Initial Value (Slave mode)	0Bh	0	0	0	0	1	0	1	1

Bit 3-0 : BUCK3_ON[3:0] Sets the BUCK3 output voltage during "ON, STNDBY, SLEEP" mode.
See Table 5 and Table 6 for all possible configurations.

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Address 0Dh: BUCK3_MODE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Dh	BUCK3_MODE	R/W	-	-	BUCK3_OMODE	-	BUCK3_ONSTBYMODE[3:0]			
	Initial Value (Master mode)	06h	0	0	0	0	0	1	1	0
	Initial Value (Slave mode)	06h	0	0	0	0	0	1	1	0

Bit 5 : BUCK3_OMODE BUCK3 Operational Mode control when "PWRON = H → L"(Slave Mode Only)
0 : OFF Mode
1 : SLEEP Mode

Bit 3-0 : BUCK3_ONSTBYMODE[3:0] BUCK3 Operational Mode control when in "ON, STANDBY" mode

BUCK3 ONSTBYMODE[3:0]	ON Mode	STANDBY Mode
0000	OFF	OFF
0001	PWM	OFF
0010	Reserved	Reserved
0011	PFM	OFF
0100	PFM/PWM Auto	OFF
0101	PWM	PWM
0110	PWM	PFM/PWM Auto
0111	Reserved	Reserved
1000	PFM/PWM Auto	PFM/PWM Auto
1001	Reserved	Reserved
1010	Reserved	Reserved
1011	Reserved	Reserved
1100	PFM/PWM Auto	PFM
1101	PWM	PFM
1110	Reserved	Reserved
1111	Reserved	Reserved

Address 0Eh: BUCK4_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Eh	BUCK4_VOLT	R/W	-	-	-	BUCK4_ON[4:0]				
	Initial Value (Master mode)	10h	0	0	0	1	0	0	0	0
	Initial Value (Slave mode)	04h	0	0	0	0	0	1	0	0

Bit 4-0 : BUCK4_ON[4:0] Sets the BUCK4 output voltage during "ON, STNDBY, SLEEP" mode.
See Table 5 and Table 6 for all possible configurations.

Address 0Fh: BUCK4_MODE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Fh	BUCK4_MODE	R/W	-	-	BUCK4_OMODE	-	BUCK4_ONSTBYMODE[3:0]			
	Initial Value (Master mode)	06h	0	0	0	0	0	1	1	0
	Initial Value (Slave mode)	06h	0	0	0	0	0	1	1	0

Bit 5 : BUCK4_OMODE BUCK4 Operational Mode control when "PWRON = H → L"(Slave Mode Only)
0 : OFF Mode
1 : SLEEP Mode

Bit 3-0 : BUCK4_ONSTBYMODE[3:0] BUCK4 Operational Mode control when in "ON, STANDBY" mode

BUCK4 ONSTBYMODE[3:0]	ON Mode	STANDBY Mode
0000	OFF	OFF
0001	PWM	OFF
0010	Reserved	Reserved
0011	PFM	OFF
0100	PFM/PWM Auto	OFF
0101	PWM	PWM
0110	PWM	PFM/PWM Auto
0111	Reserved	Reserved
1000	PFM/PWM Auto	PFM/PWM Auto
1001	Reserved	Reserved
1010	Reserved	Reserved
1011	Reserved	Reserved
1100	PFM/PWM Auto	PFM
1101	PWM	PFM
1110	Reserved	Reserved
1111	Reserved	Reserved

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Address 10h: LDO1_CTRL Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	LDO1_CTRL	R/W	-	-	-	VOSNVS_SW_EN	DVREF_EN	LDO3_EN	LDO2_EN	LDO1_EN
	Initial Value (Master mode)	11h	0	0	0	1	0	0	0	1
	Initial Value (Slave mode)	0Fh	0	0	0	0	1	1	1	1

Bit 4 : VOSNVS_SW_EN SNVSEN VOSNVS Power ON/OFF control 0 : OFF / 1 : ON

Bit 3 : DVREF_EN DVREFEN DDRVREF Power ON/OFF control 0 : OFF / 1 : ON

Bit 2 : LDO3_EN LDO3EN LDO3 Power ON/OFF control 0 : OFF / 1 : ON

Bit 1 : LDO2_EN LDO2EN LDO2 Power ON/OFF control 0 : OFF / 1 : ON

Bit 0 : LDO1_EN LDO1EN LDO1 Power ON/OFF control 0 : OFF / 1 : ON

Address 11h: LDO2_CTRL Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
11h	LDO2_CTRL	R/W	-	-	LDO3_LPWR	LDO3_STBY	LDO2_LPWR	LDO2_STBY	LDO1_LPWR	LDO1_STBY
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 5 : LDO3_LPWR Enable Low Power Mode for LDO3
See LDO Control table.

Bit 4 : LDO3_STBY Set LDO3 output state when in Standby.
See LDO Control table.

Bit 3 : LDO2_LPWR Enable Low Power Mode for LDO2
See LDO Control table.

Bit 2 : LDO2_STBY Set LDO2 output state when in Standby.
See LDO Control table.

Bit 1 : LDO1_LPWR Enable Low Power Mode for LDO1
See LDO Control table.

Bit 0 : LDO1_STBY Set LDO1 output state when in Standby.
See LDO Control table.

LDO Control

LDOx_EN	LDOx_LPWR	LDOx_STBY	STANDBY	VOx Output
0	X	X	X	OFF
1	0	0	X	ON
1	1	0	X	Low Power
1	X	1	0	ON
1	0	1	1	OFF
1	1	1	1	Low Power

Address 12h: LDO1_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
12h	LDO1_VOLT	R/W	-	-	LDO1[5:0]					
	Initial Value (Master mode)	08h	0	0	0	0	1	0	0	0
	Initial Value (Slave mode)	22h	0	0	1	0	0	0	1	0

Bit 5-0 : LDO1[5:0] Sets the LDO1 output voltage.
See Table 5 and Table 6 for all possible configurations.

Address 13h: LDO2_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
13h	LDO2_VOLT	R/W	-	-	LDO2[5:0]					
	Initial Value (Master mode)	32h	0	0	1	1	0	0	1	0
	Initial Value (Slave mode)	14h	0	0	0	1	0	1	0	0

Bit 5-0 : LDO2[5:0] Sets the LDO2 output voltage.
See Table 5 and Table 6 for all possible configurations.

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Address 14h: LDO3_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
14h	LDO3_VOLT	R/W	-	-	LDO3[5:0]					
	Initial Value (Master mode)	32h	0	0	1	1	0	0	1	0
	Initial Value (Slave mode)	08h	0	0	0	0	1	0	0	0

Bit 5-0 : LDO3[5:0] Sets the LDO3 output voltage.
See Table 5 and Table 6 for all possible configurations.

Address 15h: BUCK_PDEN Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
15h	BUCK_PDEN	R/W	-	-	-	-	BUCK4_PDEN	BUCK3_PDEN	BUCK2_PDEN	BUCK1_PDEN
	Initial Value (Master mode)	0Fh	0	0	0	0	1	1	1	1
	Initial Value (Slave mode)	0Fh	0	0	0	0	1	1	1	1

Bit 3 : BUCK4_PDEN BUCK4 Power-down Discharge control 0 : Power-down Discharge disabled / 1 : Power-down Discharge enabled

Bit 2 : BUCK3_PDEN BUCK3 Power-down Discharge control 0 : Power-down Discharge disabled / 1 : Power-down Discharge enabled

Bit 1 : BUCK2_PDEN BUCK2 Power-down Discharge control 0 : Power-down Discharge disabled / 1 : Power-down Discharge enabled

Bit 0 : BUCK1_PDEN BUCK1 Power-down Discharge control 0 : Power-down Discharge disabled / 1 : Power-down Discharge enabled

Address 16h: LDO_PDEN Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
16h	LDO_PDEN	R/W	-	-	-	-	DVREF_PDEN	LDO3_PDEN	LDO2_PDEN	LDO1_PDEN
	Initial Value (Master mode)	0Fh	0	0	0	0	1	1	1	1
	Initial Value (Slave mode)	0Fh	0	0	0	0	1	1	1	1

Bit 3 : DVREF_PDEN DVREF Power-down Discharge control 0 : Power-down Discharge disabled / 1 : Power-down Discharge enabled

Bit 2 : LDO3_PDEN LDO3 Power-down Discharge control 0 : Power-down Discharge disabled / 1 : Power-down Discharge enabled

Bit 1 : LDO2_PDEN LDO2 Power-down Discharge control 0 : Power-down Discharge disabled / 1 : Power-down Discharge enabled

Bit 0 : LDO1_PDEN LDO1 Power-down Discharge control 0 : Power-down Discharge disabled / 1 : Power-down Discharge enabled

Address 17h: GPO Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
17h	GPO	R/W	-	GPO3_MODE	GPO2_MODE	GPO1_MODE	-	GPO3_OUT	GPO2_OUT	GPO1_OUT
	Initial Value (Master mode)	07h	0	0	0	0	0	1	1	1
	Initial Value (Slave mode)	07h	0	0	0	0	0	1	1	1

Bit 6 : GPO3_MODE GPO3 Output mode setting
0 : Open drain output mode
1 : CMOS output mode

Bit 5 : GPO2_MODE GPO2 Output mode setting
0 : Open drain output mode
1 : CMOS output mode

Bit 4 : GPO1_MODE GPO1 Output mode setting
0 : Open drain output mode
1 : CMOS output mode

Bit 2 : GPO3_OUT GPO3 Output setting at GPO3_MODE=0 (Open drain output mode)
0 : Low
1 : Hiz [Open drain output mode] / High [CMOS output mode]

Bit 1 : GPO2_OUT GPO2 Output setting at GPO2_MODE=0 (Open drain output mode)
0 : Low
1 : Hiz [Open drain output mode] / High [CMOS output mode]

Bit 0 : GPO1_OUT GPO1 Output setting at GPO1_MODE=0 (Open drain output mode)
0 : Low
1 : Hiz [Open drain output mode] / High [CMOS output mode]

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Address 18h: OUT32K Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
18h	OUT32K	R/W	-	-	-	-	-	-	OUT32K_MODE	OUT32K_EN
	Initial Value (Master mode)	01h	0	0	0	0	0	0	0	1
	Initial Value (Slave mode)	01h	0	0	0	0	0	0	0	1

Bit 1 : OUT32K_MODE — CLK32KOUT output mode setting
0 : Open drain output mode
1 : CMOS output mode

Bit 0 : OUT32K_EN — CLK32KOUT clock output enable
0 : Disable [Hiz]
1 : Enable

Address 19h: SEC Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19h	SEC	R/W	-	S40	S20	S10	S8	S4	S2	S1
	Initial Value (Master mode)	XXh	0	x	x	x	x	x	x	x
	Initial Value (Slave mode)	XXh	0	x	x	x	x	x	x	x

Bit 6-0 : S1 to S40 — Second Counter
The second digits range from 00 to 59 and are carried to the minute digit in transition from 59 to 00.
(configured in BCD（Bianary-Coded Decimal))
Any writing to the second counter resets divider units of less than 1 second.

Address 1Ah: MIN Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Ah	MIN	R/W	-	M40	M20	M10	M8	M4	M2	M1
	Initial Value (Master mode)	XXh	0	x	x	x	x	x	x	x
	Initial Value (Slave mode)	XXh	0	x	x	x	x	x	x	x

Bit 6-0 : M1 to M40 — Minute Counter
The minute digits range from 00 to 59 and are carried to the hour digits in transition from 59 to 00.
(configured in BCD（Bianary-Coded Decimal))

Address 1Bh: HOUR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Bh	HOUR	R/W	12/24	-	H20/PA	H10	H8	H4	H2	H1
	Initial Value (Master mode)	XXh	0	0	x	x	x	x	x	x
	Initial Value (Slave mode)	XXh	0	0	x	x	x	x	x	x

Bit 7 : 12/24 — 12hour clock or 24hour clock select bit.
0 : 12hour clock.
1 : 24hour clock.

Bit 5-0 : H20 to H1 — Hour Counter
The hour digits range as shown this table and are carried to the day-of-month and day-of-week digits in transition from PM11 to AM12 or from 23 to 00.(configured in BCD（Bianary-Coded Decimal))

24 hour clock	12 hour clock	24 hour clock	12 hour clock
0	12(AM0)	12	32(PM0)
1	01(AM1)	13	21(PM1)
2	02(AM2)	14	22(PM2)
3	03(AM3)	15	23(PM3)
4	04(AM4)	16	24(PM4)
5	05(AM5)	17	25(PM5)
6	06(AM6)	18	26(PM6)
7	07(AM7)	19	27(PM7)
8	08(AM8)	20	28(PM8)
9	09(AM9)	21	29(PM9)
10	10(AM10)	22	30(PM10)
11	11(AM11)	23	31(PM11)

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Address 1Ch: WEEK Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Ch	WEEK	R/W	-	-	-	-	-	W4	W2	W1
	Initial Value (Master mode)	0Xh	0	0	0	0	0	x	x	x
	Initial Value (Slave mode)	0Xh	0	0	0	0	0	x	x	x

Bit 2-0 : W4 to W1

Day-of-week Counter
The day-of-week counter is incremented by 1 when the day-of-week digits are carried to the day-of-month digits.
(configured in BCD（Bianary-Coded Decimal))
Correspondences between days of the week and the day-of-week digit are user-definable. (Ex. Sunday = 0, 0, 0)
The writing of (1, 1, 1) to (W4, W2, W1) is prohibited except when days of the week are unused.

Address 1Dh: DAY Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Dh	DAY	R/W	-	-	D20	D10	D8	D4	D2	D1
	Initial Value (Master mode)	XXh	0	0	x	x	x	x	x	x
	Initial Value (Slave mode)	XXh	0	0	x	x	x	x	x	x

Bit 5-0 : D20 to D1

Day-of-month Counter
The day-of-month digits (D20 to D1) range from 1 to 31 for January, March, May, July, August, October, and December,
from 1 to 30 for April, June, September, and November, from 1 to 29 for February in leap years, from 1 to 28 for February in ordinary years.
The day-of-month digits are carried to the month digits in reversion from the last day of the month to 1.
(configured in BCD（Bianary-Coded Decimal))

Address 1Eh: MONTH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Eh	MONTH	R/W	-	-	-	MO10	MO8	MO4	MO2	MO1
	Initial Value (Master mode)	XXh	0	0	0	x	x	x	x	x
	Initial Value (Slave mode)	XXh	0	0	0	x	x	x	x	x

Bit 4-0 : MO10 to MO1

Month Counter
The month digits (MO10 to MO1) range from 1 to 12 and are carried to the year digits in reversion from 12 to 1.
(configured in BCD（Bianary-Coded Decimal))

Address 1Fh: YEAR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Fh	YEAR	R/W	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	Initial Value (Master mode)	XXh	x	x	x	x	x	x	x	x
	Initial Value (Slave mode)	XXh	x	x	x	x	x	x	x	x

Bit 7-0 : Y80 to Y1

Year Counter
The year digits (Y80 to Y1) range from 00 to 99 and are carried to the 19/20 digits in reversion from 99 to 00.
00, 04, 08, ..., 92 and 96 in leap years.(configured in BCD（Bianary-Coded Decimal))

Address 20h: ALM0_SEC Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h	ALM0_SEC	R/W	-	A0S40	A0S20	A0S10	A0S8	A0S4	A0S2	A0S1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 6-0 : A0S40 to A0S1

Alarm0 Second threshold value.(configured in BCD（Bianary-Coded Decimal))

Address 21h: ALM0_MIN Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
21h	ALM0_MIN	R/W	-	A0M40	A0M20	A0M10	A0M8	A0M4	A0M2	A0M1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 6-0 : A0M40 to A0M1

Alarm0 Minute threshold value.(configured in BCD（Bianary-Coded Decimal))

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Address 22h: ALM0_HOUR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
22h	ALM0_HOUR	R/W	A0_12/24	-	A0H20/PA	A0H10	A0H8	A0H4	A0H2	A0H1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 : A0_1224 12hour clock / 24hour clock select bit.

Bit 5-0 : A0H20/PA, A0H40 to A0H1 Alarm0 Hour threshold value.(configured in BCD（Bianary-Coded Decimal))

Address 23h: ALM0_WEEK Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
23h	ALM0_WEEK	R/W	-	-	-	-	-	A0W4	A0W2	A0W1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 2-0 : A0W4 to A0W1 Alarm0 day of the Week threshold value.(configured in BCD（Bianary-Coded Decimal))

Address 24h: ALM0_DAY Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
24h	ALM0_DAY	R/W	-	-	A0D20	A0D10	A0D8	A0D4	A0D2	A0D1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 5-0 : A0D20 to A0D1 Alarm0 Day threshold value.(configured in BCD（Bianary-Coded Decimal))

Address 25h: ALM0_MONTH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
25h	ALM0_MONTH	R/W	-	-	-	A0MO10	A0MO8	A0MO4	A0MO2	A0MO1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 4-0 : A0MO10 to A0MO1 Alarm0 Month threshold value.(configured in BCD（Bianary-Coded Decimal))

Address 26h: ALM0_YEAR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
26h	ALM0_YEAR	R/W	A0Y80	A0Y40	A0Y20	A0Y10	A0Y8	A0Y4	A0Y2	A0Y1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7-0 : A0Y80 to A0Y1 Alarm0 Year threshold value

Address 27h: ALM1_SEC Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
27h	ALM1_SEC	R/W	-	A1S40	A1S20	A1S10	A1S8	A1S4	A1S2	A1S1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 6-0 : A1S40 to A1S1 Alarm1 Second threshold value.(configured in BCD（Bianary-Coded Decimal))

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Address 28h: ALM1_MIN Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
28h	ALM1_MIN	R/W	-	A1M40	A1M20	A1M10	A1M8	A1M4	A1M2	A1M1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 6-0 : A1M80 to A1M1 Alarm1 Minute threshold value.(configured in BCD（Bianary-Coded Decimal))

Address 29h: ALM1_HOUR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
29h	ALM1_HOUR	R/W	A1_12/24	-	A1H20/PA	A1H10	A1H8	A1H4	A1H2	A1H1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 : A1_12/24 12hour clock / 24hour clock select bit.

Bit 5-0 : A1H20/PA, A1H10 to A1H1 Alarm1 Hour threshold value.(configured in BCD（Bianary-Coded Decimal))

Address 2Ah: ALM1_WEEK Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ah	ALM1_WEEK	R/W	-	-	-	-	-	A1W4	A1W2	A1W1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 2-0 : A1W4 to A1W1 Alarm1 day of the Week threshold value.(configured in BCD（Bianary-Coded Decimal))

Address 2Bh: ALM1_DAY Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Bh	ALM1_DAY	R/W	-	-	A1D20	A1D10	A1D8	A1D4	A1D2	A1D1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 5-0 : A1D20 to A1D1 Alarm1 Day threshold value.(configured in BCD（Bianary-Coded Decimal))

Address 2Ch: ALM1_MONTH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ch	ALM1_MONTH	R/W	-	-	-	A1MO10	A1MO8	A1MO4	A1MO2	A1MO1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 4-0 : A1MO10 to A1MO1 Alarm1 Month threshold value.(configured in BCD（Bianary-Coded Decimal))

Address 2Dh: ALM1_YEAR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Dh	ALM1_YEAR	R/W	A1Y80	A1Y40	A1Y20	A1Y10	A1Y8	A1Y4	A1Y2	A1Y1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7-0 : A1Y80 to A1Y1 Alarm1 Year threshold value.(configured in BCD（Bianary-Coded Decimal))

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Address 2Eh: ALM0_MASK Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Eh	ALM0_MASK	R/W	A0_ONESEC	A0_YEAR	A0_MON	A0_DAY	A0_WEEK	A0_HOUR	A0_MIN	A0_SEC
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 : A0_ONESEC — Alarm0 interrupt occur once every second. (Synchronized with second counter increment)
0 : Disable
1 : Enable — Regardless of any other setting in the ALM0_MASK register and the contents of the respective ALM0_SEC to ALM0_YEAR registers.

Bit 6-0 : A0_YEAR to A0_SEC — Alarm0 interrupt threshold mask bit.
0 : Mask
1 : Non-Mask

Address 2Fh: ALM1_MASK Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Fh	ALM1_MASK	R/W	A1_ONESEC	A1_YEAR	A1_MON	A1_DAY	A1_WEEK	A1_HOUR	A1_MIN	A1_SEC
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 : A1_ONESEC — Alarm1 interrupt occur once every second. (Synchronized with second counter increment)
0 : Disable
1 : Enable — Regardless of any other setting in the ALM1_MASK register and the contents of the respective ALM1_SEC to ALM1_YEAR registers.

Bit 6-0 : A1_YEAR to A1_SEC — Alarm1 interrupt threshold mask bit.
0 : Mask
1 : Non-Mask

Address 30h: ALM2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
30h	ALM2	R/W	-	-	-	-	-	-	ALM2[1:0]	
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 1-0 : ALM2[1:0] — Invalidate alarm2 when change the value of clock and calendar.
00 : OFF (Initial State)
01 : Once per 1 second (Synchronized with second counter increment)
10 : Once per minute (at 00 seconds of every minute)
11 : Once per hour (at 00 minutes, and 00 seconds of every hour)

Address 31h: TRIM Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
31h	TRIM	R/W	DEV	TRIM[6:0]						
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 : DEV
0 : The Oscillation Adjustment Circuit operates 00, 30 seconds.
1 : The Oscillation Adjustment Circuit operates 00 seconds.

Bit 6-0 : TRIM[6:0] — The Oscillation Adjustment Circuit is configured to change time counts of 1 second on the basis of the settings of the Oscillation Adjustment at the timing set by DEV.
The Oscillation Adjustment Circuit will not operate with the same timing (00, or 30 seconds) as the timing of writing to the Oscillation Adjusti
TRIM[6] : bit setting of '0' causes an increment (TRIM[5:0]-1) x 2 of time counts by.
TRIM[6] : bit setting of '1' causes a decrement (TRIM[5:0]+1) x 2 of time counts by.
TRIM[6:0] : bit setting of "x00000x" causes neither an increment nor decrement of time counts.

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Address 32h: CONF Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
32h	CONF	R/W	-	-	-	-	-	-	XSTB	PON
	Initial Value (Master mode)	01h	0	0	0	0	0	0	0	1
	Initial Value (Slave mode)	01h	0	0	0	0	0	0	0	1

Bit 1 : XSTB Oscillation Halt Sensing Monitor Bit.
0 : Sensing a halt of oscillation
1 : Sensing a normal condition of oscillation.
The XSTB accepts the reading and writing of "0" and "1". The XSTB bit will be set to "0" when the oscillation halt sensing. The XSTB bit will hold "0" even after the restart of oscillation.

Bit 0 : PON Power-on-reset Flag.
0 : Normal condition
1 : Detecting power-on-reset The PON bit will be set to "1" when supply voltage above the SNVS UVLO setting.
The PON bit will hold the setting of "1" even after power-on. The PON bit accepts only the writing of "0".
When PON bit set to "0", SNVS UVLO behave intermittent monitoring mode.

Address 33h: SYS_INIT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
33h	SYS_INIT	R/W	-	-	-	-	-	-	CHGRST	-
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 1(W) : CHGRST
0 : Releases reset operation
1 : Resets Battery Charger Block The related control registers are not initialized.

Address 34h: CHG_STATE Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
34h	CHG_STATE	R	-	CHG_STATE[6:0]						
	Initial Value (Master mode)	XXh	0	x	x	x	x	x	x	x
	Initial Value (Slave mode)	XXh	0	x	x	x	x	x	x	x

Bit 6-0 : CHG_STATE[6:0] The current state of the battery charger.
Table shows the details of the register values.

Address 35h: CHG_LAST_STATE Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
35h	CHG_LAST_STATE	R	-	CHG_LAST_STATE[6:0]						
	Initial Value (Master mode)	XXh	0	x	x	x	x	x	x	x
	Initial Value (Slave mode)	XXh	0	x	x	x	x	x	x	x

Bit 6-0 : CHG_LAST_STATE[6:0] The previous state of the battery charger.
Table shows the details of the register values.

CHG_STATE	State	Description
00h	SUSPEND	Suspend charging
01h	TRICKLE CHARGE	Trickle charging (Pre-conditioning)
02h	PRE CHARGE	Pre-charging
03h	FAST CHARGE	Fast Charging
0Dh	BATDET	Battery detection
0Eh	TOP OFF	Reached to Termination Current
0Fh	DONE	Charging finished
10h	Temp Err 1	Out of standard temperature while PRE CHARGE State
11h	Temp Err 2	Out of standard temperature while FAST CHARGE or TOPOFF State
12h	Temp Err 3	Out of standard temperature while DONE State
13h	Temp Err 4	Out of standard temperature while SUSPEND State
14h	Temp Err 5	Out of standard temperature while PRE CHARGE State
20h	TSD 1	Thermal Shut Down while PRE CHARGE State (> Tjmax)
21h	TSD 2	Thermal Shut Down while FAST CHARGE State (> Tjmax)
22h	TSD 3	Thermal Shut Down while TOP OFF State (> Tjmax)
23h	TSD 4	Thermal Shut Down while DONE State (> Tjmax)
24h	TSD 5	Thermal Shut Down while TRICKLE CHARGE State (> Tjmax)
30h	BATT ASSIST 1	VSYS < VBAT while FAST CHARGE State
31h	BATT ASSIST 2	VSYS < VBAT while TOP OFF State
32h	BATT ASSIST 3	VSYS < VBAT after TOP OFF State (DONE)
7Fh	Batt Error	Battery Error
others	(reserved)	-

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Address 36h: BAT_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
36h	BAT_STAT	R	-	-	BAT_DET	BAT_DET_DONE	VBAT_OV	LOW_BAT	VBAT_SHORT	DBAT_DET
	Initial Value (Master mode)	XXh	0	0	x	x	x	x	x	x
	Initial Value (Slave mode)	XXh	0	0	x	x	x	x	x	x

Bit 5 : BAT_DET Battery detection result
0 : Battery removed or no battery detected
1 : Battery presence

Bit 4 : BAT_DET_DONE Battery detection status
0 : Detection running
1 : Detection finished

Bit 3 : VBAT_OV VBAT over-voltage Status
0 : VBAT < VBAT_OVP - 150mV (Hysteresis)
1 : VBAT > VBAT_OVP
For example, VBAT_OV might be detected when the battery is removed while Fast charging.

Bit 2 : LOW_BAT Battery low-voltage Status
0 : VBAT > VBAT_LO
1 : VBAT < VBAT_LO while DCINOK

Bit 1 : VBAT_SHORT Battery short-circuits detection status
0 : VBAT > 1.6V (Hysteresis)
1 : VBAT < 1.5V

Bit 0 : DBAT_DET Dead Battery detection status
0 : Not detected
1 : Detected
VBAT keeps under VBAT_LO until the timer is expired, the battery is assumed as a weak battery or a dead battery.
The timer expiration time is set by TIM_DBP register.

Address 37h: DCIN_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
37h	DCIN_STAT	R	-	-	-	-	DCIN_OV	INHIBIT(Note1)	DCIN_CLPS	DCIN_DET
	Initial Value (Master mode)	0Xh	0	0	0	0	x	x	x	x
	Initial Value (Slave mode)	0Xh	0	0	0	0	x	x	x	x

Bit 3 : DCIN_OV DCIN over-voltage status
0 : Normal voltage
1 : DCIN > 6.5V

Bit 2 : INHIBIT(Note1) For ROHM factory only

Bit 1 : DCIN_CLPS DCIN anti-collapse status
0 : Normal operation
1 : Anti-collapse

Bit 0 : DCIN_DET DCIN detection status
0 : Not detected or low level
1 : DCIN detected (over UVLO level)

Address 38h: VSYS_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38h	VSYS_STAT	R	-	-	-	-	-	-	VSYS_LO	VSYS_UVN
	Initial Value (Master mode)	0Xh	0	0	0	0	0	0	x	x
	Initial Value (Slave mode)	0Xh	0	0	0	0	0	0	x	x

Bit 1 : VSYS_LO VSYS low voltage detection status
0 : VSYS < VSYS_MIN
1 : VSYS > VSYS_MAX

Bit 0 : VSYS_UVN VSYS UVLO detection status
0 : Low voltage
1 : Normal voltage

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Address 39h: CHG_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
39h	CHG_STAT	R	-	-	-	-	-	-	-	VRECHG_DET
	Initial Value (Master mode)	0Xh	0	0	0	0	0	0	0	x
	Initial Value (Slave mode)	0Xh	0	0	0	0	0	0	0	x

Bit 0 : VRECHG_DET Re-charge voltage detection status voltage.
0 : VBAT > VBAT_MNT
1 : VBAT < VBAT_MNT

Address 3Ah: CHG_WDT_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Ah	CHG_WDT_STAT	R	CHGWDTS[7:0]							
	Initial Value (Master mode)	XXh	x	x	x	x	x	x	x	x
	Initial Value (Slave mode)	XXh	x	x	x	x	x	x	x	x

Bit 7-0 : CHGWDTS[7:0] Actual watch-dog timer counter value for Pre-charging & Tricle-Charging or Fast Charging & Top Off.
PCHG(or TCHG) : (CHGWDTS -1) X (64/60) min.
FCHG(or TOFF) : (CHGWDTS * 8 -240) * (64/60/2) min.
FCHG(or TOFF) COLD1 condition : (CHGWDTS * 8 -3) * (64/60) min.

Address 3Bh: BAT_TEMP Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Bh	BAT_TEMP	R	-	-	-	-	-	BAT_TEMP[2:0]		
	Initial Value (Master mode)	0Xh	0	0	0	0	0	x	x	x
	Initial Value (Slave mode)	0Xh	0	0	0	0	0	x	x	x

Bit 2-0 : BAT_TEMP[2:0] The temperature thresholds have hysteresis.
Table lists the temperature threshold values.

BAT_TEMP	Temperature Range	Description
0h	Room Temp	T2 < Tbat < T3
1h	HOT1	T3 < Tbat < T5
2h	HOT2	T5 < Tbat < T4
3h	HOT3	T4 < Tbat
4h	COLD1	T1 < Tbat < T2
5h	COLD2	Tbat < T1
6h	Temp. Disable	Disable thermal control (No Thermistor)
7h	Battery Open	TS port is open

No.	Description	Default Value	Note
1	Lower threshold of T1	2 deg.	T1 in JEITA profile
2	Upper threshold of T1	5 deg.	T1 in JEITA profile
3	Lower threshold of T2	10 deg.	T2 in JEITA profile
4	Upper threshold of T2	13 deg.	T2 in JEITA profile
5	Lower threshold of T3	42 deg.	T3 in JEITA profile
6	Upper threshold of T3	45 deg.	T3 in JEITA profile
7	Lower threshold of T4	55 deg.	T4 in JEITA profile
8	Upper threshold of T4	58 deg.	T4 in JEITA profile
9	Lower threshold of T5	47 deg.	Between T3 and T4
10	Upper threshold of T5	50 deg.	Between T3 and T4

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Address 3Eh: DCIN_CLPS Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Eh	DCIN_CLPS	R/W	DCIN_CLPS[7:0]							
	Initial Value (Master mode)	36h	0	0	1	1	0	1	1	0
	Initial Value (Slave mode)	36h	0	0	1	1	0	1	1	0

Bit 7-0 : DCIN_CLPS[7:0] DCIN Anti-collapse entry voltage threshold
0 V to 20.4 V range, 80 mV steps.
When DCIN < DCIN_CLPS is detected, the charger decrease the charging current.
DCIN_CLPS voltage must set to be higher than VBAT_CHG.

DCIN_CLPS	Threshold Voltage
00h	0.0V
~	~
33h	3.08V
34h	3.16V
35h	3.24V
36h	3.32V
37h	3.40V
38h	3.48V
39h	3.56V
3Ah	3.64V
3Bh	3.72V
3Ch	3.80V
3Dh	3.88V
3Eh	3.96V
~	~
FFh	20.4V

Address 3Fh: VSYS_REG Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Fh	VSYS_REG	R/W	-	-	-	INHIBIT(Note1)	VSYS_REG[3:0]			
	Initial Value (Master mode)	09h	0	0	0	0	1	0	0	1
	Initial Value (Slave mode)	09h	0	0	0	0	1	0	0	1

Bit 4 : INHIBIT(Note1) For ROHM factory only

Bit 3-0 : VSYS_REG[3:0] VSYS regulation voltage setting
4.2V to 5.25V range

VSYS_REG	VSYS Voltage
00h	4.20 V
01h	4.30 V
02h	4.40 V
03h	4.45 V
04h	4.50 V
05h	4.55 V
06h	4.60 V
07h	4.65 V
08h	4.70 V
09h	4.75 V
0Ah	4.80 V
0Bh	4.85 V
0Ch	4.90 V
0Dh	4.95 V
0Eh	5.00 V
0Fh	5.25 V

Address 40h: VSYS_MAX Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
40h	VSYS_MAX	R/W	-	VSYS_MAX[6:0]						
	Initial Value (Master mode)	23h	0	0	1	0	0	0	1	1
	Initial Value (Slave mode)	21h	0	0	1	0	0	0	0	1

Bit 6-0 : VSYS_MAX[6:0] VSYS voltage rising detection threshold
0.5V to 7.0V range, 0.1V steps

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Address 41h: VSYS_MIN Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
41h	VSYS_MIN	R/W	-	VSYS_MIN[6:0]						
	Initial Value (Master mode)	21h	0	0	1	0	0	0	0	1
	Initial Value (Slave mode)	1Fh	0	0	0	1	1	1	1	1

Bit 6-0 : VSYS_MIN[6:0] VSYS voltage rising detection threshold
0.5V to 7.0V range, 0.1V steps

VSYS_MAX VSYS_MIN	VSYS Voltage
05h-15h	0.5V - 2.1 V
16h	2.2 V
17h	2.3 V
18h	2.4 V
19h	2.5 V
1Ah	2.6 V
1Bh	2.7 V
1Ch	2.8 V
1Dh	2.9 V
1Eh	3.0 V
1Fh	3.1 V
20h	3.2 V
21h	3.3 V
22h	3.4 V
23h	3.5 V
24h	3.6 V
25h-41h	3.7V - 7.0V

Address 42h: CHG_SET1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
42h	CHG_SET1	R/W	WDT_DIS	WDT_AUTO	AUTO_FST	FST_TRG	AUTO_RECHG	BTMP_EN	COLD_ERR_EN	CHG_EN
	Initial Value (Master mode)	6Fh	0	1	1	0	1	1	1	1
	Initial Value (Slave mode)	6Fh	0	1	1	0	1	1	1	1

Bit 7 : WDT_DIS Disable Charger WDT
0 : Normal operation
1 : Disable When WDT_DIS = "0", the charger will stop charging when the WDT expired. It means something error has been occurred.
Setting WDT_DIS = "1", the Host should handle any error by its software.

Bit 6 : WDT_AUTO WDT setting mode
0 : Manual setting
1 : Auto setting At the auto setting mode, the WDT expiration time is set to 128 minutes for Pre-charging and 640 minites for Fast-charging.
In the Manual setting mode, the WDT expiration time is set by the register WDT_PRE for Pre-charging and the register WDT_FST for Fast-

Bit 5 AUTO_FST Fast charging transition mode
0 : Manual control
1 : Auto control When VBAT > VPRE_HI is detected at Pre-charging, the charger goes to Fast Charging.
In the Manual control mode, the Host should write FST_TRG = "1" to move the charger to Fast Charging.

Bit 4 FST_TRG Trigger to move to Fast Charging
0 : No action
1 : Generate the trigger See AUTO_FST. In using this register, please set AUTO_FST as '0'.

Bit 3 AUTO_RECHG Automatic re-charging mode
0 : Manual control
1 : Auto control In the auto control mode, the charger will re-start charging when the maintenance voltage detected (VBAT < VBAT_MNT).
While the manual control mode, VBAT_MNT can be detected but re-charging should be entered by the software.

Bit 2 BTMP_EN Charging voltage is reduced by battery temperature.
0 : Disable
1 : Enable

Bit 1 COLD_ERR_EN Slow down the watch-dog timer counter in COLD1 condition
0 : Disable Count down per 4.27min
1 : Enable Count down per 8.53min

Bit 0 CHG_EN Enabling charger operation
0 : Disable
1 : Enable

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Address 43h: CHG_SET2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43h	CHG_SET2	R/W	VF_TREG_EN	-	REBATDET	BATDET_EN	-	-	TIM_CNT_SEL[1:0]	
	Initial Value (Master mode)	90h	1	0	0	1	0	0	0	0
	Initial Value (Slave mode)	90h	1	0	0	1	0	0	0	0

Bit 7 : VF_TREG_EN Thermal shutdown for charger 0 : Disable / 1 : Enable

Bit 5 : REBATDET Trigger for re-trial of the Battery detection 0 : Release the operation / 1 : Start detection

Bit 4 : BATDET_EN Enabling Battery detection 0 : Disable / 1 : Enable

Bit 1-0 : TIM_CNT_SEL[1:0] Transition Timer Setting from the Suspend State to the Trickle state

TIM_CNT_SEL[2:0]	Timer Setting (CLK32K Cycle)
0h	1600 (48.8ms)
1h	3200 (97.7ms)
2h	4800 (146.5ms)
3h	6400 (195.3ms)

Address 44h: CHG_WDT_PRE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
44h	CHG_WDT_PRE	R/W	WDT_PRE[7:0]							
	Initial Value (Master mode)	1Eh	0	0	0	1	1	1	1	0
	Initial Value (Slave mode)	1Eh	0	0	0	1	1	1	1	0

Bit 7-0 : WDT_PRE[7:0] Watch Dog Timer setting for Pre-charging
1 to 272 minutes range, 64-sec steps
This register is effective only when '0' is written to WDT_AUTO(address 42h Bit6).
PCHG(or TCHG) : (CHGWDTS -1) * (64/60) min.

Address 45h: CHG_WDT_FST Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
45h	CHG_WDT_FST	R/W	WDT_FST[7:0]							
	Initial Value (Master mode)	26h	0	0	1	0	0	1	1	0
	Initial Value (Slave mode)	26h	0	0	1	0	0	1	1	0

Bit 7-0 : WDT_FST[7:0] Watch Dog Timer setting for Fast Charging
8.5 to 2176 minutes range, 512-sec steps
This register is effective only when '0' is written to WDT_AUTO(address 42h Bit6).
FCHG(or TOFF) : (CHGWDTS * 8 -240) * (64/60/2) min.
FCHG(or TOFF) COLD1 condition : (CHGWDTS * 8 -3) X (64/60) min.

Address 46h: CHG_IPRE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
46h	CHG_IPRE	R/W	ITRI[3:0]				IPRE[3:0]			
	Initial Value (Master mode)	52h	0	1	0	1	0	0	1	0
	Initial Value (Slave mode)	52h	0	1	0	1	0	0	1	0

Bit 7-4 : ITRI[3:0] Trickle charge current setting
10 mA to 100 mA range, 10 mA steps

Bit 3-0 : IPRE[3:0] Pre-charging current setting
50 mA to 500 mA range, 50 mA steps.

ITRI	Trickle charging current
0h	0 mA
1h	10 mA
2h	20 mA
3h	30 mA
4h	40 mA
5h	50 mA
6h	60 mA
7h	70 mA
8h	80 mA
9h	90 mA
Ah	100 mA
Bh-Fh	(reserved)

IPRE	Pre-charging current
0h	0 mA
1h	50 mA
2h	100 mA
3h	150 mA
4h	200 mA
5h	250 mA
6h	300 mA
7h	350 mA
8h	400 mA
9h	450 mA
Ah	500 mA
Bh-Fh	(reserved)

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Address 47h: CHG_IFST Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
47h	CHG_IFST	R/W	-	-	-	IFST[4:0]				
	Initial Value (Master mode)	04h	0	0	0	0	0	1	0	0
	Initial Value (Slave mode)	04h	0	0	0	0	0	1	0	0

Bit 4-0 IFST[4:0] Battery Charging Current for Fast Charge
100 mA to 2000 mA range, 100 mA steps

IFST	Fast charging Current
00h	0 mA
01h	100 mA
02h	200 mA
03h	300 mA
04h	400 mA
05h	500 mA
06h	600 mA
07h	700 mA
08h	800 mA
09h	900 mA
0Ah	1000 mA
0Bh	1100 mA
0Ch	1200 mA
0Dh	1300 mA
0Eh	1400 mA
0Fh	1500 mA
10h	1600 mA
11h	1700 mA
12h	1800 mA
13h	1900 mA
14h	2000 mA
15h-1Fh	(reserved)

Address 48h: CHG_IFST_TERM Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
48h	CHG_IFST_TERM	R/W	-	-	-	-	IFST_TERM[3:0]			
	Initial Value (Master mode)	05h	0	0	0	0	0	1	0	1
	Initial Value (Slave mode)	05h	0	0	0	0	0	1	0	1

Bit 3-0 : IFST_TERM[3:0] Charging Termination Current for Fast Charge
10 mA to 200 mA range

ICHG_TERM	Termination Current
0h	0 mA
1h	10 mA
2h	20 mA
3h	30 mA
4h	40 mA
5h	50 mA
6h	100 mA
7h	150 mA
8h	200 mA
9h-Fh	(reserved)

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Address 49h: CHG_VPRE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
49h	CHG_VPRE	R/W	VPRE_HI[3:0]				VPRE_LO[3:0]			
	Initial Value (Master mode)	C9h	1	1	0	0	1	0	0	1
	Initial Value (Slave mode)	C9h	1	1	0	0	1	0	0	1

Bit 7-4 : VPRE_HI[3:0] Upper threshold of Pre-charging voltage
2.1V to 3.6V range, 0.1V steps.

Bit 3-0 : VPRE_LO[3:0] Lower threshold of Pre-charging voltage
2.1V to 3.6V range, 0.1V steps. VPRE_LO is also the upper threshold of Trickle Charging voltage.

VPRE_HI VPRE_LO	Setting Voltage
0h	2.1 V
1h	2.2 V
2h	2.3 V
3h	2.4 V
4h	2.5 V
5h	2.6 V
6h	2.7 V
7h	2.8 V
8h	2.9 V
9h	3.0 V
Ah	3.1 V
Bh	3.2 V
Ch	3.3 V
Dh	3.4 V
Eh	3.5 V
Fh	3.6 V

Address 4Ah: CHG_VBAT_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Ah	CHG_VBAT_1	R/W	-	-	-	VBAT_CHG1[4:0]				
	Initial Value (Master mode)	18h	0	0	0	1	1	0	0	0
	Initial Value (Slave mode)	18h	0	0	0	1	1	0	0	0

Bit 4-0 : VBAT_CHG1[4:0] Fast Charging Voltage for the temperature range T2-T3 (ROOM)

Address 4Bh: CHG_VBAT_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Bh	CHG_VBAT_2	R/W	-	-	-	VBAT_CHG2[4:0]				
	Initial Value (Master mode)	13h	0	0	0	1	0	0	1	1
	Initial Value (Slave mode)	13h	0	0	0	1	0	0	1	1

Bit 4-0 : VBAT_CHG2[4:0] Fast Charging Voltage for the temperature range T3-T5

Address 4Ch: CHG_VBAT_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Ch	CHG_VBAT_3	R/W	-	-	-	VBAT_CHG3[4:0]				
	Initial Value (Master mode)	10h	0	0	0	1	0	0	0	0
	Initial Value (Slave mode)	10h	0	0	0	1	0	0	0	0

Bit 4-0 : VBAT_CHG3[4:0] Fast Charging Voltage for the temperature range T5-T4 and T2-T1

VBAT_CHGx	Setting Voltage
00h	3.72 V
01h	3.74 V
02h	3.76 V
03h	3.78 V
04h	3.80 V
~	~
1Dh	4.30 V
1Eh	4.32 V
1Fh	4.34 V

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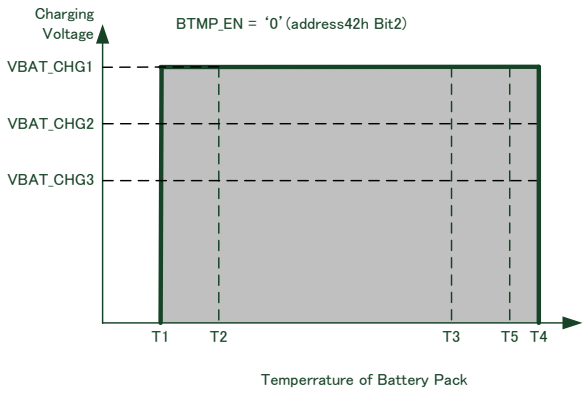

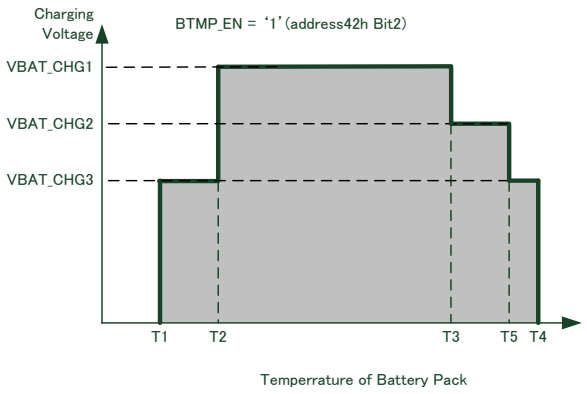

Address 4Dh: CHG_LED_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Dh	CHG_LED_1	R/W	-	-	-	-	-	TERR[2:0]		
	Initial Value (Master mode)	03h	0	0	0	0	0	0	1	1
	Initial Value (Slave mode)	03h	0	0	0	0	0	0	1	1

Bit 2-0 : TERR[2:0] CHGLED lighting setting for the battery charging temperature error indication.

TERR_TOUT	LED Lighting for Error Indication
0h	Always lighting ON
1h	Blinking in 0.128 Hz
2h	Blinking in 0.256 Hz
3h	Blinking in 0.512 Hz
4h	Blinking in 1 Hz
5h	Blinking in 4 Hz
6h	Blinking in 8 Hz
7h	Light OFF

Address 4Eh: VF_TH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Eh	VF_TH	R/W	VF_TH[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7-0 : VF_TH[7:0] Vf Voltage threshold for monitor
0.100V to 1.395V range, 1.3V/256 steps

Address 4Fh: BAT_SET_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Fh	BAT_SET_1	R/W	VBAT_HI[3:0]				VBAT_LO[3:0]			
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7-4 : VBAT_HI[3:0] Battery voltage threshold for VBAT rising
3.00V to 3.60V range, 50 mV steps.

Bit 3-0 : VBAT_LO[3:0] Battery voltage threshold for VBAT falling
2.50V to 3.10V range, 50 mV steps. VBAT_LO is also the lower threshold of dead battery detection.

VBAT_HI	Setting Voltage
0h	3.00 V
1h	3.05 V
2h	3.10 V
3h	3.15 V
4h	3.20 V
5h	3.25 V
6h	3.30 V
7h	3.35 V
8h	3.40 V
9h	3.45 V
Ah	3.50 V
Bh	3.55 V
Ch	3.60 V
Dh	3.65 V
Eh	3.70 V
Fh	3.75 V

VBAT_LO	Setting Voltage
0h	2.50 V
1h	2.55 V
2h	2.60 V
3h	2.65 V
4h	2.70 V
5h	2.75 V
6h	2.80 V
7h	2.85 V
8h	2.90 V
9h	2.95 V
Ah	3.00 V
Bh	3.05 V
Ch	3.10 V
Dh	3.15 V
Eh	3.20 V
Fh	3.25 V

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Address 50h: BAT_SET_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
50h	BAT_SET_2	R/W	VBAT_OVP[3:0]				-	VBAT_MNT[2:0]		
	Initial Value (Master mode)	30h	0	0	1	1	0	0	0	0
	Initial Value (Slave mode)	30h	0	0	1	1	0	0	0	0

Bit 7-4 : VBAT_OVP[3:0] Battery over-voltage detection threshold.
4.40V to 4.80V range, 50 mV steps

Bit 2-0 : VBAT_MNT[2:0] Battery voltage maintenance threshold.
The charger starts re-charging when VBAT < VBAT_MNT.

VBAT_OVP	Setting Voltage
0h	4.40 V
1h	4.45 V
2h	4.50 V
3h	4.55 V
4h	4.60 V
5h	4.65 V
6h	4.70 V
7h	4.75 V
8h	4.80 V
9h - Fh	(reserved)

VBAT_MNT	Setting Voltage
0h	VBAT_CHG1/2/3 - 0.35V
1h	VBAT_CHG1/2/3 - 0.30V
2h	VBAT_CHG1/2/3 - 0.25V
3h	VBAT_CHG1/2/3 - 0.20V
4h	VBAT_CHG1/2/3 - 0.15V
5h	VBAT_CHG1/2/3 - 0.10V
6h	VBAT_CHG1/2/3 - 0.05V
7h	VBAT_CHG1/2/3 - 0.00V

Address 51h: BAT_SET_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
51h	BAT_SET_3	R/W	-	-	-	-	-	TIM_DBP[2:0]		
	Initial Value (Master mode)	02h	0	0	0	0	0	0	1	0
	Initial Value (Slave mode)	02h	0	0	0	0	0	0	1	0

Bit 2-0 : TIM_DBP[2:0] Dead Battery Provisioning timer setting
Refer to the description for DBAT_DET.

TIM_DBP	DBP Timer Setting
0h	12 min
1h	32 min
2h	45 min
3h	64 min
4h	128 min
5h	5 min
6h	1 min
7h	0 min

Address 52h: ALM_VBAT_TH_U Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	ALM_VBAT_TH_U	R/W	-	-	-	-	-	-	-	VBAT_TH[8]
	Initial Value (Master mode)	01h	0	0	0	0	0	0	0	1
	Initial Value (Slave mode)	01h	0	0	0	0	0	0	0	1

Address 53h: ALM_VBAT_TH_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
53h	ALM_VBAT_TH_L	R/W	VBAT_TH[7:0]							
	Initial Value (Master mode)	FFh	1	1	1	1	1	1	1	1
	Initial Value (Slave mode)	FFh	1	1	1	1	1	1	1	1

VBAT_TH[8:0] Battery Voltage Alarm Threshold
Setting Range is from 0.00V to 8.176V, 16mV steps. See also VBAT_MON_DET/RES alarm.

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Address 54h: ALM_DCIN_TH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
54h	ALM_DCIN_TH	R/W	DCIN_TH[7:0]							
	Initial Value (Master mode)	0Fh	0	0	0	0	1	1	1	1
	Initial Value (Slave mode)	0Fh	0	0	0	0	1	1	1	1

DCIN_TH[7:0] DCIN Voltage Alarm Threshold
Setting Range is from 0V to 20.4V, 80mV steps.

Address 55h: ALM_VSYS_TH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
55h	ALM_VSYS_TH	R/W	VSYS_TH[7:0]							
	Initial Value (Master mode)	FFh	1	1	1	1	1	1	1	1
	Initial Value (Slave mode)	FFh	1	1	1	1	1	1	1	1

VSYS_TH[7:0] VSYS Voltage Alarm Threshold
Setting Range is from 0V to 12.75V, 50mV steps.

Address 56h: VM_IBAT_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
56h	VM_IBAT_U	R	-	-	-	-	IBAT[11:8]			
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 57h: VM_IBAT_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
57h	VM_IBAT_L	R	IBAT[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

IBAT[11:0] Measured Battery Current
0 A to 4.095 A range, 1mA steps.

Address 58h: VM_VBAT_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
58h	VM_VBAT_U	R	-	-	-	VBAT[12:8]				
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 59h: VM_VBAT_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
59h	VM_VBAT_L	R	VBAT[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

VBAT[12:0] Measured Battery Voltage
0 V to 8.191 V range, 1mV steps. This register value is also used for Over-Voltage detection and some Charger functions.

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Address 5Ah: VM_BTMP Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Ah	VM_BTMP	R/W	BTMP[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7-0 : BTMP[7:0] Measured / Preset Battery Temperature
-55 to 200 deg. Celsius, 1-degree steps.
(R) BTMP is measured at the same time of measuring VTH.
(W) BTMP is effective when a thermistor does not exist.

Address 5Bh: VM_VTH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Bh	VM_VTH	R/W	VTH[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7-0 : VTH[7:0] Thermistor terminal (TS) voltage
0.1 V to 1.395 V range, 1.3/256 V steps.

Address 5Ch: VM_DCIN_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Ch	VM_DCIN_U	R	-	-	-	-	DCIN[11:8]			
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 5Dh: VM_DCIN_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Dh	VM_DCIN_L	R	DCIN[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

DCIN[11:0] Measured DCIN Voltage
0 V to 20.475 V range, 5mV steps.

Address 5Eh: VM_VSYS Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Eh	VM_VSYS	R	VSYS[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7-0 : VSYS[7:0] Measured VSYS voltage
0 V to 12.75 V range, 50 mV steps.

Address 5Fh: VM_VF Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Fh	VM_VF	R	VF[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7-0 : VF[7:0] Vf Voltage threshold for monitor
0.1 V to 1.395 V range, 1.3/256 V steps.

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Address 60h: VM_IBATLOAD_PRE_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
60h	VM_IBATLOAD_PRE_U	R	-	-	-	-	IBAT_BATLOAD_PRE[11:8]			
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 61h: VM_IBATLOAD_PRE_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
61h	VM_IBATLOAD_PRE_L	R	IBAT_BATLOAD_PRE[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

VBAT_BATLOAD_PRE[11:0] Measured Battery Current previous to Load when Battery Detection
0 A to 4.095 A range, 1 mA steps.

Address 62h: VM_VBATLOAD_PRE_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
62h	VM_VBATLOAD_PRE_U	R	-	-	-	VBAT_BATLOAD_PRE[12:8]				
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 63h: VM_VBATLOAD_PRE_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
63h	VM_VBATLOAD_PRE_L	R	VBAT_BATLOAD_PRE[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

VBAT_BATLOAD_PRE[12:0] Measured Battery Voltage previous to Load when Battery Detection
0 V to 8.191 V range, 1 mV steps.

Address 64h: VM_IBATLOAD_PST_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
64h	VM_IBATLOAD_PST_U	R	-	-	-	-	IBAT_BATLOAD_PST[11:8]			
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 65h: VM_IBATLOAD_PST_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
65h	VM_IBATLOAD_PST_L	R	IBAT_BATLOAD_PST[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

IBAT_BATLOAD_PST[11:0] Measured Battery Current while in Load when Battery Detection
0 A to 4.095 A range, 1 mA steps.

Address 66h: VM_VBATLOAD_PST_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
66h	VM_VBATLOAD_PST_U	R	-	-	-	VBAT_BATLOAD_PST[12:8]				
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

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Address 67h: VM_VBATLOAD_PST_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
67h	VM_VBATLOAD_PST_L	R	VBAT_BATLOAD_PST[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

IBAT_BATLOAD_PST[12:0] Measured Battery Current while in Load when Battery Detection
0 A to 8.191 A range, 1mA steps.

Address 68h: VM_SMA_VBAT_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
68h	VM_SMA_VBAT_U	R	-	-	-	VBAT_SMA[12:8]				
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 69h: VM_SMA_VBAT_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
69h	VM_SMA_VBAT_L	R	VBAT_SMA[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

VBAT_SMA[12:0] Measured Battery Voltage calucurated simple moving average
0 V to 8.191 V range, 1 mV steps.

Address 6Ah: VM_SMA_IBAT_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Ah	VM_SMA_IBAT_U	R	-	-	-	-	IBAT_SMA[11:8]			
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 6Bh: VM_SMA_IBAT_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Bh	VM_SMA_IBAT_L	R	IBAT_SMA[7:0]							
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

IBAT_SMA[11:0] Measured Battery Current caluculated simple moving average
0 A to 4.095 A range, 1mA steps.

Address 6Dh: CC_CTRL Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Dh	CC_CTRL	R/W	CCNTRST	CCNTENB	CC_CALIB	-	-	-	-	-
	Initial Value (Master mode)	40h	0	1	0	0	0	0	0	0
	Initial Value (Slave mode)	40h	0	1	0	0	0	0	0	0

Bit7 : CCNTRST Reset the Coulomb Counter
0 : Release resetting
1 : Reset CC_CCNTD_3-0 This reset is "Pulse reset type", is not always reset.

Bit6 : CCNTENB Enabling the Coulomb Counter
0 : Disable (stop counting)
1 : Enable (counting)

Bit5 : CC_CALIB Calibration mode selection for the Coulomb Counter
0 : A calibration is carried out automatically.
1 : A calibration is carried out compulsorily.

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Address 6Eh: CC_BATCAP1_TH_U Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Eh	CC_BATCAP1_TH_U	R/W	-	-	-	-	CC_BATCAP1_TH[11:8]			
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 6Fh: CC_BATCAP1_TH_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Fh	CC_BATCAP1_TH_L	R/W	CC_BATCAP1_TH[7:0]							
	Initial Value (Master mode)	7Eh	0	1	1	1	1	1	1	0
	Initial Value (Slave mode)	7Eh	0	1	1	1	1	1	1	0

CC_BATCAP1_TH[11:0] Battery capacity monitor Threshold1

Address 70h: CC_BATCAP2_TH_U Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
70h	CC_BATCAP2_TH_U	R/W	-	-	-	-	CC_BATCAP2_TH[11:8]			
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 71h: CC_BATCAP2_TH_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
71h	CC_BATCAP2_TH_L	R/W	CC_BATCAP2_TH[7:0]							
	Initial Value (Master mode)	3Fh	0	0	1	1	1	1	1	1
	Initial Value (Slave mode)	3Fh	0	0	1	1	1	1	1	1

CC_BATCAP2_TH[11:0] Battery capacity monitor Threshold2

Address 72h: CC_BATCAP3_TH_U Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
72h	CC_BATCAP3_TH_U	R/W	-	-	-	-	CC_BATCAP3_TH[11:8]			
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 73h: CC_BATCAP3_TH_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
73h	CC_BATCAP3_TH_L	R/W	CC_BATCAP3_TH[7:0]							
	Initial Value (Master mode)	1Fh	0	0	0	1	1	1	1	1
	Initial Value (Slave mode)	1Fh	0	0	0	1	1	1	1	1

CC_BATCAP3_TH[11:0] Battery capacity monitor Threshold3

Address 74h: CC_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
74h	CC_STAT	R	-	-	-	-	-	CC_MON3	CC_MON2	CC_MON1
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 2 : CC_MON3 It indicates that the Coulomb Counter goes below the battery capacity monitor threshold 3.
Bit 1 : CC_MON2 It indicates that the Coulomb Counter goes below the battery capacity monitor threshold 2.
Bit 0 : CC_MON1 It indicates that the Coulomb Counter goes below the battery capacity monitor threshold 1.

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Address 75h: CC_CCNTD_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
75h	CC_CCNTD_3	R/W	-	-	-	-	CCNTD[27:24]			
	Initial Value (Master mode)	0Xh	0	0	0	0	x	x	x	x
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 76h: CC_CCNTD_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
76h	CC_CCNTD_2	R/W	CCNTD[23:16]							
	Initial Value (Master mode)	XXh	x	x	x	x	x	x	x	x
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 77h: CC_CCNTD_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
77h	CC_CCNTD_1	R/W	CCNTD[15:8]							
	Initial Value (Master mode)	XXh	x	x	x	x	x	x	x	x
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Address 78h: CC_CCNTD_0 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
78h	CC_CCNTD_0	R/W	CCNTD[7:0]							
	Initial Value (Master mode)	XXh	x	x	x	x	x	x	x	x
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

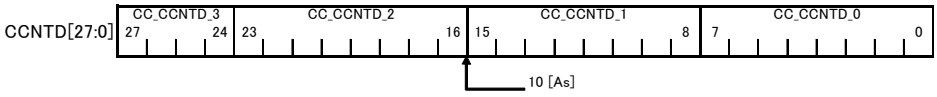
CCNTD[27:0] Coulomb Counter

It indicates the Coulomb Counter accumulated result. CCNTD[27:16] means the battery capacity in 10 [As] (Ampere-second) unit, and CCNTD[1:0] is always "00". For example, when the battery capacity is 1350 [mAh], the register value will be shown as below 1350 [mAh] / 1000 [mA/A] x 3600 [s/h] = 4860 [As]. CCNTD[27:16] = 4860 / 10 = 486 (1E6h)

When CCNTENB = "1", the Coulomb Counter is enabled accumulation of the charge or discharge current value.
In the battery charging, the measured current value is added to the Coulomb Counter at every conversion period.
Before starting the battery charging, CCNTD must be reset to zero or initialized with an estimated SoC (State of Charge) value by software.
If an empty battery is full-charged, CCNTD value indicates the actual battery capacity.

This read-only register is able to reset by the register bit CCNTRST.

In the battery discharging, the Coulomb Counter decreases the value. Before discharging, CCNTD must be initialized with BATCAP value by software, if the remaining battery capacity is unknown.



Address 79h: CC_CURCD_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
79h	CC_CURCD_U	R	CURDIR	-	CURCD[13:8]					
	Initial Value (Master mode)	XXh	x	0	x	x	x	x	x	x
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 : CURDIR Battery current direction 0 : Charging / 1 : Discharging

Address 7Ah: CC_CURCD_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Ah	CC_CURCD_L	R	CURCD[7:0]							
	Initial Value (Master mode)	XXh	x	x	x	x	x	x	x	x
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

CURCD[13:0] Battery current value converted from DS-ADC output
0 mA to 16,384 mA range, 1 mA units.

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Address 7Bh: VM_OCUR_THR_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Bh	VM_OCUR_THR_1	R/W	OCURTHR1[7:0]							
	Initial Value (Master mode)	7Dh	0	1	1	1	1	1	0	1
	Initial Value (Slave mode)	7Dh	0	1	1	1	1	1	0	1

Bit 7-0 : OCURTHR1[7:0] Battery over-current threshold
The value is set in 50 mA unit.

Address 7Ch: VM_OCUR_DUR_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Ch	VM_OCUR_DUR_1	R/W	OCURDUR1[7:0]							
	Initial Value (Master mode)	64h	0	1	1	0	0	1	0	0
	Initial Value (Slave mode)	64h	0	1	1	0	0	1	0	0

Bit 7-0 : OCURDUR1[7:0] The duration time for the battery over-current detection
The value is set in 250 s unit.

Address 7Dh: VM_OCUR_THR_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Dh	VM_OCUR_THR_2	R/W	OCURTHR2[7:0]							
	Initial Value (Master mode)	5Eh	0	1	0	1	1	1	1	0
	Initial Value (Slave mode)	5Eh	0	1	0	1	1	1	1	0

Bit 7-0 : OCURTHR2[7:0] Battery over-current threshold
The value is set in 50 mA unit.

Address 7Eh: VM_OCUR_DUR_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Eh	VM_OCUR_DUR_2	R/W	OCURDUR2[7:0]							
	Initial Value (Master mode)	8Ch	1	0	0	0	1	1	0	0
	Initial Value (Slave mode)	8Ch	1	0	0	0	1	1	0	0

Bit 7-0 : OCURDUR2[7:0] The duration time for the battery over-current detection
The value is set in 250 s unit.
When CURRD > OCURTHR2 and keeps while OCURDUR1 of time length, the register bit OCUR2 will be asserted.

Address 7Fh: VM_OCUR_THR_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Fh	VM_OCUR_THR_3	R/W	OCURTHR3[7:0]							
	Initial Value (Master mode)	4Eh	0	1	0	0	1	1	1	0
	Initial Value (Slave mode)	4Eh	0	1	0	0	1	1	1	0

Bit 7-0 : OCURTHR3[7:0] Battery over-current threshold
The value is set in 50 mA unit.

Address 80h: VM_OCUR_DUR_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
80h	VM_OCUR_DUR_3	R/W	OCURDUR3[7:0]							
	Initial Value (Master mode)	A5h	1	0	1	0	0	1	0	1
	Initial Value (Slave mode)	A5h	1	0	1	0	0	1	0	1

Bit 7-0 : OCURDUR3[7:0] The duration time for the battery over-current detection.
The value is set in 250 s unit.
When CURRD > OCURTHR3 and keeps while OCURDUR3 of time length, the register bit OCUR3 will be asserted.

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Address 81h: VM_OCUR_MON Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
81h	VM_OCUR_MON	R	-	-	-	-	-	OCUR3	OCUR2	OCUR1
	Initial Value (Master mode)	0Xh	0	0	0	0	0	x	x	x
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 2 : OCUR3 Battery over-current 3 detection status 0 : Not detected / 1 : Detected
Bit 1 : OCUR2 Battery over-current 2 detection status 0 : Not detected / 1 : Detected
Bit 0 : OCUR1 Battery over-current 1 detection status 0 : Not detected / 1 : Detected

Address 82h: VM_BTMP_OV_THR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
82h	VM_BTMP_OV_THR	R/W	OVBTMPTHR[7:0]							
	Initial Value (Master mode)	8Ch	1	0	0	0	1	1	0	0
	Initial Value (Slave mode)	8Ch	1	0	0	0	1	1	0	0

Bit 7-0 : OVBTMPTHR[7:0] Battery over-temperature threshold
The value is set in 1-degree unit, -55 to 200 degree range.

Address 83h: VM_BTMP_OV_DUR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
83h	VM_BTMP_OV_DUR	R/W	OVBTMPDUR[7:0]							
	Initial Value (Master mode)	28h	0	0	1	0	1	0	0	0
	Initial Value (Slave mode)	28h	0	0	1	0	1	0	0	0

Bit 7-0 : OVBTMPDUR[7:0] The duration time for the battery over-temperature detection
The value is set in 250 us unit.
When BTMPD > OVTMPTHR and keeps while OVTMPDUR of time length, the register bit OVTMP will be asserted.

Address 84h: VM_BTMP_LO_THR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
84h	VM_BTMP_LO_THR	R/W	LOBTMPTHR[7:0]							
	Initial Value (Master mode)	C8h	1	1	0	0	1	0	0	0
	Initial Value (Slave mode)	C8h	1	1	0	0	1	0	0	0

Bit 7-0 : LOBTMPTHR[7:0] Battery low-temperature threshold
The value is set in 1-degree unit, -55 to 200 degree range.

Address 85h: VM_BTMP_LO_DUR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
85h	VM_BTMP_LO_DUR	R/W	LOBTMPDUR[7:0]							
	Initial Value (Master mode)	28h	0	0	1	0	1	0	0	0
	Initial Value (Slave mode)	28h	0	0	1	0	1	0	0	0

Bit 7-0 : LOBTMPDUR[7:0] The duration time for the battery over-temperature detection
The value is set in 250 us unit.
When BTMPD < LOTMPTHR and keeps while LOTMPDUR of time length, the register bit LOTMP will be asserted.

Address 86h: VM_BTMP_MON Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
86h	VM_BTMP_MON	R	-	-	-	-	-	-	OVBTMP	LOBTMP
	Initial Value (Master mode)	0Xh	0	0	0	0	0	0	x	x
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 1 : OVBTMP Battery over-temperature detection status 0 : Not detected / 1 : Detected
Bit 0 : LOBTMP Battery low-temperature detection status 0 : Not detected / 1 : Detected

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Address 88h: INT_EN_01 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
88h	INT_EN_01	R/W	-	-	-	-	BUCK4FAULT	BUCK3FAULT	BUCK2FAULT	BUCK1FAULT
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 3 :	BUCK4FAULT	Enabling interrupt of BUCK4 input current-limit modified	0 : Disable / 1 : Enable
Bit 2 :	BUCK3FAULT	Enabling interrupt of BUCK3 input current-limit modified	0 : Disable / 1 : Enable
Bit 1 :	BUCK2FAULT	Enabling interrupt of BUCK2 input current-limit modified	0 : Disable / 1 : Enable
Bit 0 :	BUCK1FAULT	Enabling interrupt of BUCK1 input current-limit modified	0 : Disable / 1 : Enable

Address 89h: INT_EN_02 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
89h	INT_EN_02	R/W	-	-	DCIN_OV_DET	DCIN_OV_RES	DCIN_CLPS_IN	DCIN_CLPS_OUT	DCIN_RMV	-
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 5 :	DCIN_OV_DET	Enabling interrupt of DCIN over-voltage detected	0 : Disable / 1 : Enable
Bit 4 :	DCIN_OV_RES	Enabling interrupt of DCIN over-voltage resumed	0 : Disable / 1 : Enable
Bit 3 :	DCIN_CLPS_IN	Enabling interrupt of entering to DCIN Anti-collapse operation	0 : Disable / 1 : Enable
Bit 2 :	DCIN_CLPS_OUT	Enabling interrupt of exit from DCIN Anti-collapse operation	0 : Disable / 1 : Enable
Bit 1 :	DCIN_RMV	Enabling interrupt of DCIN removal	0 : Disable / 1 : Enable

Address 8Ah: INT_EN_03 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Ah	INT_EN_03	R/W	-	-	-	-	-	-	DCIN_MON_DET	DCIN_MON_RES
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 1 :	DCIN_MON_DET	Enabling interrupt of DCIN monitor detected	0 : Disable / 1 : Enable
Bit 0 :	DCIN_MON_RES	Enabling interrupt of DCIN monitor resumed	0 : Disable / 1 : Enable

Address 8Bh: INT_EN_04 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Bh	INT_EN_04	R/W	VSYS_MON_DET	VSYS_MON_RES	-	-	VSYS_LO_DET	VSYS_LO_RES	VSYS_UV_DET	VSYS_UV_RES
	Initial Value (Master mode)	08h	0	0	0	0	1	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 :	VSYS_MON_DET	Enabling interrupt of VSYS monitor detected	0 : Disable / 1 : Enable
Bit 6 :	VSYS_MON_RES	Enabling interrupt of VSYS monitor resumed	0 : Disable / 1 : Enable
Bit 3 :	VSYS_LO_DET	Enabling interrupt of VSYS low-voltage detected	0 : Disable / 1 : Enable
Bit 2 :	VSYS_LO_RES	Enabling interrupt of VSYS low-voltage resumed	0 : Disable / 1 : Enable
Bit 1 :	VSYS_UV_DET	Enabling interrupt of VSYS under-voltage detected	0 : Disable / 1 : Enable
Bit 0 :	VSYS_UV_RES	Enabling interrupt of VSYS under-voltage resumed	0 : Disable / 1 : Enable

Address 8Ch: INT_EN_05 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Ch	INT_EN_05	R/W	CHG_TRNS	TMP_TRNS	BAT_MNT_IN	BAT_MNT_OUT	CHG_WDT_EXP	EXTEMP_TOUT	-	-
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 :	CHG_TRNS	Enabling interrupt of Charger-State transition	0 : Disable / 1 : Enable
Bit 6 :	TMP_TRNS	Enabling interrupt of Temperature range transition	0 : Disable / 1 : Enable
Bit 5 :	BAT_MNT_IN	Enabling interrupt of entering to Battery Maintenance charging	0 : Disable / 1 : Enable
Bit 4 :	BAT_MNT_OUT	Enabling interrupt of exit from Battery Maintenance charging	0 : Disable / 1 : Enable
Bit 3 :	CHG_WDT_EXP	Enabling interrupt of Charger Watchdog Timer expired	0 : Disable / 1 : Enable
Bit 2 :	EXTEMP_TOUT	Enabling interrupt of Timeout in the temperature over-range	0 : Disable / 1 : Enable

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Address 8Dh: INT_EN_06 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Dh	INT_EN_06	R/W	TH_DET	TH_RMV	BAT_DET	BAT_RMV	-	-	TMP_OUT_DET	TMP_OUT_RES
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 :	TH_DET	Enabling interrupt of the thermistor detected	0 : Disable / 1 : Enable
Bit 6 :	TH_RMV	Enabling interrupt of the thermistor removal	0 : Disable / 1 : Enable
Bit 5 :	BAT_DET	Enabling interrupt of the battery detected	0 : Disable / 1 : Enable
Bit 4 :	BAT_RMV	Enabling interrupt of the battery removed	0 : Disable / 1 : Enable
Bit 1 :	TMP_OUT_DET	Enabling interrupt of the temperature out of the charging range	0 : Disable / 1 : Enable
Bit 0 :	TMP_OUT_RES	Enabling interrupt of the temperature in to the charging range	0 : Disable / 1 : Enable

Address 8Eh: INT_EN_07 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Eh	INT_EN_07	R/W	VBAT_OV_DET	VBAT_OV_RES	VBAT_LO_DET	VBAT_LO_RES	VBAT_SHT_DET	VBAT_SHT_RES	DBAT_DET	-
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 :	VBAT_OV_DET	Enabling interrupt of VBAT over-voltage detected	0 : Disable / 1 : Enable
Bit 6 :	VBAT_OV_RES	Enabling interrupt of VBAT over-voltage resumed	0 : Disable / 1 : Enable
Bit 5 :	VBAT_LO_DET	Enabling interrupt of VBAT low-voltage detected	0 : Disable / 1 : Enable
Bit 4 :	VBAT_LO_RES	Enabling interrupt of VBAT low-voltage resumed	0 : Disable / 1 : Enable
Bit 3 :	VBAT_SHT_DET	Enabling interrupt of VBAT short-circuit detected	0 : Disable / 1 : Enable
Bit 2 :	VBAT_SHT_RES	Enabling interrupt of VBAT short-circuit resumed	0 : Disable / 1 : Enable
Bit 1 :	DBAT_DET	Enabling interrupt of Dead-Battery detected	0 : Disable / 1 : Enable

Address 8Fh: INT_EN_08 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Fh	INT_EN_08	R/W	-	-	-	-	-	-	VBAT_MON_DET	VBAT_MON_RES
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 1 :	VBAT_MON_DET	Enabling interrupt of VBAT monitor1 detected	0 : Disable / 1 : Enable
Bit 0 :	VBAT_MON_RES	Enabling interrupt of VBAT monitor1 resumed	0 : Disable / 1 : Enable

Address 90h: INT_EN_09 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
90h	INT_EN_09	R/W	-	-	-	-	-	CC8TH_DET	CC4TH_DET	CC2ND_DET
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 2 :	CC8TH_DET	Enabling interrupt of under 1/8 capacity discharging	0 : Disable / 1 : Enable
Bit 1 :	CC4TH_DET	Enabling interrupt of under 1/4 capacity discharging	0 : Disable / 1 : Enable
Bit 0 :	CC2ND_DET	Enabling interrupt of under 1/2 capacity discharging	0 : Disable / 1 : Enable

Address 91h: INT_EN_10 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
91h	INT_EN_10	R/W	-	-	OCUR3_DET	OCUR3_RES	OCUR2_DET	OCUR2_RES	OCUR1_DET	OCUR1_RES
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 5 :	OCUR3_DET	Enabling interrupt of Battery over-current 3 detected	0 : Disable / 1 : Enable
Bit 4 :	OCUR3_RES	Enabling interrupt of Battery over-current 3 resumed	0 : Disable / 1 : Enable
Bit 3 :	OCUR2_DET	Enabling interrupt of Battery over-current 2 detected	0 : Disable / 1 : Enable
Bit 2 :	OCUR2_RES	Enabling interrupt of Battery over-current 2 resumed	0 : Disable / 1 : Enable
Bit 1 :	OCUR1_DET	Enabling interrupt of Battery over-current 1 detected	0 : Disable / 1 : Enable
Bit 0 :	OCUR1_RES	Enabling interrupt of Battery over-current 1 resumed	0 : Disable / 1 : Enable

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Address 92h: INT_EN_11 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
92h	INT_EN_11	R/W	VF_DET	VF_RES	VF125_DET	VF125_RES	OVTMP_DET	OVTMP_RES	LOTMP_DET	LOTMP_RES
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 : VF_DET Enabling interrupt of the VF detected 0 : Disable / 1 : Enable
Bit 6 : VF_RES Enabling interrupt of the VF resumed 0 : Disable / 1 : Enable

Bit 5 : VF125_DET Enabling interrupt of the VF at 125℃ detected 0 : Disable / 1 : Enable
Bit 4 : VF125_RES Enabling interrupt of the VF at 125℃ resumed 0 : Disable / 1 : Enable

Bit 3 : OVTMP_DET Enabling interrupt of the battery over-temperature detected 0 : Disable / 1 : Enable
Bit 2 : OVTMP_RES Enabling interrupt of the battery over-temperature resumed 0 : Disable / 1 : Enable

Bit 1 : LOTMP_DET Enabling interrupt of the battery low-temperature detected 0 : Disable / 1 : Enable
Bit 0 : LOTMP_RES Enabling interrupt of the battery low-temperature resumed 0 : Disable / 1 : Enable

Address 93h: INT_EN_12 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
93h	INT_EN_12	R/W	-	-	-	-	-	ALM2	ALM1	ALM0
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 2 : ALM2 Enabling interrupt of the Alarm2 resumed 0 : Disable / 1 : Enable
Bit 1 : ALM1 Enabling interrupt of the Alarm1 resumed 0 : Disable / 1 : Enable
Bit 0 : ALM0 Enabling interrupt of the Alarm0 resumed 0 : Disable / 1 : Enable

Address 94h: INT_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
94h	INT_STAT	R	BUCK_AST	DCIN_AST	VSYS_AST	CHG_AST	BAT_AST	BMON_AST	TMP_AST	ALM_AST
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7(R) : BUCKAST Merged status of INT_STAT_01 0 : No event / 1 : Event occurred
Bit 7(W) : BUCKAST Global reset for INT_STAT_01 0 : Not reset / 1 : Reset
Writing "1" resets all bits of INT_STAT_01 at once.
Indicates the read data from the all bits of INT_STAT_01.

Bit 6(R) : DCINAST Merged status of INT_STAT_02-03 0 : No event / 1 : Event occurred
Bit 6(W) : DCINAST Global reset for INT_STAT_02-03 0 : Not reset / 1 : Reset
Writing "1" resets all bits of INT_STAT_02-03 at once.
Indicates the read data from the all bits of INT_STAT_02-03.

Bit 5(R) : VSYSAST Merged status of INT_STAT_04 0 : No event / 1 : Event occurred
Bit 5(W) : VSYSAST Global reset for INT_STAT_04 0 : Not reset / 1 : Reset
Writing "1" resets all bits of INT_STAT_04 at once.
Indicates the read data from the all bits of INT_STAT_04.

Bit 4(R) : CHGAST Merged status of INT_STAT_05 0 : No event / 1 : Event occurred
Bit 4(W) : CHGAST Global reset for INT_STAT_05 0 : Not reset / 1 : Reset
Writing "1" resets all bits of INT_STAT_05 at once.
Indicates the read data from the all bits of INT_STAT_05.

Bit 3(R) : BATAST Merged status of INT_STAT_06 0 : No event / 1 : Event occurred
Bit 3(W) : BATAST Global reset for INT_STAT_06of INT_STAT_06. 0 : Not reset / 1 : Reset
Writing "1" resets all bits of INT_STAT_06 at once.
Indicates the read data from the all bits of INT_STAT_06.

Bit 2(R) : BMONAST Merged status of INT_STAT_07-10 0 : No event / 1 : Event occurred
Bit 2(W) : BMONAST Global reset for INT_STAT_07-10 0 : Not reset / 1 : Reset
Writing "1" resets all bits of INT_STAT_07-10 at once.
Indicates the read data from the all bits of INT_STAT_07-10.

Bit 1(R) : TMPAST Merged status of INT_STAT_11 0 : No event / 1 : Event occurred
Bit 1(W) : TMPAST Global reset for INT_STAT_11 0 : Not reset / 1 : Reset
Writing "1" resets all bits of INT_STAT_11 at once.
Indicates the read data from the all bits of INT_STAT_11.

Bit 0(R) : ALMAST Merged status of INT_STAT_12 0 : No event / 1 : Event occurred
Bit 0(W) : ALMAST Global reset for INT_STAT_12 0 : Not reset / 1 : Reset
Writing "1" resets all bits of INT_STAT_12 at once.
Indicates the read data from the all bits of INT_STAT_12.

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Address 95h: INT_STAT_01 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
95h	INT_STAT_01	R/WC	-	-	-	-	BUCK4FAULT	BUCK3FAULT	BUCK2FAULT	BUCK1FAULT
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 3 (R) :	BUCK4FAULT	Interrupt status of entering to BUCK4 current limit operation	0 : No event / 1 : Event occurred
Bit 3 (W)	BUCK4FAULT	Interrupt clear fof status of BUCK4 current-limit operation	0 : Not reset / 1 : Reset
Bit 2 (R) :	BUCK3FAULT	Interrupt status of entering to BUCK3 current limit operation	0 : No event / 1 : Event occurred
Bit 2 (W)	BUCK3FAULT	Interrupt clear fof status of BUCK3 current-limit operation	0 : Not reset / 1 : Reset
Bit 1 (R) :	BUCK2FAULT	Interrupt status of entering to BUCK2 current limit operation	0 : No event / 1 : Event occurred
Bit 1 (W)	BUCK2FAULT	Interrupt clear fof status of BUCK2 current-limit operation	0 : Not reset / 1 : Reset
Bit 0 (R) :	BUCK1FAULT	Interrupt status of entering to BUCK1 current limit operation	0 : No event / 1 : Event occurred
Bit 0 (W)	BUCK1FAULT	Interrupt clear fof status of BUCK1 current-limit operation	0 : Not reset / 1 : Reset

Address 96h: INT_STAT_02 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
96h	INT_STAT_02	R/WC	-	-	DCIN_OV_DET	DCIN_OV_RES	DCIN_CLPS_IN	DCIN_CLPS_OUT	DCIN_RMV	-
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 5 (R) :	DCIN_OV_DET	Interrupt status of DCIN over-voltage detected	0 : No event / 1 : Event occurred
Bit 5 (W)	DCIN_OV_DET	Interrupt clear for status of DCIN over-voltage detected	0 : Not reset / 1 : Reset
Bit 4 (R) :	DCIN_OV_RES	Interrupt status of DCIN over-voltage resumed	0 : No event / 1 : Event occurred
Bit 4 (W)	DCIN_OV_RES	Interrupt clear for status of DCIN over-voltage resumed	0 : Not reset / 1 : Reset
Bit 3 (R) :	DCIN_CLPS_IN	Interrupt status of entering to DCIN Anti-collapse op	0 : No event / 1 : Event occurred
Bit 3 (W)	DCIN_CLPS_IN	Interrupt clear for status of entering to DCIN Anti-collapse op	0 : Not reset / 1 : Reset
Bit 2 (R) :	DCIN_CLPS_OUT	Interrupt status of exit from DCIN Anti-collapse op	0 : No event / 1 : Event occurred
Bit 2 (W)	DCIN_CLPS_OUT	Interrupt clear for status of exit from DCIN Anti-collapse op	0 : Not reset / 1 : Reset
Bit 1 (R) :	DCIN_RMV	Interrupt status of DCIN removal	0 : No event / 1 : Event occurred
Bit 1 (W)	DCIN_RMV	Interrupt clear for status of DCIN removal	0 : Not reset / 1 : Reset

Address 97h: INT_STAT_03 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
97h	INT_STAT_03	R/WC	-	-	-	-	-	-	DCIN_MON_DET	DCIN_MON_RES
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 1 (R) :	DCIN_MON_DET	Interrupt clear for status of DCIN voltage monitor detected	0 : No event / 1 : Event occurred
Bit 1 (W)	DCIN_MON_DET	Interrupt status of DCIN voltage monitor detected	0 : Not reset / 1 : Reset
Bit 0 (R) :	DCIN_MON_RES	Interrupt status of DCIN voltage monitor resumed	0 : No event / 1 : Event occurred
Bit 0 (W)	DCIN_MON_RES	Interrupt clear for status of DCIN voltage monitor resumed	0 : Not reset / 1 : Reset

Address 98h: INT_STAT_04 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
98h	INT_STAT_04	R/WC	VSYS_MON_DET	VSYS_MON_RES	-	-	VSYS_LO_DET	VSYS_LO_RES	VSYS_UVDET	VSYS_UV_RES
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 (R) :	VSYS_MON_DET	Interrupt status of VSYS voltage monitor detected	0 : No event / 1 : Event occurred
Bit 7 (W)	VSYS_MON_DET	Interrupt clear for status of VSYS voltage monitor detected	0 : Not reset / 1 : Reset
Bit 6 (R) :	VSYS_MON_RES	Interrupt status of VSYS voltage monitor resumed	0 : No event / 1 : Event occurred
Bit 6 (W)	VSYS_MON_RES	Interrupt clear for status of VSYS voltage monitor resumed	0 : Not reset / 1 : Reset
Bit 3 (R) :	VSYS_LO_DET	Interrupt status of VSYS low-voltage detected	0 : No event / 1 : Event occurred
Bit 3 (W)	VSYS_LO_DET	Interrupt clear for status of VSYS low-voltage detected	0 : Not reset / 1 : Reset
Bit 2 (R) :	VSYS_LO_RES	Interrupt status of VSYS low-voltage resumed	0 : No event / 1 : Event occurred
Bit 2 (W)	VSYS_LO_RES	Interrupt clear for status of VSYS low-voltage resumed	0 : Not reset / 1 : Reset
Bit 1 (R) :	VSYS_UVDET	Interrupt status of VSYS under-voltage detected	0 : No event / 1 : Event occurred
Bit 1 (W)	VSYS_UVDET	Interrupt clear for status of VSYS under-voltage detected	0 : Not reset / 1 : Reset
Bit 0 (R) :	VSYS_UV_RES	Interrupt status of VSYS under-voltage resumed	0 : No event / 1 : Event occurred
Bit 0 (W)	VSYS_UV_RES	Interrupt clear for status of VSYS under-voltage resumed	0 : Not reset / 1 : Reset

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Address 99h: INT_STAT_05 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
99h	INT_STAT_05	R/WC	CHG_TRNS	TMP_TRNS	BAT_MNT_IN	BAT_MNT_OUT	CHG_WDT_EXP	EXTEMP_TOUT	-	-
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 (R) : CHG_TRNS — Interrupt status of Charger-State transition — 0 : No event / 1 : Event occurred
Bit 7 (W) CHG_TRNS — Interrupt clear for status of Charger-State transition — 0 : Not reset / 1 : Reset

Bit 6 (R) : TMP_TRNS — Interrupt status of Temperature range transition — 0 : No event / 1 : Event occurred
Bit 6 (W) TMP_TRNS — Interrupt clear for status of Temperature range transition — 0 : Not reset / 1 : Reset

Bit 5 (R) : BAT_MNT_IN — Interrupt status of entering to Battery Maintenance charging — 0 : No event / 1 : Event occurred
Bit 5 (W) BAT_MNT_IN — Interrupt clear for status of entering to Battery Maintenance charging — 0 : Not reset / 1 : Reset

Bit 4 (R) : BAT_MNT_OUT — Interrupt status of exit from Battery Maintenance charging — 0 : No event / 1 : Event occurred
Bit 4 (W) BAT_MNT_OUT — Interrupt clear for status of exit from Battery Maintenance charging — 0 : Not reset / 1 : Reset

Bit 3 (R) : CHG_WDT_EXP — Interrupt status of Charger Watchdog Timer expired — 0 : No event / 1 : Event occurred
Bit 3 (W) CHG_WDT_EXP — Interrupt clear for status of Charger Watchdog Timer expired — 0 : Not reset / 1 : Reset

Bit 2 (R) : EXTEMP_TOUT — Interrupt status of Timeout in the temperature over-range — 0 : No event / 1 : Event occurred
Bit 2 (W) EXTEMP_TOUT — Interrupt clear for status of Timeout in the temperature over-range — 0 : Not reset / 1 : Reset

Address 9Ah: INT_STAT_06 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Ah	INT_STAT_06	R/WC	TH_DET	TH_RMV	BAT_DET	BAT_RMV	-	-	TMP_OUT_DET	TMP_OUT_RES
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 (R) : TH_DET — Interrupt status of the thermistor detected — 0 : No event / 1 : Event occurred
Bit 7 (W) TH_DET — Interrupt clear for status of the thermistor detected — 0 : Not reset / 1 : Reset

Bit 6 (R) : TH_RMV — Interrupt status of the thermistor removal — 0 : No event / 1 : Event occurred
Bit 6 (W) TH_RMV — Interrupt clear for status of the thermistor removal — 0 : Not reset / 1 : Reset

Bit 5 (R) : BAT_DET — Interrupt status of the battery detected — 0 : No event / 1 : Event occurred
Bit 5 (W) BAT_DET — Interrupt clear for status of the battery detected — 0 : Not reset / 1 : Reset

Bit 4 (R) : BAT_RMV — Interrupt status of the battery removed — 0 : No event / 1 : Event occurred
Bit 4 (W) BAT_RMV — Interrupt clear for status of the battery removed — 0 : Not reset / 1 : Reset

Bit 1 (R) : TMP_OUT_DET — Interrupt status of the temperature out of the charging range — 0 : No event / 1 : Event occurred
Bit 1 (W) TMP_OUT_DET — Interrupt clear for status of the temperature out of the charging range — 0 : Not reset / 1 : Reset

Bit 0 (R) : TMP_OUT_RES — Interrupt status of the temperature in to the charging range — 0 : No event / 1 : Event occurred
Bit 0 (W) TMP_OUT_RES — Interrupt clear for status of the temperature in to the charging range — 0 : Not reset / 1 : Reset

Address 9Bh: INT_STAT_07 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Bh	INT_STAT_07	R/WC	VBAT_OV_DET	VBAT_OV_RES	VBAT_LO_DET	VBAT_LO_RES	VBAT_SHT_DET	VBAT_SHT_RES	DBAT_DET	-
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 (R) : VBAT_OV_DET — Interrupt status of VBAT over-voltage detected — 0 : No event / 1 : Event occurred
Bit 7 (W) VBAT_OV_DET — Interrupt clear for status of VBAT over-voltage detected — 0 : Not reset / 1 : Reset

Bit 6 (R) : VBAT_OV_RES — Interrupt status of VBAT over-voltage resumed — 0 : No event / 1 : Event occurred
Bit 6 (W) VBAT_OV_RES — Interrupt clear for status of VBAT over-voltage resumed — 0 : Not reset / 1 : Reset

Bit 5 (R) : VBAT_LO_DET — Interrupt status of VBAT low-voltage detected — 0 : No event / 1 : Event occurred
Bit 5 (W) VBAT_LO_DET — Interrupt clear for status of VBAT low-voltage detected — 0 : Not reset / 1 : Reset

Bit 4 (R) : VBAT_LO_RES — Interrupt status of VBAT low-voltage resumed — 0 : No event / 1 : Event occurred
Bit 4 (W) VBAT_LO_RES — Interrupt clear for status of VBAT low-voltage resumed — 0 : Not reset / 1 : Reset

Bit 3 (R) : VBAT_SHT_DET — Interrupt status of VBAT short-circuit detected — 0 : No event / 1 : Event occurred
Bit 3 (W) VBAT_SHT_DET — Interrupt clear for status of VBAT short-circuit detected — 0 : Not reset / 1 : Reset

Bit 2 (R) : VBAT_SHT_RES — Interrupt status of VBAT short-circuit resumed — 0 : No event / 1 : Event occurred
Bit 2 (W) VBAT_SHT_RES — Interrupt clear for status of VBAT short-circuit resumed — 0 : Not reset / 1 : Reset

Bit 1 (R) : DBAT_DET — Interrupt status of Dead-Battery detected — 0 : No event / 1 : Event occurred
Bit 1 (W) DBAT_DET — Interrupt clear for status of Dead-Battery detected — 0 : Not reset / 1 : Reset

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Address 9Ch: INT_STAT_08 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Ch	INT_STAT_08	R/WC	-	-	-	-	-	-	VBAT_MON_DET	VBAT_MON_RES
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 1 (R) : VBAT_MON_DET Interrupt status of VBAT monitor detected 0 : No event / 1 : Event occurred
Bit 1 (W) VBAT_MON_DET Interrupt clear for status of VBAT monitor detected 0 : Not reset / 1 : Reset

Bit 0 (R) : VBAT_MON_RES Interrupt status of VBAT monitor resumed 0 : No event / 1 : Event occurred
Bit 0 (W) VBAT_MON_RES Interrupt clear for status of VBAT monitor resumed 0 : Not reset / 1 : Reset

Address 9Dh: INT_STAT_09 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Dh	INT_STAT_09	R/WC	-	-	-	-	-	CC8TH_DET	CC4TH_DET	CC2ND_DET
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 2 (R) : CC8TH_DET Interrupt status of under 1/8 capacity discharging 0 : No event / 1 : Event occurred
Bit 2 (W) CC8TH_DET Interrupt clear for status of under 1/8 capacity discharging 0 : Not reset / 1 : Reset

Bit 1 (R) : CC4TH_DET Interrupt status of under 1/4 capacity discharging 0 : No event / 1 : Event occurred
Bit 1 (W) CC4TH_DET Interrupt clear for status of under 1/4 capacity discharging 0 : Not reset / 1 : Reset

Bit 0 (R) : CC2ND_DET Interrupt status of under 1/2 capacity discharging 0 : No event / 1 : Event occurred
Bit 0 (W) CC2ND_DET Interrupt clear for status of under 1/2 capacity discharging 0 : Not reset / 1 : Reset

Address 9Eh: INT_STAT_10 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Eh	INT_STAT_10	R/WC	-	-	OCUR3_DET	OCUR3_RES	OCUR2_DET	OCUR2_RES	OCUR1_DET	OCUR1_RES
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 5 (R) : OCUR3_DET Interrupt status of Battery over-current 3 detected 0 : No event / 1 : Event occurred
Bit 5 (W) OCUR3_DET Interrupt clear for status of Battery over-current 3 detected 0 : Not reset / 1 : Reset

Bit 4 (R) : OCUR3_RES Interrupt status of Battery over-current 3 resumed 0 : No event / 1 : Event occurred
Bit 4 (W) OCUR3_RES Interrupt clear for status of Battery over-current 3 resumed 0 : Not reset / 1 : Reset

Bit 3 (R) : OCUR2_DET Interrupt status of Battery over-current 2 detected 0 : No event / 1 : Event occurred
Bit 3 (W) OCUR2_DET Interrupt clear for status of Battery over-current 2 detected 0 : Not reset / 1 : Reset

Bit 2 (R) : OCUR2_RES Interrupt status of Battery over-current 2 resumed 0 : No event / 1 : Event occurred
Bit 2 (W) OCUR2_RES Interrupt clear for status of Battery over-current 2 resumed 0 : Not reset / 1 : Reset

Bit 1 (R) : OCUR1_DET Interrupt status of Battery over-current 1 detected 0 : No event / 1 : Event occurred
Bit 1 (W) OCUR1_DET Interrupt clear for status of Battery over-current 1 detected 0 : Not reset / 1 : Reset

Bit 0 (R) : OCUR1_RES Interrupt status of Battery over-current 1 resumed 0 : No event / 1 : Event occurred
Bit 0 (W) OCUR1_RES Interrupt clear for status of Battery over-current 1 resumed 0 : Not reset / 1 : Reset

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Address 9Fh: INT_STAT_11 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Fh	INT_STAT_11	R/WC	VF_DET	VF_RES	VF125_DET	VF125_RES	OVTMP_DET	OVTMP_RES	LOTMP_DET	LOTMP_RES
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 7 (R) : VF_DET — Interrupt status of Thermal Regulation detected — 0 : No event / 1 : Event occurred
Bit 7 (W) VF_DET — Interrupt clear for status of Thermal Regulation detected — 0 : Not reset / 1 : Reset

Bit 6 (R) : VF_RES — Interrupt status of Thermal Regulation resumed — 0 : No event / 1 : Event occurred
Bit 6 (W) VF_RES — Interrupt clear for status of Thermal Regulation resumed — 0 : Not reset / 1 : Reset

Bit 6 (R) : VF125_DET — Interrupt status of Thermal Regulation at 125℃ resumed — 0 : No event / 1 : Event occurred
Bit 6 (W) VF125_DET — Interrupt clear for status of Thermal Regulation at 125℃ resumed — 0 : Not reset / 1 : Reset

Bit 6 (R) : VF125_RES — Interrupt status of Thermal Regulation at 125℃ resumed — 0 : No event / 1 : Event occurred
Bit 6 (W) VF125_RES — Interrupt clear for status of Thermal Regulation at 125℃ resumed — 0 : Not reset / 1 : Reset

Bit 3 (R) : OVTMP_DET — Interrupt status of the battery over-temperature detected — 0 : No event / 1 : Event occurred
Bit 3 (W) OVTMP_DET — Interrupt clear for status of the battery over-temperature detected — 0 : Not reset / 1 : Reset

Bit 2 (R) : OVTMP_RES — Interrupt status of the battery over-temperature resumed — 0 : No event / 1 : Event occurred
Bit 2 (W) OVTMP_RES — Interrupt clear for status of the battery over-temperature resumed — 0 : Not reset / 1 : Reset

Bit 1 (R) : LOTMP_DET — Interrupt status of the battery low-temperature detected — 0 : No event / 1 : Event occurred
Bit 1 (W) LOTMP_DET — Interrupt clear for status of the battery low-temperature detected — 0 : Not reset / 1 : Reset

Bit 0 (R) : LOTMP_RES — Interrupt status of the battery low-temperature resumed — 0 : No event / 1 : Event occurred
Bit 0 (W) LOTMP_RES — Interrupt clear for status of the battery low-temperature resumed — 0 : Not reset / 1 : Reset

Address A0h: INT_STAT_12 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A0h	INT_STAT_12	R/WC	-	-	-	-	-	ALM2	ALM1	ALM0
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 2 (R) : ALM2 — Interrupt status of the Alarm2 resumed — 0 : No event / 1 : Event occurred
Bit 2 (W) ALM2 — Interrupt clear for status of the Alarm2 resumed — 0 : Not reset / 1 : Reset

Bit 1 (R) : ALM1 — Interrupt status of the Alarm1 resumed — 0 : No event / 1 : Event occurred
Bit 1 (W) ALM1 — Interrupt clear for status of the Alarm1 resumed — 0 : Not reset / 1 : Reset

Bit 0 (R) : ALM0 — Interrupt status of the Alarm0 resumed — 0 : No event / 1 : Event occurred
Bit 0 (W) ALM0 — Interrupt clear for status of the Alarm0 resumed — 0 : Not reset / 1 : Reset

Address A1h: INT_UPDATE Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A1h	INT_UPDATE	R/WC	-	-	-	-	-	-	-	INT_UPDATE
	Initial Value (Master mode)	00h	0	0	0	0	0	0	0	0
	Initial Value (Slave mode)	00h	0	0	0	0	0	0	0	0

Bit 0 : INT_UPDATE — The present interruption status is updated.
0 : Interruption is not updated.
1 : Interruption is updated.

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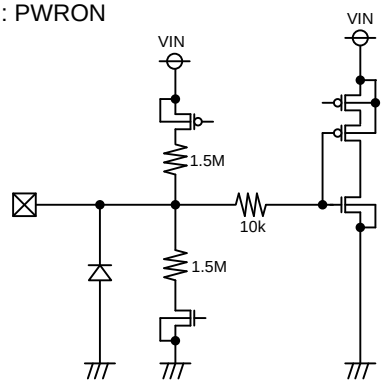
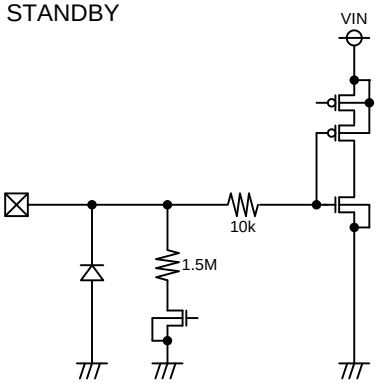
I/O Equivalent Circuits

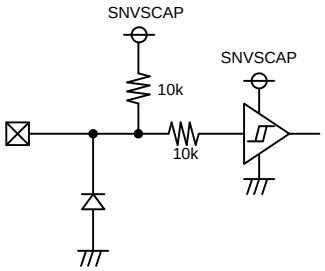
A : PWRON



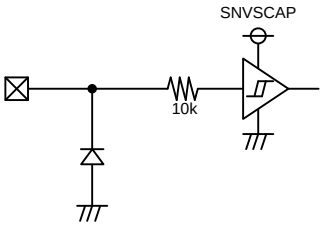
B : STANDBY



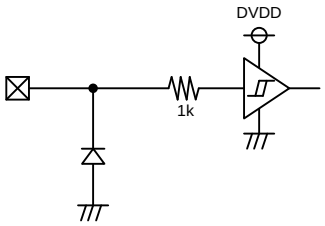
C : RESETINB



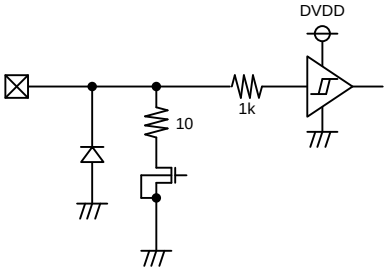
D : MSSEL



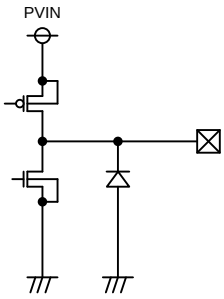
E : SCL



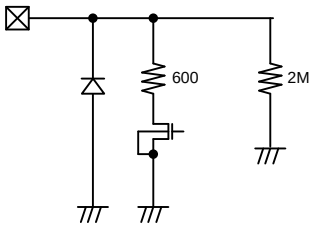
F : SDA



G : LX1, LX2, LX3, LX4



H : FB1, FB2, FB3, FB4



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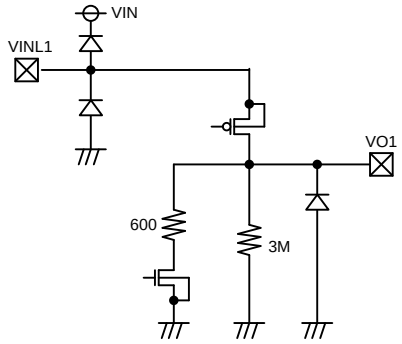
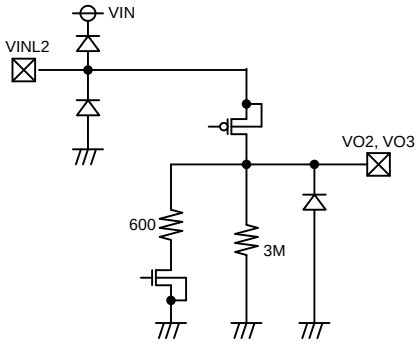
I/O Equivalent Circuits - continued

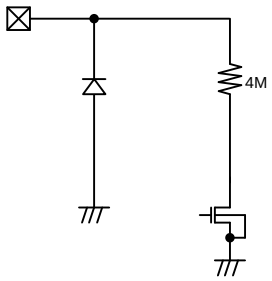
I : VINL1, VO1



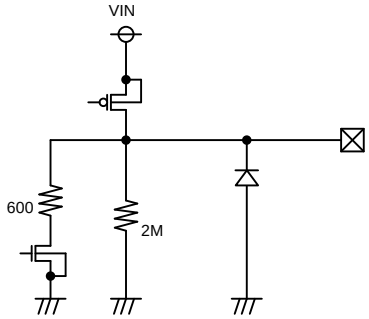
J : VINL2, VO2, VO3



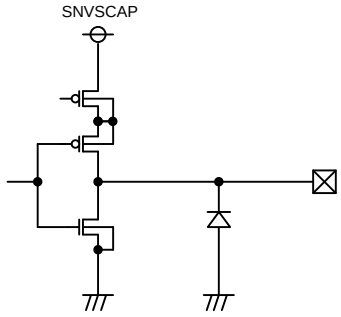
K : DVREFIN



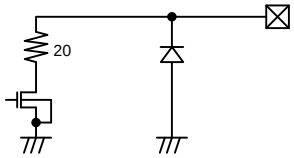
L : VODVREF



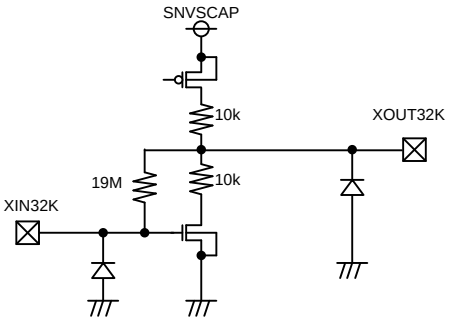
M : GPO1,2,3, CLK32KOUT



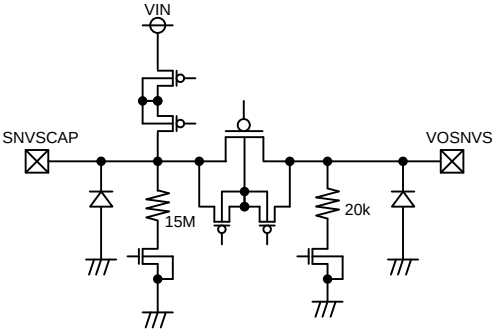
N : POR, INTB, CHGLED



O : XIN32K, XOUT32K



P : SNVSCAP, VOSNVS



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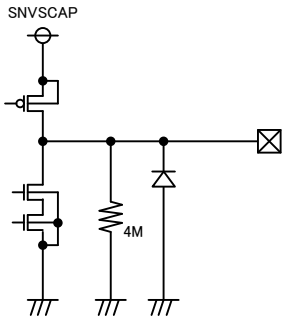
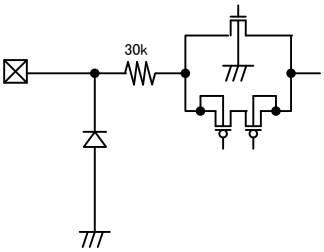
I/O Equivalent Circuits - continued

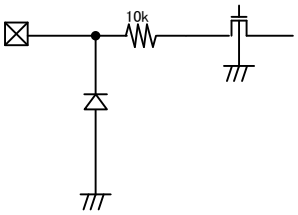
Q : CHGREF



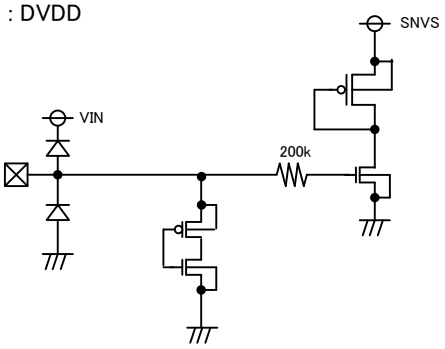
R : TS



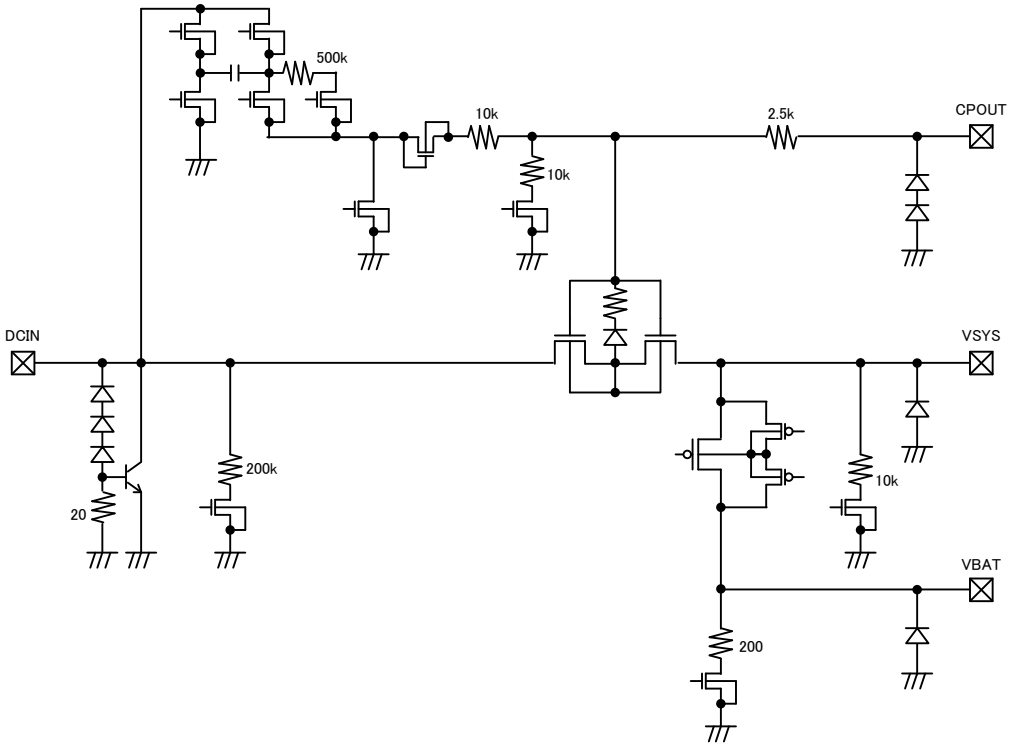
S : BATTP, BATTM



U : DVDD



T : DCIN, VSYS, VBAT, CPOUT



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Typical Performance Curves

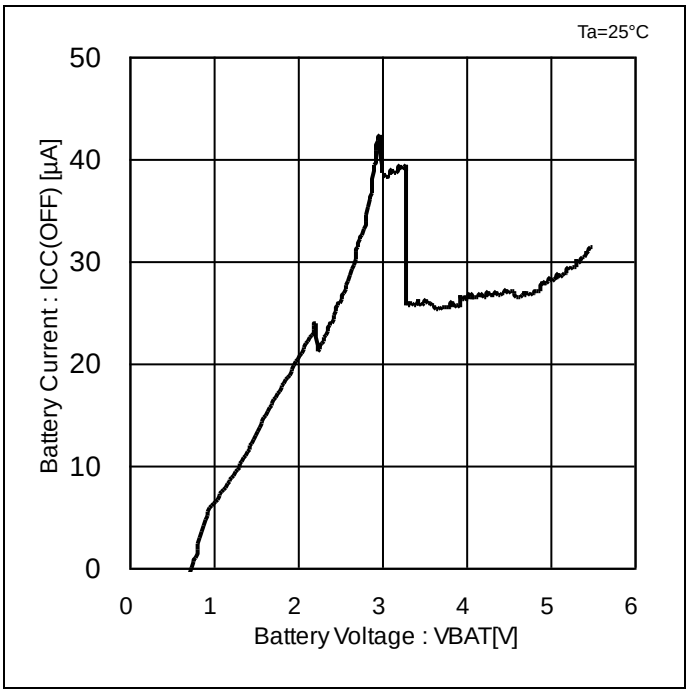

Figure 26. Battery Current vs Battery Voltage
(OFF Mode, Master Mode)

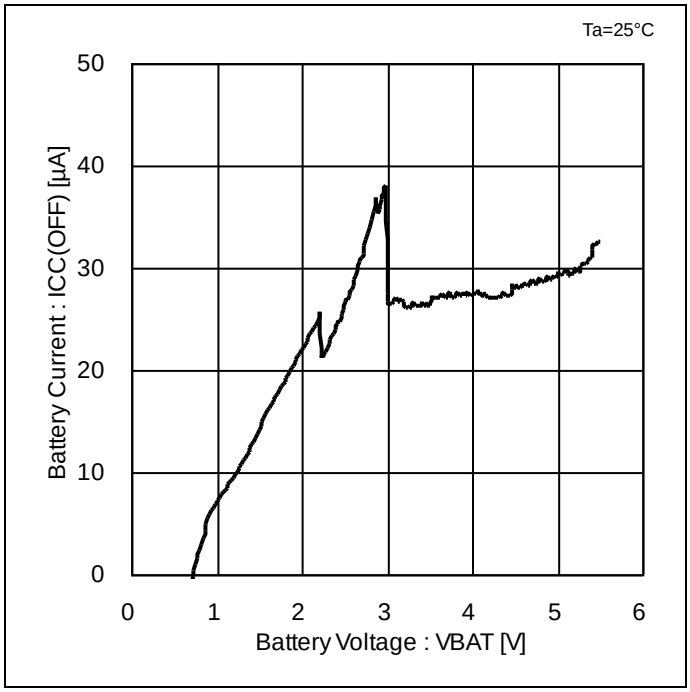

Figure 27. Battery Current vs Battery Voltage
(OFF Mode, Slave Mode)

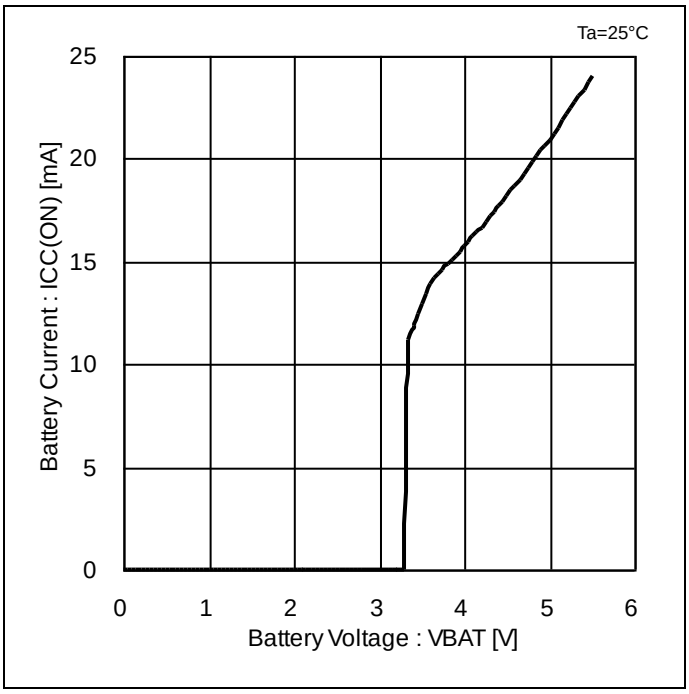

Figure 28. Battery Current vs Battery Voltage
(ON Mode, Master Mode)

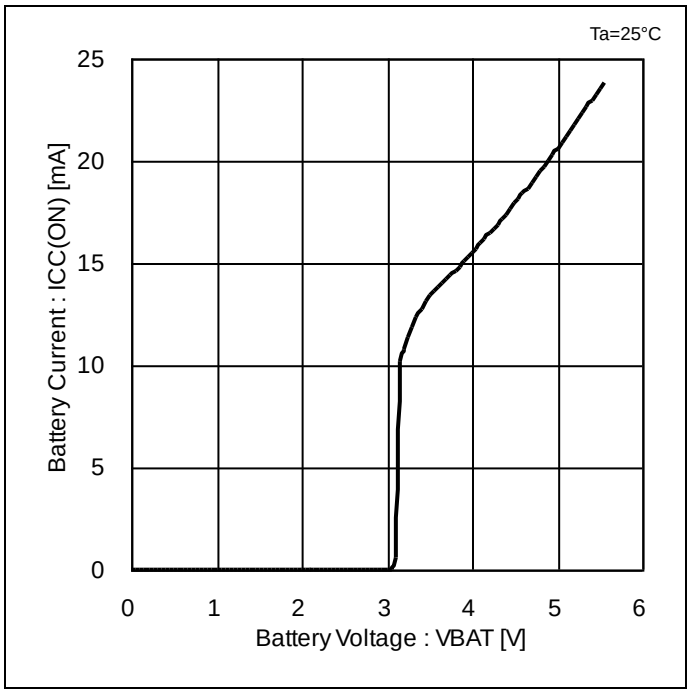

Figure 29. Battery Current vs Battery Voltage
(ON Mode, Slave Mode)

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Typical Performance Curves - continued

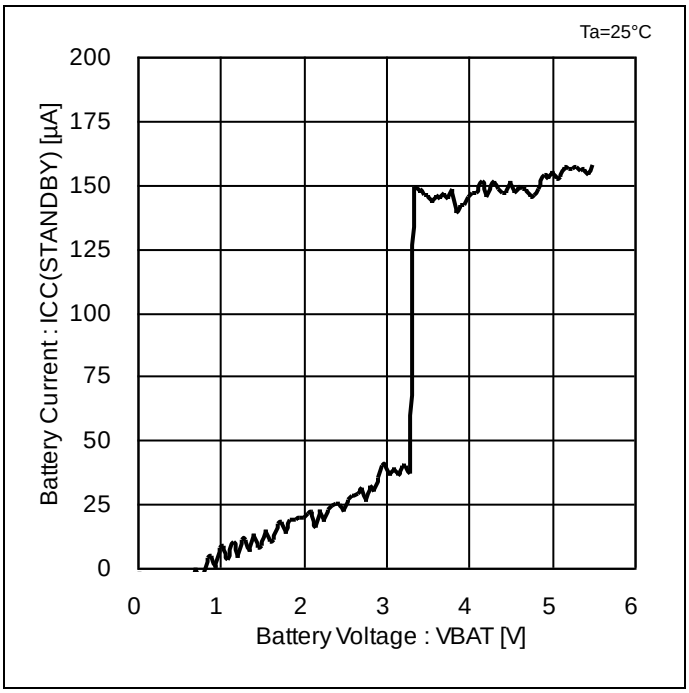

Figure 30. Battery Current vs Battery Voltage
(STANDBY Mode, Master Mode)

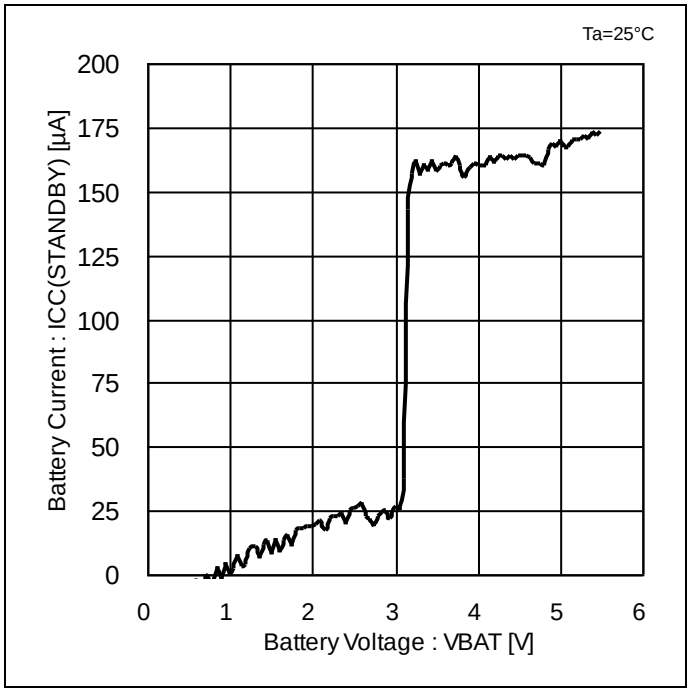

Figure 31. Battery Current vs Battery Voltage
(STANDBY Mode, Slave Mode)

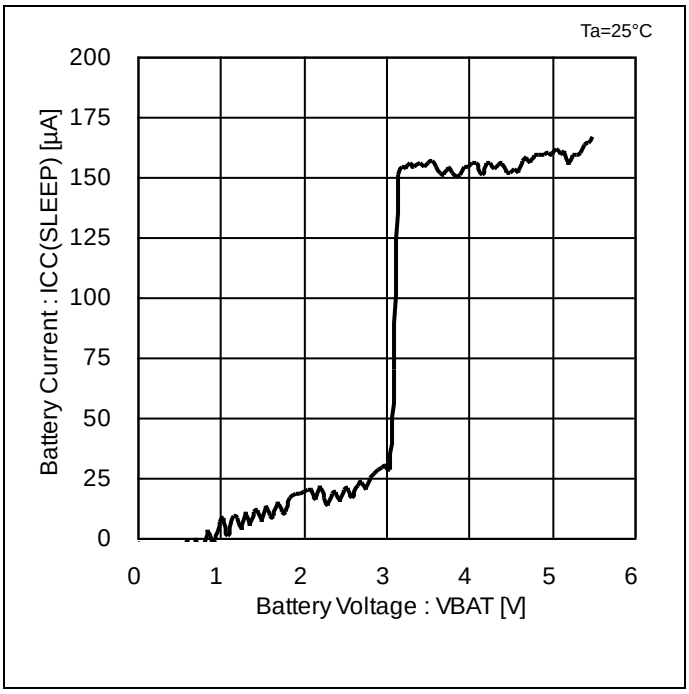

Figure 32. Battery Current vs Battery Voltage
(SLEEP Mode, Master Mode)

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Typical Performance Curves - continued

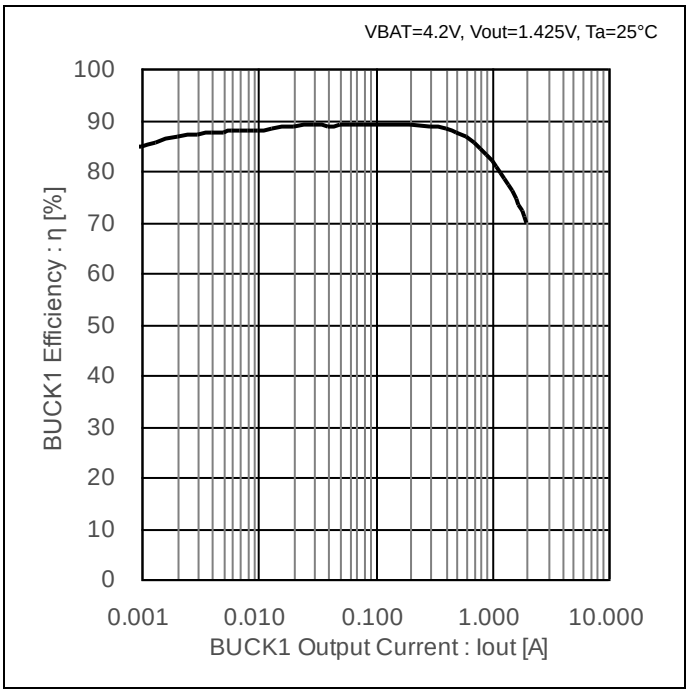

Figure 33. BUCK1 – Efficiency
(Auto Mode)

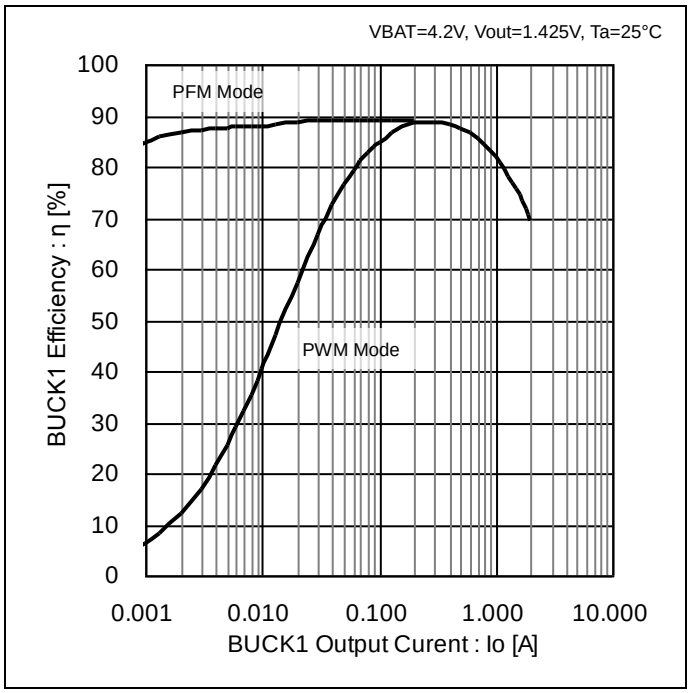

Figure 34. BUCK1 – Efficiency
(PWM Mode / PFM Mode)

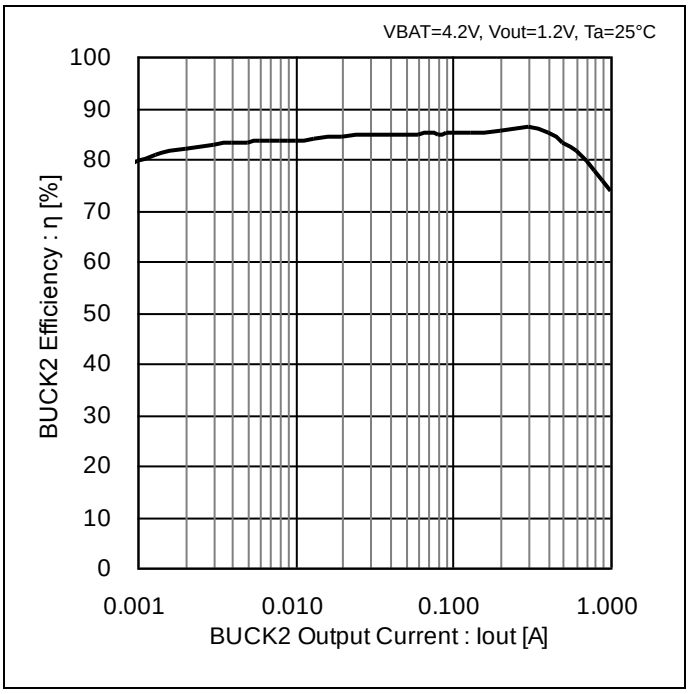

Figure 35. BUCK2 – Efficiency
(Auto Mode)

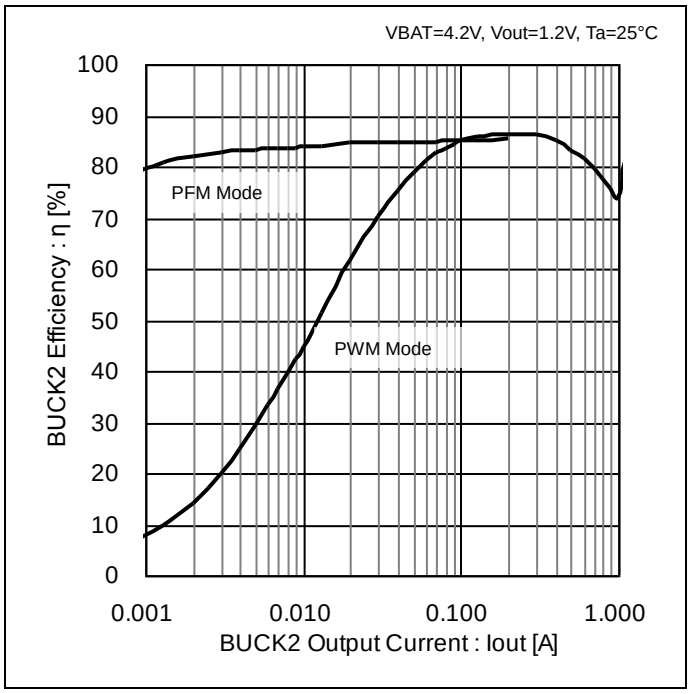

Figure 36. BUCK2 – Efficiency
(PWM Mode / PFM Mode)

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Typical Performance Curves - continued

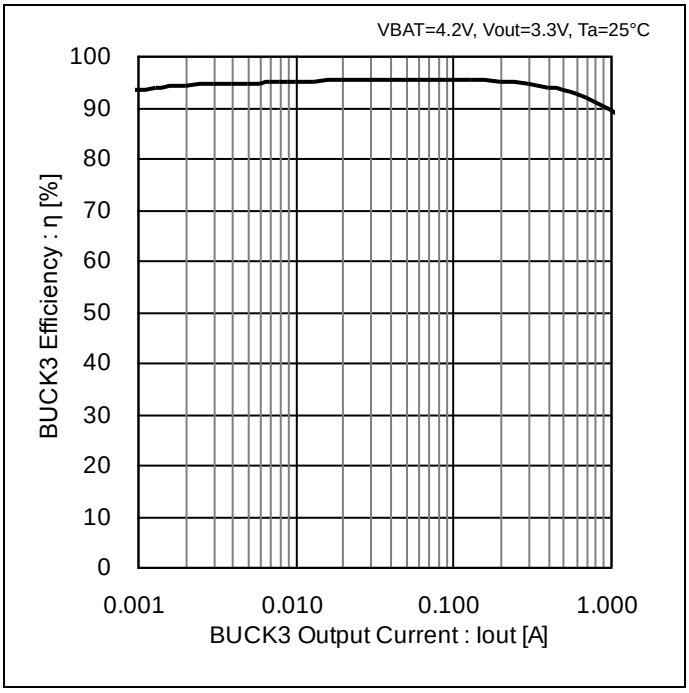

Figure 37. BUCK3 – Efficiency
(Auto Mode)

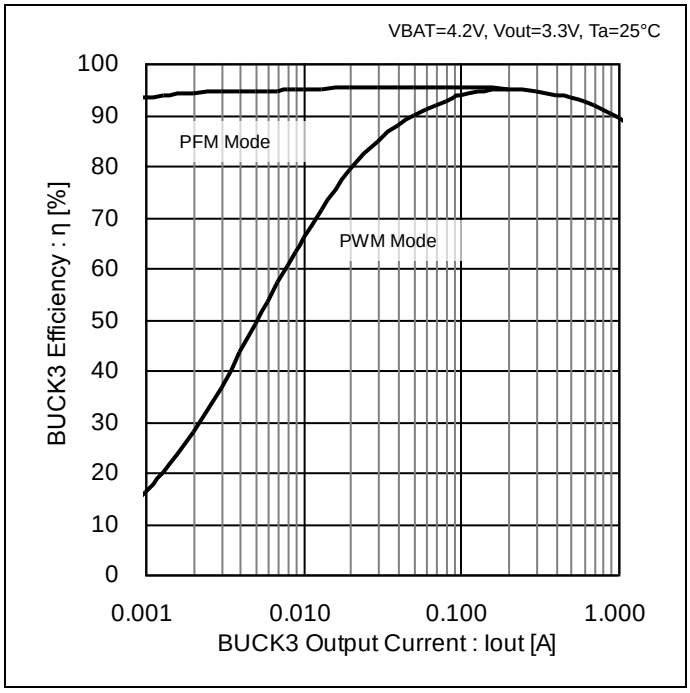

Figure 38. BUCK3 – Efficiency
(PWM Mode / PFM Mode)

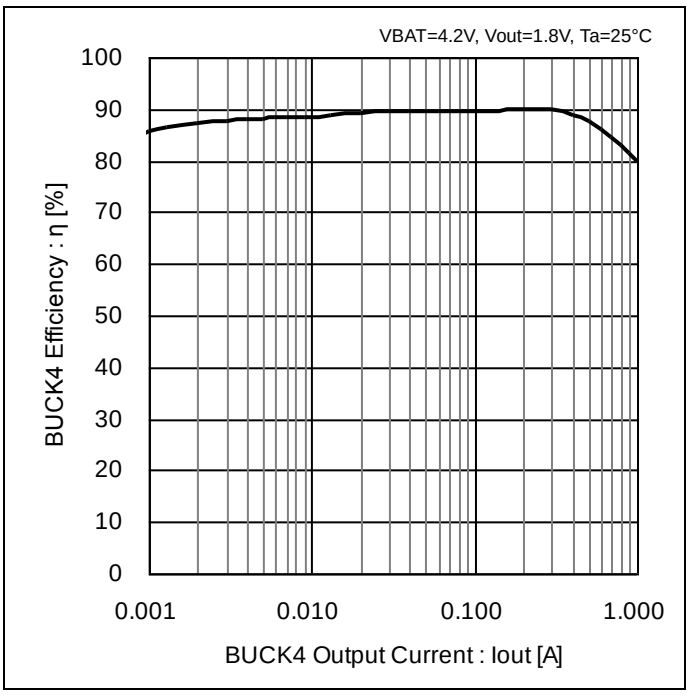

Figure 39. BUCK4 – Efficiency
(Auto Mode)

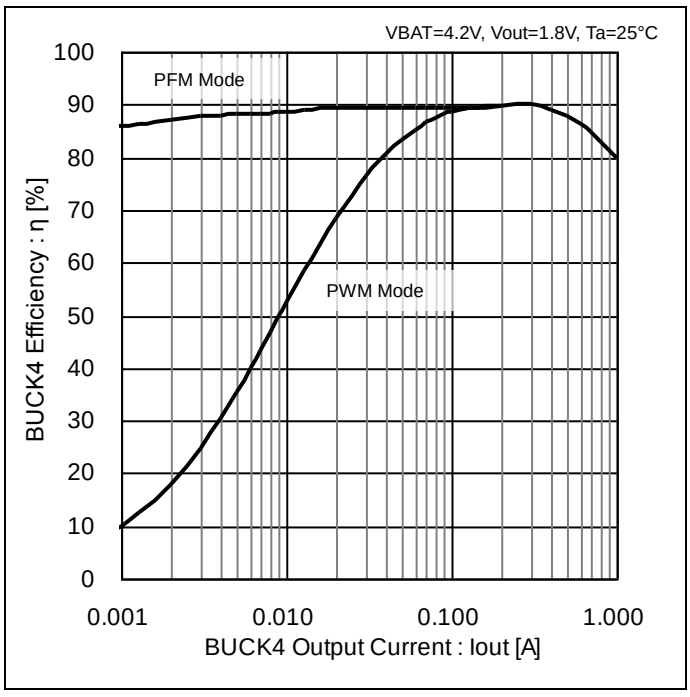

Figure 40. BUCK4 – Efficiency
(PWM Mode / PFM Mode)

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Typical Performance Curves - continued

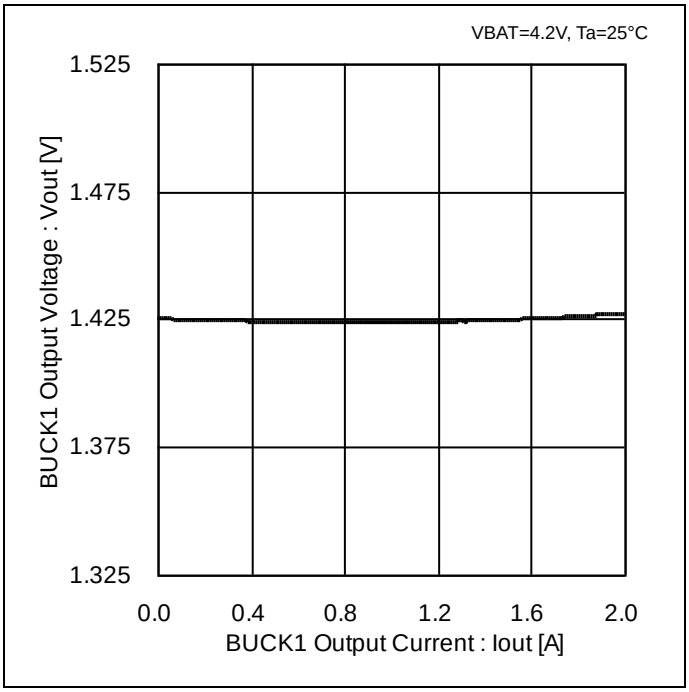

Figure 41. BUCK1 - Load Regulation (PWM mode)

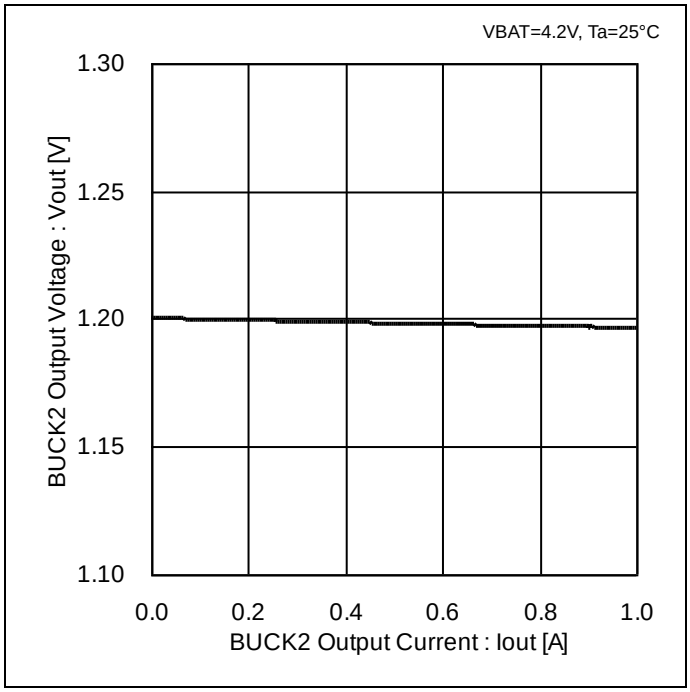

Figure 42. BUCK2 - Load Regulation (PWM mode)

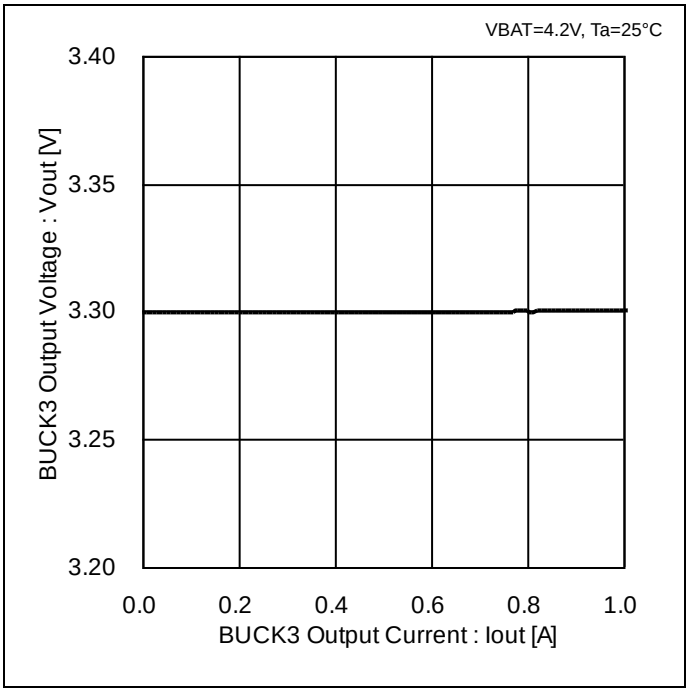

Figure 43. BUCK3 - Load Regulation (PWM mode)

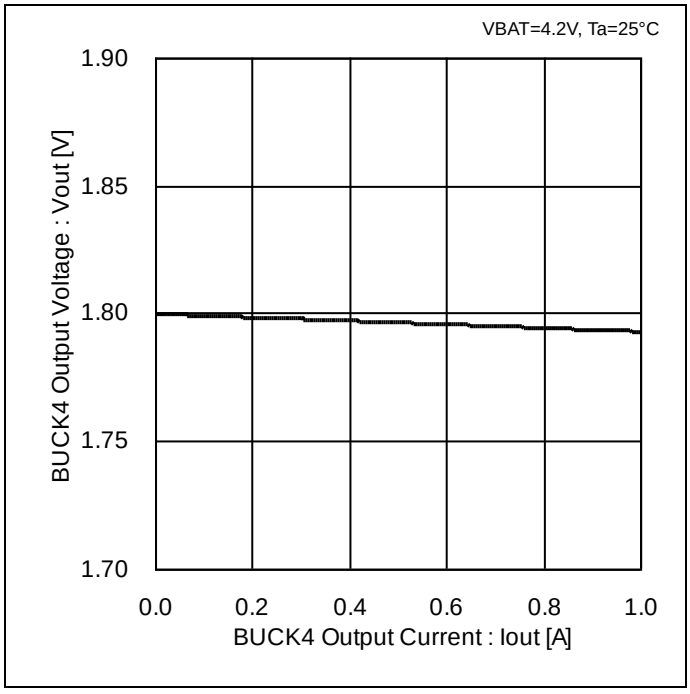

Figure 44. BUCK4 - Load Regulation (PWM mode)

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Typical Performance Curves - continued

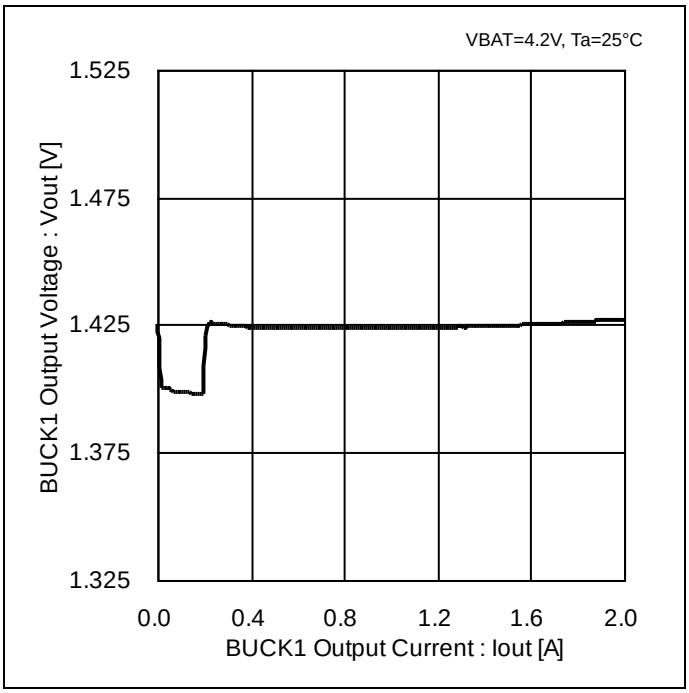

Figure 45. BUCK1 - Load Regulation (Auto Mode)

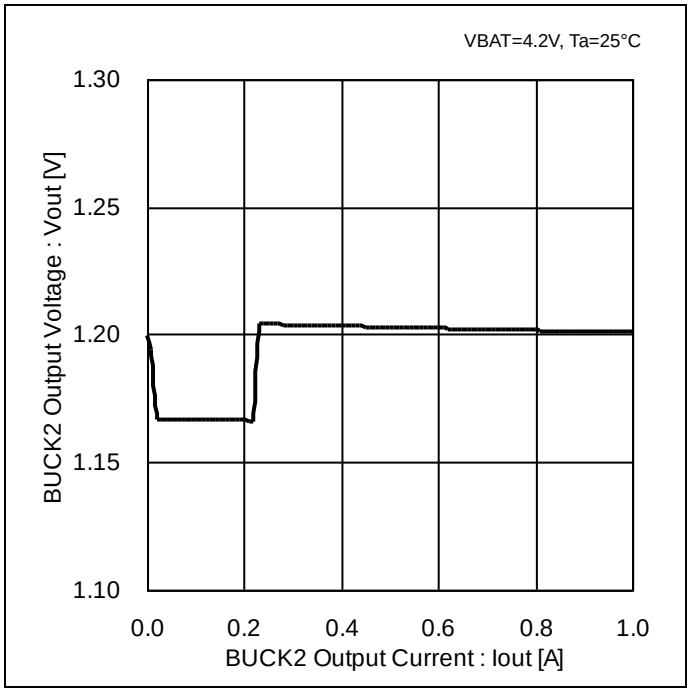

Figure 46. BUCK2 - Load Regulation (Auto Mode)

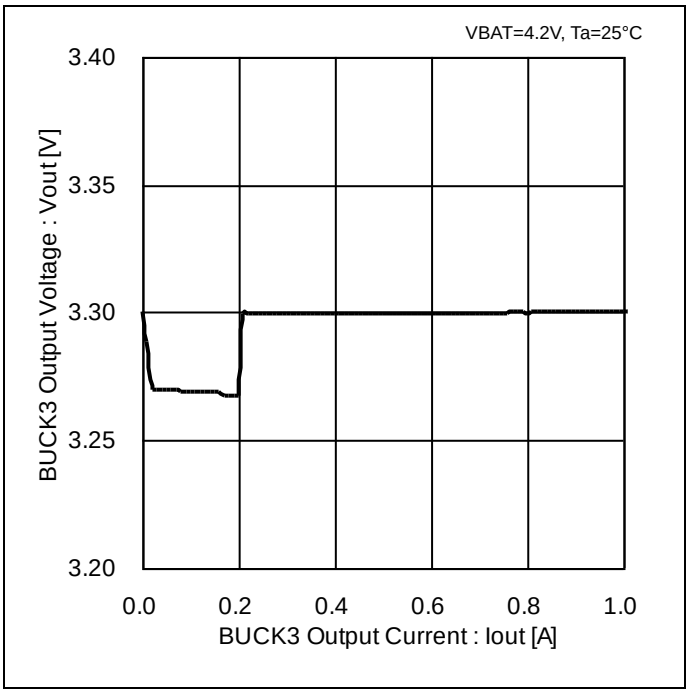

Figure 47. BUCK3 - Load Regulation (Auto Mode)

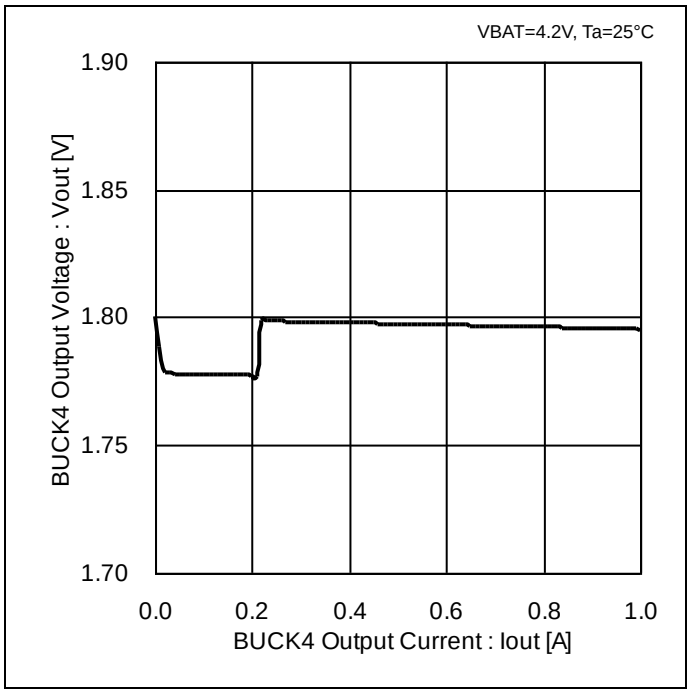

Figure 48. BUCK4 - Load Regulation (Auto Mode)

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Typical Performance Curves - continued

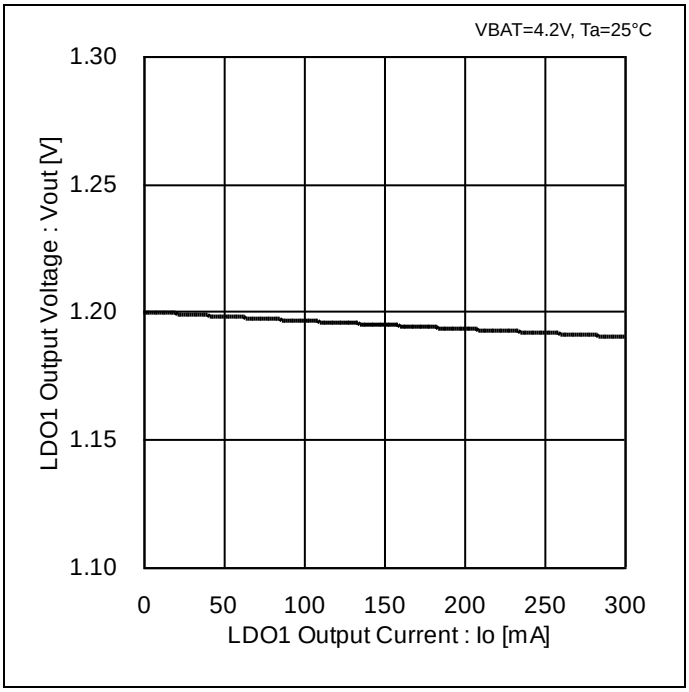

Figure 49. LDO1 - Load Regulation

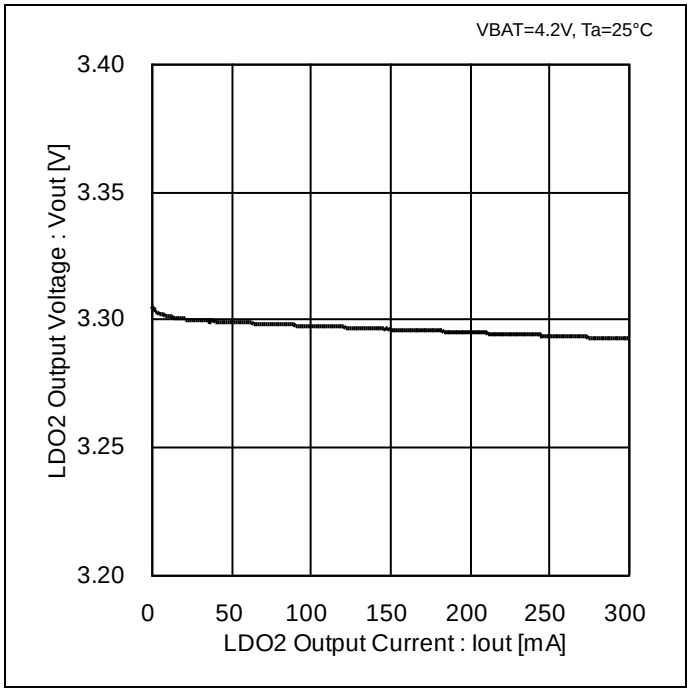

Figure 50. LDO2 - Load Regulation

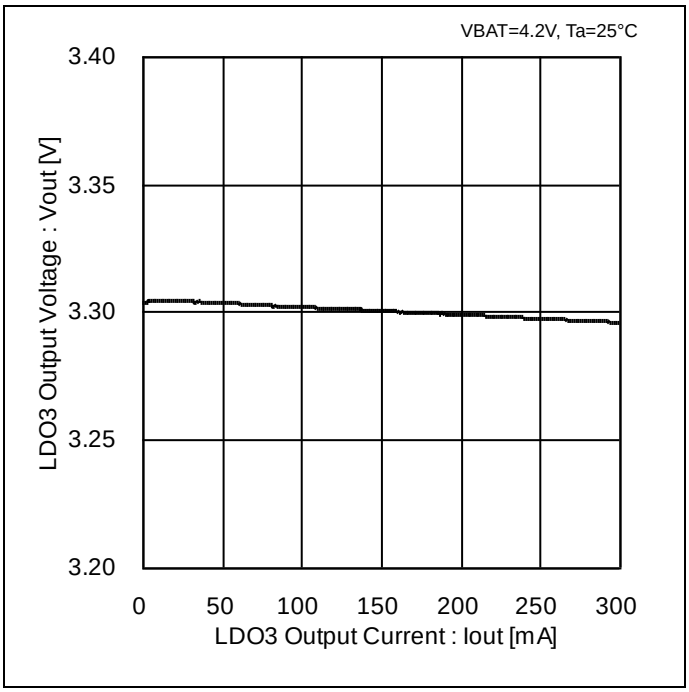

Figure 51. LDO3 - Load Regulation

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Typical Performance Curves - continued

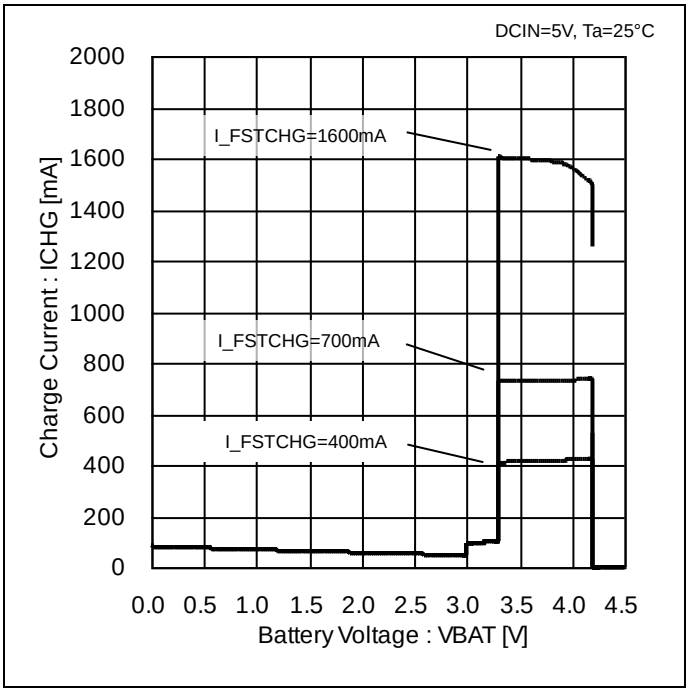

Figure 52. Charge Current vs Battery Voltage

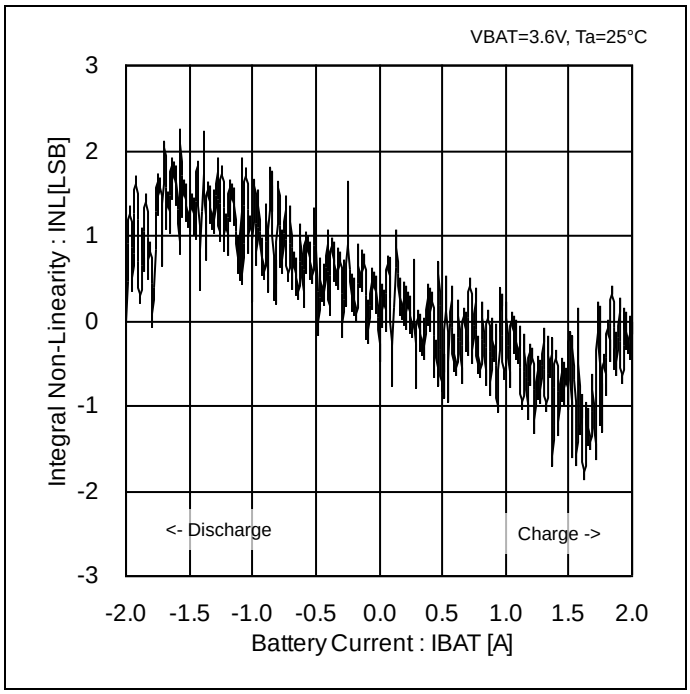

Figure 53. DSA-INL vs Input Voltage

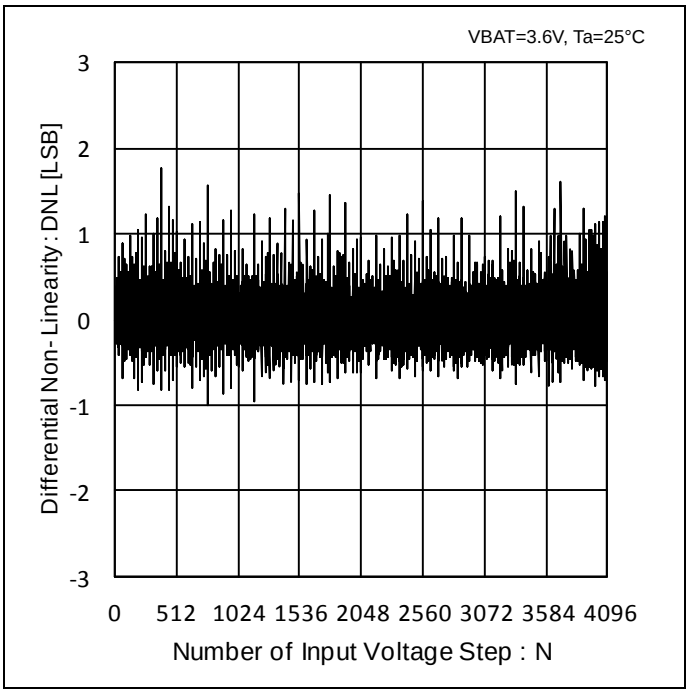

Figure 54. SAR-DNL vs Number of Input Voltage Step

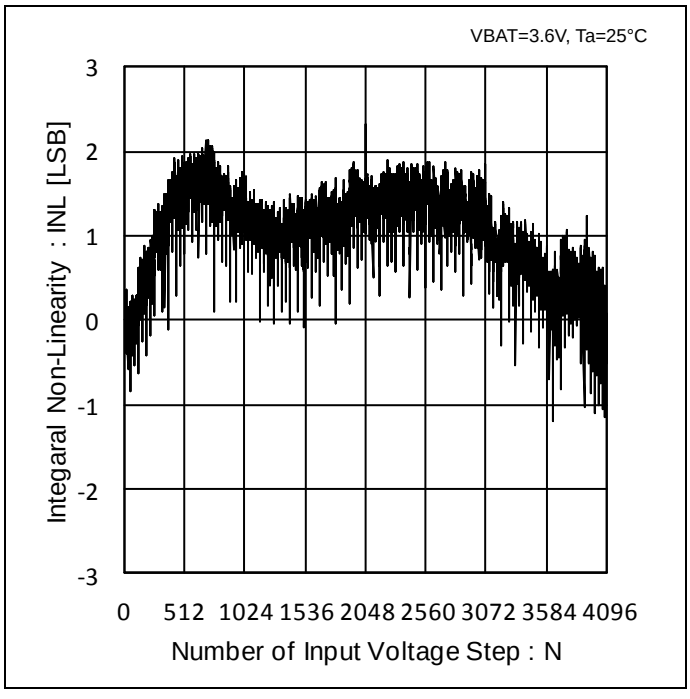

Figure 55. SAR-INL vs Number of Input Voltage Ste

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 74.2mm x 74.2mm x 1.6tmm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

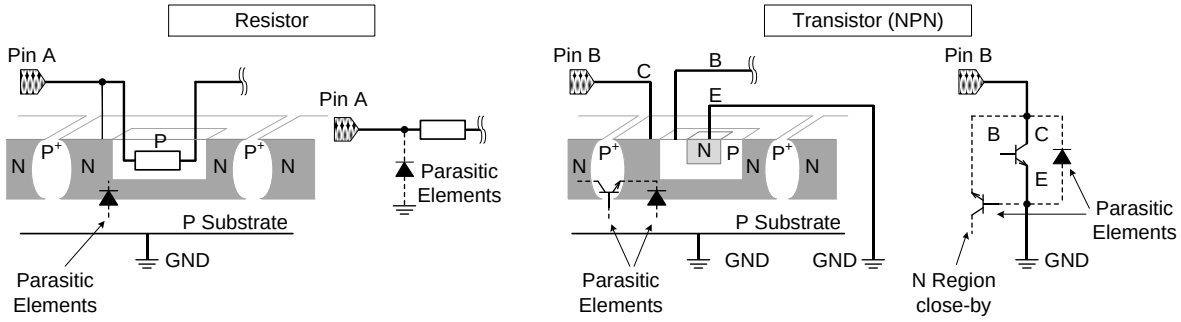

Figure 56. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated over-current protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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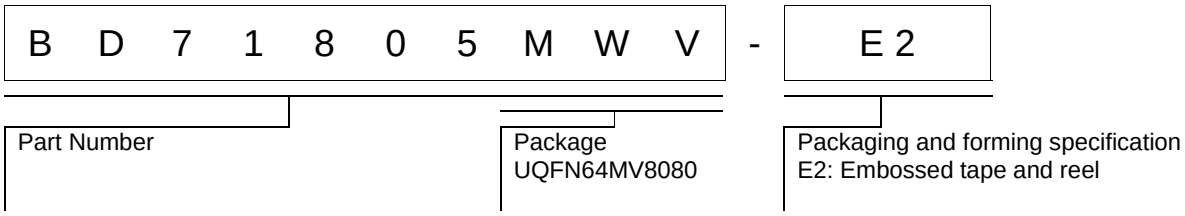
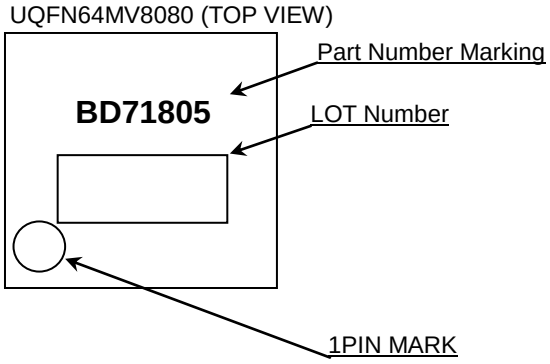
Ordering Information



Marking Diagram



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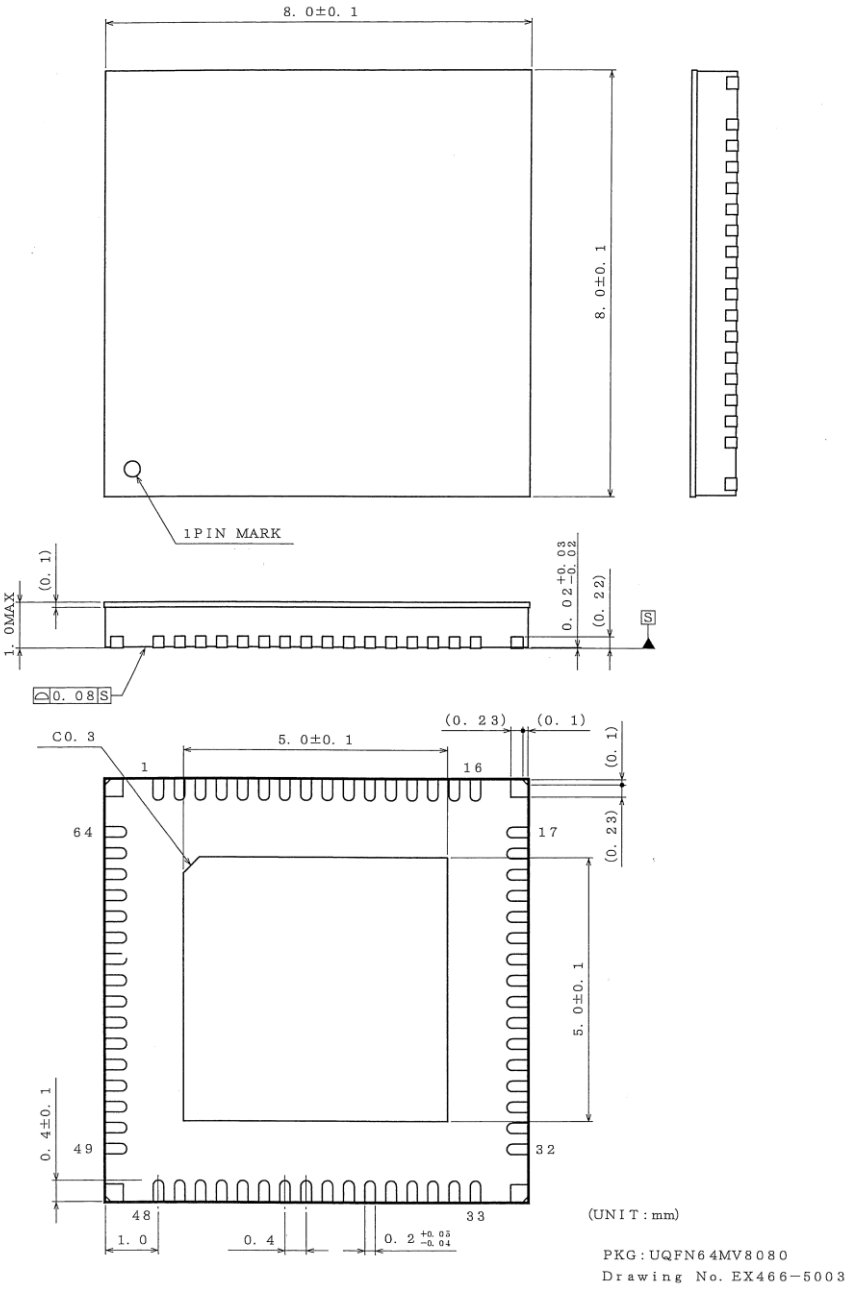
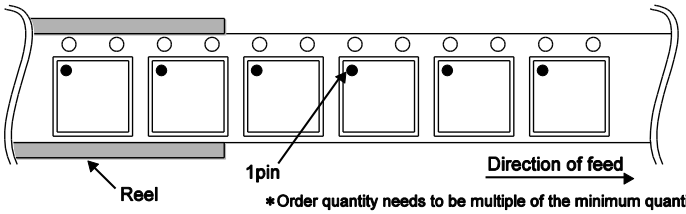
Physical Dimension, Tape and Reel Information

Package Name	UQFN64MV8080



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
27.Feb.2015	001	New Release

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Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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General Precaution

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BD71805MWV - Web Page

Part Number	BD71805MWV
Package	UQFN64MV8080
Unit Quantity	1000
Minimum Package Quantity	1000
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes