

SN74AUP1G240 Low-Power Single Inverter With 3-State Output

1 Features

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption
 - $I_{CC} = 0.9 \mu\text{A}$ Maximum
- Low Dynamic-Power Consumption
 - $C_{pd} = 4.2 \text{ pF}$ at 3.3 V Typical
- Low Input Capacitance
 - $C_i = 1.5 \text{ pF}$ Typical
- Low Noise – Overshoot and Undershoot <10% of V_{CC}
- Input-Disable Feature Allows Floating Input Conditions
- I_{off} Supports Partial Power-Down-Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4.7 \text{ ns}$ Maximum at 3.3 V
- Suitable for Point-to-Point Applications

2 Applications

- Grid infrastructure
- Telecom Infrastructure
- Medical, Healthcare, and Fitness
- Factory Automation and Control
- Printers and Other Peripherals

3 Description

The AUP family is TI's premier solution to the industry's low power needs in battery-powered portable applications. This family assures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see [AUP – The Lowest-Power Family](#)).

This buffer/driver is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high. This device has the input-disable feature, which allows floating input signals.

To assure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G240DBV	SOT-23 (5)	1.60 mm × 2.90 mm
SN74AUP1G240DCK	SC70 (5)	1.25 mm × 2.00 mm
SN74AUP1G240DRY	SON (6)	1.00 mm × 1.45 mm
SN74AUP1G240DSF	SON (6)	1.00 mm × 1.00 mm
SN74AUP1G240YFP	DSBGA (6)	0.76 mm × 1.16 mm
SN74AUP1G240YZP	DSBGA (5)	0.89 mm × 1.39 mm
SN74AUP1G240DPW	X2SON (5)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

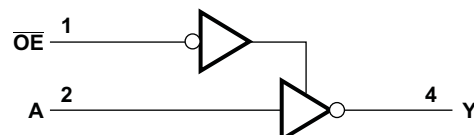


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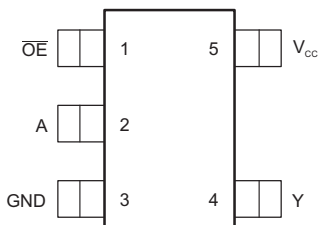
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2010) to Revision D	Page
• Added List of common applications	1
• Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Application and Implementation</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Deleted <i>Ordering Information</i> table, see <i>Mechanical, Packaging, and Orderable Information</i> at the end of the data sheet	1

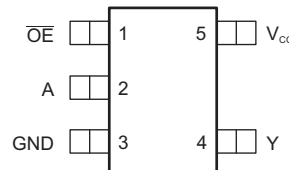
5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View

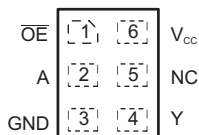


NC – No internal connection

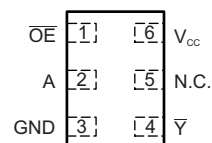
DCK Package
5-Pin SC70
Top View



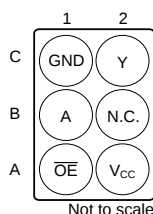
DRY Package
6-Pin SON
Top View



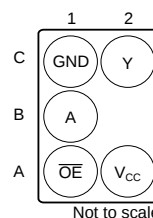
DSF Package
6-Pin SON
Top View



YFP Package
6-Pin DSBGA
Bottom View



YZP Package
5-Pin DSBGA
Bottom View



DPW Package⁽¹⁾
5-Pin (X2SON)
Top View



See mechanical drawings for dimensions.

Pin Functions

NAME	PIN						I/O	DESCRIPTION
	DBV, DCK	DRY	DSF	DPW	YFP	YZP		
A	2	2	2	2	B1	B1	I	A Input
GND	3	3	3	3	C1	C1	—	Ground
N.C.	—	5	5	—	B2	—	—	Do not connect
$\overline{OE}$	1	1	1	1	A1	A1	I	Active low output enable
V_{CC}	5	6	6	5	A2	A2	—	Positive Supply
Y	4	4	—	4	C2	C2	O	Y Output
$\overline{Y}$	—	—	4	—	—	—	O	Inverted Y Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	4.6	V
V _I	Input voltage ⁽²⁾		−0.5	4.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		−0.5	4.6	V
V _O	Output voltage range in the high or low state ⁽²⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50		mA
I _{OK}	Output clamp current	V _O < 0	−50		mA
I _O	Continuous output current		±20		mA
	Continuous current through V _{CC} or GND		±50		mA
T _j	Junction Temperature		150		°C
T _{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}	V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	1.6	
		V _{CC} = 3 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0	V
		V _{CC} = 1.1 V to 1.95 V	0	
		V _{CC} = 2.3 V to 2.7 V	0	
		V _{CC} = 3 V to 3.6 V	0	
V _O	Output voltage	Active state	0	V
		3-state	0	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V	200	ns/V
T _A	Operating free-air temperature	−40	85	°C

(1) The A data input pins may be floated if the $\overline{OE}$ is high and the outputs are disabled; otherwise, all unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AUP1G240							UNIT
	DBV (SOT-23)	DCK (SC70)	DRY (SON)	DSF (SON)	YFP (DSBGA)	YZP (DSBGA)	DPW (X2SON)	
	5 PINS	5 PINS	6 PINS	6 PINS	6 PINS	5 PINS	5 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	230.5	303.6	342.1	377.1	125.4	146.2	504.3	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	172.7	203.8	233.1	187.7	1.9	1.4	234.9	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	62.2	100.9	206.7	236.6	37.2	39.3	370.3	°C/W
Ψ_{JT} Junction-to-top characterization parameter	49.3	76.1	63.4	29.0	0.5	0.7	44.5	°C/W
Ψ_{JB} Junction-to-board characterization parameter	61.6	99.3	206.7	236.3	37.5	39.8	369.7	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	165.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = −20 μA	T _A = 25°C	0.8 V to 3.6 V	V _{CC} − 0.1		V	
		T _A = −40°C to +85°C		V _{CC} − 0.1			
	I _{OH} = −1.1 mA	T _A = 25°C	1.1 V	0.75 × V _{CC}			
		T _A = −40°C to +85°C		0.7 × V _{CC}			
	I _{OH} = −1.7 mA	T _A = 25°C	1.4 V	1.11			
		T _A = −40°C to +85°C		1.03			
	I _{OH} = −1.9 mA	T _A = 25°C	1.65 V	1.32			
		T _A = −40°C to +85°C		1.3			
	I _{OH} = −2.3 mA	T _A = 25°C	2.3 V	2.05			
		T _A = −40°C to +85°C		1.97			
	I _{OH} = −3.1 mA	T _A = 25°C		1.9			
		T _A = −40°C to +85°C		1.85			
	I _{OH} = −2.7 mA	T _A = 25°C	3 V	2.72			
		T _A = −40°C to +85°C		2.67			
	I _{OH} = −4 mA	T _A = 25°C		2.6			
		T _A = −40°C to +85°C		2.55			

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OL}	I _{OL} = 20 µA	T _A = 25°C	0.8 V to 3.6 V			0.1	V
		T _A = –40°C to +85°C				0.1	
	I _{OL} = 1.1 mA	T _A = 25°C	1.1 V			0.3 × V _{CC}	
		T _A = –40°C to +85°C				0.3 × V _{CC}	
	I _{OL} = 1.7 mA	T _A = 25°C	1.4 V			0.31	
		T _A = –40°C to +85°C				0.37	
	I _{OL} = 1.9 mA	T _A = 25°C	1.65 V			0.31	
		T _A = –40°C to +85°C				0.35	
	I _{OL} = 2.3 mA	T _A = 25°C	2.3 V			0.31	
		T _A = –40°C to +85°C				0.33	
	I _{OL} = 3.1 mA	T _A = 25°C				0.44	
		T _A = –40°C to +85°C				0.45	
	I _{OL} = 2.7 mA	T _A = 25°C	3 V			0.31	
		T _A = –40°C to +85°C				0.33	
	I _{OL} = 4 mA	T _A = 25°C				0.44	
		T _A = –40°C to +85°C				0.45	
I _I	A or $\overline{\text{OE}}$ input	V _I = GND to 3.6 V	0 V to 3.6 V			0.1	µA
		T _A = –40°C to +85°C				0.5	
I _{off}	V _I or V _O = 0 V to 3.6 V	T _A = 25°C	0 V			0.2	µA
		T _A = –40°C to +85°C				0.6	
ΔI _{off}	V _I or V _O = 0 V to 3.6 V	T _A = 25°C	0 V to 0.2 V			0.2	µA
		T _A = –40°C to +85°C				0.6	
I _{OZ}	V _O = V _{CC} or GND	T _A = 25°C	3.6 V			0.1	µA
		T _A = –40°C to +85°C				0.5	
I _{CC}	V _I = GND or (V _{CC} to 3.6 V), OE = GND, I _O = 0	T _A = 25°C	0.8 V to 3.6 V			0.5	µA
		T _A = –40°C to +85°C				0.9	
ΔI _{CC}	A input	T _A = 25°C	3.3 V			40	µA
		T _A = –40°C to +85°C				50	
	$\overline{\text{OE}}$ input	T _A = 25°C				110	
		T _A = –40°C to +85°C				120	
	All inputs	T _A = 25°C	0.8 V to 3.6 V			0	
		T _A = –40°C to +85°C				0	
C _I	V _I = V _{CC} or GND, T _A = 25°C		0 V		1.5		pF
			3.6 V		1.5		
C _O	V _O = V _{CC} or GND, T _A = 25°C		3.6 V		3		pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND

(2) To show I_{CC} is very low when $\overline{\text{OE}}$ is high and the inputs and outputs are disabled

6.6 Switching Characteristics: $C_L = 5 \text{ pF}$

over recommended operating free-air temperature range, $C_L = 5 \text{ pF}$ (unless otherwise noted) (see [Figure 2](#) and [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		17.1		ns
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	4.4	7.5	10.3	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.5		15.5	
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	3.3	5.4	6.9	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.3		10.3	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	2.6	4.4	5.8	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.8		8.3	
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$T_A = 25^\circ\text{C}$	1.9	3.3	4.3	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.3		5.8	
t_{en}	$\overline{OE}$	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		16.5		ns
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	4.5	8.1	13.4	
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	3		18.6	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	3.8	5.7	8.4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.8		12.2	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	3.1	4.5	6.3	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.3		9.7	
t_{dis}	$\overline{OE}$	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		9		ns
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.6	2.6	4.7	
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	2.2		8.4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	2	2.8	3.2	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.7		5.9	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	1.8	2.5	3.1	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.6		5.5	
t_{dis}	$\overline{OE}$	Y	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$T_A = 25^\circ\text{C}$	1.3	1.9	2.1	ns
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.1		4	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$T_A = 25^\circ\text{C}$	1.6	2.4	2.9	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.4		4.1	

6.7 Switching Characteristics: $C_L = 10 \text{ pF}$

over recommended operating free-air temperature range, $C_L = 10 \text{ pF}$ (unless otherwise noted) (see [Figure 2](#) and [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		19.5		ns
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	5.4	8.6	11.5	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	4.4		17.3	
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	4	6.2	7.7	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3		11.3	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	3.3	5.1	6.5	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.4		9.1	
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$T_A = 25^\circ\text{C}$	2.5	3.8	4.9	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.8		6.3	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$T_A = 25^\circ\text{C}$	2	3.2	4.1	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.5		5.2	
t_{en}	$\overline{OE}$	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		18.7		ns
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	5.1	8.9	14.4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.7		20.9	
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	4.3	6.3	9.1	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.3		13.7	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	3.6	5	6.8	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.8		10.9	
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$T_A = 25^\circ\text{C}$	2.8	3.7	4.6	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.2		7.7	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$T_A = 25^\circ\text{C}$	2.5	3.1	3.7	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.9		6.3	
t_{dis}	$\overline{OE}$	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		9.7		ns
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	4.1	5.3	6.6	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.9		12.9	
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	2.4	3.7	4.6	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.1		9.6	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	2.7	3.6	3.9	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.4		10.1	
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$T_A = 25^\circ\text{C}$	1.7	2.5	2.8	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.5		7.3	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$T_A = 25^\circ\text{C}$	2.5	3.2	3.8	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.2		9.1	

6.8 Switching Characteristics: $C_L = 15\text{ pF}$

over recommended operating free-air temperature range, $C_L = 15\text{ pF}$ (unless otherwise noted) (see [Figure 2](#) and [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	$V_{CC} = 0.8\text{ V}$	$T_A = 25^\circ\text{C}$		22.4		ns
			$V_{CC} = 1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	6.4	9.7	12.9	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	5.4		19.8	
			$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	4.8	7.1	8.7	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.8		13.3	
			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	3.9	5.8	7.2	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.1		10.8	
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	2.9	4.4	5.4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.3		7.6	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	2.4	3.6	4.5	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.9		6.1	
t_{en}	$\overline{OE}$	Y	$V_{CC} = 0.8\text{ V}$	$T_A = 25^\circ\text{C}$		23.3		ns
			$V_{CC} = 1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	6	10.1	15.8	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	4.6		22.9	
			$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	4.9	7	9.9	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.9		15	
			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	4	5.5	7.5	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.3		12.1	
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	3.2	4	4.9	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.6		8.6	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	2.8	3.4	4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.2		7	
t_{dis}	$\overline{OE}$	Y	$V_{CC} = 0.8\text{ V}$	$T_A = 25^\circ\text{C}$		11.1		ns
			$V_{CC} = 1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	4.1	5.3	5.8	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3		14	
			$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2.7	4	5.5	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.4		10.1	
			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	3.1	4.5	5.4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.9		10.9	
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	2.4	3	3.2	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.6		7.9	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	3.3	4.7	5.4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3		10	

6.9 Switching Characteristics: $C_L = 30 \text{ pF}$

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see [Figure 2](#) and [Figure 3](#))

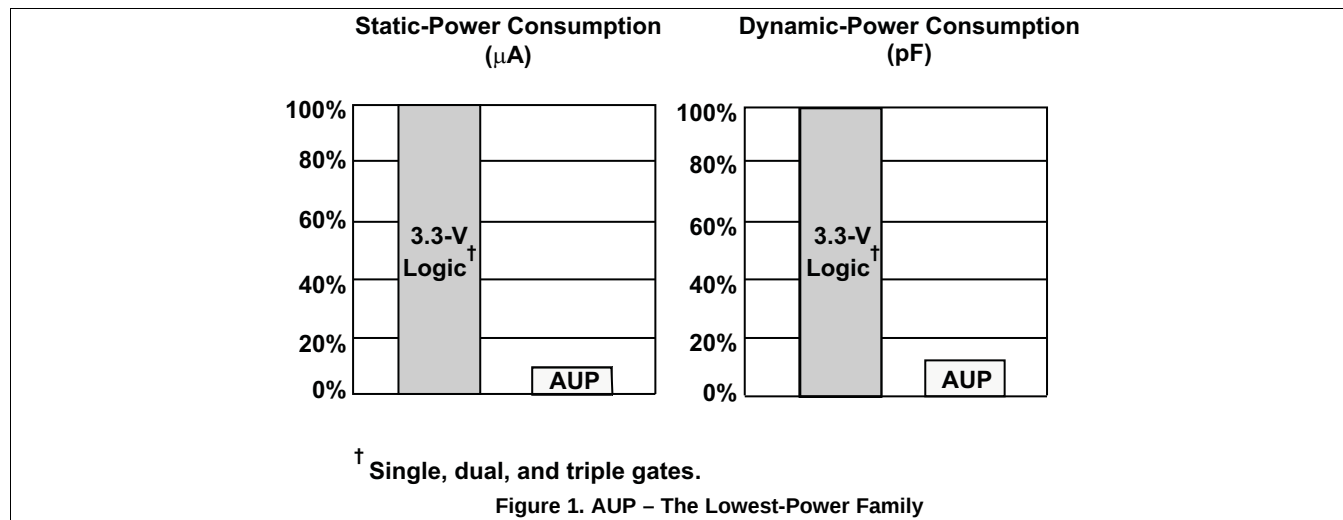
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		29		ns
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	8.9	12.6	16.1	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	7.3		25.7	
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	6.8	9.2	11	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	5.5		17.1	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	5.5	7.6	9.2	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	4.5		13.8	
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$T_A = 25^\circ\text{C}$	4.2	5.7	6.8	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.5		9.7	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$T_A = 25^\circ\text{C}$	3.5	4.7	5.7	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.3		7.8	
t_{en}	$\overline{OE}$	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		30.9		ns
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	8.2	12.6	18.5	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	6.8		27.4	
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	6.6	8.8	11.8	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	5.6		18	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	5.5	7.1	9.1	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	4.7		14.2	
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$T_A = 25^\circ\text{C}$	4.4	5.3	6.2	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	4.8		14.8	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$T_A = 25^\circ\text{C}$	3.9	4.5	5.1	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.8		10.2	
t_{dis}	$\overline{OE}$	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		14		ns
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	5	6.2	7.4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.1		8.2	
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	4.2	5.7	7.7	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.9		10.8	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	5.1	7.2	9	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	4.9		11.7	
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$T_A = 25^\circ\text{C}$	4.3	5.3	5.9	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	4.1		9.1	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$T_A = 25^\circ\text{C}$	7.4	8.3	9.4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	4.3		11.6	

6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

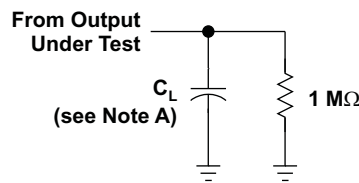
PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd} Power dissipation capacitance	Outputs enabled	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	3.9	
			1.5 V ± 0.1 V	3.9	
			1.8 V ± 0.15 V	3.9	
			2.5 V ± 0.2 V	4	
			3.3 V ± 0.3 V	4.2	
	Outputs disabled		0.8 V	0	
			1.2 V ± 0.1 V	0	
			1.5 V ± 0.1 V	0	
			1.8 V ± 0.15 V	0	
			2.5 V ± 0.2 V	0	
			3.3 V ± 0.3 V	0	

6.11 Typical Characteristics

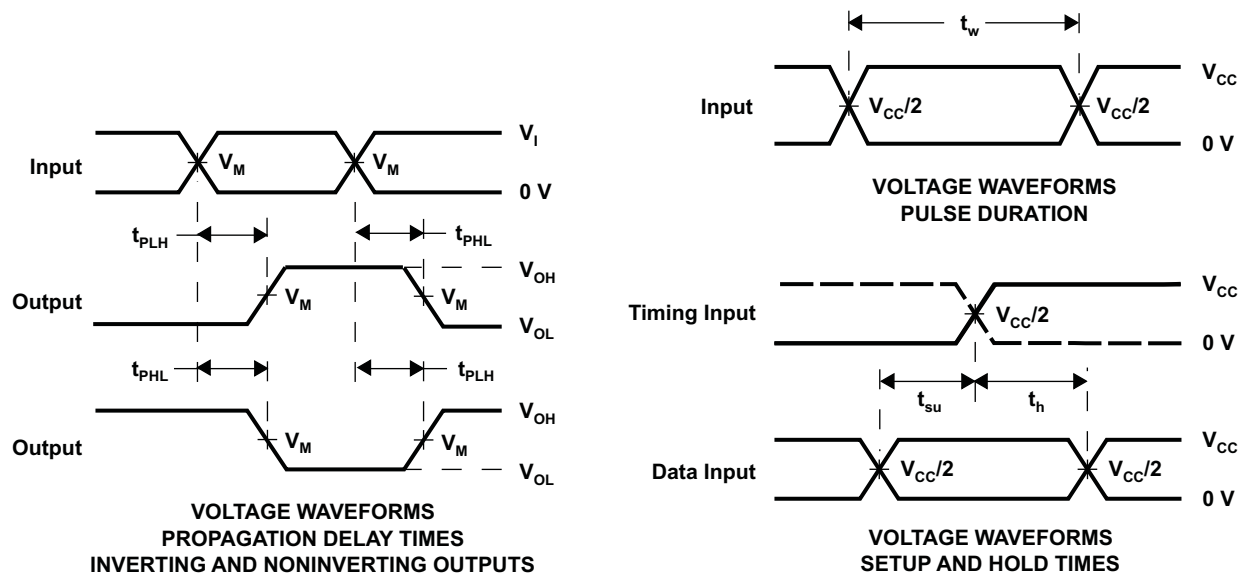


7 Parameter Measurement Information

7.1 Propagation Delays, Setup and Hold Times, and Pulse Width


LOAD CIRCUIT

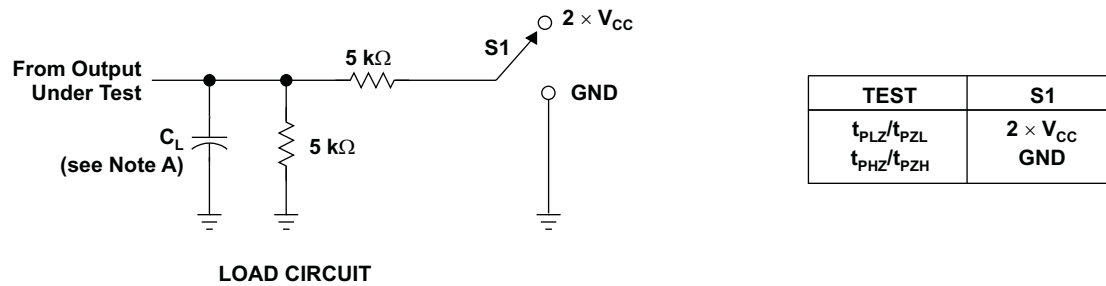
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



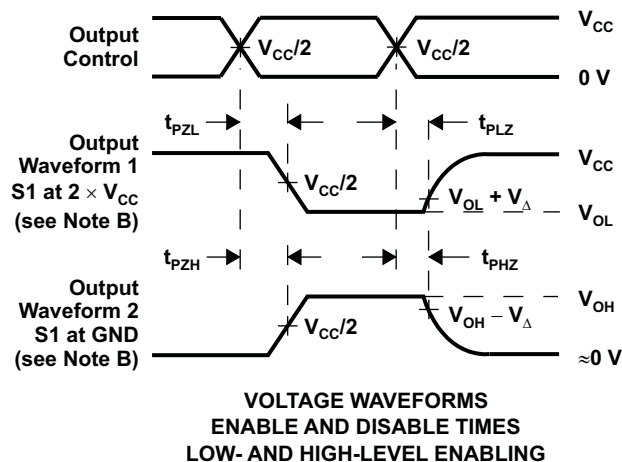
- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd} .
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

7.2 Enable and Disable Times



	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r/t_f = 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AUP1G240 device contains one inverter gate device with active low output enable control and performs the Boolean function $Y = \overline{A}$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device, which prevents damage to the device. To assure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram

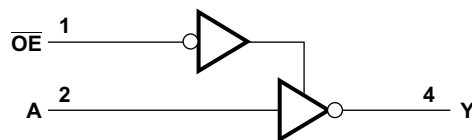


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced 3-State High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) table must be followed at all times.

3-State outputs can be put into a high-impedance mode, in which the device will neither source nor sink current.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#) table. The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#) table, and the maximum input leakage current, given in the [Electrical Characteristics](#) table, using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in the [Recommended Operating Conditions](#) table to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

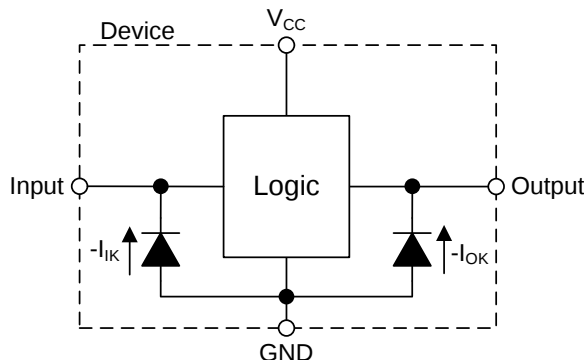


Figure 5. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Electrical Characteristics](#) table.

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Absolute Maximum Ratings](#) table.

8.4 Device Functional Modes

[Table 1](#) lists the functional modes of the SN74AUP1G240 device.

Table 1. Function Table

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	L
L	L	H
H	X ⁽¹⁾	Z

(1) Floating inputs allowed.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family assures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals.

The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs. The AUP family of single gate logic makes excellent translators for the new lower voltage microprocessors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the lower voltage levels.

The SN74AUP1G240 is essentially an inverter that can be placed into a high-impedance state. In this application, the output is forced to V_{CC} when the SN74AUP1G240's output is disabled, and when the output is enabled, the device performs the function $Y = \bar{A}$.

9.2 Typical Application

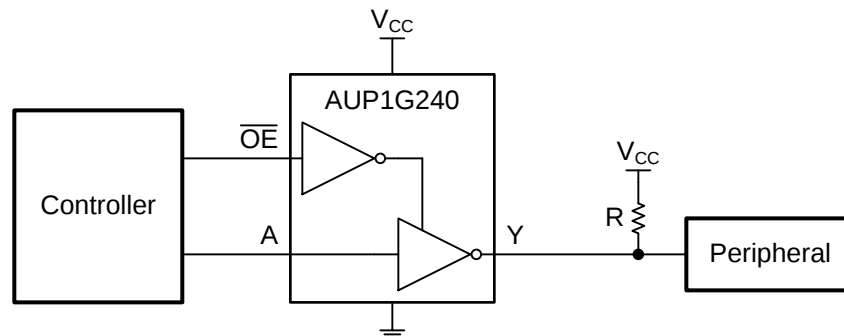


Figure 6. Simplified Application Schematic

9.2.1 Design Requirements

SN74AUP1G240 uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

Pull-up resistor selection is based on leakage current into the Peripheral's input (I_I) and the high-impedance output of the SN74AUP1G240 (I_{OZ}). See the next section for equations for pull-up resistor (R) selection.

9.2.2 Detailed Design Procedure

1. Recommended Supply Conditions
 - A bypass capacitor should be connected between V_{CC} and ground of the device. See [Power Supply Recommendations](#) section for more details.
2. Recommended Input Conditions
 - Rise time and fall time specifications. See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table
 - Inputs are overvoltage tolerant allowing them to go as high as $V_{I(max)}$ at any valid V_{CC} , as specified in the [Absolute Maximum Ratings](#) table
3. Recommended Output Conditions

Typical Application (continued)

- Load currents should not exceed the continuous output current maximum rating. See (I_O) in the [Absolute Maximum Ratings](#) table
- Outputs should not be pulled above the voltage range applied to any output in the high-impedance or power-off state maximum rating. See (V_O) in the [Absolute Maximum Ratings](#) table
- Pull-up resistor (R) selection depends on three primary factors: desired output high voltage (V_{OH}), which is directly related to total leakage current into the SN74AUP1G240 and the peripheral device's input (I_L), desired 0 to 90% rising edge time (t_r), which is directly related to the parasitic line capacitance (C_P), and the maximum current during low output (I_{OL}), which is directly related to the supply value. These three equations govern pull-up resistor selection:
 - $R \leq (V_{CC} - V_{OH}) / I_L$
 - $R \leq t_r / (2.3 \times C_P)$
 - $R \geq V_{CC} / I_{OL(max)}$

9.2.3 Application Curve

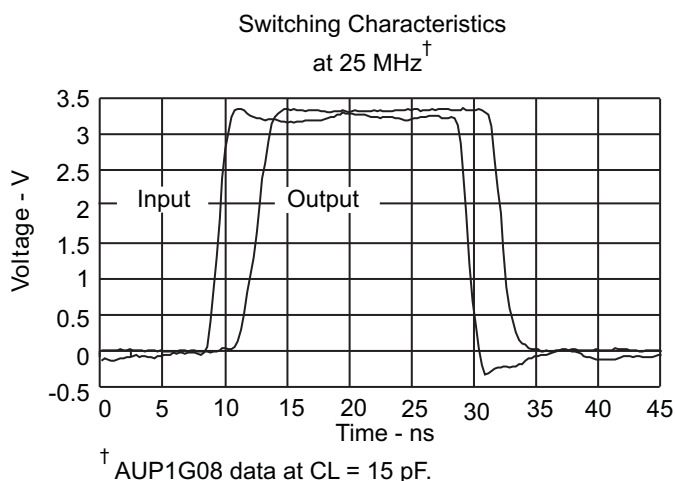


Figure 7. Excellent Signal Integrity

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

The V_{CC} pin must have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended, and it is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

An example layout is given in Figure 9 for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout

11.2 Layout Example

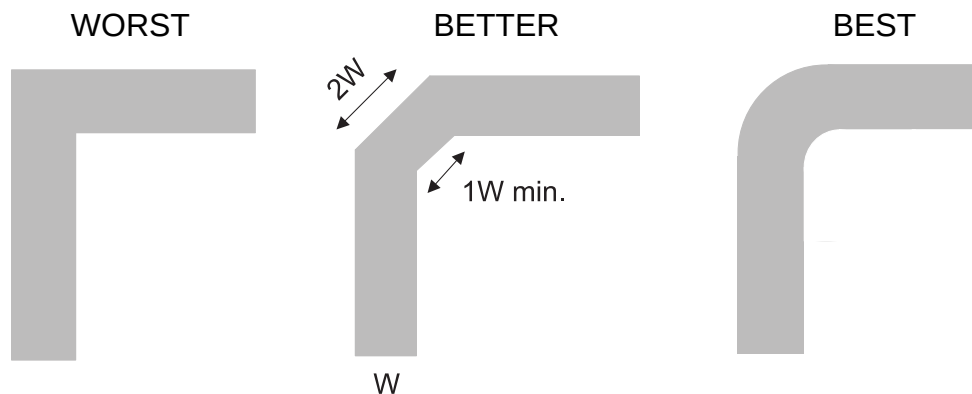


Figure 8. Trace Example

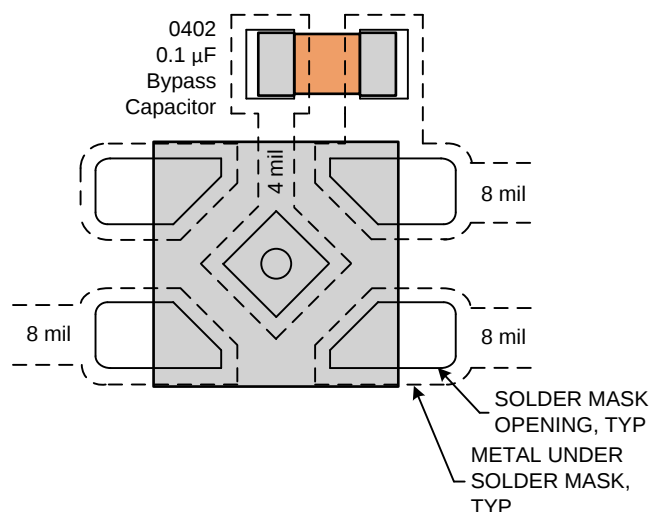


Figure 9. Example Layout With DPW (X2SON-5) Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs Application Report](#)
- Texas Instruments, [Designing and Manufacturing with TI's X2SON Packages Application Report](#)
- Texas Instruments, [How to Select Little Logic Application Report](#)
- Texas Instruments, [Introduction to Logic Application Report](#)
- Texas Instruments, [Understanding Schmitt Triggers Application Report](#)
- Texas Instruments, [Semiconductor Packing Material Electrostatic Discharge \(ESD\) Protection Application Report](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoStar, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PSN74AUP1G240DPWR	ACTIVE	X2SON	DPW	5	3000	TBD	Call TI	Call TI	-40 to 85		Samples
SN74AUP1G240DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H40R	Samples
SN74AUP1G240DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H40R	Samples
SN74AUP1G240DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HK5, HKF, HKK, HK R)	Samples
SN74AUP1G240DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HK5, HKR)	Samples
SN74AUP1G240DPWR	PREVIEW	X2SON	DPW	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CF	
SN74AUP1G240DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HK	Samples
SN74AUP1G240DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HK	Samples
SN74AUP1G240YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		HKN	Samples
SN74AUP1G240YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HKN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- ⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- ⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- ⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G240DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G240DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G240DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G240DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G240DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G240DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G240DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G240YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G240YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G240DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G240DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G240DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G240DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G240DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G240DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G240DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G240YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G240YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

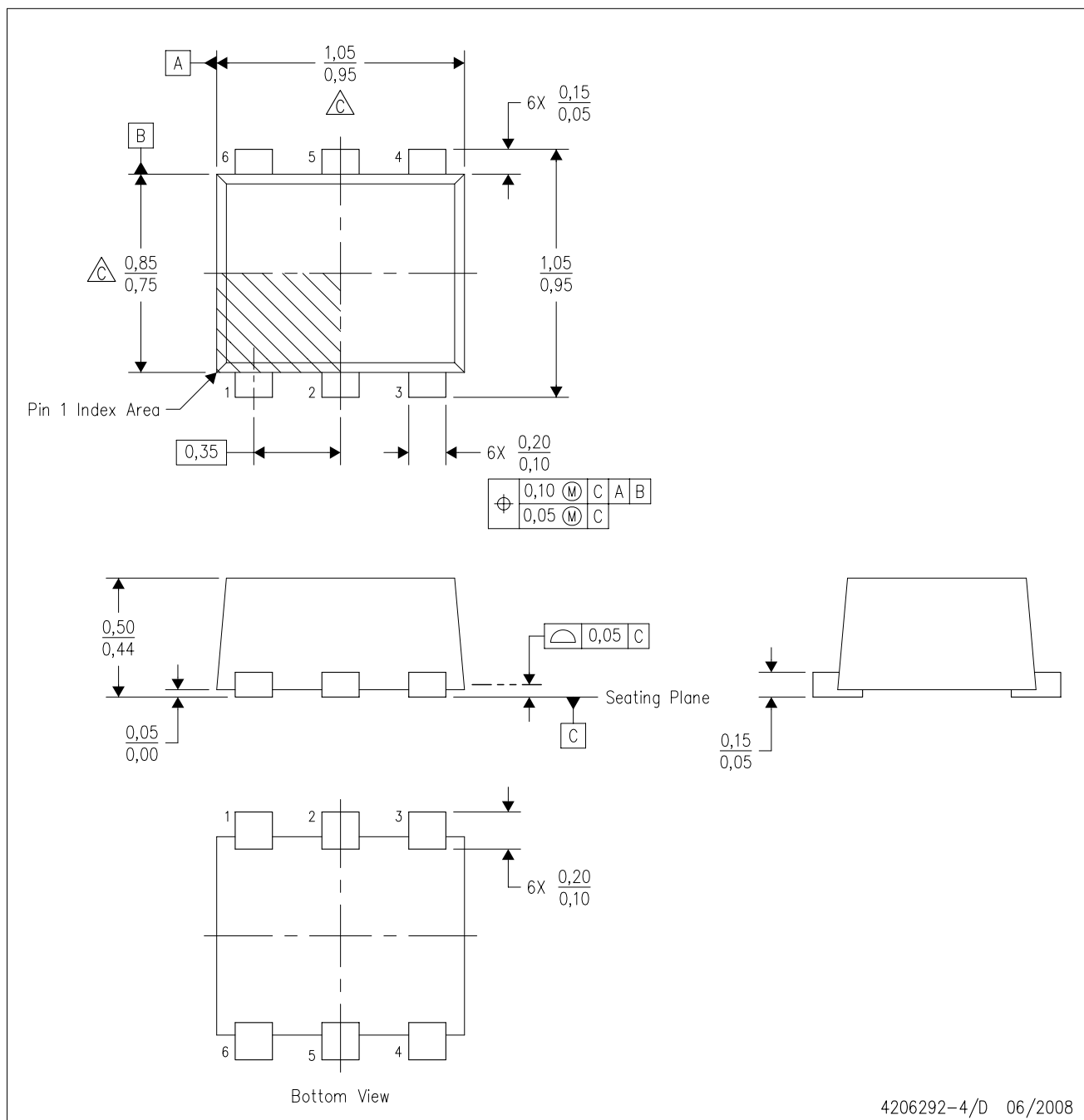
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

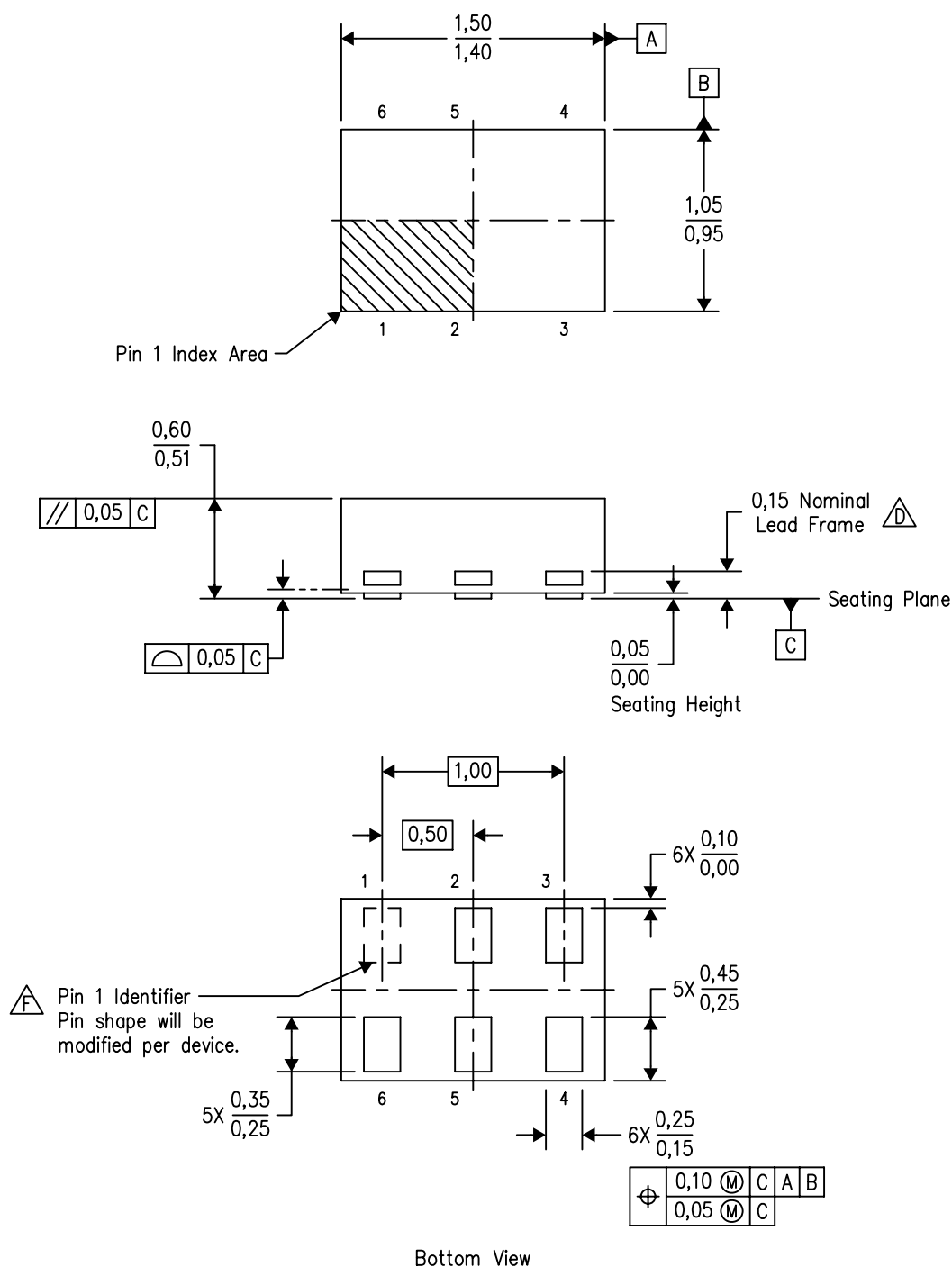


4206292-4/D 06/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,10 per end or side.
 - D. JEDEC package registration is pending.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

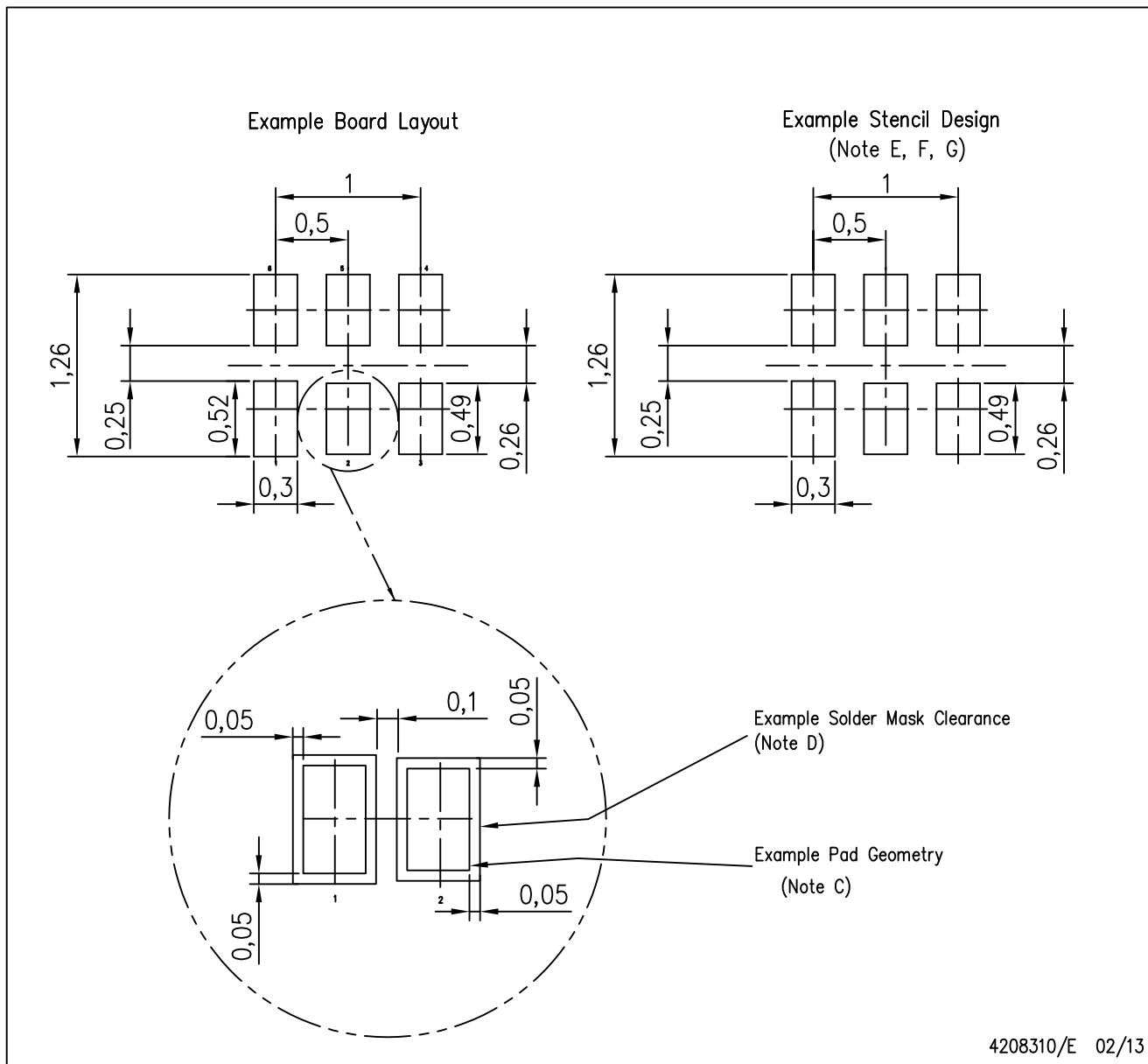


4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - $\triangle D$ The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
 - E. This package complies to JEDEC MO-287 variation UFAD.
 - $\triangle F$ See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

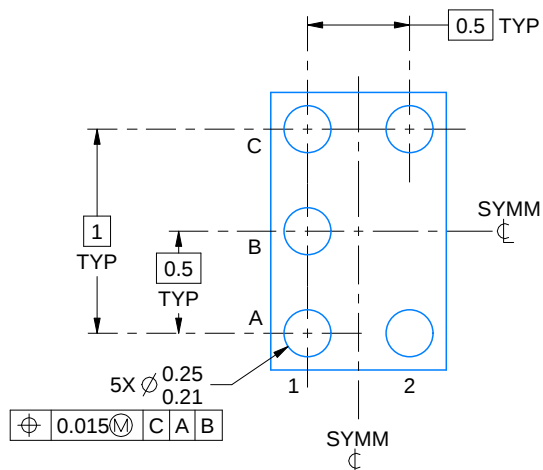
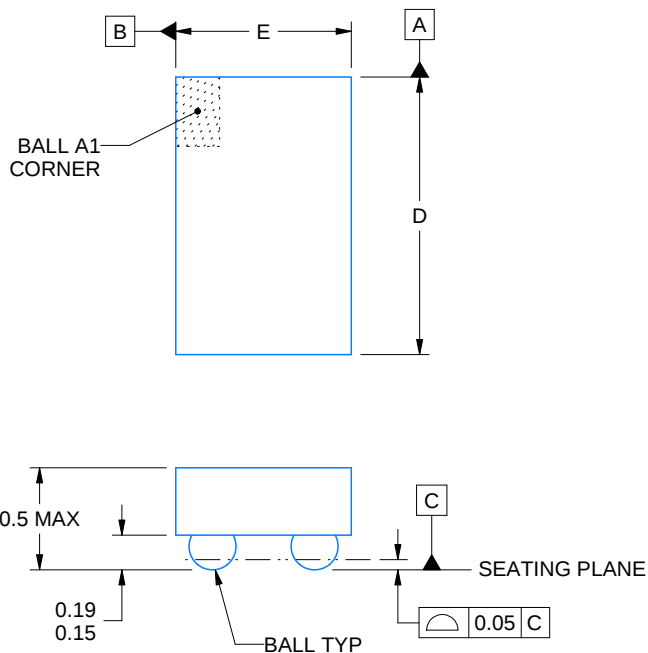
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm

E: Max = 0.918 mm, Min = 0.858 mm

4219492/A 05/2017

NOTES:

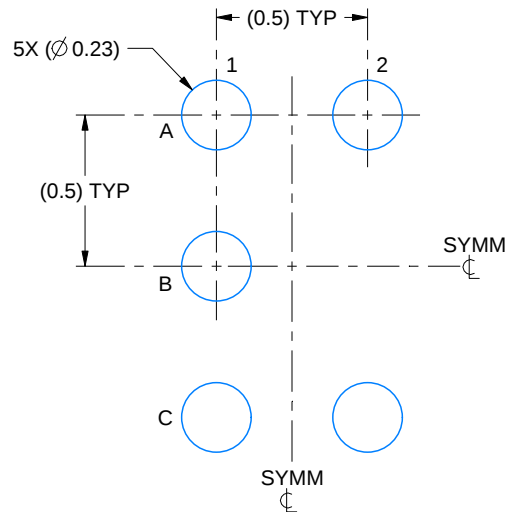
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

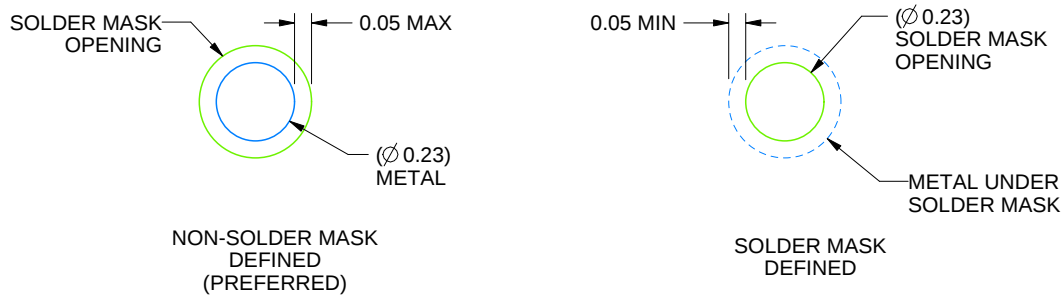
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

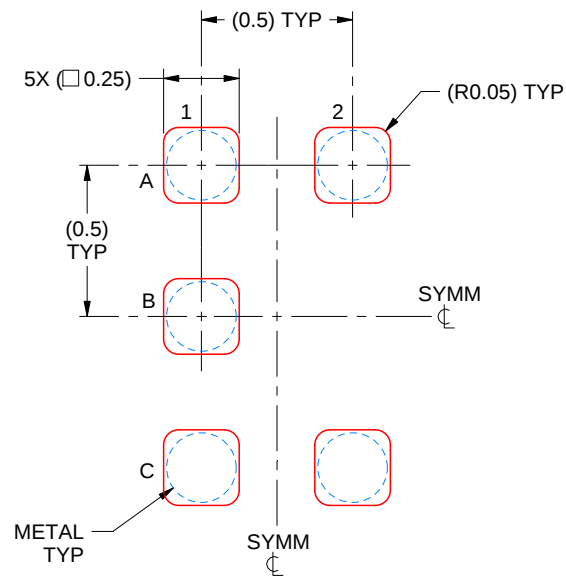
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

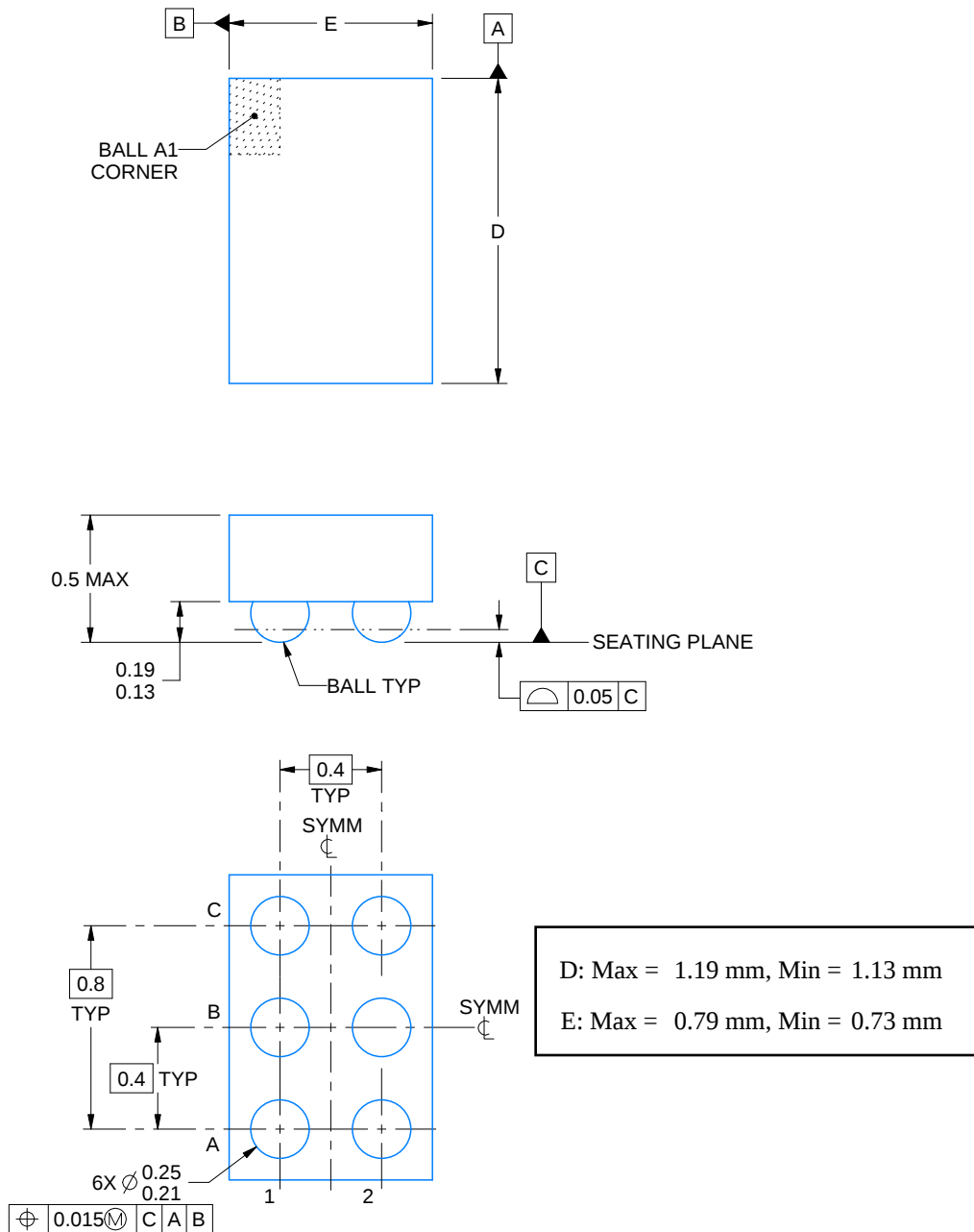
YFP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223410/A 11/2016

NOTES:

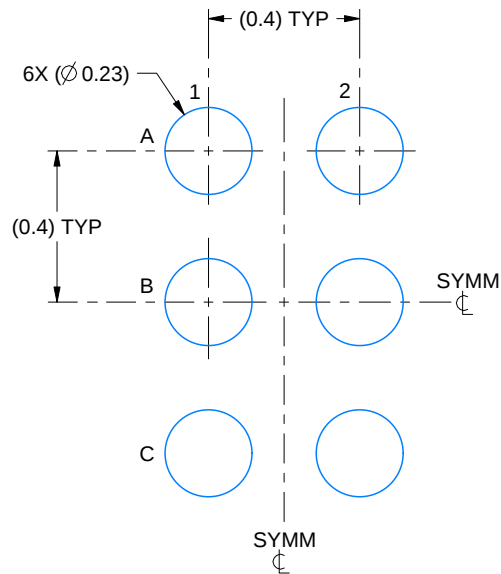
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

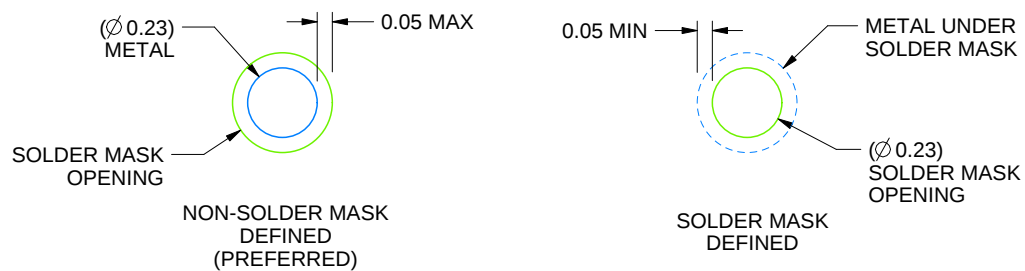
YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X

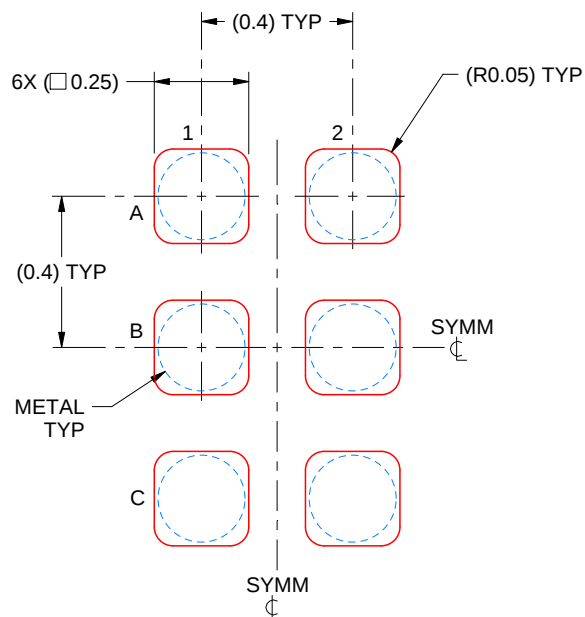


SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
 BASED ON 0.1 mm THICK STENCIL
 SCALE:50X

4223410/A 11/2016

NOTES: (continued)

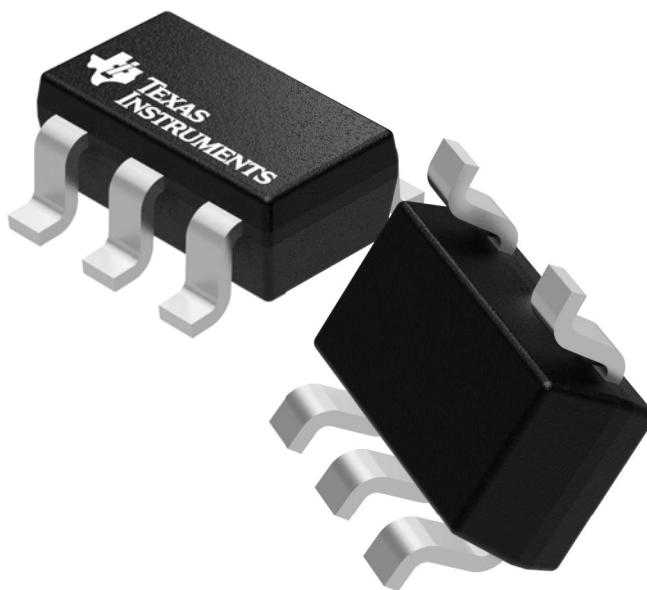
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

GENERIC PACKAGE VIEW

DBV 5

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073253/P

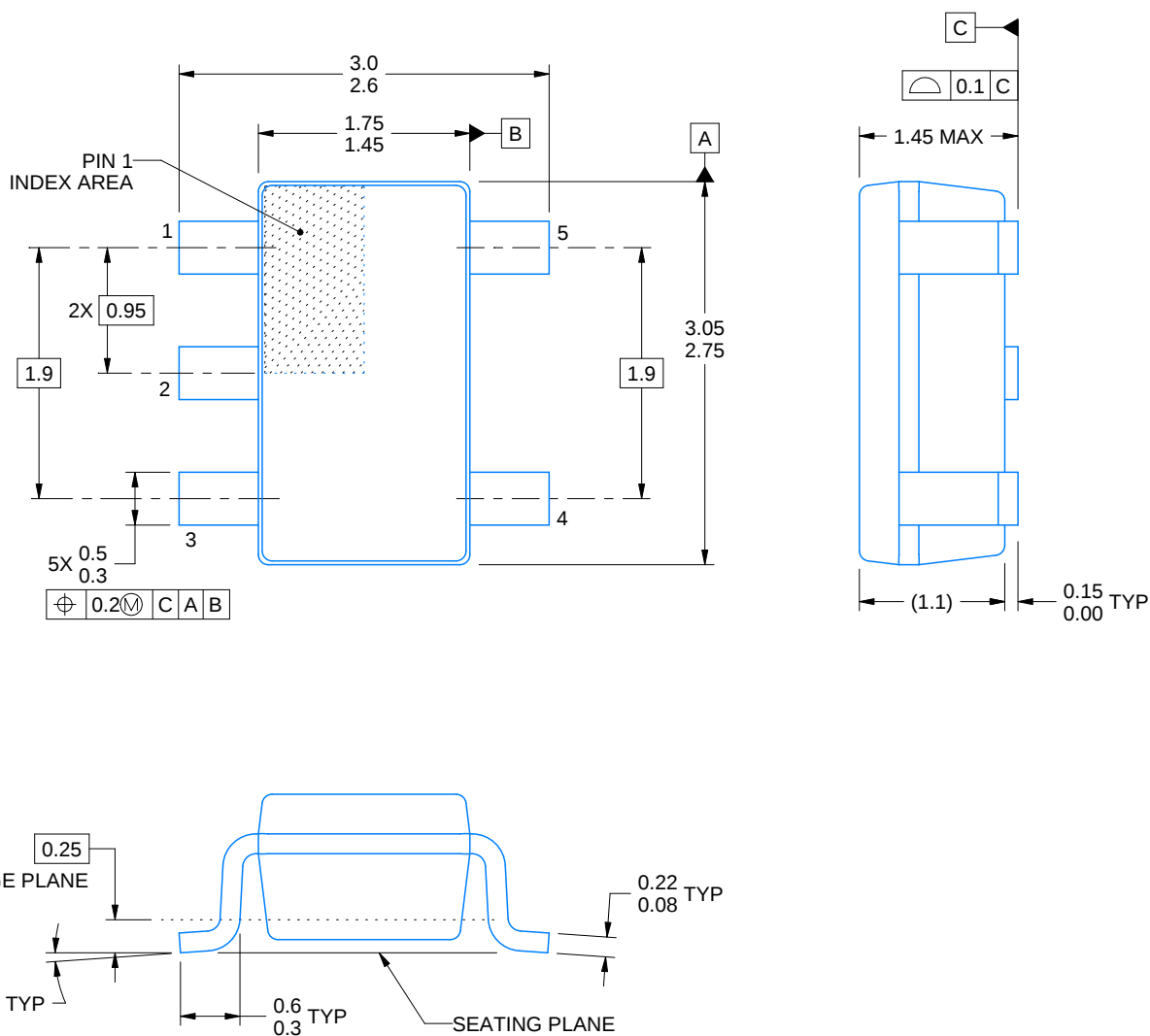


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

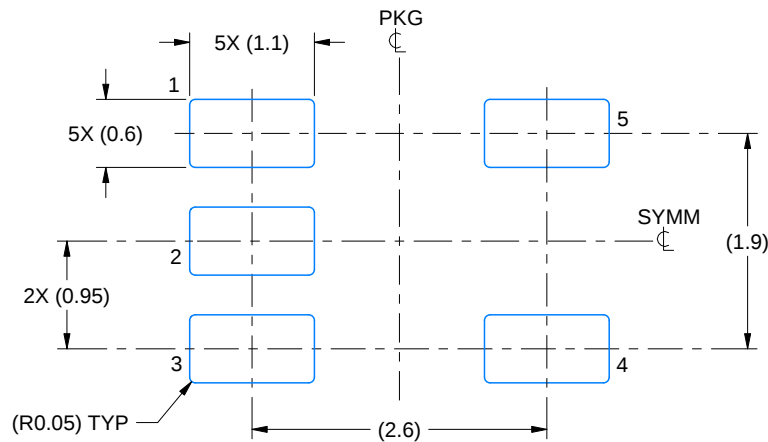
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

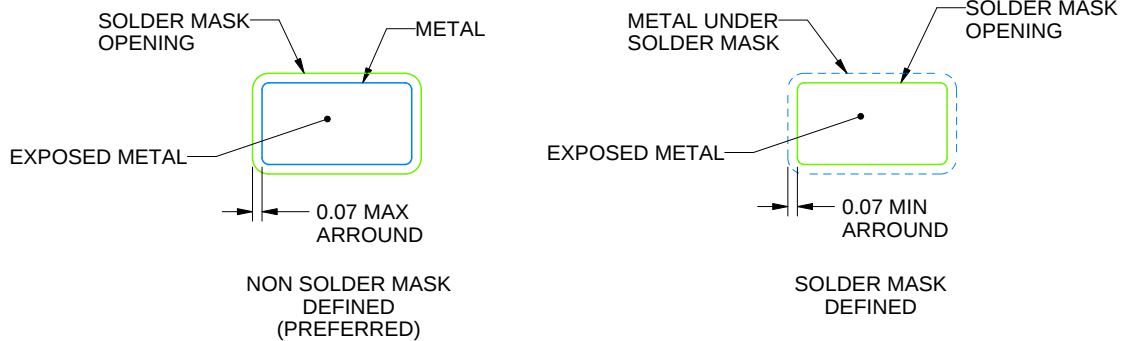
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

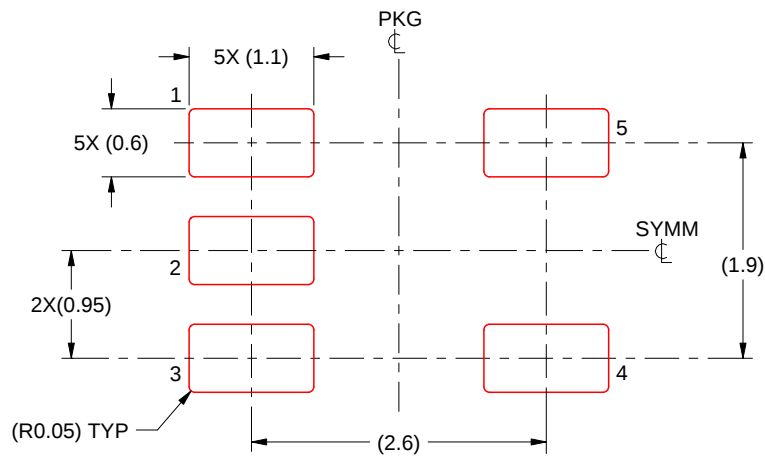
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

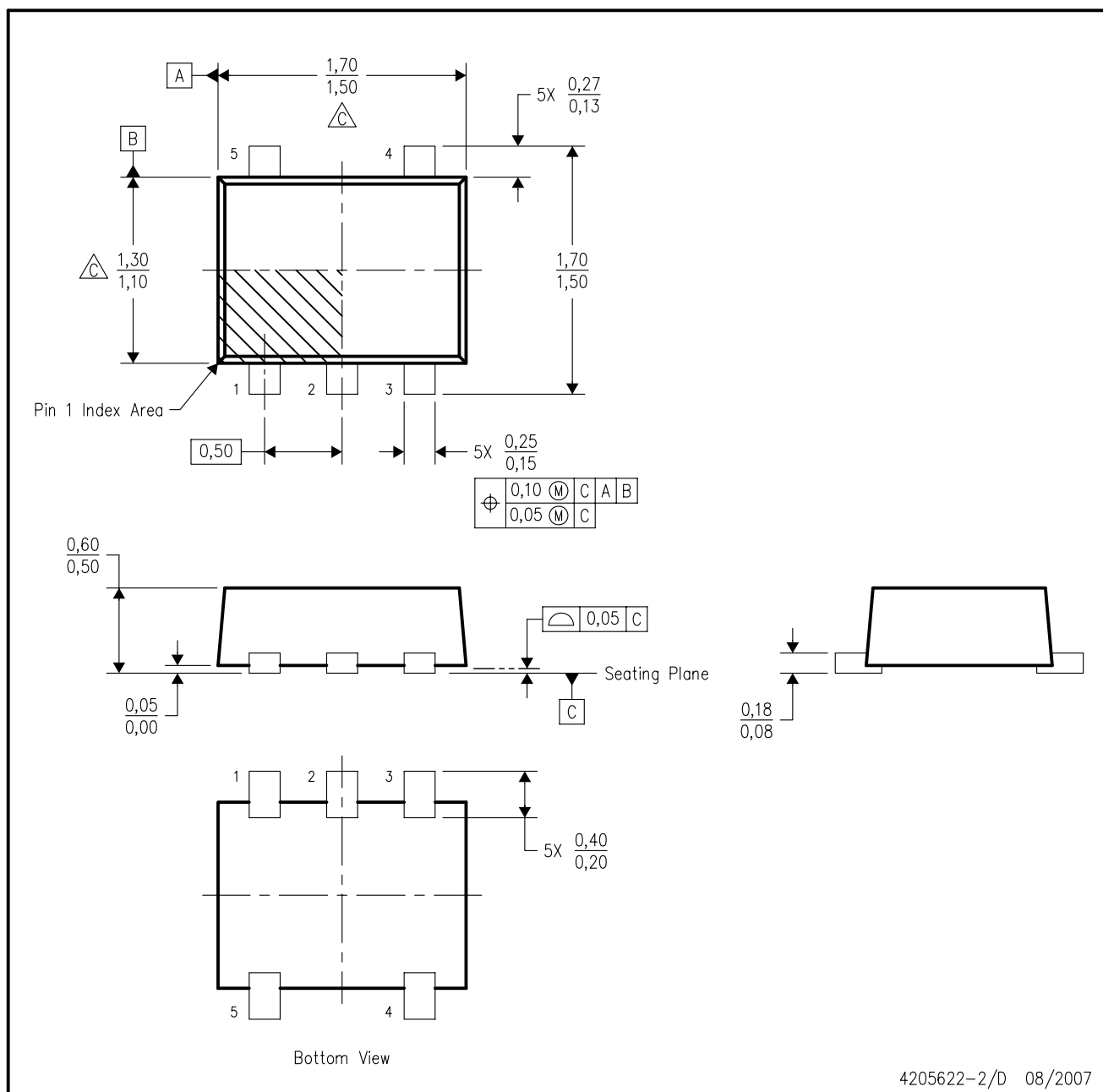


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

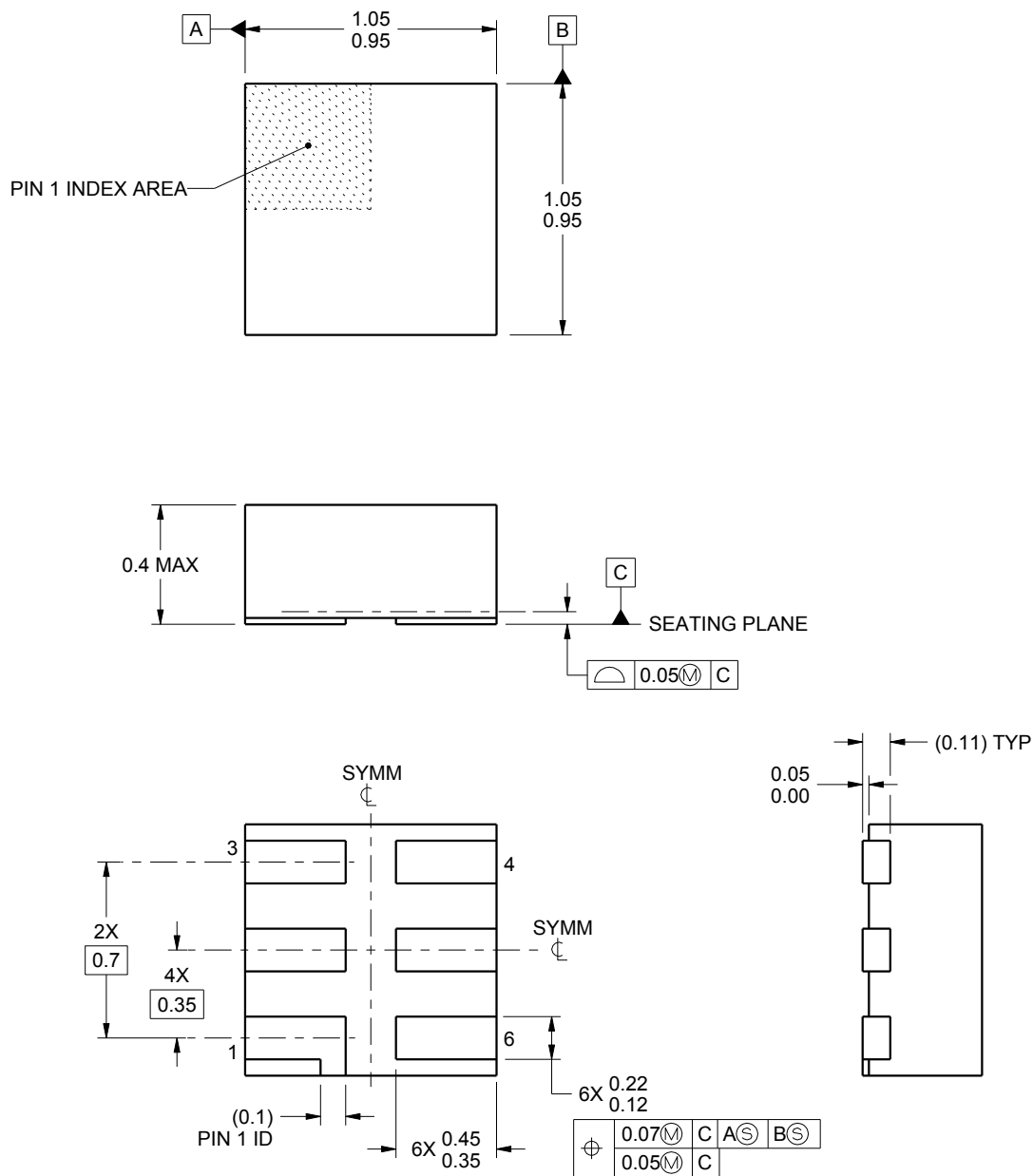


4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



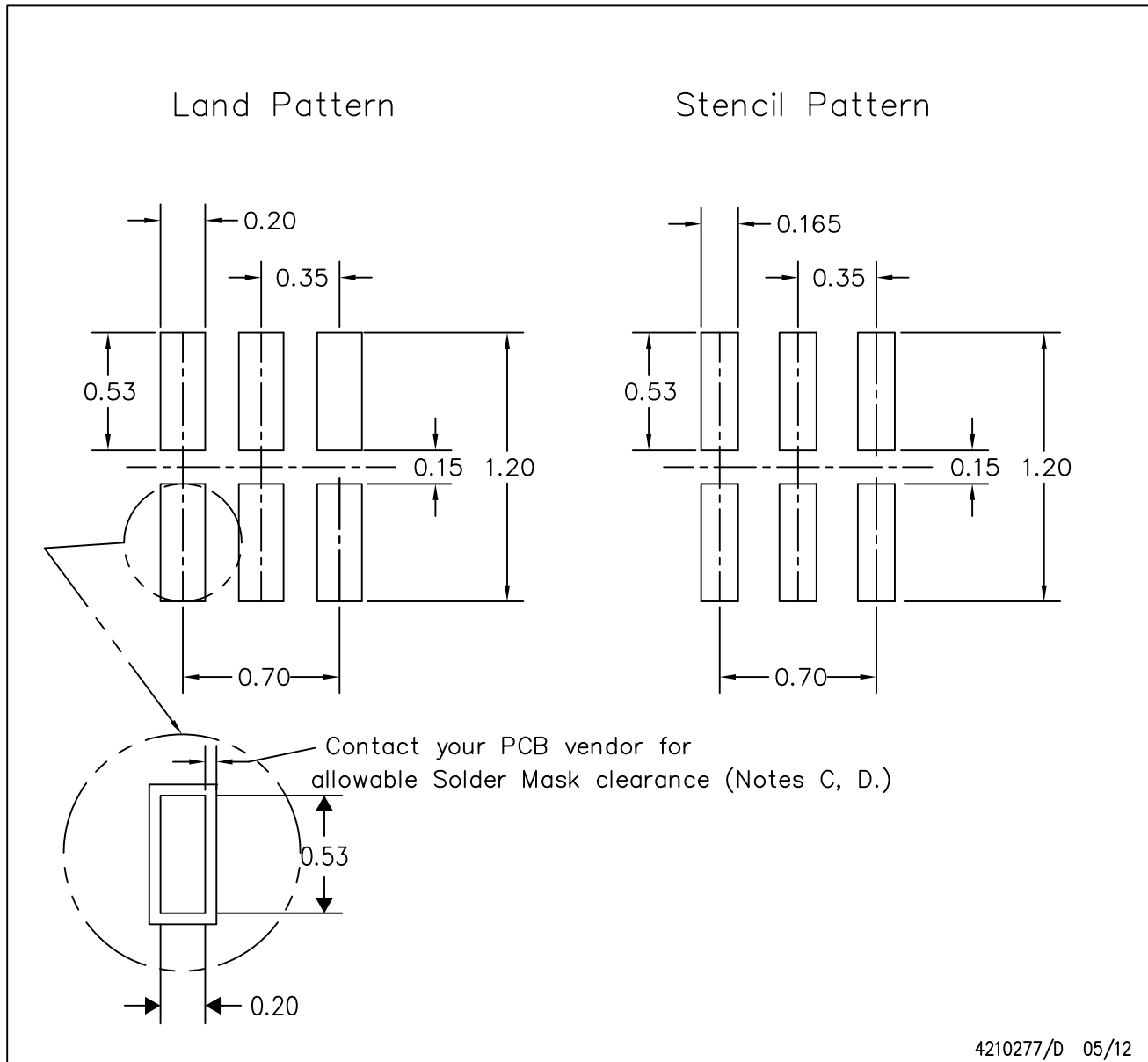
4208186/F 10/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4210277/D 05/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 - H. Component placement force should be minimized to prevent excessive paste block deformation.

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