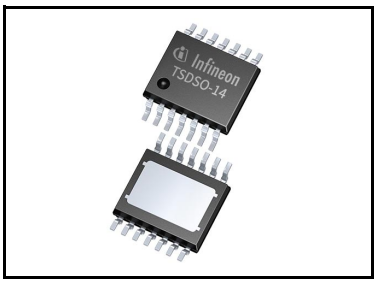
ITS4040D-EP-D

ITS4040D-EP-D

40 mΩ Dual Channel Smart High-Side Power Switch

RoHS



1 Overview

Features

- Dual channel Smart High-Side Power Switch with integrated protection and diagnosis
- Maximum $R_{DS(ON)}$ 40 mΩ per channel at T_j = 25°C
- High output current capability: nominal current up to 2.6 A
- Low and accurate current limitation: 4.1 A (± 20 %)
- Extended supply voltage range up to 45 V
- All control inputs 24 V capable and support direct interface to optocouplers
- All control inputs 3.3 V and 5 V logic level compatible
- 4 kV electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Very small, thermally enhanced TSDSO-14 package
- Device robustness validated by extended qualification according to JEDEC standard “JESD47J”
- Green product (RoHS compliant)

Applications

- Digital output modules (PLC applications, factory automation)
- Industrial peripheral switches and power distribution
- Switching resistive, inductive and capacitive loads in harsh industrial environments
- Replacement for electromechanical relays, fuses and discrete circuits
- Most suitable for loads that require a precise current limit

Description

The ITS4040D-EP-D is a 40 mΩ Dual Channel Smart High-Side Power Switch providing integrated protection functions and a diagnosis feedback. With two channels capable of currents of more than 2 A each, very low typical $R_{DS(ON)}$ values of 60 mΩ at T_j = 125°C and the small PG-TSDSO-14 exposed pad package it combines high current capability with minimum space requirements. The exposed pad of the thermally enhanced PG-TSDSO-14 package allows a very efficient heat transfer from the device to inner layers of the PCB by means of thermal vias. The power transistors are built by N-channel vertical power MOSFETs (DMOS) with charge pump.

Overview

The ITS4040D-EP-D is specifically designed to switch resistive, inductive or capacitive loads in harsh industrial environments. The ITS4040D-EP-D is equipped with essential protection features that make it extremely robust. Diagnostic information can be read out via the STATUS output (ST). The two channel device can be controlled with two separate input pins. Due to their high voltage capability the input pins can be directly interfaced to optocouplers without additional external components.

Diagnostic Functions

- Short circuit to ground (overload) indication
- Overtemperature switch off indication
- Stable diagnostic signal during short circuit and overtemperature shutdown
- Intelligent channel fault detection system

Protection Functions

- Stable behavior during undervoltage
- Overtemperature protection with restart after cooling down phase
- Overload- and short circuit protection
- Reverse polarity / inverse current protection with external components
- Overvoltage protection with external components
- Loss of ground protection

The qualification of this product is based on JEDEC JESD47J and may reference existing qualification results of similar products. Such referring is justified by the structural similarity of the products. The product is not qualified and manufactured according to the requirements of Infineon Technologies with regard to automotive and/or transportation applications. Infineon Technologies administrates a comprehensive quality management system according to the latest version of the ISO9001 and IATF 16949.

The most updated certificates of the ISO9001 and IATF 16949 are available at **www.infineon.com/cms/en/product/technology/quality/**

Type	Package	Marking
ITS4040D-EP-D	PG-TSDSO-14	ITS4040D

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2 Block Diagram

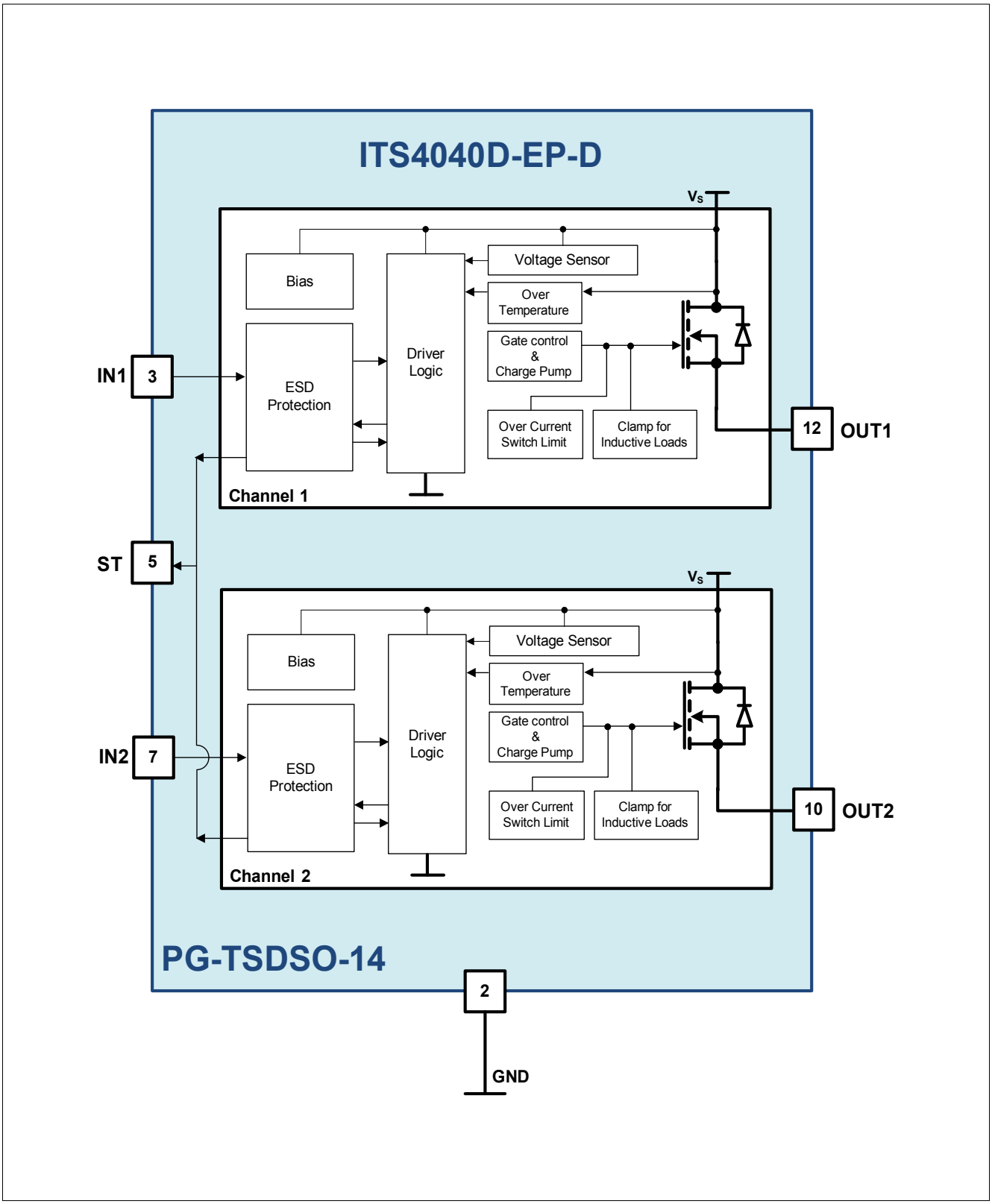


Figure 1 Block Diagram: ITS4040D-EP-D

3 Pin Configuration

3.1 Pin Assignment PG-TSDSO-14

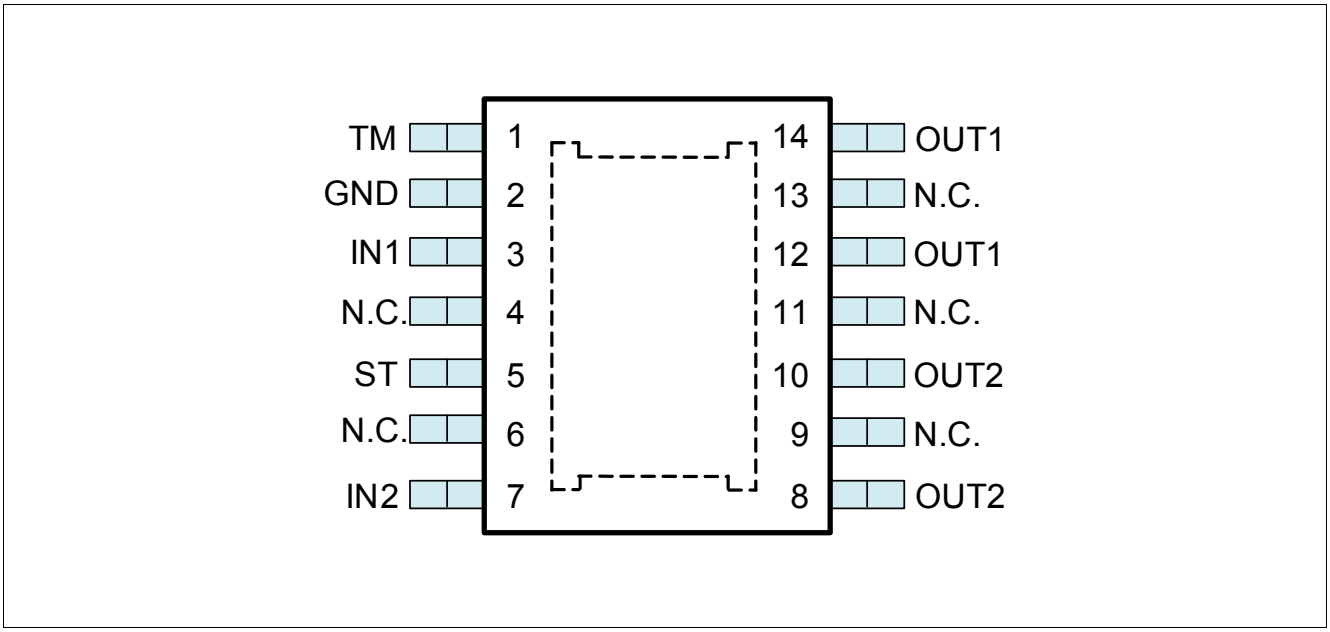


Figure 2 Pin Configuration PG-TSDSO-14

3.2 Pin Definitions and Functions PG-TSDSO-14

Pin	Symbol	Function
1	TM	**Test Mode Entry;** must be connected to device GND (pin 2) via resistor [1)]
2	GND	**Ground**
3	IN1	**INput channel 1;** Input signal for channel 1 activation, Active “High”
5	ST	**STatus feedback**; Active “Low”; connect with external pull-up resistor to “High”
7	IN2	**INput channel 2;** Input signal for channel 2 activation, Active “High”
8,10	OUT2	**OUTput 2;** Protected high-side power output channel 2
12, 14	OUT1	**OUTput 1;** Protected high -side power output channel 1
4, 6, 9, 11,13	N.C.	Not Connected
Exposed Pad	VS	**Voltage Supply**

1) to ensure proper functionality of the device the TM pin must be connected to device ground. In order to protect the pin furthermore in case of reverse polarity conditions or ground shifts the TM pin needs to be connected with a serial resistor to device ground. The recommended value for this resistor is 2.2 kΩ.

3.3 Voltage and Current Definitions

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

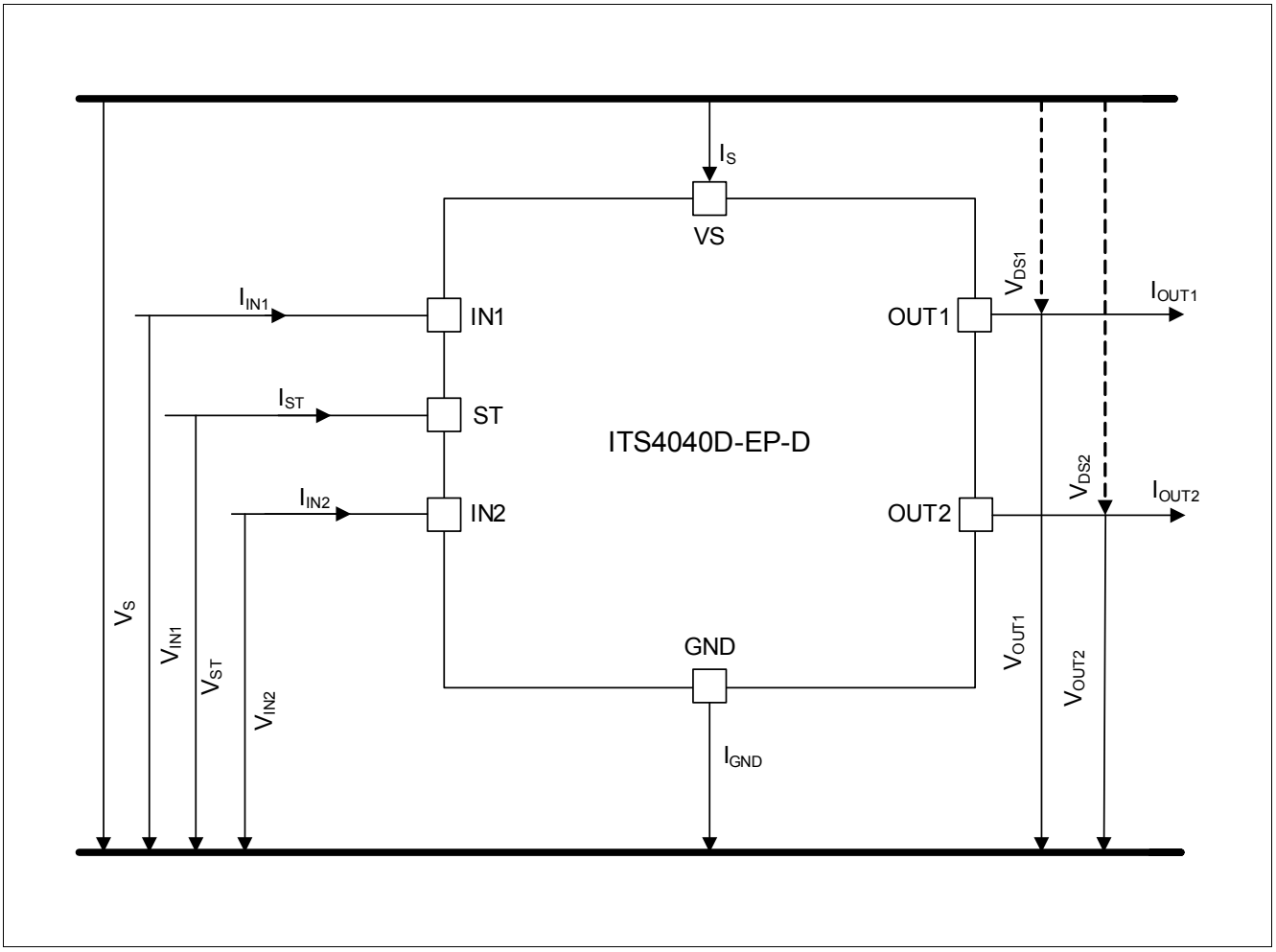


Figure 3 Voltage and Current Definitions

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings [1)]

T_j = -40°C to 150°C, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Supply voltage	V_S	-0.3	–	45	V	–	P_4.1.1
Reverse polarity voltage	$-V_{S(REV)}$	0	–	28	V	[2)] t < 2 min T_A = 25°C R_L ≥ 25 Ω Z_{GND} = 150 Ω Power Resistor	P_4.1.3
Supply voltage for short circuit protection	$V_{S(SC)}$	0	–	36	V	–	P_4.1.4
Input Pins							
Voltage at INPUT pins	V_{IN}	-0.3	–	45	V	$V_S > V_{IN}$	P_4.1.5
Current through INPUT pins	I_{IN}	-2	–	2	mA	–	P_4.1.6
STATUS Pin							
Voltage at ST pin	V_{ST}	-0.3	–	45	V	$V_S > V_{ST}$	P_4.1.7
Current through ST pin	I_{ST}	-2	–	2	mA	–	P_4.1.8
Power Stage							
Power dissipation (DC)	P_{TOT}	–	–	1.9	W	[3)] T_A = 85°C T_j < 150°C	P_4.1.10
Maximum energy dissipation single pulse (one channel)	E_{AS}	–	–	185	mJ	I_L = 2 A T_j = 150°C V_S = 28 V	P_4.1.11
Voltage at power transistor	V_{DS}	–	–	65	V	–	P_4.1.12
Currents							
Current through ground pin	I_{GND}	-20	–	20	mA	–	P_4.1.13
Temporary reverse current through ground pin to V_S	I_{GND}	-200	–	–	mA	t < 2 min	P_4.1.21
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.14
Storage temperature	T_{STG}	-55	–	150	°C	–	P_4.1.15
ESD Susceptibility							
ESD susceptibility (all pins)	V_{ESD_HBM}	-2	–	2	kV	HBM[4)]	P_4.1.16
ESD susceptibility OUT Pin vs. GND and V_S connected	V_{ESD_HBM}	-4	–	4	kV	HBM[4)]	P_4.1.17

Table 1 Absolute Maximum Ratings [1)] (cont'd)

T_j = -40°C to 150°C, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ESD susceptibility	V_{ESD_CDM}	-500	–	500	V	CDM[5)]	P_4.1.18
ESD susceptibility pin (corner pins)	V_{ESD_CDM}	-750	–	750	V	CDM[5)]	P_4.1.19

1) Not subject to production test; specified by design.

2) Reverse polarity protection can only be achieved in combination with external components: to limit the current through the GND-path a 150 Ω power resistor needs to be placed between GND-pin and ground. An alternative solution is to use a reverse current diode in the GND-path to realize reverse polarity protection. In this case placing a resistor in the range of ≥ 27 Ω in series to the diode is recommended to improve at the same time the overvoltage capability in case of overvoltage pulses on V_S.

3) This parameter serves as reference for the thermal budget: it illustrates the power dissipation that can be handled by the device in an application under the given boundary conditions before exceeding the maximum rating of T_j when assuming a R_{thJA} value for a thermally well dimensioned PCB connection like given in the JEDEC case **P_4.3.3** in **Chapter 4.4**. As R_{thJA} depends strongly on the applied PCB and layout of any individual application the actual achievable values of P_{TOT} can either be lower or higher depending on the given application.

4) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001(1.5 kΩ, 100 pF).

5) ESD susceptibility, Charged Device Model "CDM" JEDEC JESD22-C101.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

T_j = -40°C to 150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	$V_{S(NOM)}$	8	24	36	V	$V_S > V_{IN}$	P_4.2.1
Extended operating voltage	$V_{S(EOP)}$	5	–	45	V	1) $V_S > V_{IN}$ I_{OUT} = 2 A V_{DS} < 0.5 V	P_4.2.2
Minimum functional supply voltage during power-up	$V_{S(OP)_MIN}$	–	4.3	5	V	$V_S > V_{IN}$ I_{OUT} = 0 A to V_{DS} < 0.5 V (V_S rising; powering up)	P_4.2.3
Undervoltage shutdown	$V_{S(UV)}$	3	3.5	4.1	V	$V_S > V_{IN}$ from V_{DS} < 0.5 V to I_{OUT} = 0 A (V_S dropping from functional range)	P_4.2.4
Undervoltage shutdown hysteresis	$V_{S(UV)_HYS}$	–	850	–	mV	1)	P_4.2.5
Operating current One channel active	I_{GND_1}	–	3	4.1	mA	$V_S = V_{IN}$ = 24 V Device in $R_{DS(ON)}$	P_4.2.6
Operating current Both channels active ($T_j \leq$ 25°C)	I_{GND_2}	–	5.2	6.8	mA	$V_S = V_{IN}$ = 24 V Device in $R_{DS(ON)}$ $T_j \leq$ 25°C	P_4.2.7
Operating current Both channels active (T_j = 150°C)	$I_{GND_2_150}$	–	4.8	6.0	mA	$V_S = V_{IN}$ = 24 V Device in $R_{DS(ON)}$ T_j = 150°C	P_4.2.9
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.8

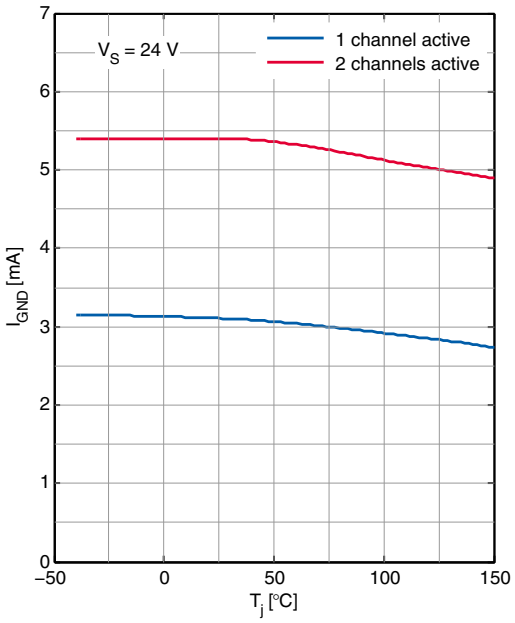
1) Not subject to production test; specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

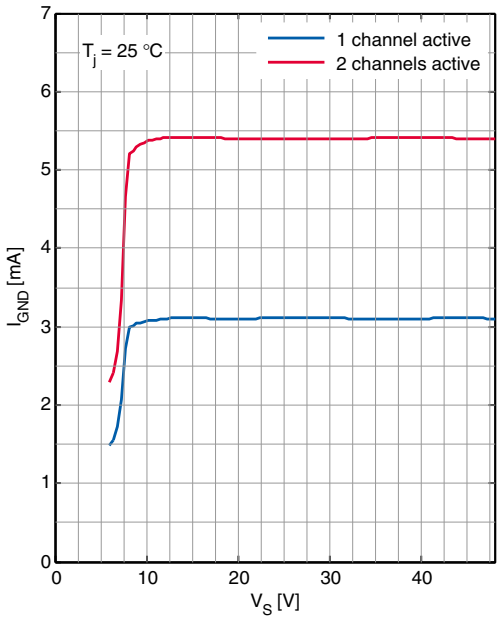
4.3 Typical Performance Characteristics Operating Current

Typical Performance Characteristics

Operating Current I_{GND} versus Junction Temperature T_j



Operating Current I_{GND} versus Supply Voltage V_S



4.4 Thermal Resistance

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to exposed pad soldering point	R_{thJC}	–	1	–	K/W	–	P_4.3.1
Junction to ambient All channels active	$R_{thJA_2s2pvia}$	–	34	–	K/W	2)	P_4.3.3
Junction to ambient All channels active	R_{thJA_1s0p}	–	109	–	K/W	3)	P_4.3.4
Junction to ambient All channels active	$R_{thJA_1s0p_300mm}$	–	51	–	K/W	4)	P_4.3.5
Junction to ambient All channels active	$R_{thJA_1s0p_600mm}$	–	42	–	K/W	5)	P_4.3.6

1) Not subject to production test; specified by design.

2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board, footprint; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1 x 70 µm Cu.

4) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board, 300 mm; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1 x 70 µm Cu.

5) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board, 600 mm; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1 x 70 µm Cu.

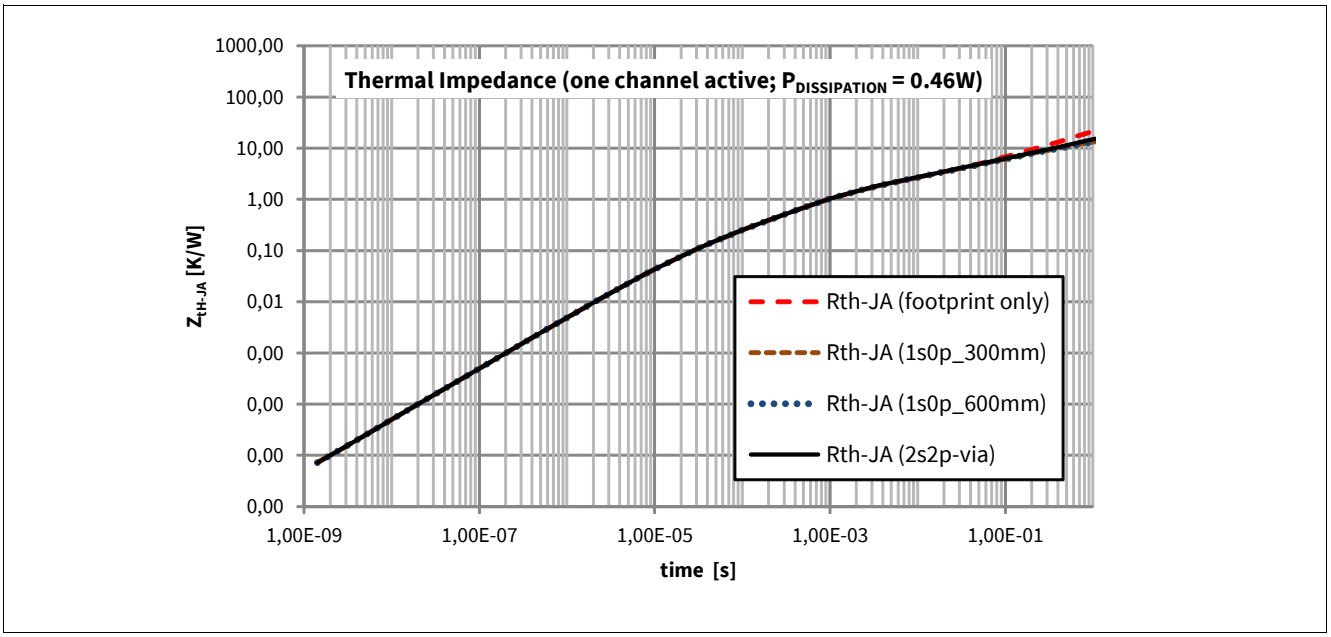


Figure 4 Thermal Impedance (short time scale; one channel active)

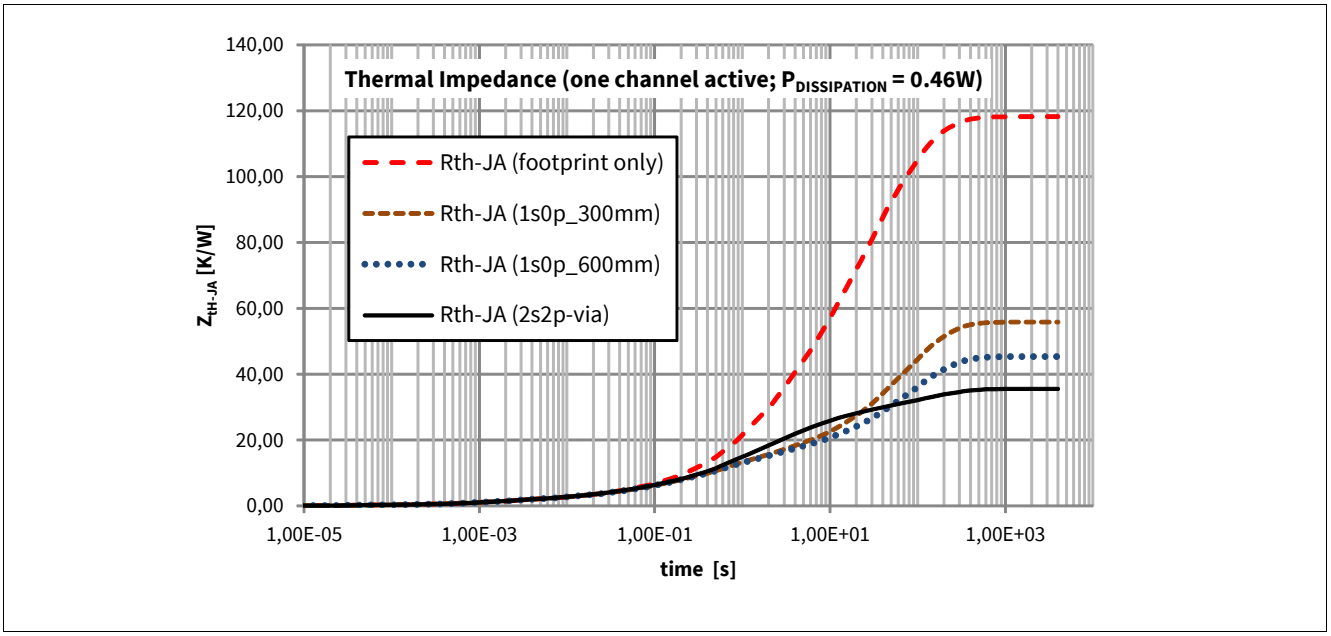


Figure 5 Thermal Impedance (long time scale; one channel active)

5 Power Stage

The power stages are built using an N-channel vertical power MOSFET (DMOS) with charge pump.

5.1 Output ON-state Resistance

The ON-state resistance $R_{DS(ON)}$ of the power stage depends on supply voltage as well as on junction temperature T_j. **Figure 6** shows the influence of temperature on the typical ON-state resistance. The behavior of the power stage in reverse polarity condition is described in **Chapter 6.3**.

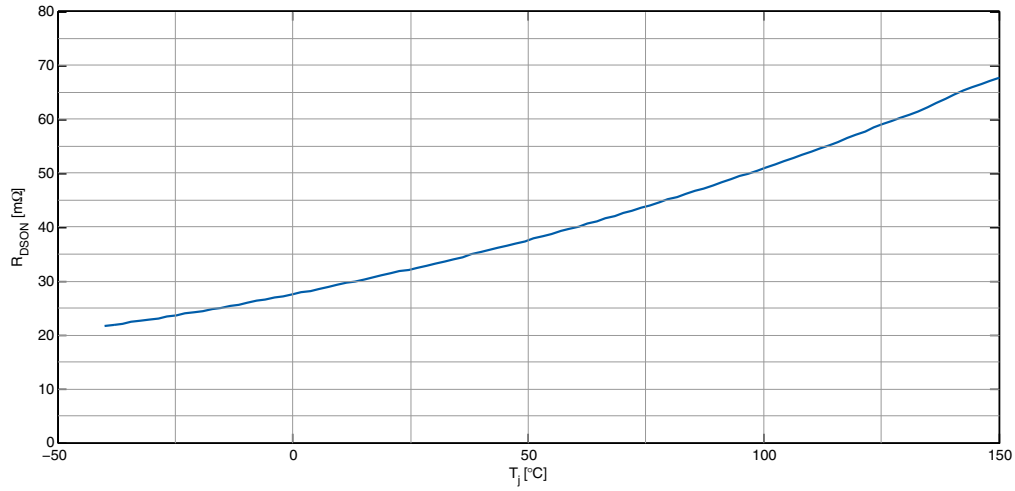


Figure 6 Typical ON-state Resistance

5.2 Turn ON/OFF Characteristics with Resistive Load

A “High” signal at the input pin (see **Chapter 8**) causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission. **Figure 7** shows the typical timing when switching a resistive load.

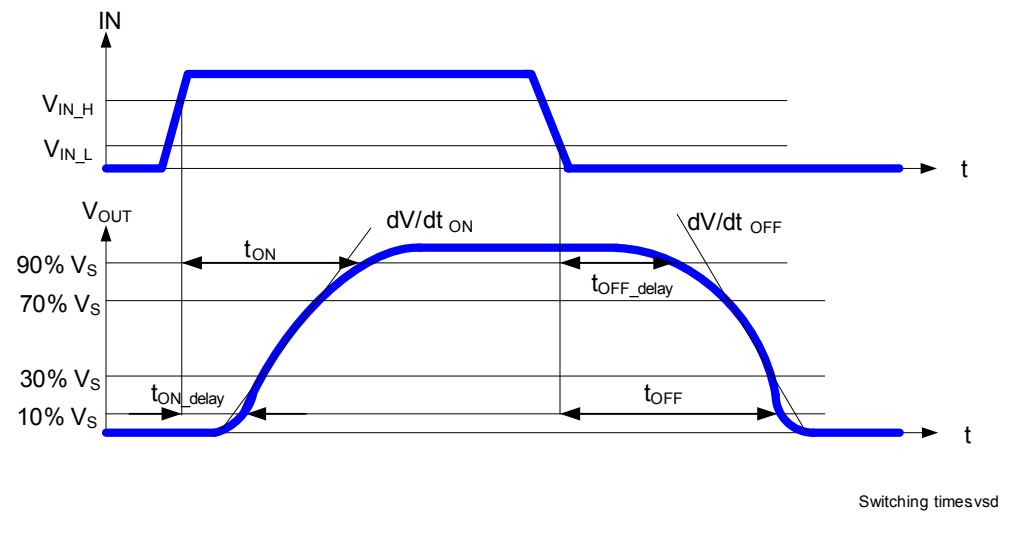


Figure 7 Switching a Resistive Load Timing

5.3 Inductive Load

5.3.1 Output Clamping

When switching OFF inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device by avalanche due to high voltage drop over the power stage a voltage clamp mechanism $Z_{DS(AZ)}$ is implemented that limits negative output voltage to a certain level (V_S - $V_{DS(AZ)}$). The clamping mechanism allows in addition a fast demagnetization of inductive loads because during the phase of active clamping the power is dissipated to a great extent rapidly inside the switch. On the other hand the power dissipated inside the switch while switching off inductive loads can cause considerable stress to the device. Therefore the maximum allowed energy at a given current (and by this also the inductance) is limited. In **Figure 8** and **Figure 9** the basic principle of active clamping as well as simplified waveforms when switching off inductive loads are illustrated.

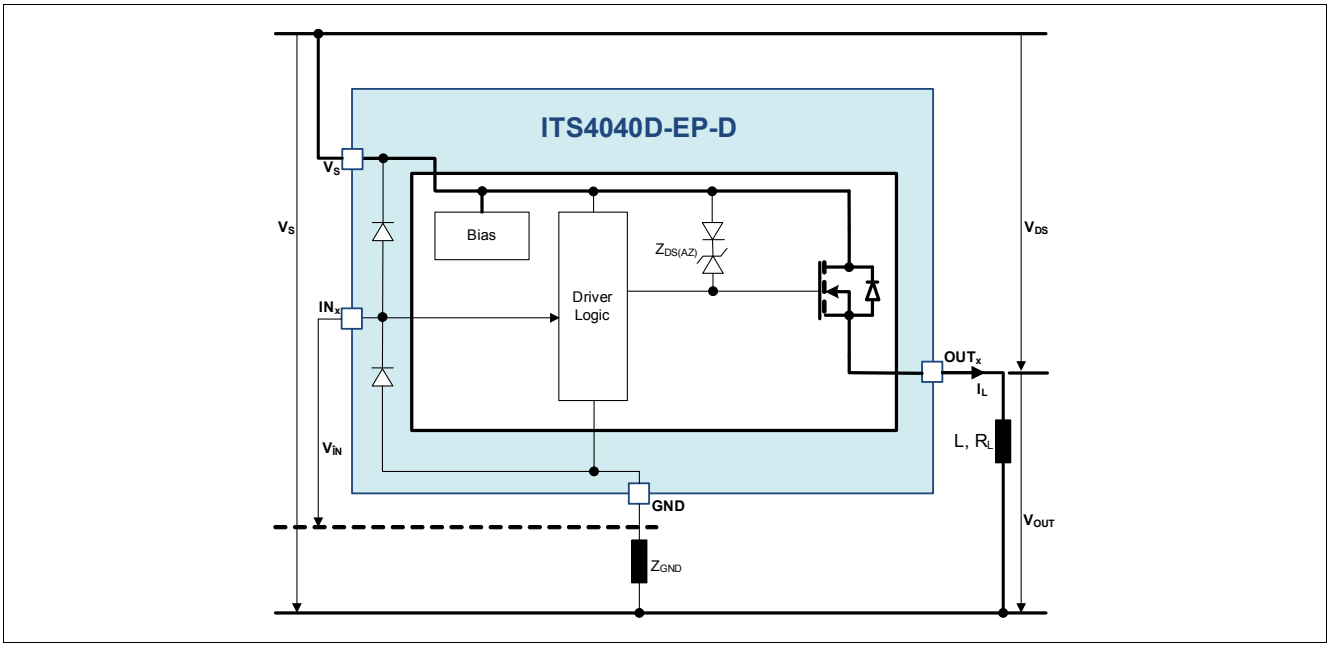


Figure 8 Output Clamp

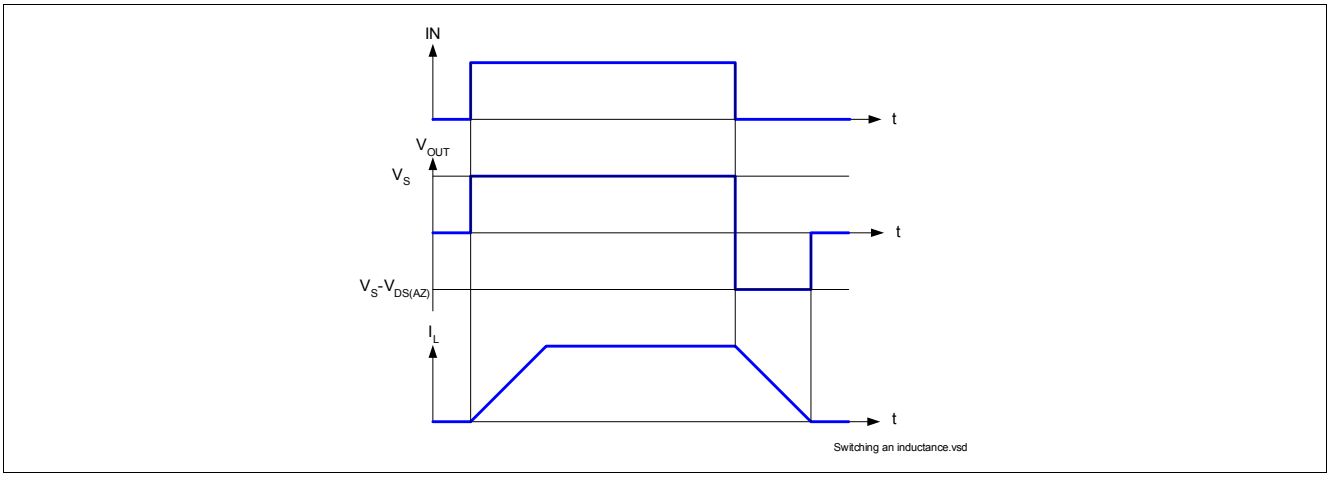


Figure 9 Switching an Inductive Load Timing

5.3.2 Maximum Load Inductance

During demagnetization of inductive loads, the following energy must be dissipated in the ITS4040D-EP-D:

$$E = V_{DS(AZ)} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{DS(AZ)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{DS(AZ)}}\right) + I_L \right] \quad (5.1)$$

Assuming R_L = 0 Ω simplifies the calculation:

$$E = \frac{1}{2} \times L \times I^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(AZ)}}\right) \quad (5.2)$$

The energy, which may be converted into heat, is limited by the thermal design of the component. **Figure 10** shows the maximum allowed energy dissipation as a function of the load current for a singular pulse event on one channel.

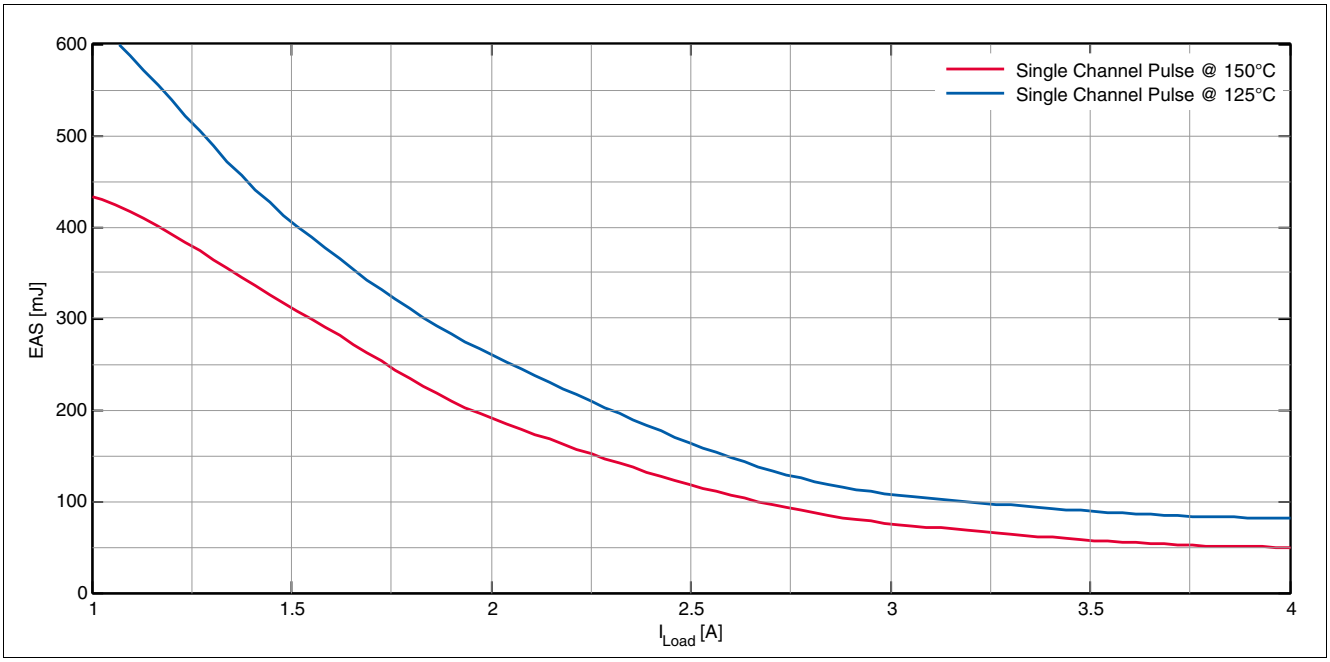


Figure 10 Maximum Energy Dissipation Single Pulse for a Single Channel, T_{j_START} = 150 °C; V_S = 28 V

5.4 Inverse Current Capability

In case of inverse current, meaning a voltage V_{INV} at the OUTput higher than the supply voltage V_S, a current I_{INV} will flow from output to V_S pin via the body diode of the power transistor (please refer to **Figure 11**). Channels that are active (ON-state) by the time when the inverse current condition appears will remain active and their output stage will follow the state of the corresponding IN pin, which means that the channel can be switched off during inverse current condition. Channels that are inactive (OFF-state) by the time when the inverse current condition appears will remain inactive regardless of the state of the corresponding IN pin. If during an inverse current condition the IN-pin of a channel is set from “Low” to “High” in order to activate the channel, the output stage of the channel is kept OFF until the inverse current disappears. For all cases the current I_{INV} should not be higher than $I_{L(INV)}$. Please note that during inverse current condition the protection functions of concerned channels are not available.

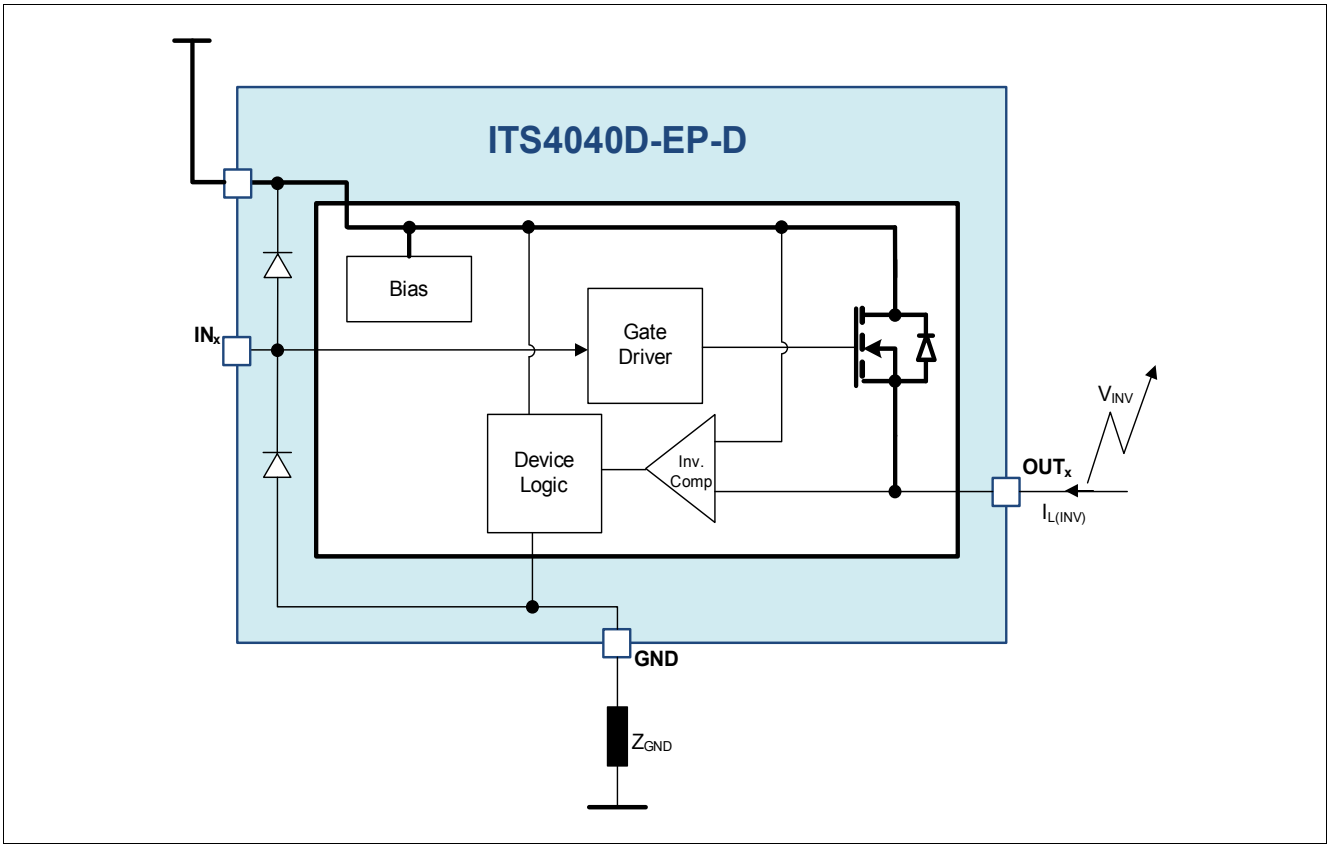


Figure 11 Inverse Current Circuitry

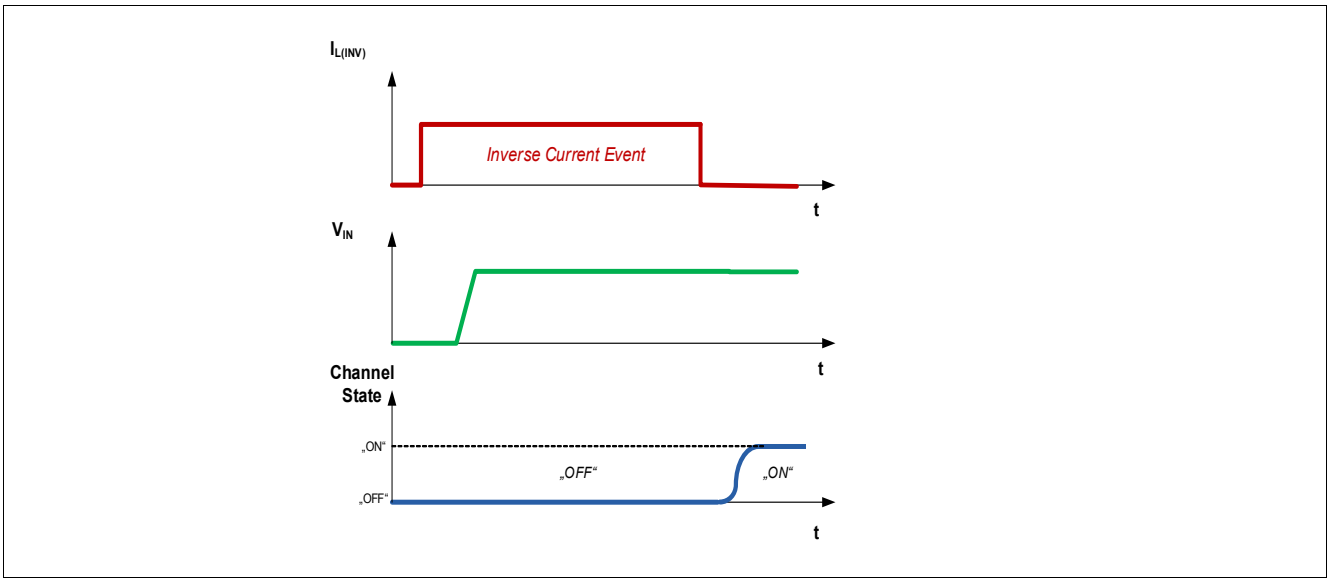


Figure 12 Inverse Current event: channel in OFF-state (channel remains off for duration of inverse current event)

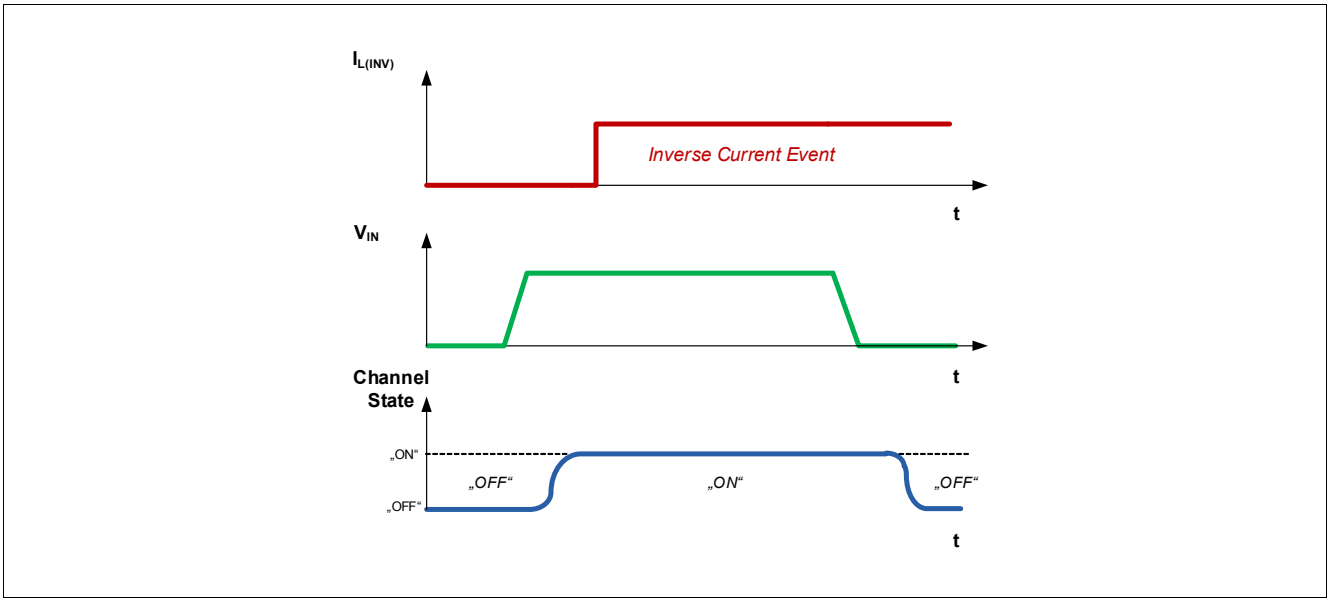


Figure 13 Inverse Current event: channel in ON-state (output not influenced but can be switched off)

5.5 Electrical Characteristics: Power Stage

Table 4 Electrical Characteristics: Power Stage

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified).
Typical values are given at V_S = 24 V, T_j = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ON-state resistance per channel (T_j = 25°C)	$R_{DS(ON)}$	–	–	40	mΩ	I_{Lx} = 2 A V_{IN} = 4.5 V T_j = 25°C	P_5.5.18
ON-state resistance per channel (T_j = 125°C)	$R_{DS(ON)_125}$	–	60	–	mΩ	1) I_{Lx} = 2 A V_{IN} = 4.5 V T_j = 125°C	P_5.5.19
ON-state resistance per channel (T_j = 150°C)	$R_{DS(ON)_150}$	–	–	80	mΩ	I_{Lx} = 2 A V_{IN} = 4.5 V T_j = 150°C	P_5.5.1
Nominal load current per channel	$I_{L(NOM)1}$	–	–	2.6	A	1) 2) T_j < 150°C	P_5.5.2
Drain to source clamping voltage $V_{DS(AZ)} = [V_S - V_{OUT}]$	$V_{DS(AZ)}$	65	70	75	V	I_{DS} = 5 mA	P_5.5.5
Output leakage current per channel	$I_{L(OFF)}$	–	0.1	0.5	µA	1) V_{IN} floating V_{OUT} = 0 V $T_j \leq$ 85°C	P_5.5.6
Output leakage current per channel	$I_{L(OFF)_150}$	–	1	5	µA	V_{IN} floating V_{OUT} = 0 V T_j = 150°C	P_5.5.4

Table 4 Electrical Characteristics: Power Stage (cont'd)

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified).
Typical values are given at V_S = 24 V, T_j = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Inverse current capability	$I_{L(INV)}$	–	2.2	–	A	[1) 3)] $V_S < V_{OUTX}$ $t < 2$ min	P_5.5.7
Slew rate (switch on) 30% to 70% of V_S	$\Delta V/\Delta t_{ON}$	0.3	0.75	1.9	V/µs	R_L = 12 Ω V_S = 24 V	P_5.5.8
Slew rate (switch off) 70% to 30% of V_S	$-\Delta V/\Delta t_{OFF}$	0.3	0.75	1.9	V/µs	R_L = 12 Ω V_S = 24 V	P_5.5.9
Turn-ON time to VOUT = 90% V_S	t_{ON}	20	55	100	µs	R_L = 12 Ω V_S = 24 V	P_5.5.11
Turn-OFF time to VOUT = 10% V_S	t_{OFF}	20	55	100	µs	R_L = 12 Ω V_S = 24 V	P_5.5.12
Turn-ON / OFF matching t_{OFF} - t_{ON}	Δt_{SW}	-50	0	50	µs	R_L = 12 Ω V_S = 24 V	P_5.5.13
Turn-ON time to VOUT = 10% V_S	t_{ON_delay}	–	25	50	µs	R_L = 12 Ω V_S = 24 V	P_5.5.14
Turn-OFF time to VOUT = 90% V_S	t_{OFF_delay}	–	25	50	µs	R_L = 12 Ω V_S = 24 V	P_5.5.15

1) Not subject to production test; specified by design.

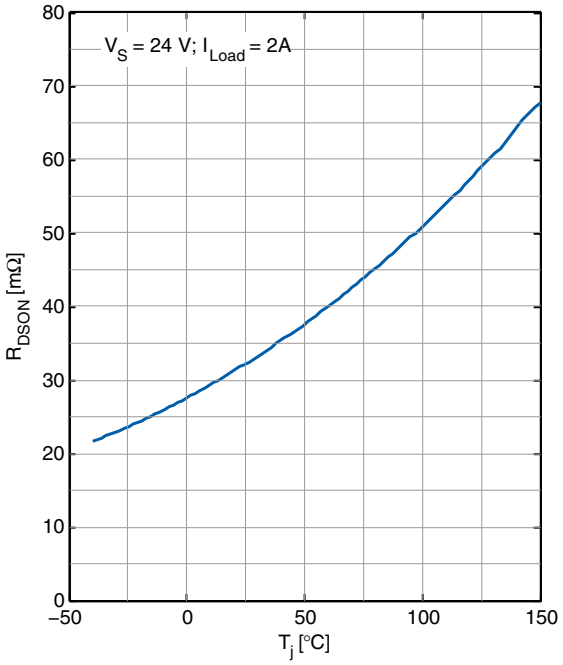
2) This parameter describes the nominal load capability per channel from an electrical point of view respecting a maximum $T_j \leq 150$°C. Please note that depending on the individual thermal design of a real application (and a potentially insufficient thermal budget resulting hereof) additional restrictions for $I_{L(NOM)}$ may occur for pure thermal reasons in order not to exceed the maximum allowed junction temperature T_j = 150°C. The latter needs to be considered especially for cases where both channels are operating simultaneously under high load conditions and at high ambient temperature T_{AMB}. For further details about potential derating of the nominal load current due to thermal restrictions please refer to **"Thermal Considerations" on Page 38**.

3) Please note that during inverse current condition the protection features are not operational.

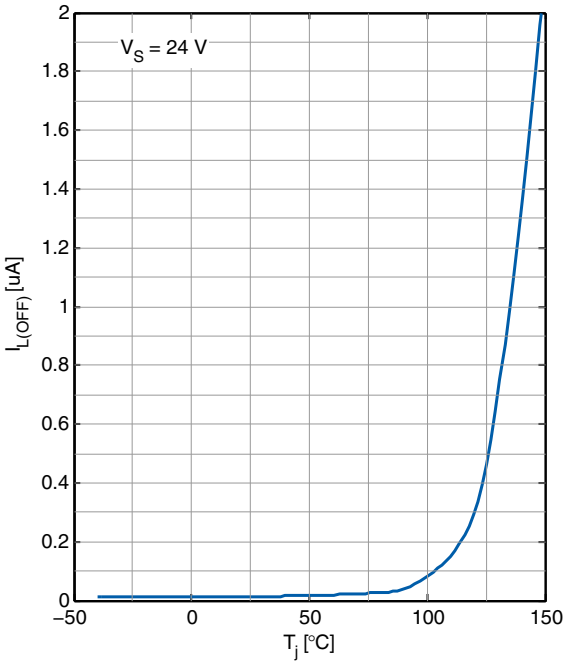
5.6 Typical Performance Characteristics Power Stage

Typical Performance Characteristics

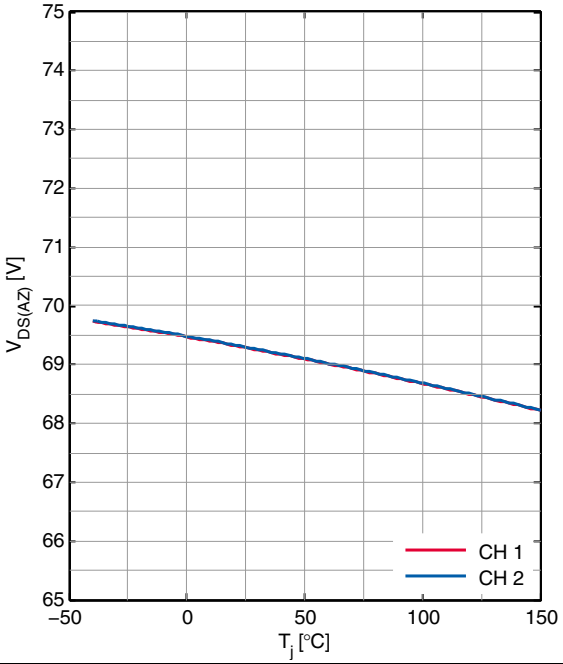
ON-State Resistance R_{DSON} versus Junction Temperature T_j



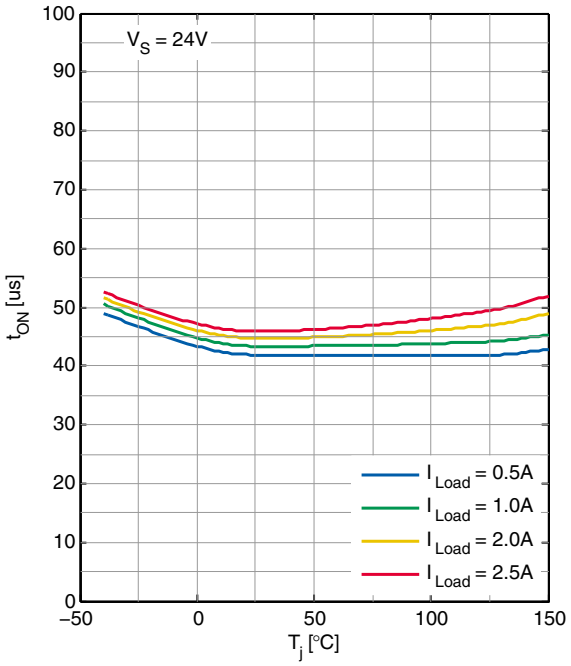
Leakage Current per channel $I_{L(OFF)}$ versus Junction Temperature T_j



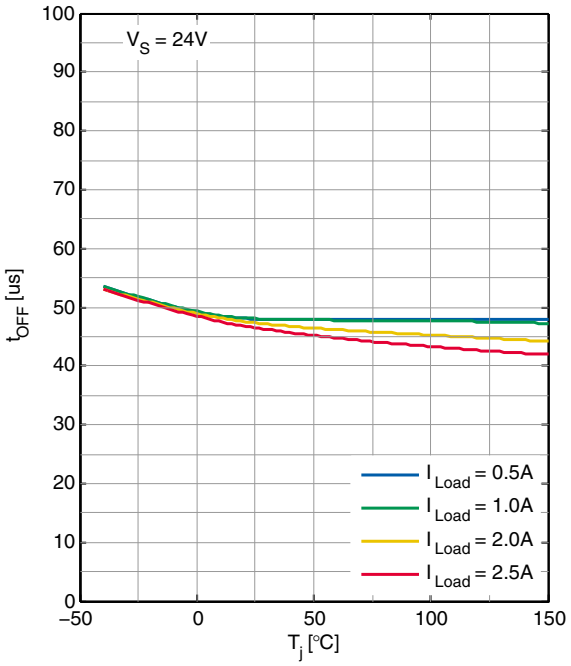
Output Clamp Voltage $V_{DS(AZ)}$ versus Junction Temperature T_j



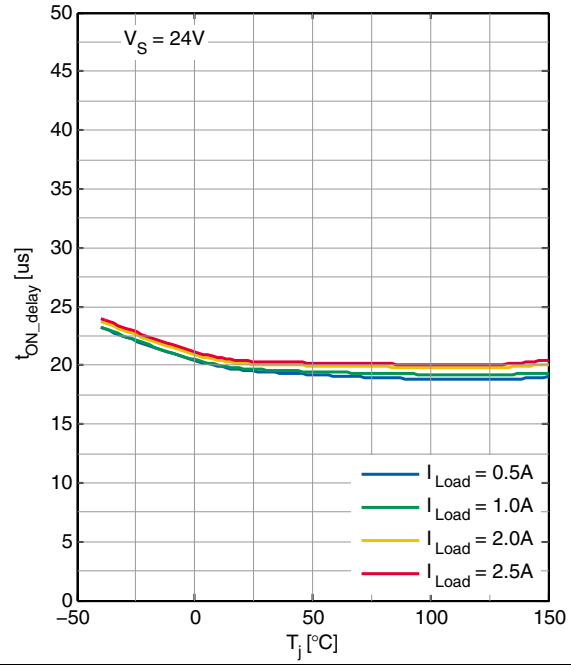
Turn-ON time t_{ON} to V_{OUT} = 90% versus Junction Temperature T_j



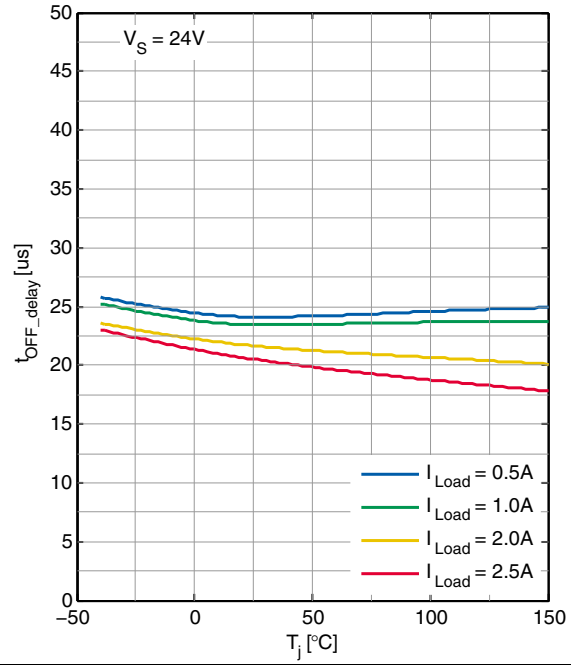
Turn-OFF time t_{OFF} to V_{OUT} = 90% versus Junction Temperature T_j



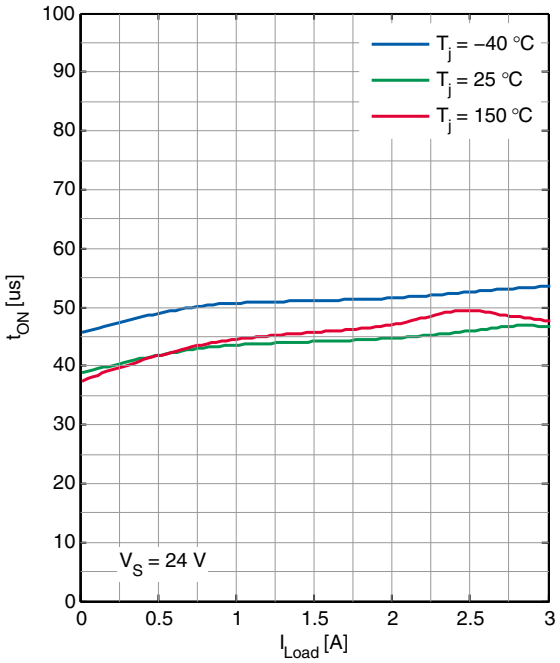
Turn-ON delay time t_{ON_delay} to V_{OUT} = 10% versus Junction Temperature T_j



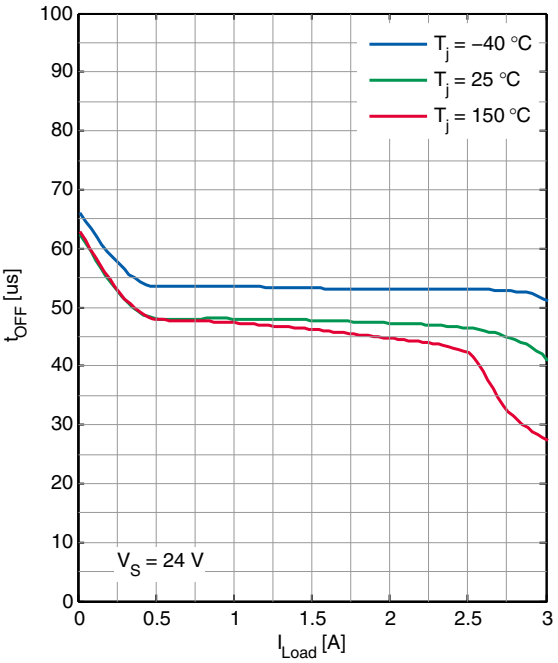
Turn-OFF delay time t_{OFF_delay} to V_{OUT} = 10% versus Junction Temperature T_j



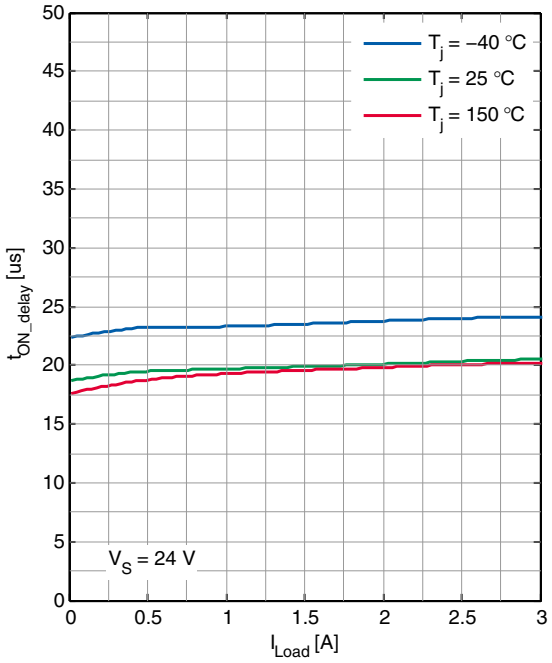
Turn-ON time t_{ON} to V_{OUT} = 90% versus Load Current I_{Load}



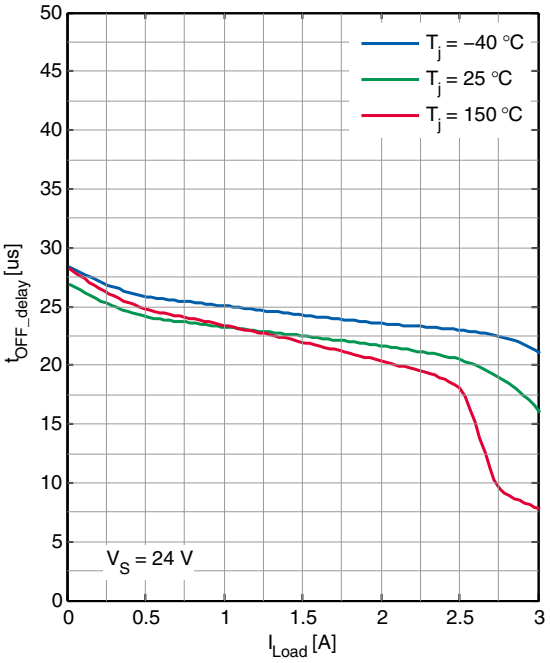
Turn-OFF time t_{OFF} to V_{OUT} = 90% versus Load Current I_{Load}



Turn-ON delay time t_{ON_delay} to V_{OUT} = 10% versus Load Current I_{Load}



Turn-OFF delay time t_{OFF_delay} to V_{OUT} = 10% versus Load Current I_{Load}



6 Protection Functions

The device provides integrated protection functions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Protection functions are designed to prevent the destruction of the ITS4040D-EP-D due to fault conditions described in the data sheet. Please note that fault conditions are not considered as normal operation conditions and the protection functions are neither designed for continuous operation nor for repetitive operation.

6.1 Loss of Ground Protection

In case of loss of module ground when the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied at the input pins.

In an application where the inputs are directly controlled by logic levels < V_S (e.g. by a microcontroller without galvanic isolation), it is recommended to use input resistors [1] between the external control circuit (microcontroller) and the ITS4040D-EP-D to protect also the external control circuit in case of loss of device ground.

In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS. **Figure 14** sketches the situation.

Z_{GND} is recommended to be a resistor in series to a diode.

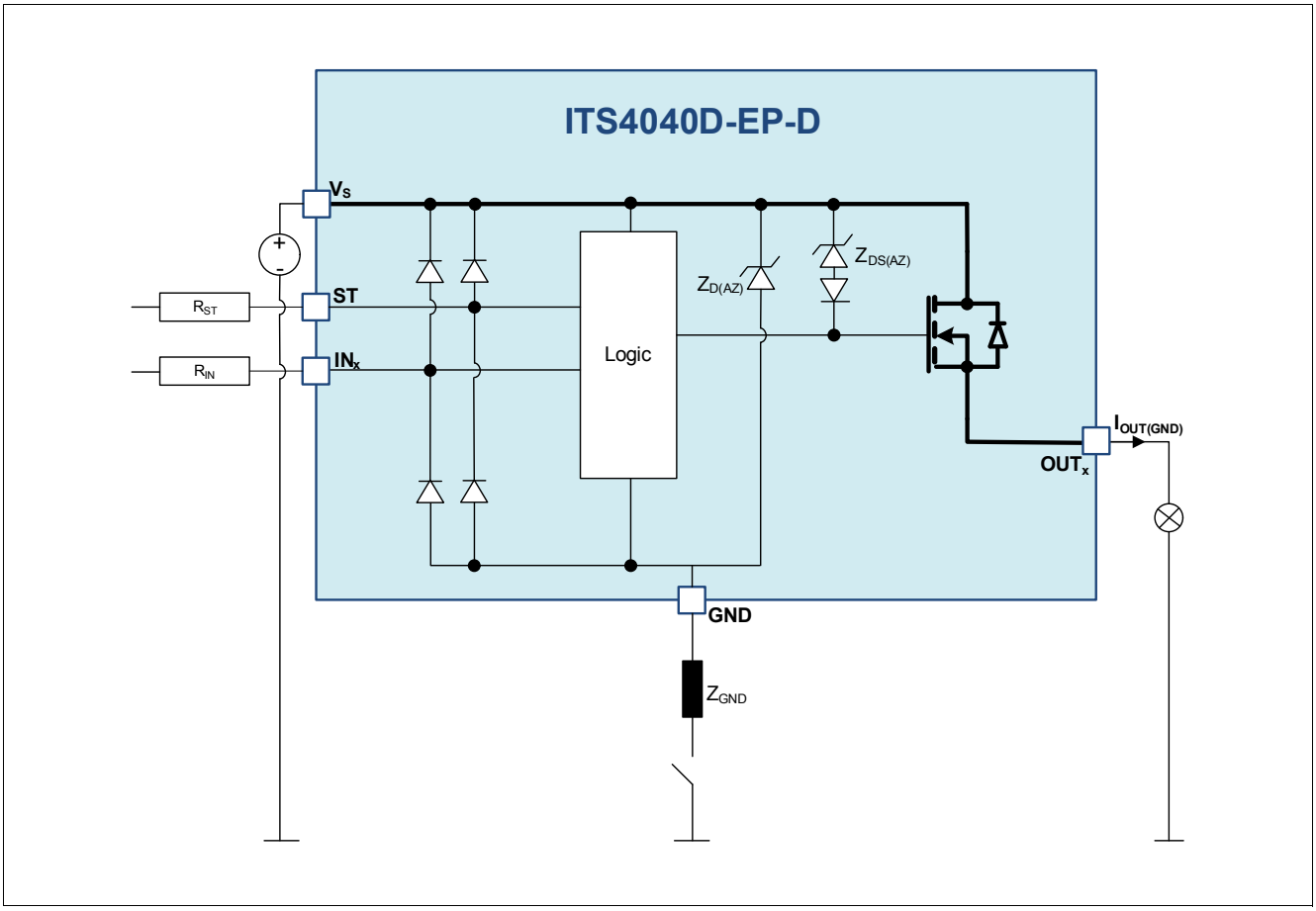


Figure 14 Loss of Ground Protection with External Components

1) Recommended value is 10 kΩ

6.2 Undervoltage Protection

If the supply voltage falls below $V_{S(UV)}$ the undervoltage protection of the device is triggered. $V_{S(UV)}$ represents hence the minimum voltage for which the switch still can hold ON. Once the device is off $V_{S(OP)_MIN}$ represents the lowest voltage where the device is turning on again (and thus the channels can be switched again). If the supply voltage is below the undervoltage threshold $V_{S(UV)}$, the channels of the device are OFF (or turning OFF). As soon as the supply voltage is recovering and exceeding the threshold of the functional supply voltage $V_{S(OP)_MIN}$, the device is re-powering and its channels can be switched again. In addition the protection functions as well as diagnosis become operational once $V_{S(OP)_MIN}$ is reached. **Figure 15** sketches the undervoltage mechanism.

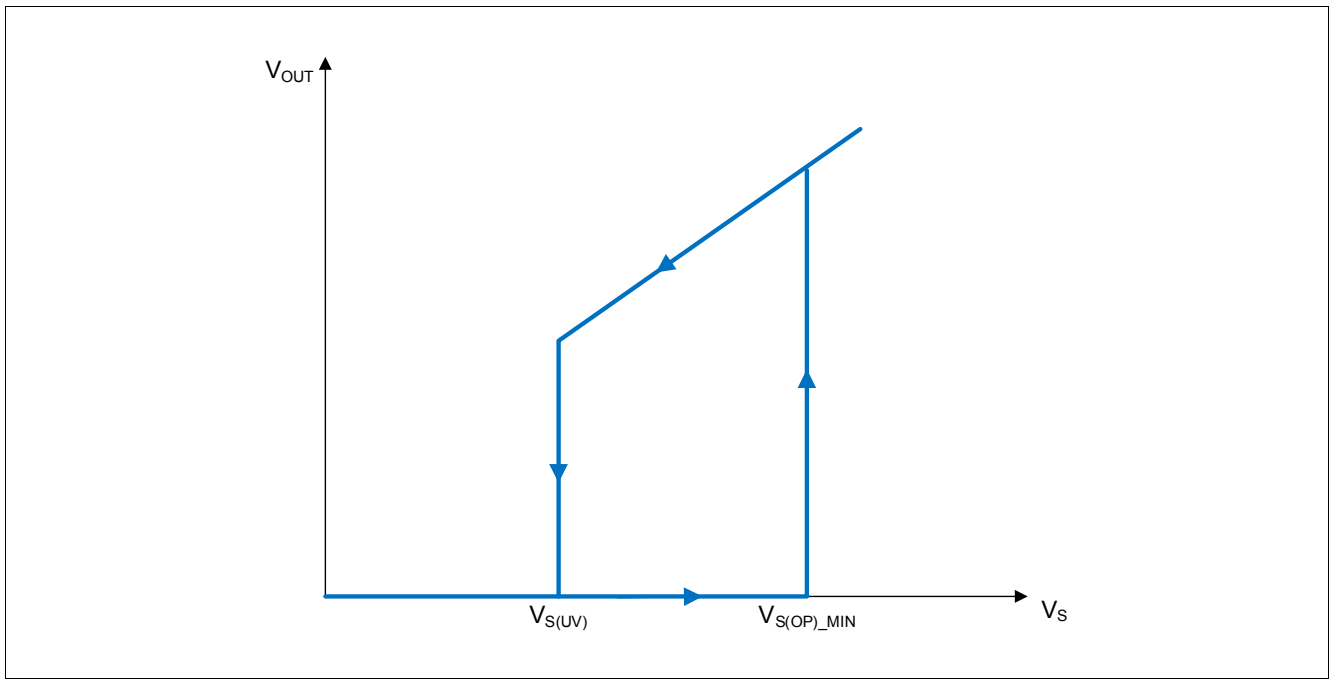


Figure 15 Undervoltage Behavior

6.2.1 Overvoltage Protection

There is an integrated clamping mechanism for overvoltage protection ($Z_{D(AZ)}$). To ensure this mechanism operates properly in the application, the current in the Zener diode $Z_{D(AZ)}$ must be limited by a ground resistor. **Figure 16** shows a typical application to withstand overvoltage issues. In case of supply voltage higher than $V_{S(AZ)}$, the voltage across supply to ground path is clamped. As a result, the internal ground potential rises to V_S - $V_{S(AZ)}$. Due to the ESD Zener diodes, the potential at pin INx rises almost to that potential, depending on the impedance of the connected circuitry [1]. In the case the device was ON, prior to overvoltage, the ITS4040D-EP-D remains ON. In case the ITS4040D-EP-D was OFF, prior to overvoltage, the power transistor can be activated. In case the supply voltage is above $V_{S(SC)}$ and below $V_{DS(AZ)}$, the output transistor is still operational and follows the input. If at least one channel is in ON-state, parameters are no longer within specified range and lifetime is reduced compared to the nominal supply voltage range. This especially impacts the short circuit robustness, as well as the maximum energy E_{AS} capability. Z_{GND} is recommended to be either a resistor (27 Ω) in series to a diode or alternatively a 150 Ω power resistor.

1) Hence, the usage of external input resistors needs to be considered.

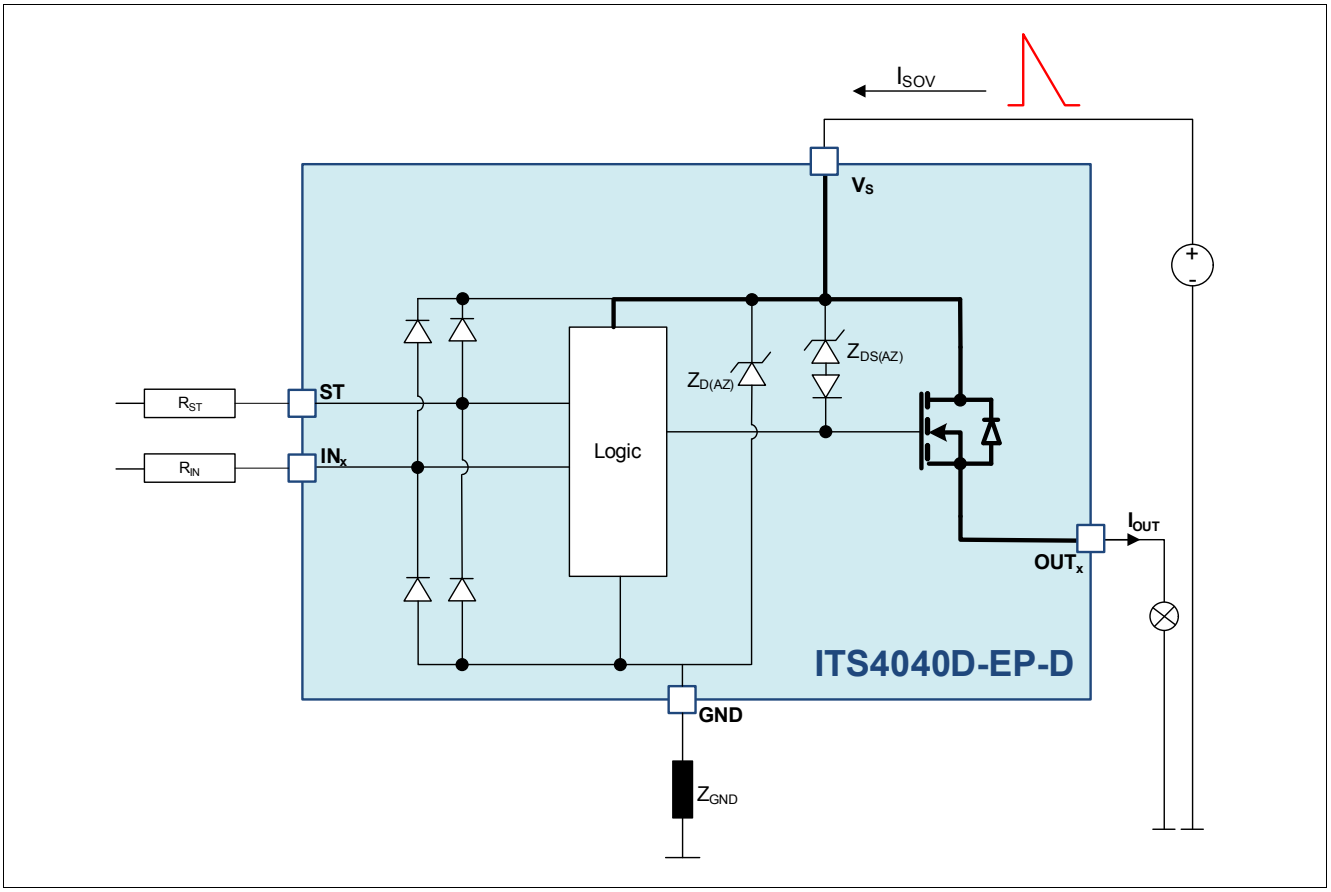


Figure 16 Overvoltage Protection with External Components

6.3 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diodes of the affected power DMOS-channels will dissipate power. The current flowing through the intrinsic body diode is limited externally by the load itself. But in addition the current into the ground path and the logic pins must be limited by an external resistor to the maximum allowed current described in **Chapter 4.1**. **Figure 17** shows a typical application. Z_{GND} resistor is used to limit the current through the Zener protection of the device. Z_{GND} is recommended to be either a resistor (~ 27 Ω) in series to a diode or alternatively a power resistor (~ 150 Ω).

During reverse polarity no protection functions are available.

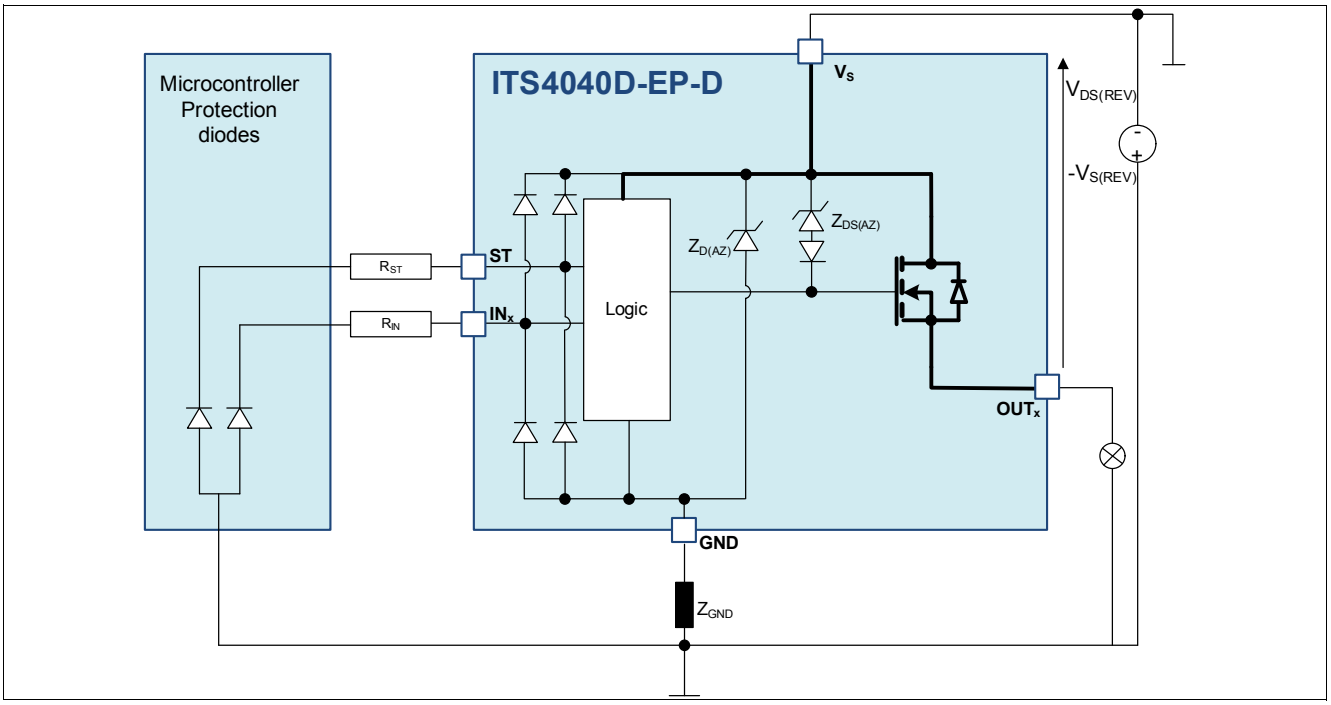


Figure 17 Reverse Polarity Protection with External Components

6.4 Overload Protection

In case of overload, such as high inrush current of a cold lamp filament, or short circuit to ground, the ITS4040D-EP-D offers a set of protection mechanisms which is illustrated in **Figure 18**.

6.4.1 Current Limitation

As a first step, the instantaneous power in the switch is contained within a safe range by limiting the current to the maximum current allowed in the switch $I_{L(LIM)}$. During this time, where the current is limited to $I_{L(LIM)}$ the DMOS temperature is increasing caused by the voltage drop V_{DS} over the DMOS.

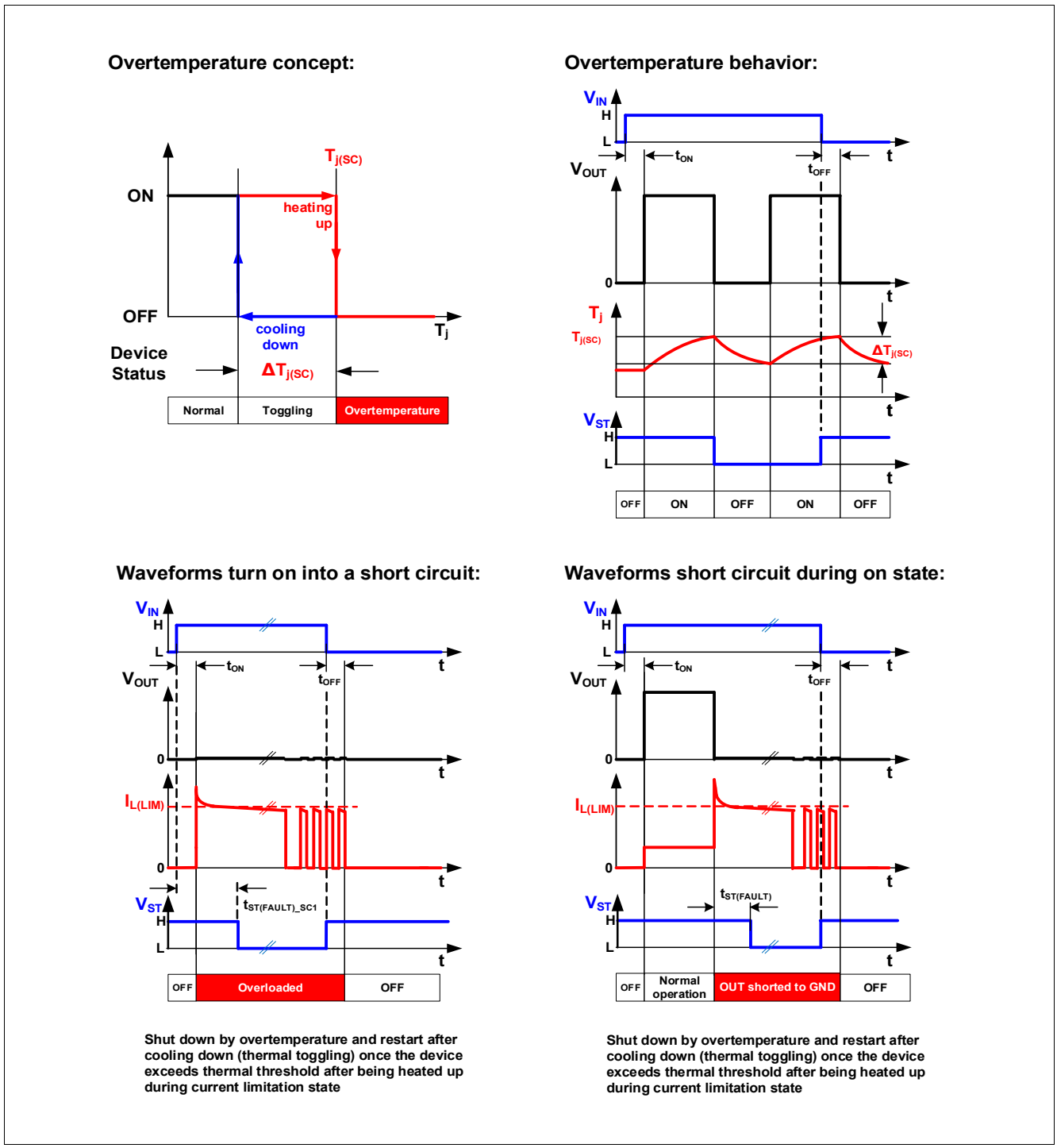


Figure 18 Protection behavior of the ITS4040D-EP-D

6.4.2 Temperature Limitation in the Power DMOS

Each channel incorporates one temperature sensor. Activation of this temperature sensor will cause an overheated channel to switch OFF to prevent destruction. Any protective overtemperature shutdown event triggered within a channel is switching OFF the output of the corresponding channel until the temperature reaches an acceptable value again.

A restart functionality is implemented that is switching the channel ON again after the DMOS temperature has sufficiently cooled down.

6.5 Electrical Characteristics: Protection Functions

Table 5 Electrical Characteristics: Protection Functions[1)]

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified).
Typical values are given at V_S = 24 V, T_j = 25°C

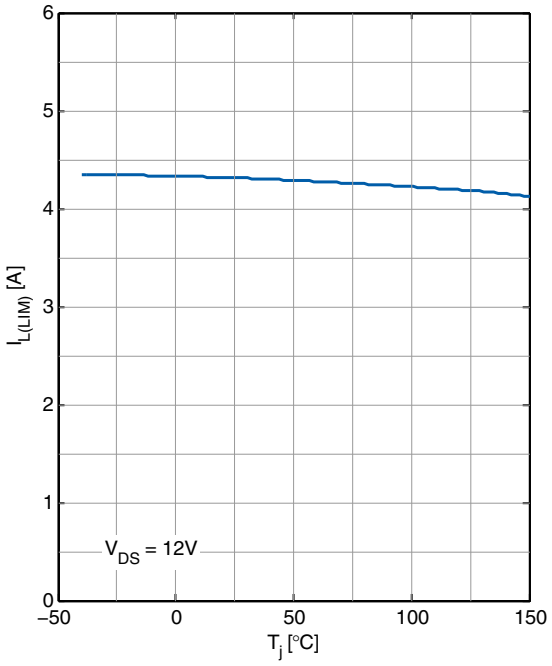
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Loss of Ground							
Output leakage current while GND disconnected	$I_{OUT(GND)}$	–	0.1	–	mA	[2) 3)] V_S = 24 V	P_6.5.1
Reverse Polarity							
Drain source diode voltage during reverse polarity	$V_{DS(REV)}$	–	650	700	mV	I_L = -2 A T_j = 150°C	P_6.5.2
Overvoltage							
Overvoltage protection	$V_{S(AZ)}$	65	70	75	V	[4)] I_{SOV} = 5 mA	P_6.5.3
Overload Condition							
Load current limitation	$I_{L(LIM)}$	3.3	4.1	4.9	A	–	P_6.5.4
Thermal shutdown temperature	$T_{j(SC)}$	150	175	200	°C	[3)] –	P_6.5.6
Thermal shutdown hysteresis	$\Delta T_{j(SC)}$	–	30	–	K	[3)] –	P_6.5.7

1) Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC from destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed neither for continuous nor repetitive operation.
2) All pins are disconnected except V_S and OUT.
3) Not subject to production test; specified by design.
4) For practical cases it is recommended to place a resistor in the range of ≥ 27 Ω into the GND path to limit the GND current associated with overvoltage events.

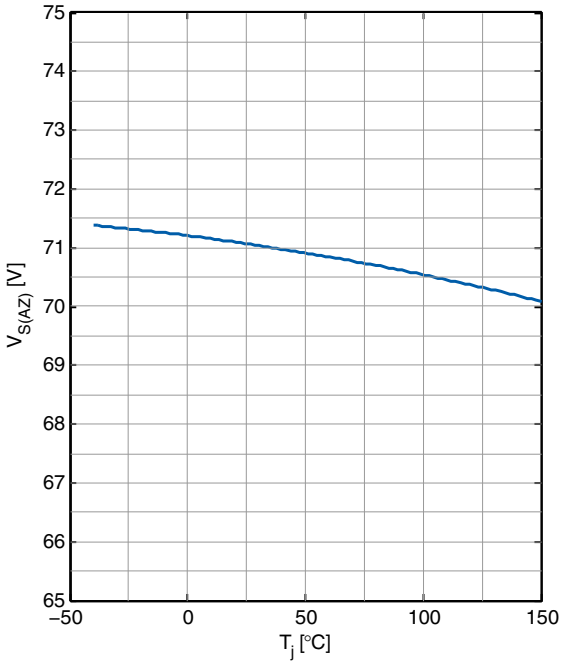
6.6 Typical Performance Characteristics Protection Functions

Typical Performance Characteristics

Current Limit $I_{L(LIM)}$ versus Junction Temperature T_j



Clamping Voltage $V_{S(AZ)}$ versus Voltage T_j



7 Diagnostic Functions

For diagnosis purpose, the ITS4040D-EP-D provides a digital signal at pin ST. This signal is called STATUS. The STATUS pin is realized as open drain output and must be connected to an external pull-up resistor. During normal operation the STATUS signal is logic “High” (H). During short circuit to ground or overtemperature condition the STATUS signal is logic “Low” (L). **Table 6** shows the corresponding truth table.

Table 6 Diagnostic Truth Table [1) 2)]

Device Operation	IN1	IN2	OUT1	OUT2	ST	Comment
Normal Operation	L	L	OFF	OFF	H	External pull up at ST pin
	H	H	ON	ON	H	
	H	L	ON	OFF	H	
	L	H	OFF	ON	H	
Short Circuit to GND on CH1	H	H	ON	ON	L	3)
	H	L	ON	OFF	L	
Short Circuit to GND on CH2	H	H	ON	ON	L	
	L	H	OFF	ON	L	
Short Circuit to GND on CH 1 + 2	H	H	ON	ON	L	
Overtemperature on CH1	H	H	OFF [4)]	ON	L	
	H	L	OFF [4)]	OFF	L	
Overtemperature on CH2	H	H	ON	OFF [4)]	L	
	L	H	OFF	OFF [4)]	L	
Overtemperature on CH 1 + 2	H	H	OFF [4)]	OFF [4)]	L	

1) Please refer to **Table 7** for more details.
2) Not subject to production test; specified by design.
3) Device not in specified $R_{DS(ON)}$.
4) Channel remains OFF during cooling-down phase of power stage; then channel tries to re-start.

7.1 Electrical Characteristics Diagnostic Function

Table 7 Electrical Characteristics: Diagnostics

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified).
Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Diagnostic Timing in Overload Condition							
STATUS settling time for overload detection	$t_{ST(FAULT)}$	–	25	–	µs	[1] V_S = 24 V load jump of R_L: 12 Ω -> 3.3 Ω Please refer to **Figure 18** for more details	P_7.1.1
STATUS settling time for channel start-up into existing overload [2]	$t_{ST(FAULT)_SC1}$	-	35	90	µs	V_{DS} ≥ 8 V; Please refer to **Figure 18** for more details	P_7.1.9
"Low" level STATUS voltage	$V_{ST(L)}$	–	–	0.5	V	[3] I_{ST} = 1.6 mA	P_7.1.3
"High" level STATUS voltage	$V_{ST(H)}$	2	–	– [4]	V	$V_S > V_{ST}$	P_7.1.4
Current through STATUS pin (Operating Range)	I_{ST}	–	–	1.6	mA	V_{ST} < 0.5 V	P_7.1.5
Channel fault detection interrogation time (Sequential Pulse Width)	T_x	3	–	6	µs	V_{ST} < 0.5 V [5]	P_7.1.2
STATUS signal "High" valid window after T_x on fault affected channel	T_m	40	80	150	µs	– [5]	P_7.1.6
Minimum delay between subsequent T_x interrogation windows	$T_{X\text{-}2\text{-}X}$	200	–	–	µs	– [1]	P_7.1.8
Maximum delay time between T_x ("High" to "Low") on fault affected channel and STATUS "High" signal T_m	T_D	–	8	–	µs	– [1]	P_7.1.7

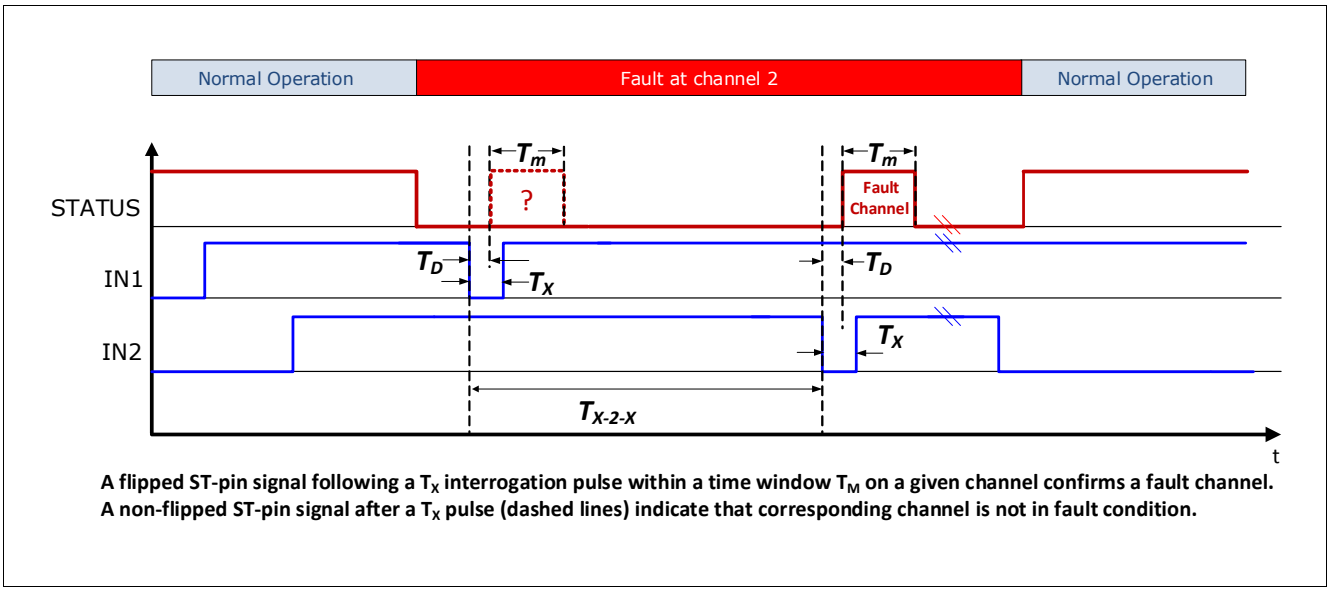
1) Not subject to production test, specified by design
2) This parameter describes the status settling time when a channel is switched on into an already existing overload condition. This parameter is referenced to the edge of the input pin IN that switches the channel into overload.
3) Levels referenced to device ground.
4) Depends on pull-up circuit that is used within application; maximum ratings of STATUS pin need to be respected.
5) Please refer to **"Channel Fault Detection" on Page 31** for more details.

7.2 Channel Fault Detection

The ITS4040D-EP-D is equipped with an intelligent channel fault detection system, which allows with the aid of a microcontroller to identify and communicate the channel on which the fault occurs.

Diagnostic Functions

During normal operation the STATUS pin is kept “High” by the external pull-up resistor as shown in **Table 6**. If - in case of a fault - the application requires the information on which of the channels the fault occurs when a “Low” STATUS is flagged, then the microcontroller can be programmed according to the sequence depicted as an example in **Figure 19**. The figure shows a case where both channels are active. During normal operation of channels 1 and 2 the status signal is “High”. Let us now assume that a fault occurs on channel 2. The status signal goes low to flag an error to the microcontroller. In order to distinguish whether the fault occurs on channel 1 or channel 2 the microcontroller must send a low pulse T_X sequentially to each input pin of the activated channels. The pulses T_X versus time are shown in **Figure 19**. Time T_x should be between 3 µs up to 6 µs in order to ensure that the output does not react to this “Low” pulse at the input. The status signal goes “High” for a short period of time T_m only after the channel on which the fault occurs gets a “Low” pulse from the microcontroller, which in this case is after channel 2 receives a low pulse for a time T_x. By this means, the microcontroller is able to detect on which channel the fault occurs. Once the microcontroller receives this information, it can switch OFF the channel on which the fault occurs (channel 2 in this case) via the input pin IN2. For the maximum delay time T_D between T_x going “Low” and T_m going “High” a value of 8 µs needs to be taken into account.



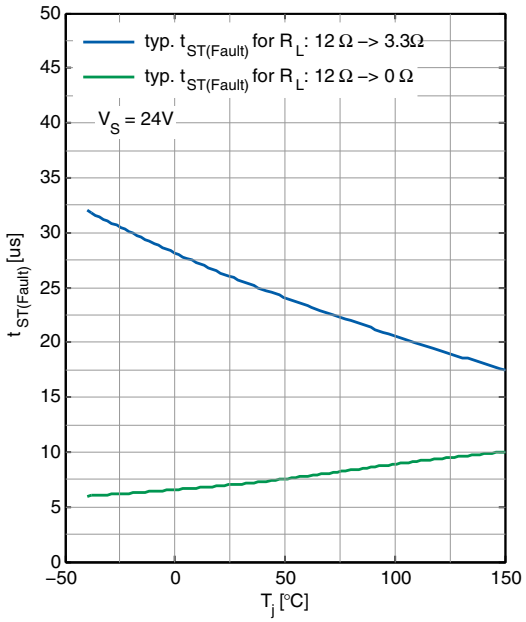
A flipped ST-pin signal following a T_X interrogation pulse within a time window T_M on a given channel confirms a fault channel. A non-flipped ST-pin signal after a T_X pulse (dashed lines) indicate that corresponding channel is not in fault condition.

Figure 19 Channel Fault Detection Timing Diagram

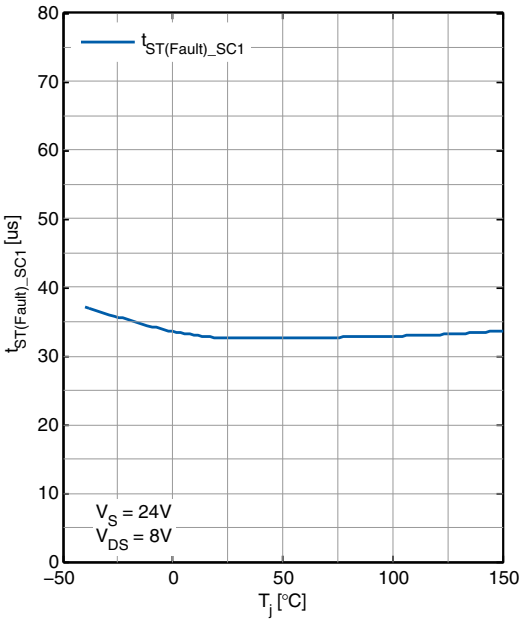
7.3 Typical Performance Characteristics Diagnostic Functions

Typical Performance Characteristics

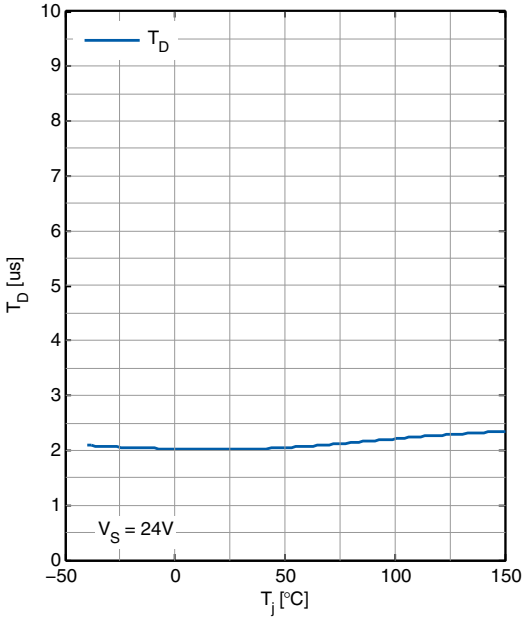
Status Settling Time $t_{ST(FAULT)}$ versus Junction Temperature T_j (overload during ON)



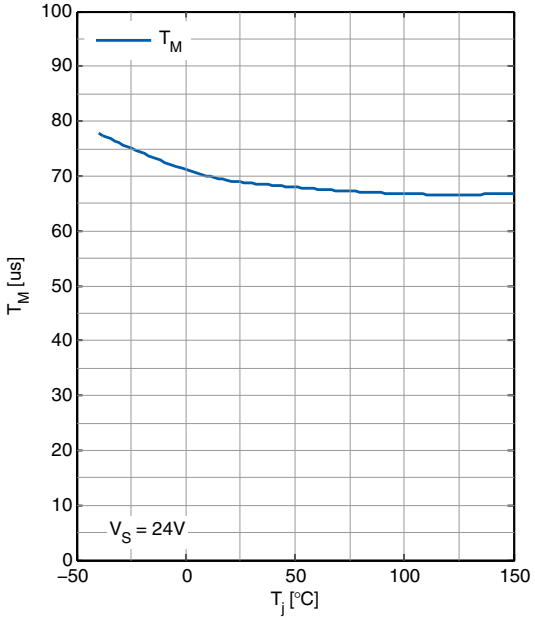
Status Settling Time $t_{ST(Fault)_SC1}$ versus Junction Temperature T_j (switch on into overload)



Maximum Delay Time T_D (T_X 'H->L' to ST 'L->H') vs Junction Temperature T_j



ST "HIGH" Valid window (after T_X) T_M versus Junction Temperature T_j



8 Input Pins

8.1 Input Circuitry

The input circuitry is compatible with 3.3 V and 5 V microcontrollers as well as input levels up to V_S [1]. The concept of the input pin is to react to voltage thresholds which are referenced to device ground. An implemented Schmitt trigger avoids any undefined state if the voltage on the input pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in a linear or undefined state. **Figure 20** shows the electrical equivalent input circuitry. In case a channel is permanently not needed, the corresponding input pin shall not be left floating but tied with a serial resistor to device ground (not module ground). The recommended value for the serial resistor is 2.2 kΩ.

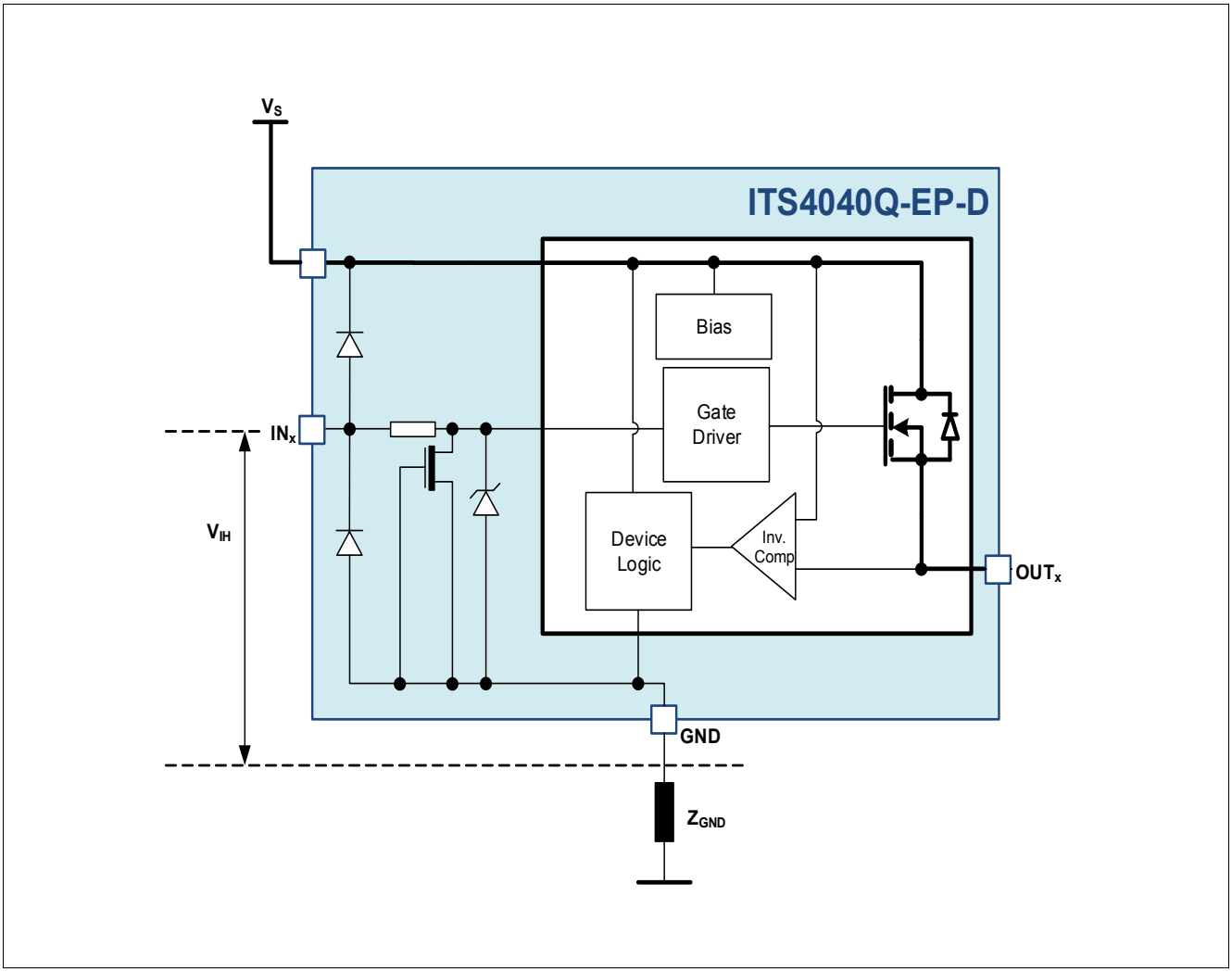


Figure 20 Input Pin Circuitry

8.2 Input Pin Voltage

The input pin IN uses a comparator with hysteresis. Switching “ON / OFF” of the channels takes place in a defined region, set by the thresholds $V_{IN(L)}$,max and $V_{IN(H)}$,min. The exact values where the “ON” and “OFF” take

1) V_{IN} must not exceed V_S. The relation $V_{IN} \leq V_S$ must always be fulfilled.

place depend on the process, as well as the temperature. To avoid cross talk and parasitic turn-ON or turn-OFF, a hysteresis is implemented. This ensures an improved immunity to noise.

8.3 Electrical Characteristics: Input Pins

Table 8 Electrical Characteristics: Input Pins

8 V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified).
Typical values are given at V_S = 24 V, T_j = 25 °C

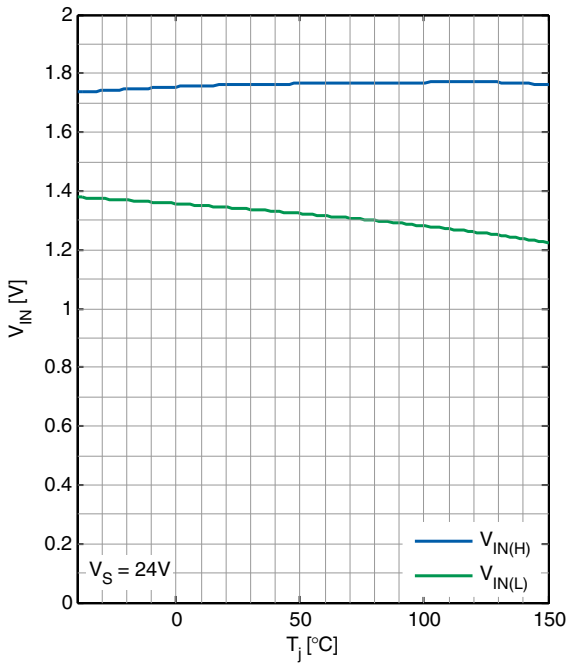
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
INput Pins Characteristics							
"Low" level input voltage range	$V_{IN(L)}$	-0.3	–	0.8	V	[1] –	P_8.3.1
"High" level input voltage range	$V_{IN(H)}$	2	–	36	V	$V_S > V_{IN}$ [1]	P_8.3.2
Input voltage hysteresis	$V_{IN(HYS)}$	–	450	–	mV	[2] –	P_8.3.3
"Low" level input current	$I_{IN(L)}$	–	37	70	µA	V_{IN} = 0.8 V	P_8.3.4
"High" level input current	$I_{IN(H)}$	–	44	70	µA	V_{IN} = 24 V	P_8.3.5

1) Levels referenced to device ground.
2) Not subject to production test; specified by design.

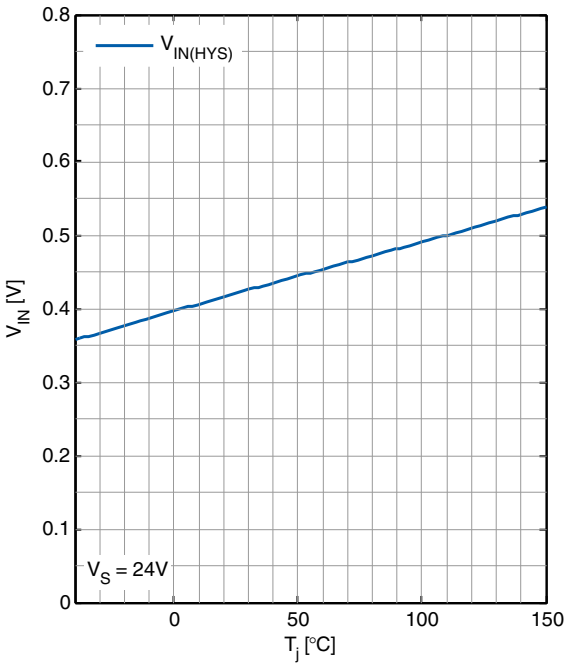
8.4 Typical Performance Characteristics Input Pins

Typical Performance Characteristics

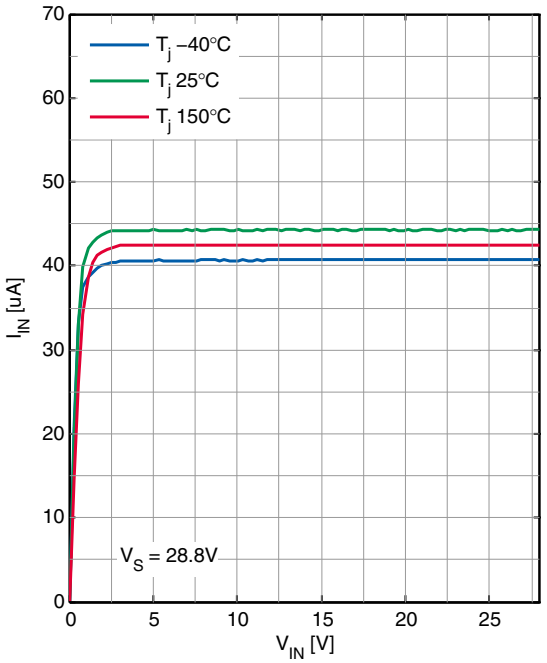
Input Voltage thresholds $V_{IN(L)}$ $V_{IN(H)}$ versus Junction Temperature T_j



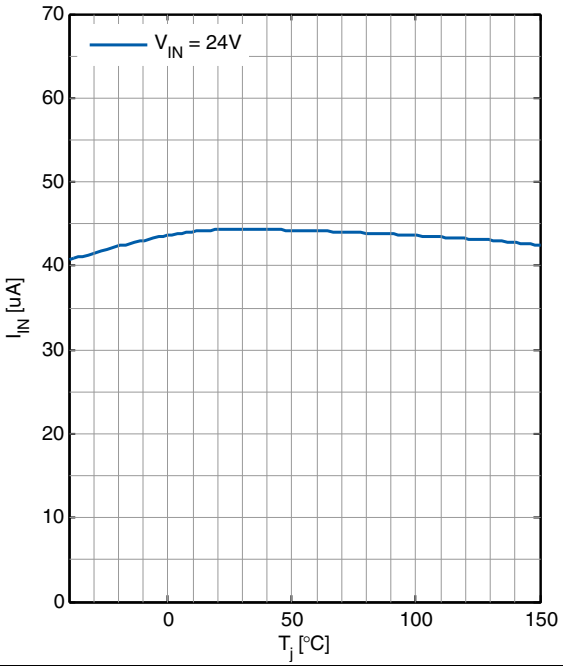
Input Voltage hysteresis $V_{IN(HYS)}$ versus Junction Temperature T_j



Input Pin Current $I_{IN(H)}$ versus Supply Voltage V_S



Input Pin Current $I_{IN(H)}$ versus Junction Temperature T_j



9 Application Information

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

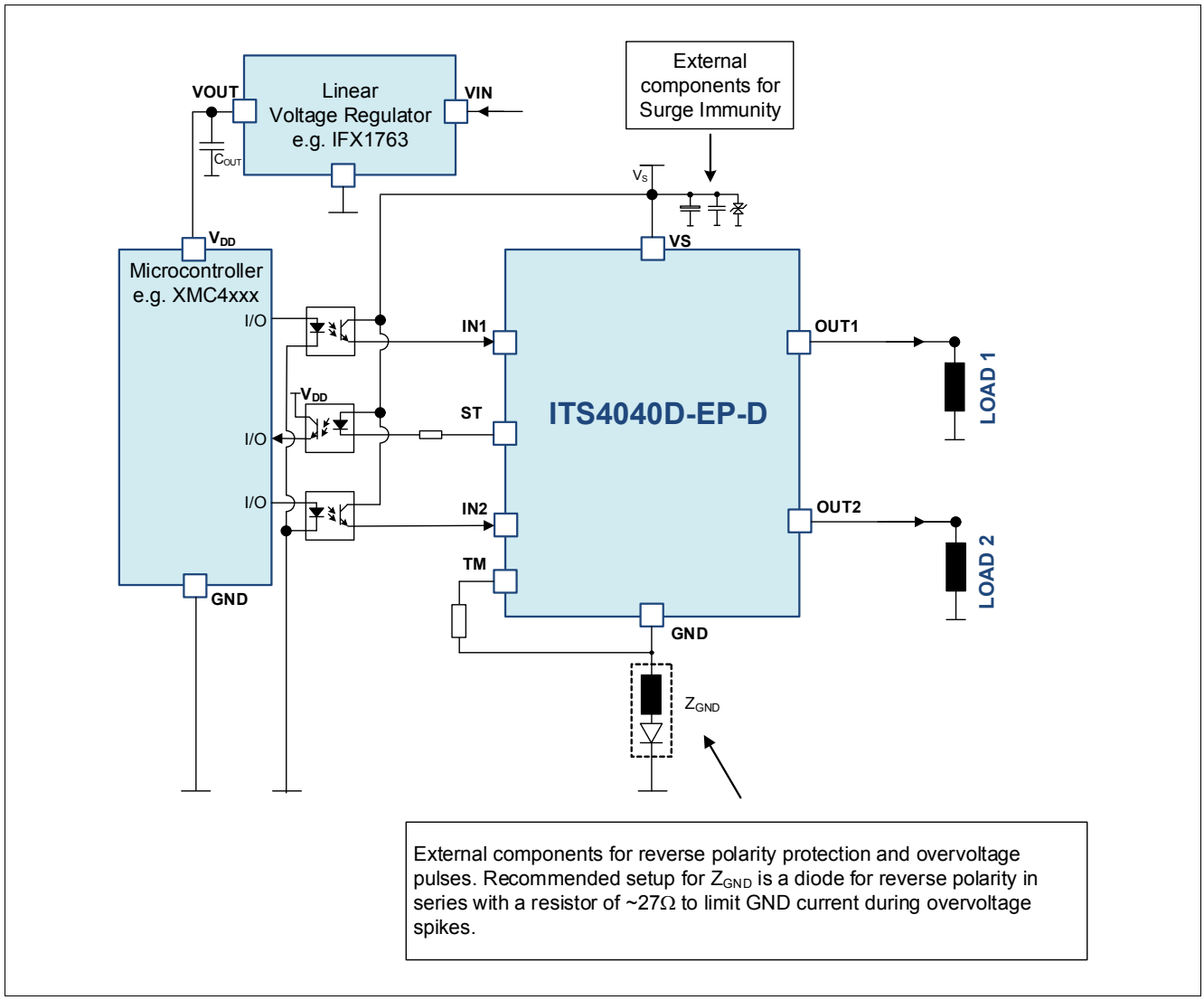


Figure 21 Application Diagram with ITS4040D-EP-D

In **Figure 21** above a simplified application diagram is shown where the inputs are galvanically isolated from V_S with optocouplers. Thanks to the fact that the input pins are 24 V capable they can be directly connected to the optocouplers. Reverse polarity protection can be achieved with external components. In this context it should be noted that input pins of channels which are permanently unused have to be tied with 2.2 kΩ resistance to device ground. In addition the TM-pin must be always tied with a serial resistor to device ground in order to protect the pin in case of reverse polarity. The recommended value for this serial resistor is also 2.2 kΩ. For applications where no galvanic isolation is present between the external control circuitry (e.g microcontroller) and the input pins of the ITS4040D-EP-D serial input resistors need to be placed in order to protect the external control circuitry and the input structures of the ITS4040D-EP-D under fault conditions (like e.g. reverse polarity, loss of ground or overvoltage). For further details please also refer to the corresponding sections in **Chapter 6**. The recommended value for such serial input resistors is 10 kΩ however

application specific optimized values may also depend on the individual application conditions as well as the applied external control circuitry / microcontroller.

9.1 Thermal Considerations

If the cooling possibilities within the application are not sufficient to sink the heat of the dissipated power the junction temperature T_j of the device may exceed its maximum specified rating of 150°C and eventually trigger a thermal shutdown of the overheated channels to protect the device from destruction. Such thermal shutdown events may occur e.g. if one or more channels are operated in overload conditions that are causing the current limitation functionality to become active. If the current limitation of a channel becomes active the power dissipation will rise rapidly and in many cases lead to thermal shutdown events of the corresponding channels within short periods of time.

But also under nominal load conditions the power dissipation can become too high inside an application if it is applied at high environmental temperature T_{AMB} and if at the same time the cooling capability of the PCB is not sufficient. In general the cooling capability of an IC on a PCB within an application can be described for static cases by its thermal resistance from junction-to-ambient R_{thJA}. The thermal resistance R_{thJA} can be improved by adding cooling area on top- or bottom layer of the PCB or by adding inner layers that are connected to the V_S layer with thermal vias. Thermal vias show the best efficiency for heat distribution if directly placed underneath the exposed pad of the ITS4040D. The achievable values for R_{thJA} will differ from application to application. As reference simulation results for a set of standardized JEDEC cases are provided in **Chapter 4.4 “Thermal Resistance” on Page 12**. Actual values in real applications naturally can be lower or higher.

For cases where the achievable thermal resistance R_{thJA} and the hereof resulting thermal budget within an application is not sufficient for a given ambient temperature T_{AMB} there is no other choice than to lower the load current to smaller numbers than the electrically allowed maximum nominal current of 2.6 A. **Figure 22** illustrates how the derating of the nominal current as a function of achievable R_{thJA} at a given T_{AMB} can look like. The graphs show how the thermal budget with its limiting condition T_j = 150°C can be shared between the influencing parameters T_{AMB}, R_{thJA}, I_{Load} depending on the number of active channels n_{CH}. One can see that thanks to the excellent RDSON values of the ITS4040D a derating needs to be applied only in cases with PCB’s showing extremely poor thermal performance.

The calculation of the thermal budget follows simple rules as given in the equations below. It should be noted that the calculation is restricted to static cases where the resulting T_{AMB} and T_j have reached a stable equilibrium.

$$T_j = T_{AMB} + R_{thJA} \times P_{DISS} \tag{9.1}$$

$$P_{DISS} = I_{Load}^2 \times R_{DS(ON)} \times n_{CH} + V_S \times I_{GND} \tag{9.2}$$

Application Information

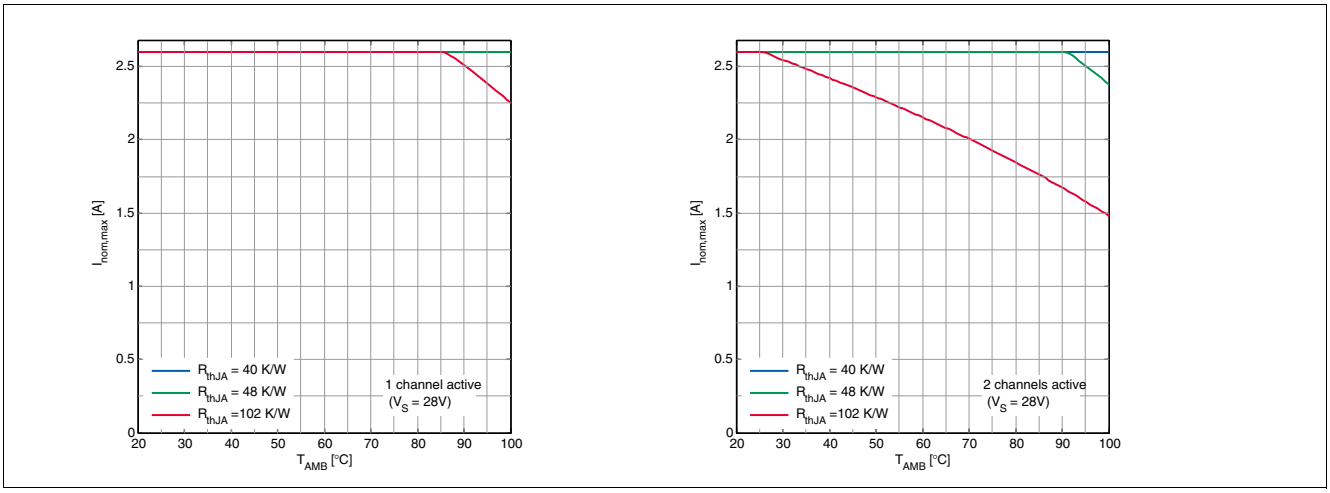


Figure 22 Thermal derating of nominal current due to insufficient cooling performance of PCB

10 Package Outlines

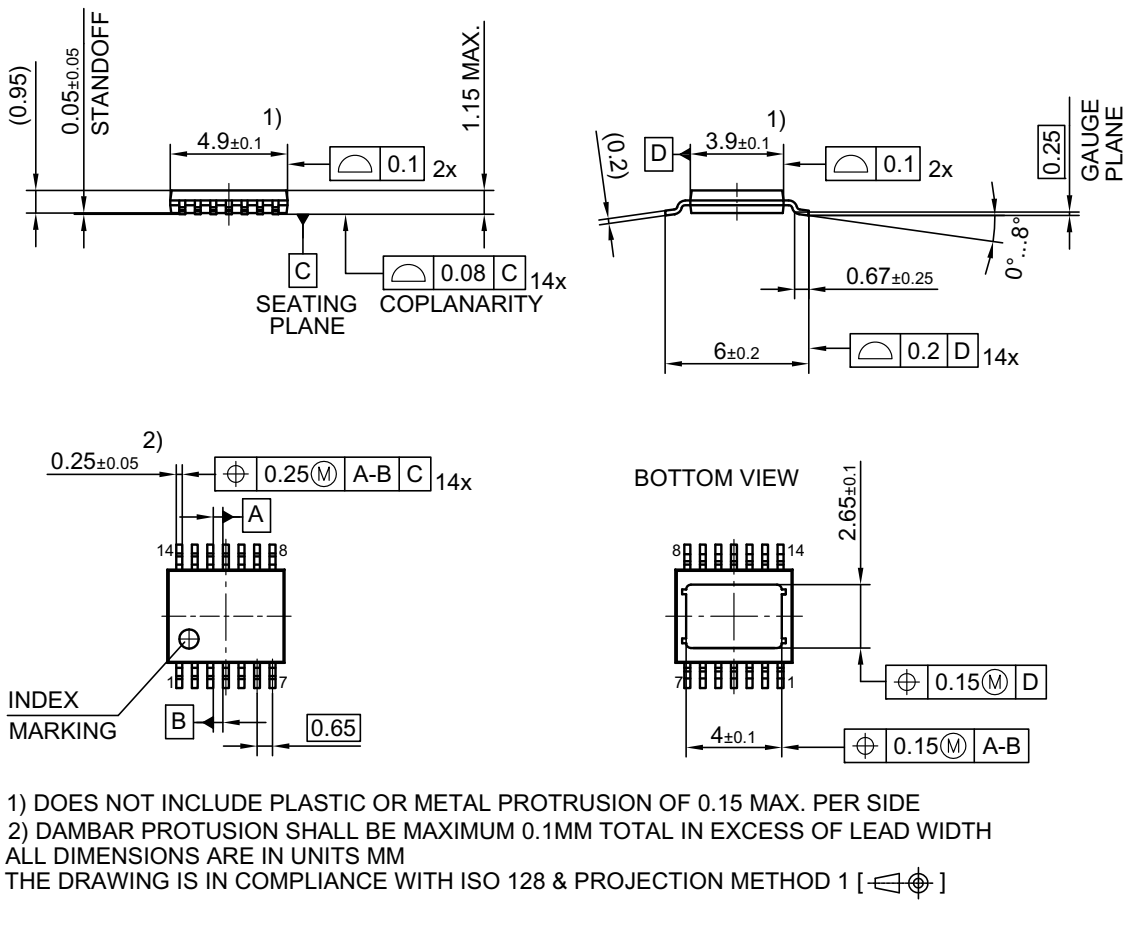


Figure 23 **PG-TSDSO-14** (Plastic Dual Small Outline Package) (RoHS-Compliant)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

11 Revision History

Revision	Date	Changes
1.0	2018-06-14	Data Sheet (Initial Release)

Revision History

Revision History

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