Voltage Variable Attenuator

VACC-22

50Ω 1600 to 2200 MHz

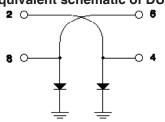
Maximum Ratings

Operating Temperature	-45°C to 85°C		
Storage Temperature	-55°C to 100°C		
Absolute Max. Control Current	10mA		
Absolute Max. RF Input Level	15dBm		

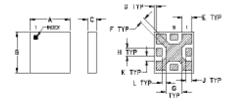
Pin Connections

RF IN	2
V CONTROL 1	8
V CONTROL 2	4
RF OUT	6
GROUND	1,3,5,7

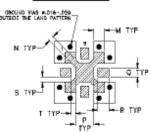
Equivalent schematic of DUT



Outline Drawing



PCB Land Pattern



Suggested Layout, Tolerance to be within ±.002

Outline Dimensions (inch)

A .150 3.81		.050	.008	.036	F .018 0.46	.062	.028	.022	
.017	.014	.036	.018	.062	Q .028 0.71	.037	.017	.014	grams

Features

- frequency range, 1600-2200 MHz
- IP3, 42 dBm typ.
- minimum current at min. attenuation
- low insertion loss
- · aqueous washable
- protected by US Patent 7,030,713



CASE STYLE: GF995

+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Applications

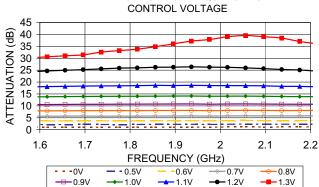
- variable gain amplifier
- feed forward amps
- ALC circuits

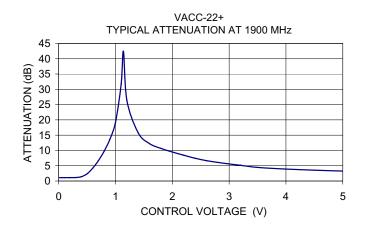
Electrical Specifications

FREQ. (MHz)		INSERTION LOSS (dB)	ATTENUATION (dB)	IP3* (dBm)	RETURN LOSS (dB)		CONTROL VOLTAGE**
		at 0V control voltage			Input	Output	(V)
Min.	Max.	Тур. Мах.	Typ. Min.	Typ. Min.	Тур.	Тур.	
1600	2220	1.2 1.5	25 23	42 38	20	20	0-5

Input IP3 tested with two tones separated by 1 MHz at 7 dBm each and 0V control voltage.

VACC-22+ ATTENUATION Vs. FREQUENCY Vs.





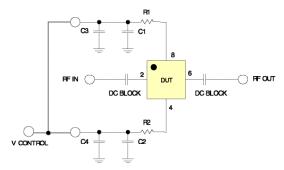
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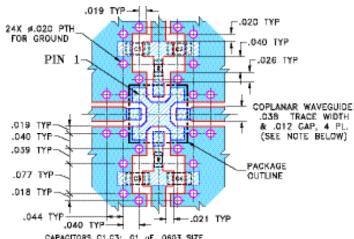
^{*} Using recommended control port biasing

Recommended control port biasing configuration



R1. R2: 2K OHM CHIP RESISTOR (0402, AS CLOSE AS POSSIBLE TO THE DEVICE) C1, C2: 0.01 UF CHIP CAPACITOR (0603) C3, C4: 6.8 PF CHIP CAPACITOR (0603)

Demo Board MCL P/N: TB-250 Suggested PCB Layout (PL-148)



CAPACITORS C1,C3: .01 uF, 0603 SIZE CAPACITORS C2,C4: 6.8 pF, 0603 SIZE RESISTORS R1,R2: 2 KOhm. 0402 SIZE

NOTES: 1. COPLANAR WAVEQUIDE PARAMETERS ARE SHOWN FOR ROGERS ROASSON WITH DIELECTRIC THICKNESS .C2C" ± .C015"; COPPER: 1/2 CZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.

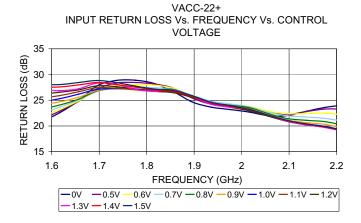
2. IF YOUR PCB DESIGN RULES ALLOW, CROUND VIAS SHOULD BE PLACED UNDER THE LAND PATTERN FOR BETTER RF PERFORMANCE.

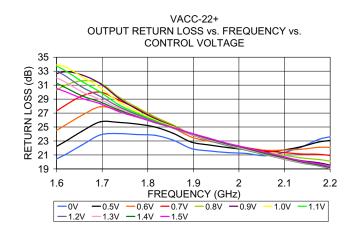
3. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

DENOTES PCB COPPER LAYOUT WITH SMORC (SOLDER MASK

OVER BARE COPPER).

DENOTES COPPER LANG PATTERN FREE OF SOLDER MASK

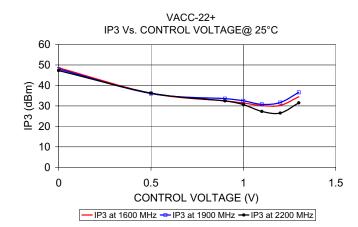


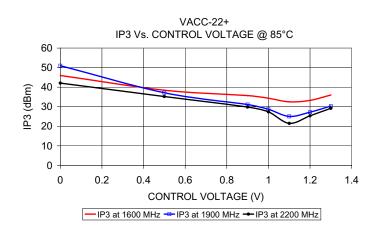


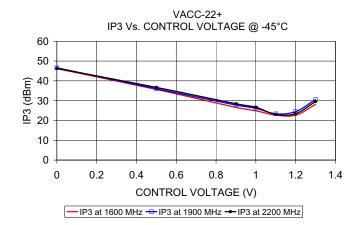
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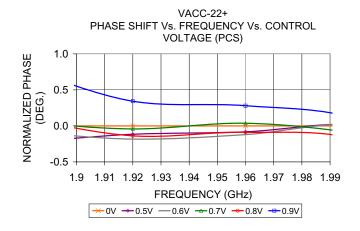
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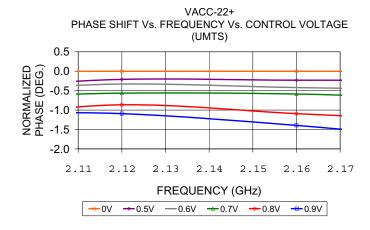
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