14-Bit, Dual, Parallel Input, Multiplying Digital-to-Analog Converter

FEATURES

- ±0.5LSB DNL
- ±0.5LSB INL
- Low Noise: 12nV/√Hz
- Low Power: I_{DD} = 1μA per channel at 2.7V
- 2mA Full-Scale Current, with V_{REF} = 10V
- Settling Time: 0.5μs
- 14-Bit Monotonic
- 4-Quadrant Multiplying Reference Inputs
- Reference Bandwidth: 10MHz
- Reference Input: ±18V
- Reference Dynamics: –105 THD
- Midscale or Zero Scale Reset
- Analog Power Supply: +2.7V to +5.5V
- TSSOP-38 Package
- Industry-Standard Pin Configuration
- Pin Compatible with the 16-Bit DAC8822
- Temperature Range: –40°C to +125°C

APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Digitally Controlled Calibration
- Industrial Control PLCs

DESCRIPTION

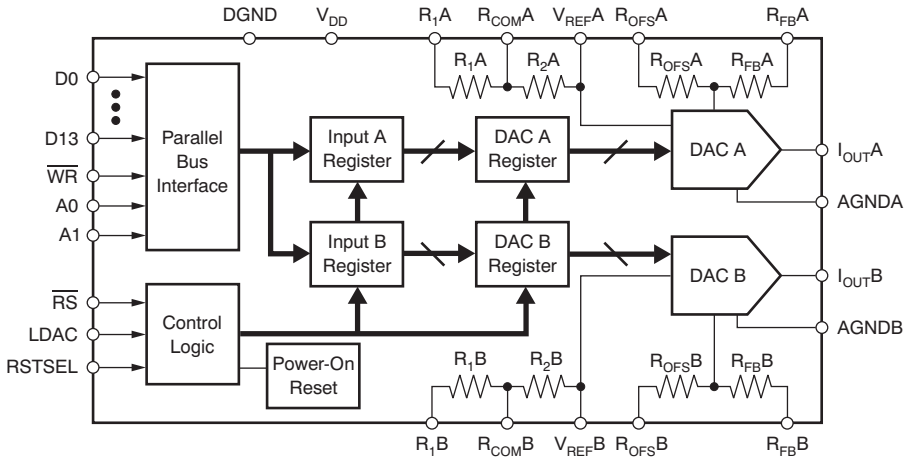
The DAC8805 dual, multiplying digital-to-analog converter (DAC) is designed to operate from a single 2.7V to 5.5V supply.

The applied external reference input voltage V_{REF} determines the full-scale output current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external, current-to-voltage (I/V) precision amplifier.

A RSTSEL pin allows system reset assertion ($\overline{RS}$) to force all registers to zero code when RSTSEL = '0', or to mid-scale code when RSTSEL = '1'. Additionally, an internal power-on reset forces all registers to zero or mid-scale code at power-up, depending on the state of the RSTSEL pin.

A parallel interface offers high-speed communications. The DAC8805 is packaged in a space-saving TSSOP-38 package and has an industry-standard pinout. The device is specified from –40°C to +125°C.

For a 16-bit, pin-compatible version, see the DAC8822.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD (DESIGNATOR)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC8805Q	±1	±1	TSSOP-38 (DBT)	–40°C to +125°C	DAC8805

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		DAC8805	UNIT
V_{DD} to GND		–0.3 to +7	V
Digital input voltage to GND		–0.3 to +V_{DD} + 0.3	V
V (I_{OUT}) to GND		–0.3 to +V_{DD} + 0.3	V
REF, R_{OFS}, R_{FB}, R_1, R_{COM} to AGND, DGND		±25	V
Operating temperature range		–40 to +125	°C
Storage temperature range		–65 to +150	°C
Junction temperature range (T_J max)		+150	°C
Power dissipation		(T_J max – T_A) / $R_{\theta JA}$	W
Thermal impedance, $R_{\theta JA}$		53	°C/W
ESD rating	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	500	V

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

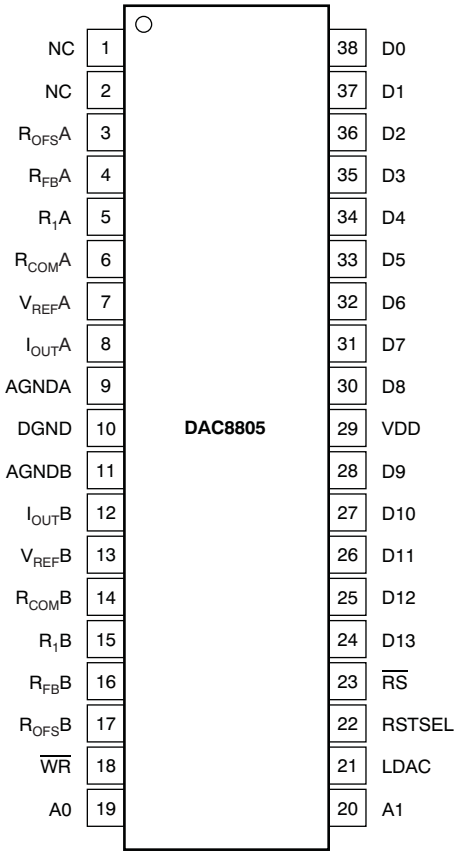
All specifications at T_A = –40°C to +125°C, V_{DD} = +2.7V to +5.5V, I_{OUT} = virtual GND, GND = 0V, and V_{REF} = 10V, unless otherwise noted.

PARAMETER		CONDITIONS	DAC8805 MIN	DAC8805 TYP	DAC8805 MAX	UNITS
STATIC PERFORMANCE						
Resolution			14			Bits
Relative accuracy	INL			±0.5	±1	LSB
Differential nonlinearity	DNL			±0.5	±1	LSB
Output leakage current		Data = 0000h, T_A = +25°C			10	nA
Output leakage current		Data = 0000h, Full temperature range			20	nA
Full-scale gain error		Unipolar, data = 3FFFh		±1	±4	mV
		Bipolar, data = 3FFFh		±1	±4	mV
Full-scale temperature coefficient				±1	±2	ppm/°C
Bipolar zero error		T_A = +25°C		±1	±3	mV
		Full temperature range		±1	±3	mV
Power-supply rejection ratio	PSRR	V_{DD} = 5V ±10%		±0.1	±0.5	LSB/V
OUTPUT CHARACTERISTICS(1)						
Output current				2		mA
Output capacitance		Code dependent		50		pF
REFERENCE INPUT						
Reference voltage range	V_{REF}		–18		18	V
Input resistance (unipolar)	R_{REF}		4	5	6	kΩ
Input capacitance				5		pF
R_1, R_2			4	5	6	kΩ
Feedback and offset resistance	R_{OFS}, R_{FB}		8	10	12	kΩ
LOGIC INPUTS AND OUTPUT(1)						
Input low voltage	V_{IL}	V_{DD} = +2.7V			0.6	V
	V_{IL}	V_{DD} = +5V			0.8	V
Input high voltage	V_{IH}	V_{DD} = +2.7V	2.1			V
	V_{IH}	V_{DD} = +5V	2.4			V
Input leakage current	I_{IL}			0.001	1	µA
Input capacitance	C_{IL}				8	pF
POWER REQUIREMENTS						
Supply voltage	V_{DD}		2.7		5.5	V
Supply current	I_{DD}	Normal operation, logic inputs = 0V		3	6	µA
V_{DD} = +4.5V to +5.5V		V_{IH} = V_{DD} and V_{IL} = GND		3	6	µA
V_{DD} = +2.7V to +3.6V		V_{IH} = V_{DD} and V_{IL} = GND		1	3	µA
AC CHARACTERISTICS(1)(2)						
Output current settling time	t_S	To 0.1% of full-scale, Data = 0000h to 3FFFh to 0000h		0.3		µs
	t_S	To 0.006% of full-scale, Data = 0000h to 3FFFh to 0000h		0.5		µs
Reference multiplying BW	BW – 3dB	V_{REF} = $5V_{PP}$, Data = 3FFFh, 2-quadrant mode		10		MHz
DAC glitch impulse		V_{REF} = 0V to 10V, Data = 1FFFh to 2000h to 1FFFh		5		nV–s
Feedthrough error	V_{OUT}/V_{REF}	Data = 0000h, V_{REF} = 100kHz, $\pm 10V_{PP}$, 2-quadrant mode		–70		dB
Crosstalk error	$V_{OUT}A/V_{REF}B$	Data = 0000h, $V_{REF}B$ = $100mV_{RMS}$, f = 100kHz		–100		dB
Digital feedthrough		LDAC = Logic low, V_{REF} = –10V to + 10V Any code change		1		nV–s
Total harmonic distortion	THD	V_{REF} = $6V_{RMS}$, Data = 3FFFh, f = 1kHz		–105		dB
Output noise density	e_N	f = 1kHz, BW = 1Hz, 2-quadrant mode		12		nV/√Hz

(1) Specified by design and characterization; not production tested.
(2) All ac characteristic tests are performed in a closed-loop system using a THS4011 I-to-V converter amplifier.

PIN ASSIGNMENTS

DBT PACKAGE
TSSOP-38
(TOP VIEW)



PIN ASSIGNMENTS (continued)

Table 1. TERMINAL FUNCTIONS

PIN #	NAME	DESCRIPTION
1, 2	NC	No connection
3	$R_{OFS}A$	Bipolar Offset Resistor A. Accepts up to ±18V. In 2-quadrant mode, $R_{OFS}A$ ties to $R_{FB}A$. In 4-quadrant mode, $R_{OFS}A$ ties to R_1A and the external reference.
4	$R_{FB}A$	Internal Matching Feedback Resistor A. Connects to the external op amp for I-V conversion.
5	R_1A	4-Quadrant Resistor. In 2-quadrant mode, R_1A shorts to the $V_{REF}A$ pin. In 4-quadrant mode, R_1A ties to $R_{OFS}A$ and the reference input.
6	$R_{COM}A$	Center Tap Point of the Two 4-Quadrant Resistors, R_1A and R_2A. In 2-quadrant mode, $R_{COM}A$ shorts to the V_{REF} pin. In 4-quadrant mode, $R_{COM}A$ ties to the inverting node of the reference amplifier.
7	$V_{REF}A$	DAC A Reference Input in 2-Quadrant Mode, R_2 Terminal in 4-Quadrant Mode. In 2-quadrant mode, $V_{REF}A$ is the reference input with constant input resistance versus code. In 4-quadrant mode, $V_{REF}A$ is driven by the external reference amplifier.
8	$I_{OUT}A$	DAC A Current Output. Connects to the inverting terminal of external precision I-V op amp for voltage output.
9	AGNDA	DAC A Analog Ground.
10	DGND	Digital Ground.
11	AGNDB	DAC B Analog Ground.
12	$I_{OUT}B$	DAC B Current Output. Connects to the inverting terminal of external precision I-V op amp for voltage output.
13	$V_{REF}B$	DAC B Reference Input in 2-Quadrant Mode, R_2 Terminal in 4-Quadrant Mode. In 2-quadrant mode, $V_{REF}B$ is the reference input with constant input resistance versus code. In 4-quadrant mode, $V_{REF}B$ is driven by the external reference amplifier.
14	$R_{COM}B$	Center Tap Point of the Two 4-Quadrant Resistors, R_1B and R_2B. In 2-quadrant mode, $R_{COM}B$ shorts to the V_{REF} pin. In 4-quadrant mode, $R_{COM}B$ ties to the inverting node of the reference amplifier.
15	R_1B	4-Quadrant Resistor. In 2-quadrant mode, R_1B shorts to the $V_{REF}B$ pin. In 4-quadrant mode, R_1B ties to $R_{OFS}B$ and the reference input.
16	$R_{FB}B$	Internal Matching Feedback Resistor B. Connects to external op amp for I-V conversion.
17	$R_{OFS}B$	Bipolar Offset Resistor B. Accepts up to ±18V. In 2-quadrant mode, $R_{OFS}B$ ties to $R_{FB}B$. In 4-quadrant mode, $R_{OFS}B$ ties to R_1B and the external reference.
18	$\overline{WR}$	Write Control Digital Input In, Active Low. $\overline{WR}$ enables input registers. Signal level must be ≤ V_{DD} + 0.3V.
19	A0	Address 0. Signal level must be ≤ V_{DD} + 0.3V.
20	A1	Address 1. Signal level must be ≤ V_{DD} + 0.3V.
21	LDAC	Digital Input Load DAC Control. Signal level must be ≤ V_{DD} + 0.3V. See the Function of Control Inputs table for details.
22	RSTSEL	Power-On Reset State. RSTSEL = 0 corresponds to zero-scale reset. RSTSEL = 1 corresponds to mid-scale reset. The signal level must be ≤ V_{DD} + 0.3V.
23	$\overline{RS}$	Reset. Active low resets both input and DAC registers. Resets to zero-scale if RSTSEL= 0, and to mid-scale if RSTSEL = 1. Signal level must be equal to or less than VDD + 0.3 V.
24-28, 30-38	D0-D13	Digital Input Data Bits D0 to D13. Signal level must be ≤ V_{DD} +0.3V. D13 is MSB.
29	V_{DD}	Positive Power Supply Input. The specified range of operation is 2.7V to 5.5V.

TIMING AND FUNCTIONAL INFORMATION

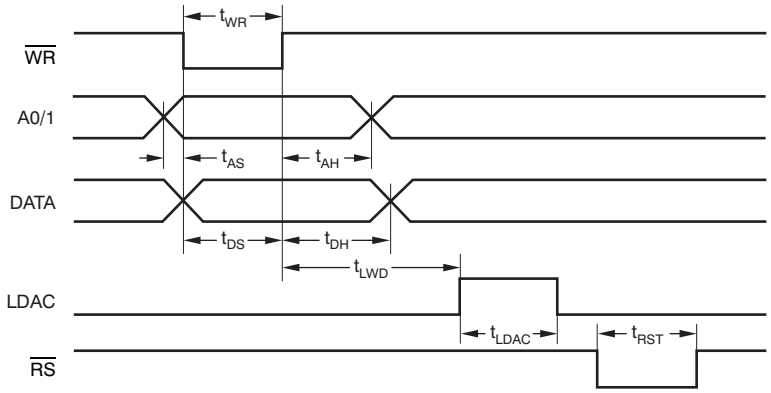


Figure 1. Timing Diagram

TIMING CHARACTERISTICS

All specifications at T_A = –40°C to +125°C, I_{OUT} = virtual GND, GND = 0V, and V_{REF} = 10V, unless otherwise noted

PARAMETER		CONDITIONS	DAC8805			UNITS
			MIN	TYP	MAX	
Data to $\overline{WR}$ setup time	t_{DS}	V_{DD} = +5.0V	10			ns
		V_{DD} = +2.7V	10			ns
A0/1 to $\overline{WR}$ setup time	t_{AS}	V_{DD} = +5.0V	10			ns
		V_{DD} = +2.7V	10			ns
Data to $\overline{WR}$ hold time	t_{DH}	V_{DD} = +5.0V	0			ns
		V_{DD} = +2.7V	0			ns
A0/1 to $\overline{WR}$ hold time	t_{AH}	V_{DD} = +5.0V	0			ns
		V_{DD} = +2.7V	0			ns
$\overline{WR}$ pulse width	t_{WR}	V_{DD} = +5.0V	10			ns
		V_{DD} = +2.7V	10			ns
LDAC pulse width	t_{LDAC}	V_{DD} = +5.0V	10			ns
		V_{DD} = +2.7V	10			ns
$\overline{RS}$ pulse width	t_{RST}	V_{DD} = +5.0V	10			ns
		V_{DD} = +2.7V	10			ns
$\overline{WR}$ to LDAC delay time	t_{LWD}	V_{DD} = +5.0V	0			ns
		V_{DD} = +2.7V	0			ns

Table 2. Address Decoder Pins

A1	A0	OUTPUT UPDATE
0	0	DAC A
0	1	None
1	0	DAC A and DAC B
1	1	DAC B

Table 3. Function of Control Inputs

CONTROL INPUTS			REGISTER OPERATION
$\overline{RS}$	$\overline{WR}$	LDAC	
0	X	X	Asynchronous operation. Reset the input and DAC register to '0' when the RSTSEL pin is tied to DGND, and to midscale when RSTSEL is tied to V_{DD}.
1	0	0	Load the input register with all 14 data bits.
1	1	1	Load the DAC register with the contents of the input register.
1	0	1	The input and DAC register are transparent.
1	⊓	⊓	LDAC and $\overline{WR}$ are tied together and programmed as a pulse. The 14 data bits are loaded into the input register on the falling edge of the pulse and then loaded into the DAC register on the rising edge of the pulse.
1	1	0	No register operation.

TYPICAL CHARACTERISTICS: V_{DD} = +5V

Channel A

LINEARITY ERROR
vs DIGITAL INPUT CODE

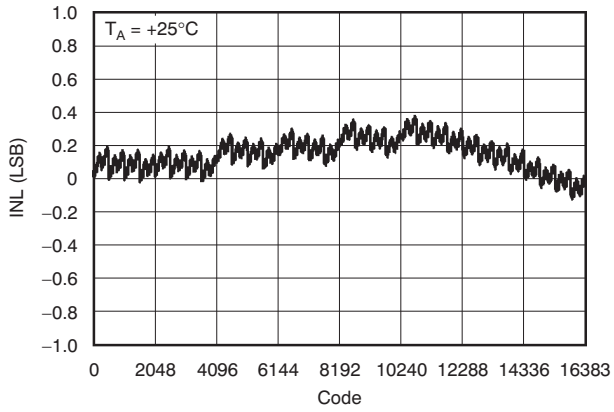


Figure 2.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

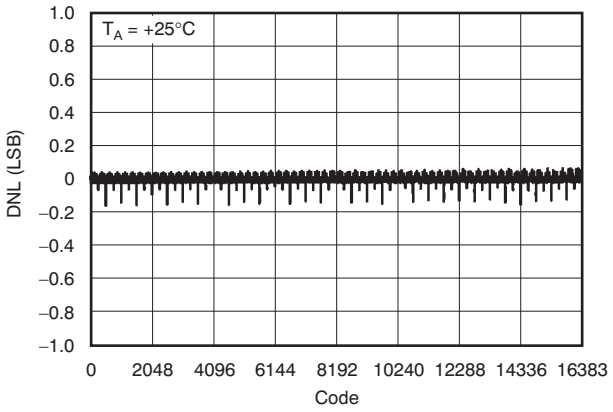


Figure 3.

LINEARITY ERROR
vs DIGITAL INPUT CODE

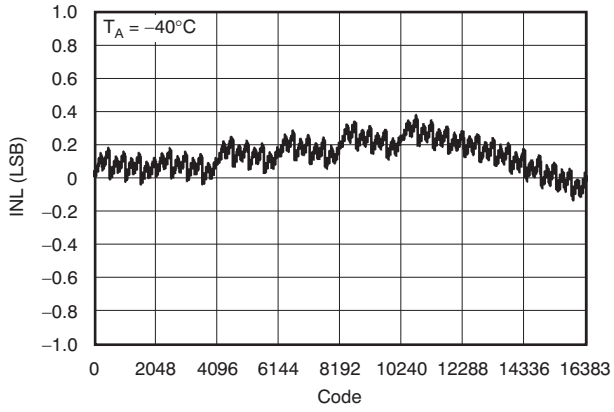


Figure 4.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

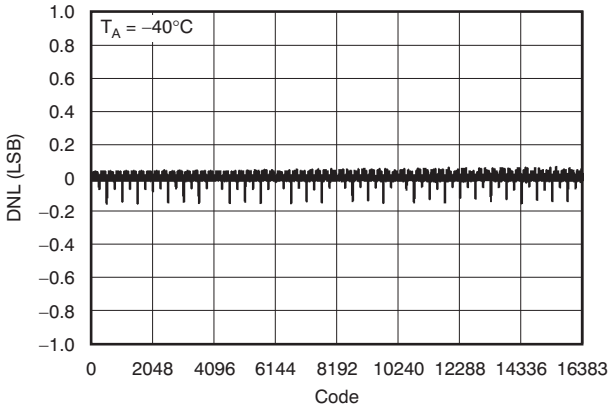


Figure 5.

LINEARITY ERROR
vs DIGITAL INPUT CODE

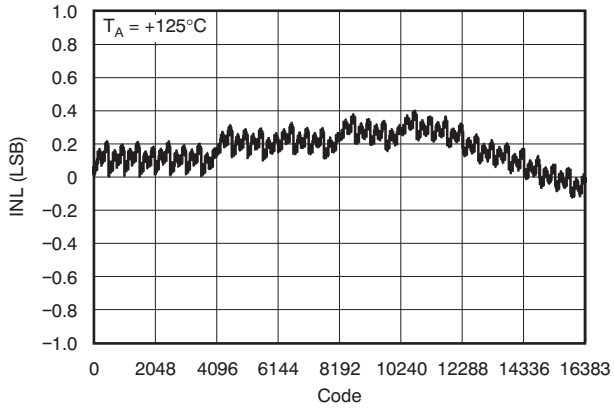


Figure 6.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

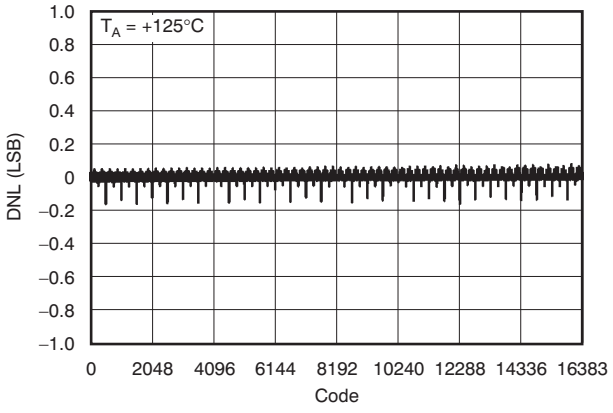


Figure 7.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

Channel B

LINEARITY ERROR
vs DIGITAL INPUT CODE

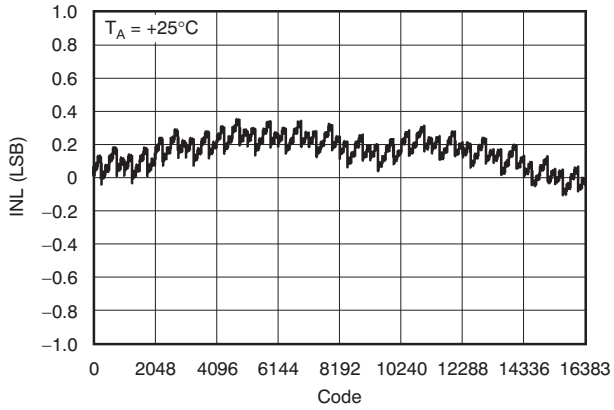


Figure 8.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

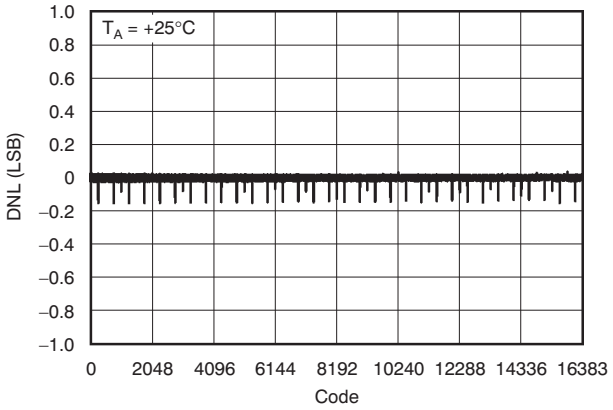


Figure 9.

LINEARITY ERROR
vs DIGITAL INPUT CODE

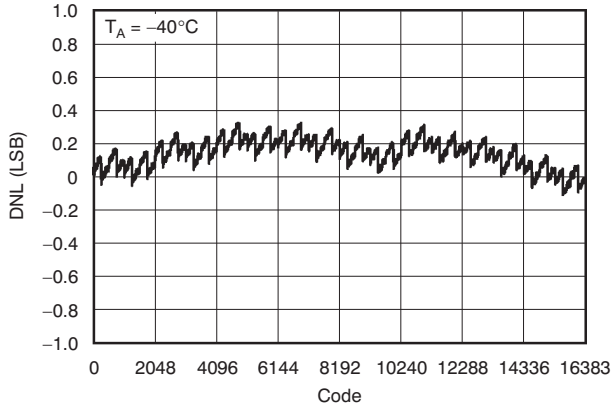


Figure 10.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

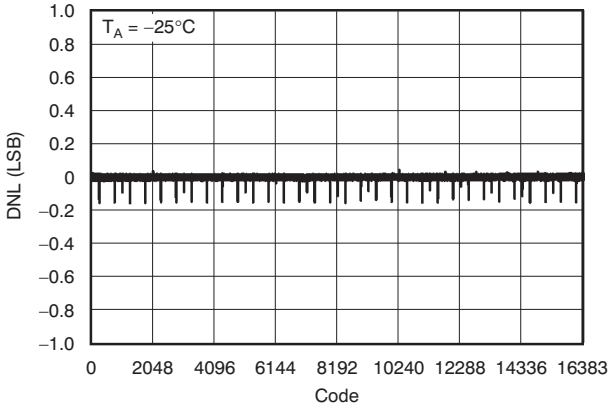


Figure 11.

LINEARITY ERROR
vs DIGITAL INPUT CODE

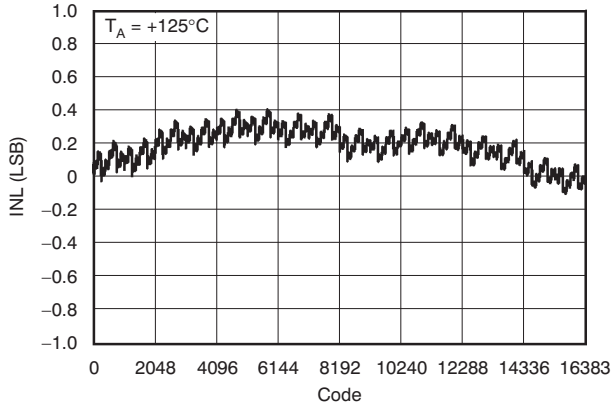


Figure 12.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

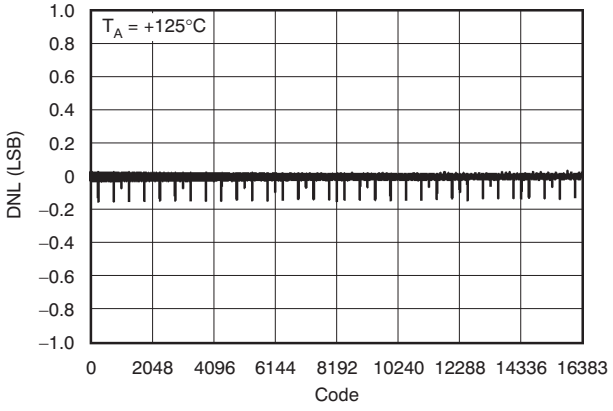


Figure 13.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

MIDSCALE DAC GLITCH

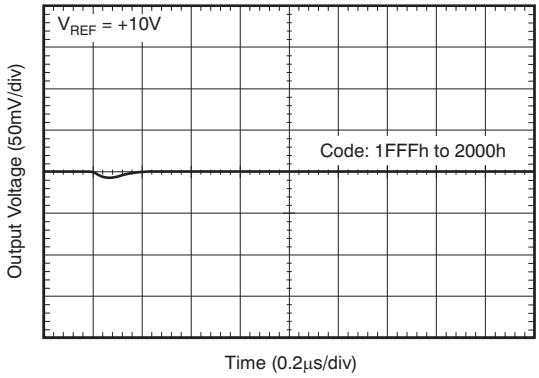


Figure 14.

MIDSCALE DAC GLITCH

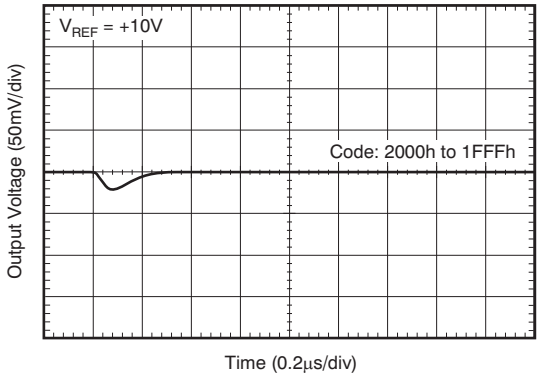


Figure 15.

FULL-SCALE ERROR vs TEMPERATURE

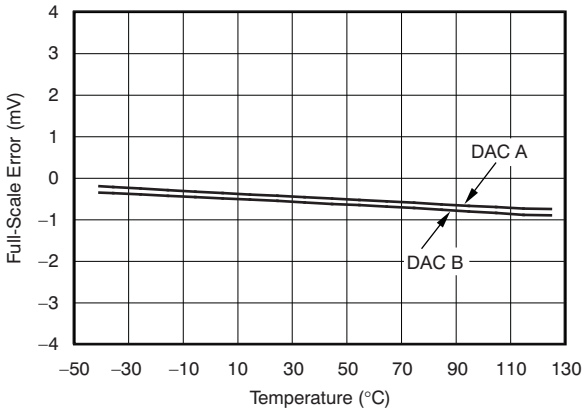


Figure 16.

BIPOLAR-ZERO ERROR vs TEMPERATURE

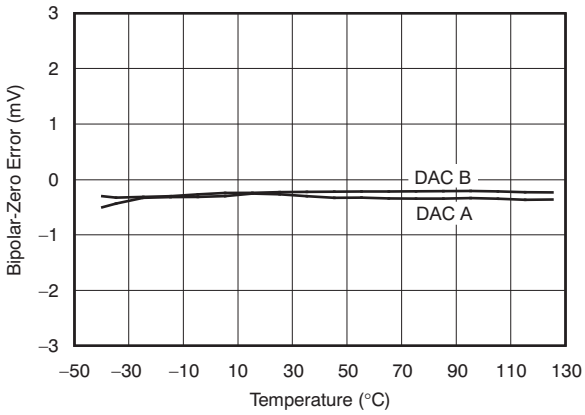


Figure 17.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V

Channel A

LINEARITY ERROR
vs DIGITAL INPUT CODE

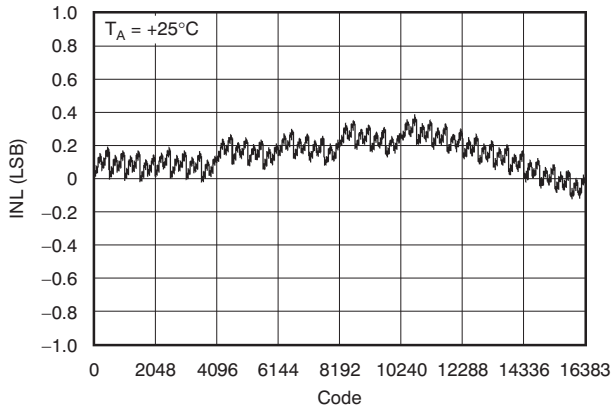


Figure 18.

LINEARITY ERROR
vs DIGITAL INPUT CODE

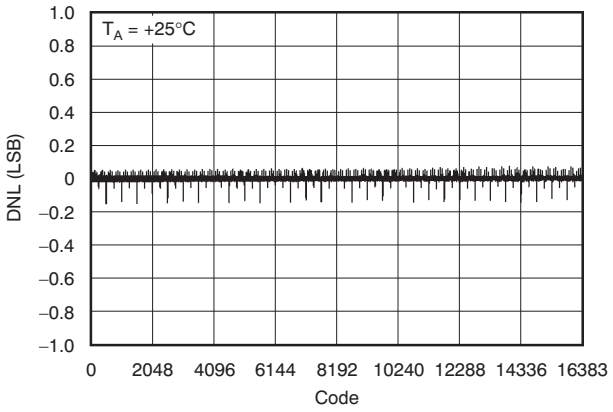


Figure 19.

LINEARITY ERROR
vs DIGITAL INPUT CODE

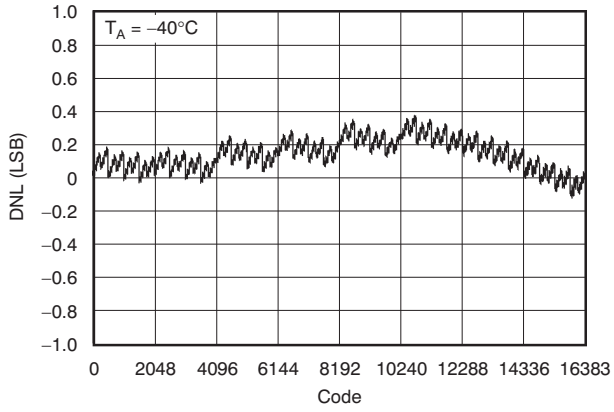


Figure 20.

LINEARITY ERROR
vs DIGITAL INPUT CODE

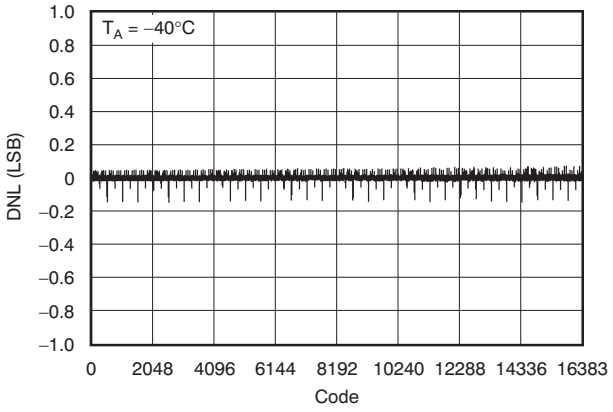


Figure 21.

LINEARITY ERROR
vs DIGITAL INPUT CODE

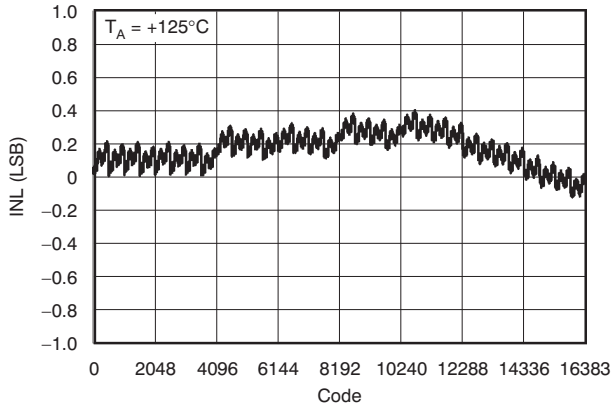


Figure 22.

LINEARITY ERROR
vs DIGITAL INPUT CODE

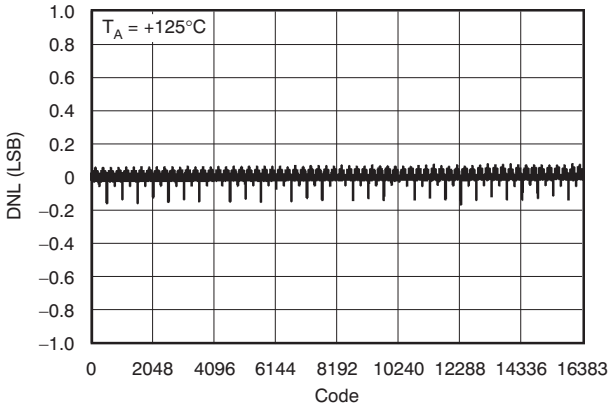


Figure 23.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

Channel B

LINEARITY ERROR
vs DIGITAL INPUT CODE

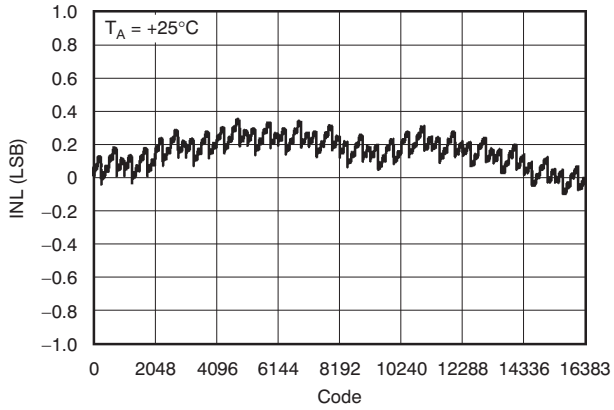


Figure 24.

LINEARITY ERROR
vs DIGITAL INPUT CODE

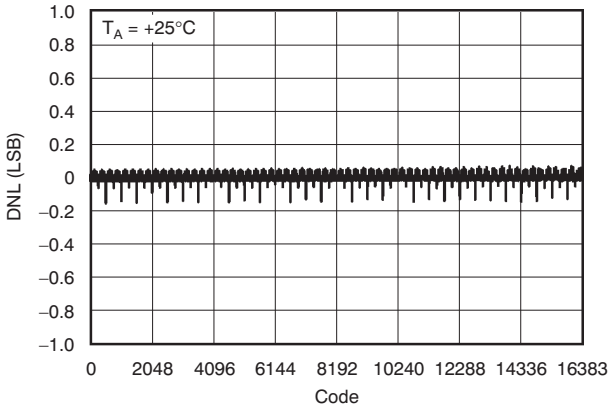


Figure 25.

LINEARITY ERROR
vs DIGITAL INPUT CODE

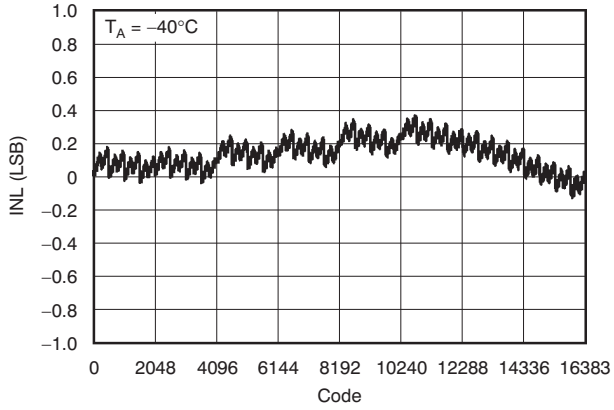


Figure 26.

LINEARITY ERROR
vs DIGITAL INPUT CODE

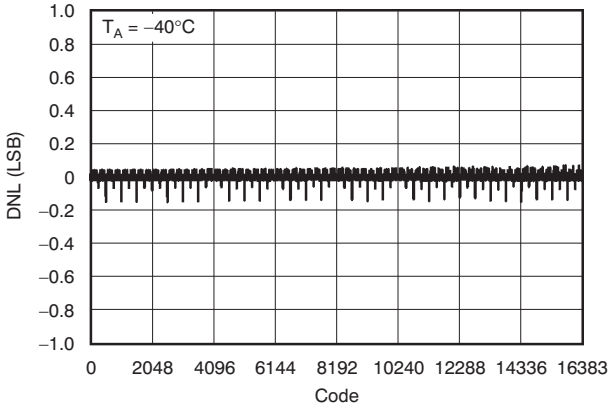


Figure 27.

LINEARITY ERROR
vs DIGITAL INPUT CODE

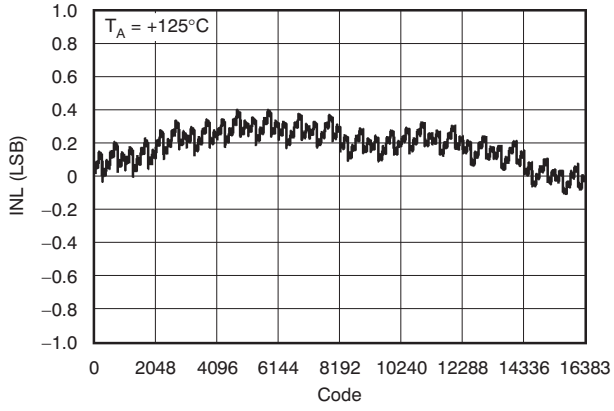


Figure 28.

LINEARITY ERROR
vs DIGITAL INPUT CODE

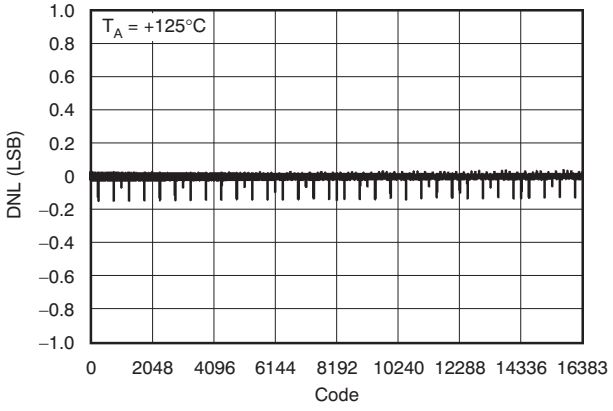


Figure 29.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

DAC GLITCH

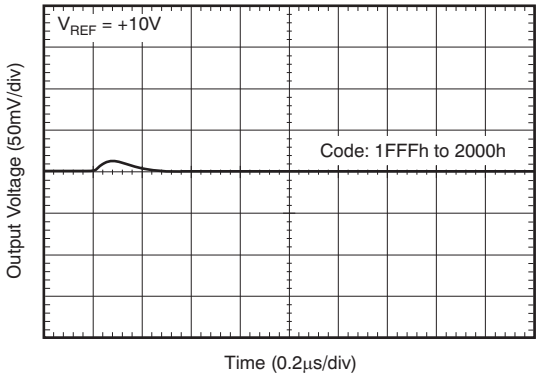


Figure 30.

DAC GLITCH

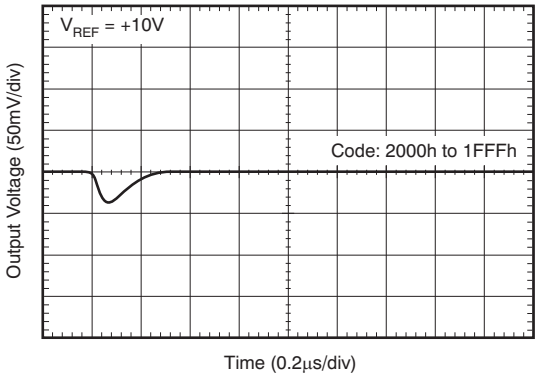


Figure 31.

FULL-SCALE ERROR vs TEMPERATURE

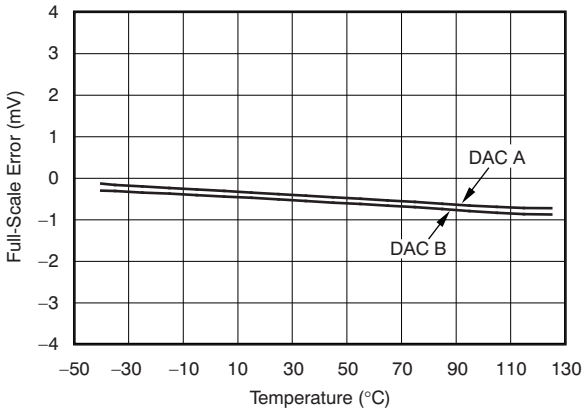


Figure 32.

BIPOLAR-ZERO ERROR vs TEMPERATURE

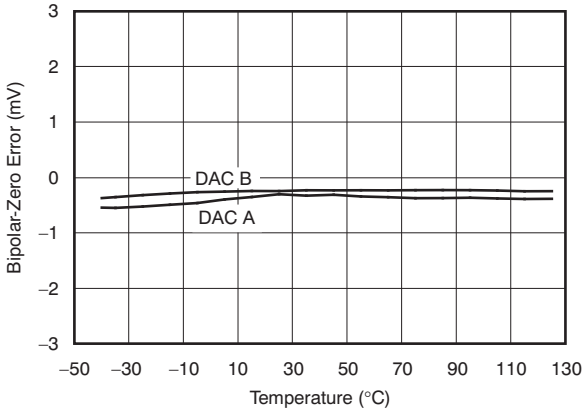


Figure 33.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V and +5V

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

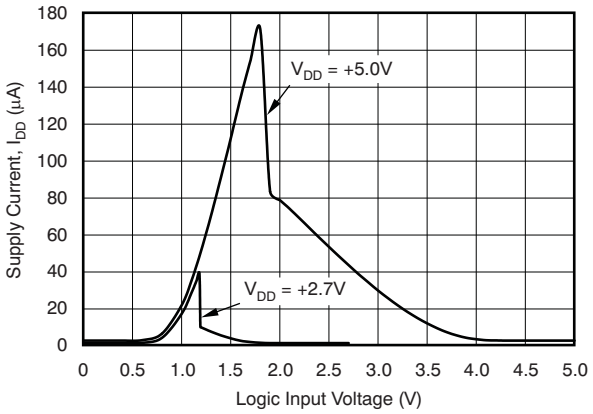


Figure 34.

REFERENCE MULTIPLYING BANDWIDTH UNIPOLAR MODE

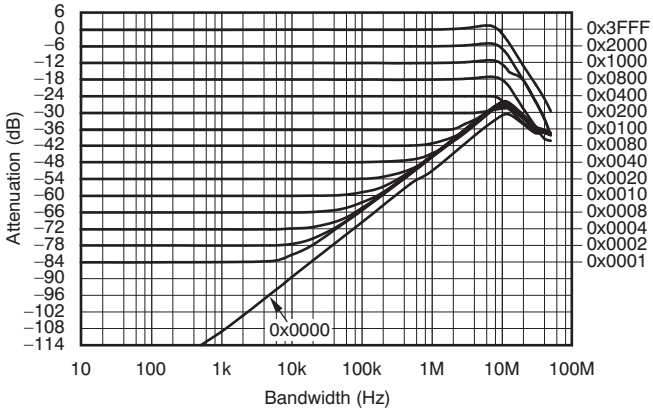


Figure 35.

REFERENCE MULTIPLYING BANDWIDTH BIPOLAR MODE

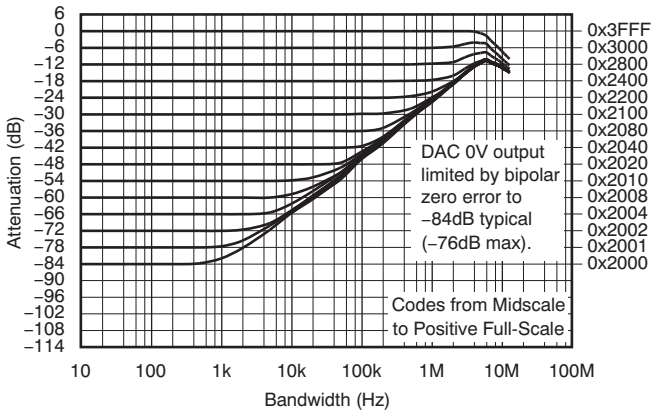


Figure 36.

REFERENCE MULTIPLYING BANDWIDTH BIPOLAR MODE

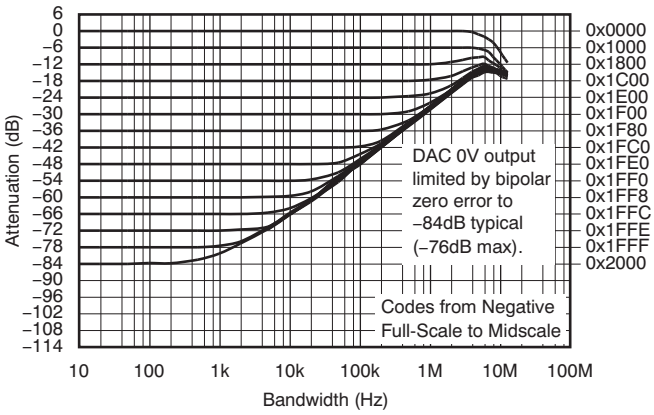


Figure 37.

SUPPLY CURRENT vs TEMPERATURE

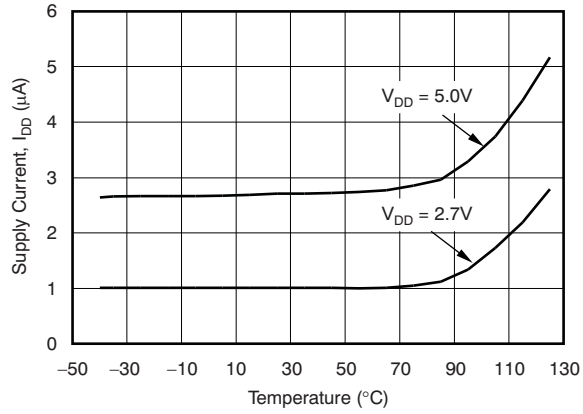


Figure 38.

DAC SETTLING TIME

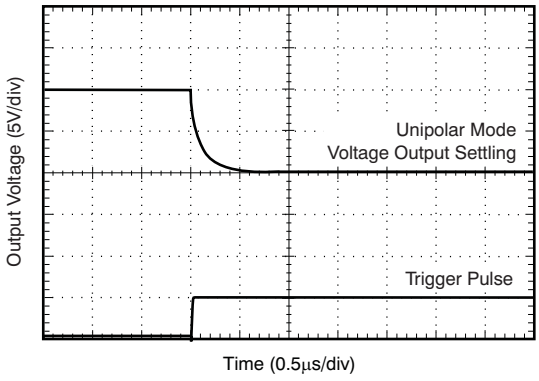


Figure 39.

THEORY OF OPERATION

The DAC8805 is a multiplying, dual-channel, current output, 14-bit DAC. The architecture, illustrated in Figure 40, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to GND or to the I_{OUT} terminal. The I_{OUT} terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input (V_{REF}) that determines the DAC full-scale output current. The R-2R ladder presents a code-independent load impedance to the external reference of 5kΩ ± 25%. The external reference voltage can vary in a range of –18V to +18V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter op amp and the R_{FB} resistor in the DAC8805, an output voltage range of $–V_{REF}$ to $+V_{REF}$ can be generated.

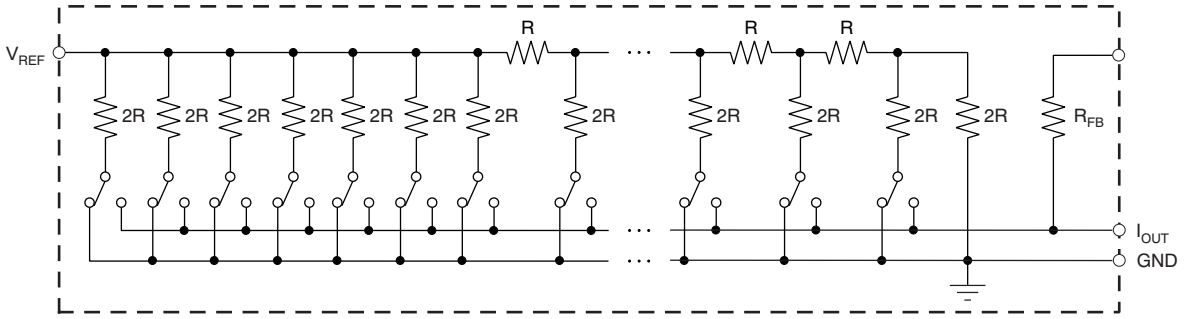


Figure 40. Equivalent R-2R DAC Circuit

The DAC output voltage is determined by V_{REF} and the digital data (D) according to Equation 1:

$$V_{OUT}A/B = -V_{REF} \times \frac{D}{16384} \quad (1)$$

Each DAC code determines the 2R-leg switch position to either GND or I_{OUT}. The external I/V converter op amp noise gain will also change because the DAC output impedance (as seen looking into the I_{OUT} terminal) changes versus code. Because of this change in noise gain, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I_{OUT} terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC8805 because of offset modulation versus DAC code. For best linearity performance of the DAC8805, an op amp (such as the OPA277) is recommended, as shown in Figure 41. This circuit allows V_{REF} to swing from –10V to +10V.

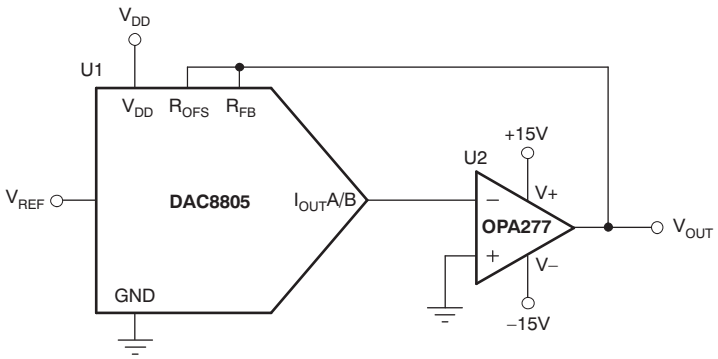


Figure 41. Voltage Output Configuration

APPLICATION INFORMATION

DIGITAL INTERFACE

The parallel bus interface of the DAC8805 is comprised of a 14-bit data bus, D0—D13, address lines A0 and A1, and a $\overline{WR}$ control signal. Timing and control functionality are shown in Figure 1, and described in Table 2 and Table 3. The address lines must be set up and stable before the $\overline{WR}$ signal goes low, to prevent loading improper data to an undesired input register.

Both channels of the DAC8805 can be simultaneously updated by control of the LDAC signal, as shown in Figure 1. Reset control ($\overline{RS}$) and reset select control (RSTSEL) signals are provided to allow user reset ability to either zero scale or midscale codes of both the input and DAC registers.

STABILITY CIRCUIT

For a current-to-voltage (I/V) design, as shown in Figure 42, the DAC8805 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and laid out according to correct printed circuit board (PCB) layout design. For each code change, there is an output step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, a compensation capacitor C_1 (4pF to 20pF, typ) can be added to the design for circuit stability, as shown in Figure 42.

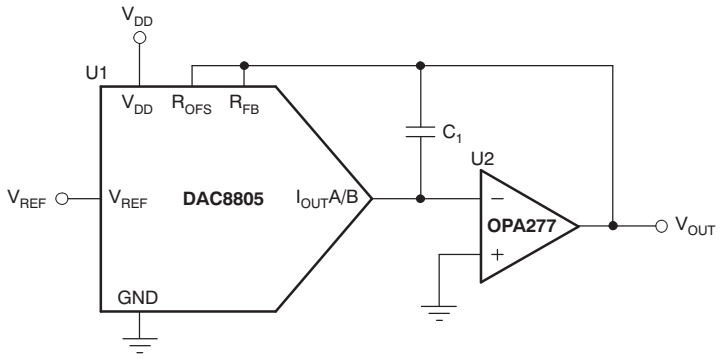


Figure 42. Gain Peaking Prevention Circuit with Compensation Capacitor

APPLICATION INFORMATION (continued)

BIPOLAR OUTPUT CIRCUIT

The DAC8805, as a 4-quadrant multiplying DAC, can be used to generate a bipolar output. The polarity of the full-scale output (I_{OUT}) is the inverse of the input reference voltage at V_{REF}.

Using a dual op amp, such as the OPA2277, full 4-quadrant operation can be achieved with minimal components. Figure 43 demonstrates a $\pm 10V_{OUT}$ circuit with a fixed +10V reference. The output voltage is shown in Equation 2:

$$V_{OUT} = \left(\frac{D}{8192} - 1\right) \times V_{REF} \quad (2)$$

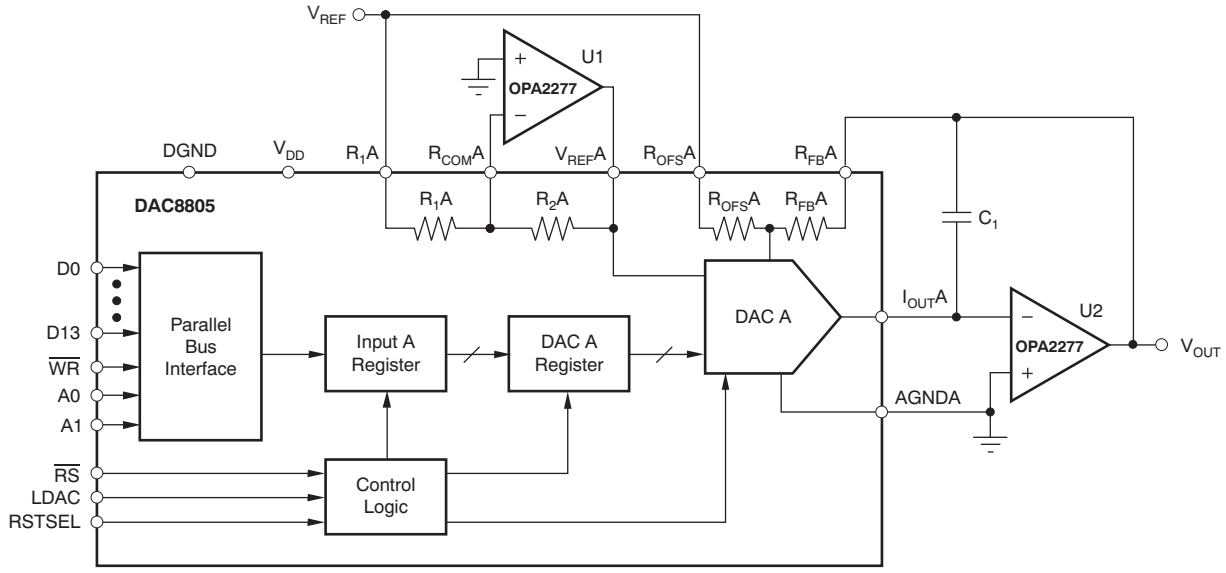


Figure 43. Bipolar Output Circuit

APPLICATION INFORMATION (continued)

PROGRAMMABLE CURRENT SOURCE CIRCUIT

The DAC8805 can be integrated into the circuit in Figure 44 to implement an improved Howland current pump for precise V/I conversions. Bidirectional current flow and high-voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by Equation 3:

$$I_L A/B = \frac{(R_2 + R_3) / R_1}{R_3} \times V_{REF} \times \frac{D}{16384} \quad (3)$$

The value of R_3 in the previous equation can be reduced to increase the output current drive of U3. U3 can drive ±20mA in both directions with voltage compliance limited up to 15V by the U3 voltage supply. Elimination of the circuit compensation capacitor (C_1) in the circuit is not suggested as a result of the change in the output impedance (Z_O), according to Equation 4:

$$Z_O = \frac{R_1' R_3 (R_1 + R_2)}{R_1 (R_2' + R_3') - R_1' (R_2 + R_3)} \quad (4)$$

As shown in Equation 4, Z_O with matched resistors is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used, Z_O is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C_1 into the circuit, possible oscillation problems are eliminated. The value of C_1 can be determined for critical applications; for most applications, however, a value of several pF is suggested.

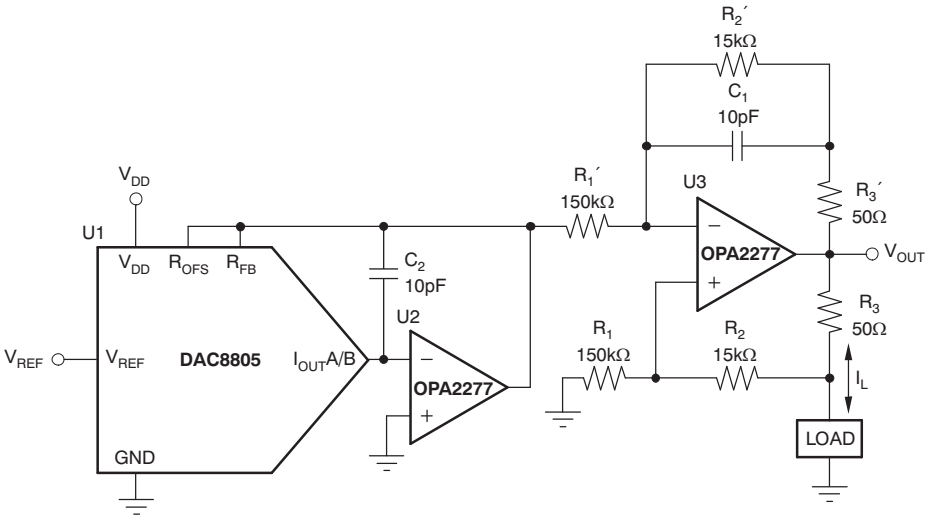


Figure 44. Programmable Bidirectional Current Source Circuit

CROSS-REFERENCE

The DAC8805 has an industry-standard pinout. Table 4 provides the cross-reference information.

Table 4. Cross-Reference

PRODUCT	BIT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC8805Q	14	1	1	–40°C to +125°C	TSSOP-38	DBT	AD5557

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8805QDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAC8805	Samples
DAC8805QDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAC8805	Samples
DAC8805QDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAC8805	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

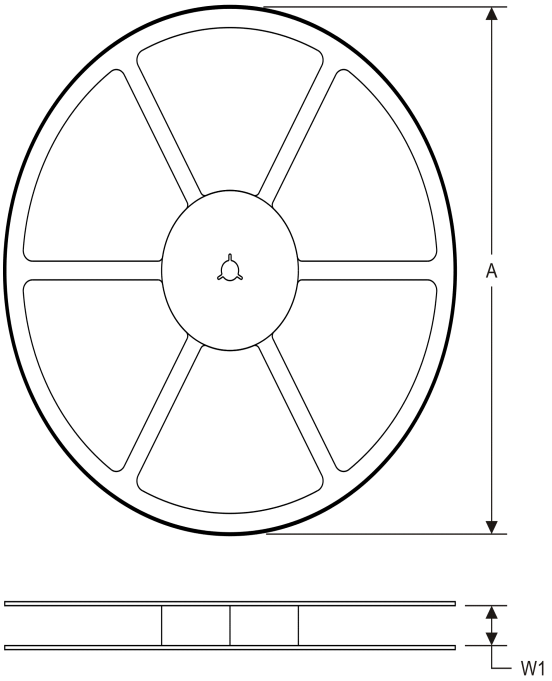
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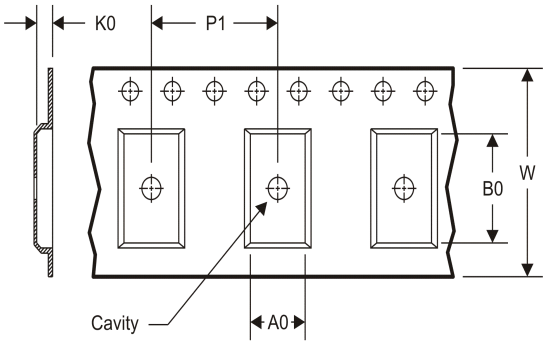
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



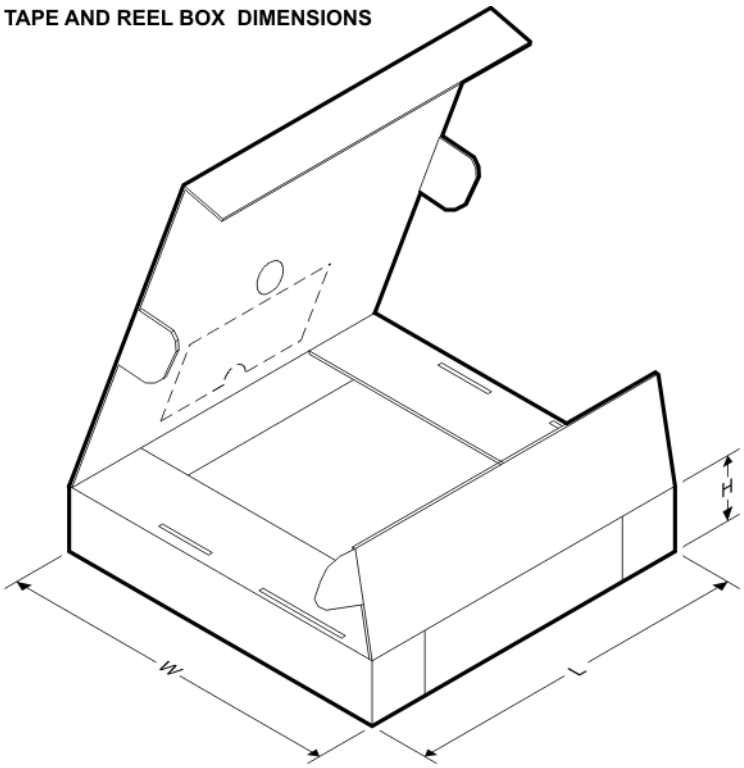
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8805QDBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

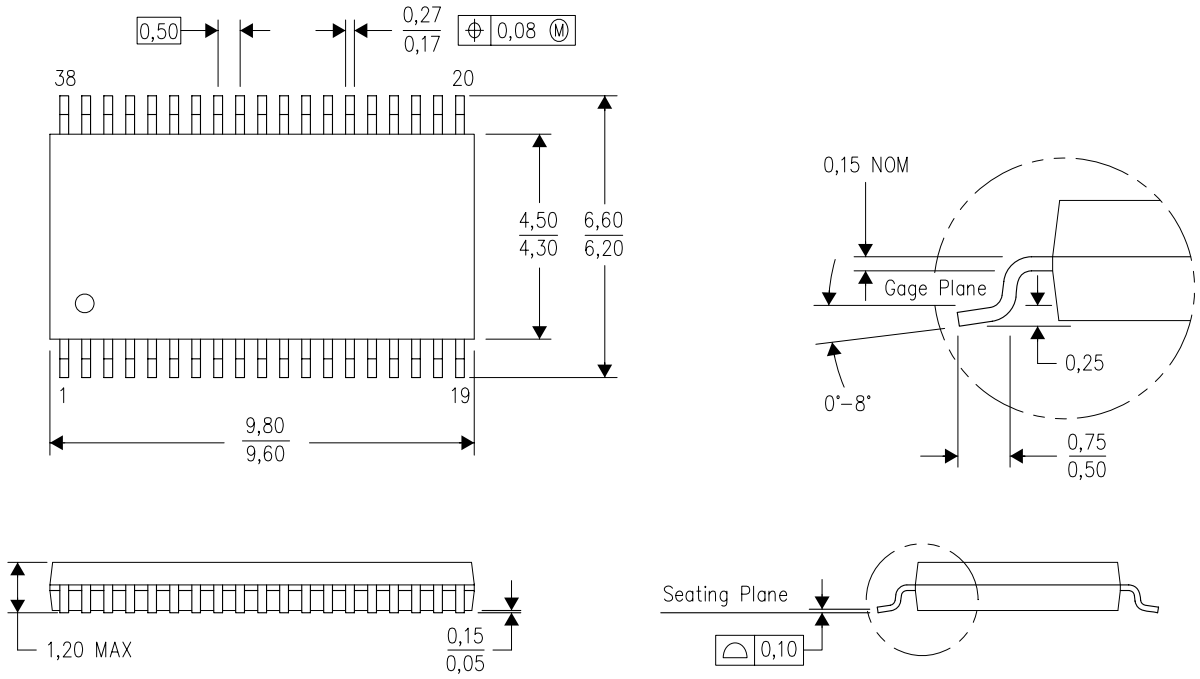
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8805QDBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0

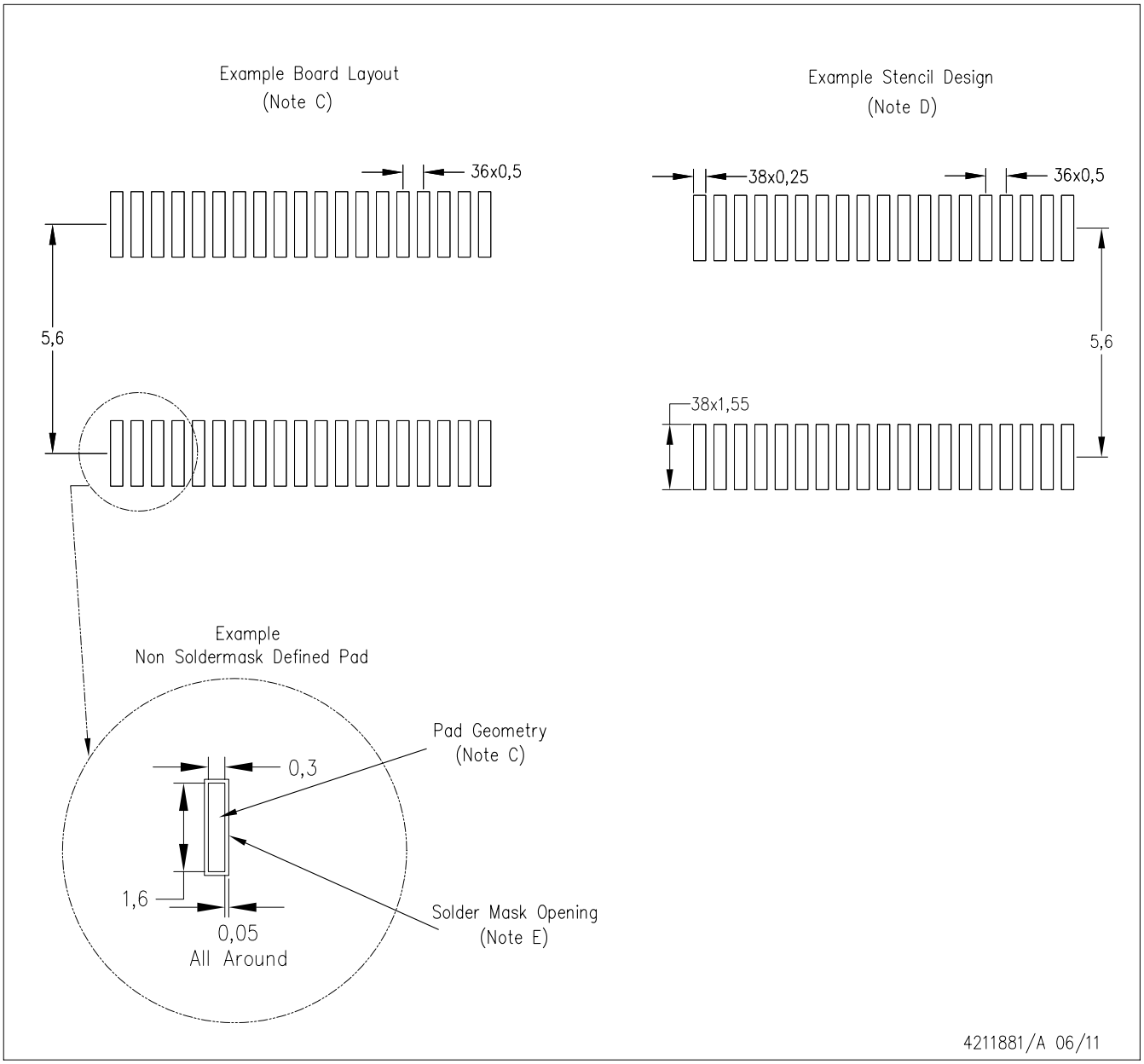
DBT (R–PDSO–G38) PLASTIC SMALL OUTLINE



4073252-6/I 03/11

NOTES:
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B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

DBT (R–PDSO–G38) PLASTIC SMALL OUTLINE



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C. Publication IPC–7351 is recommended for alternate designs
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E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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