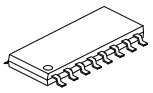
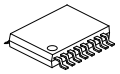
U74AHC595

CMOS IC

8-BIT SHIFT REGISTER WITH 3-STATE OUTPUT REGISTERS



SOP-16



SSOP-16(150mil)

■ DESCRIPTION

The UTC **74AHC595** contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers. The shift register has a direct overriding clear ($\overline{\text{SRCLR}}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{\text{OE}}$) input is high, all outputs, except $Q_{H'}$, are in the high-impedance state.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered. If both clocks are connected together the shift register always is one clock pulse ahead of the storage register.

■ FEATURES

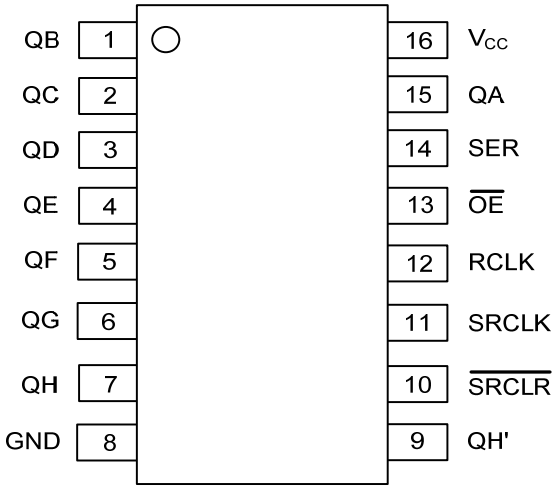
* Operation Voltage Range: 2~5.5V
* 8-bit Serial-In, Parallel-Out Shift
* Shift Register Has Direct Clear

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC595L-S16-T	U74 AHC595G-S16-T	SOP-16	Tube
U74 AHC595L-S16-R	U74 AHC595G-S16-R	SOP-16	Tape Reel
U74AHC595L-R16-T	U74 AHC595G-R16-T	SSOP-16	Tube
U74 AHC595L-R16-R	U74 AHC595G-R16-R	SSOP-16	Tape Reel

U74AHC595L-S16-T (1) Packing Type (2) Package Type (3) Lead Free	(1) T: Tube, R: Tape Reel (2) S16: SOP-16, R16: SSOP-16 (3) L: Lead Free, G: Halogen Free

■ PIN CONFIGURATION

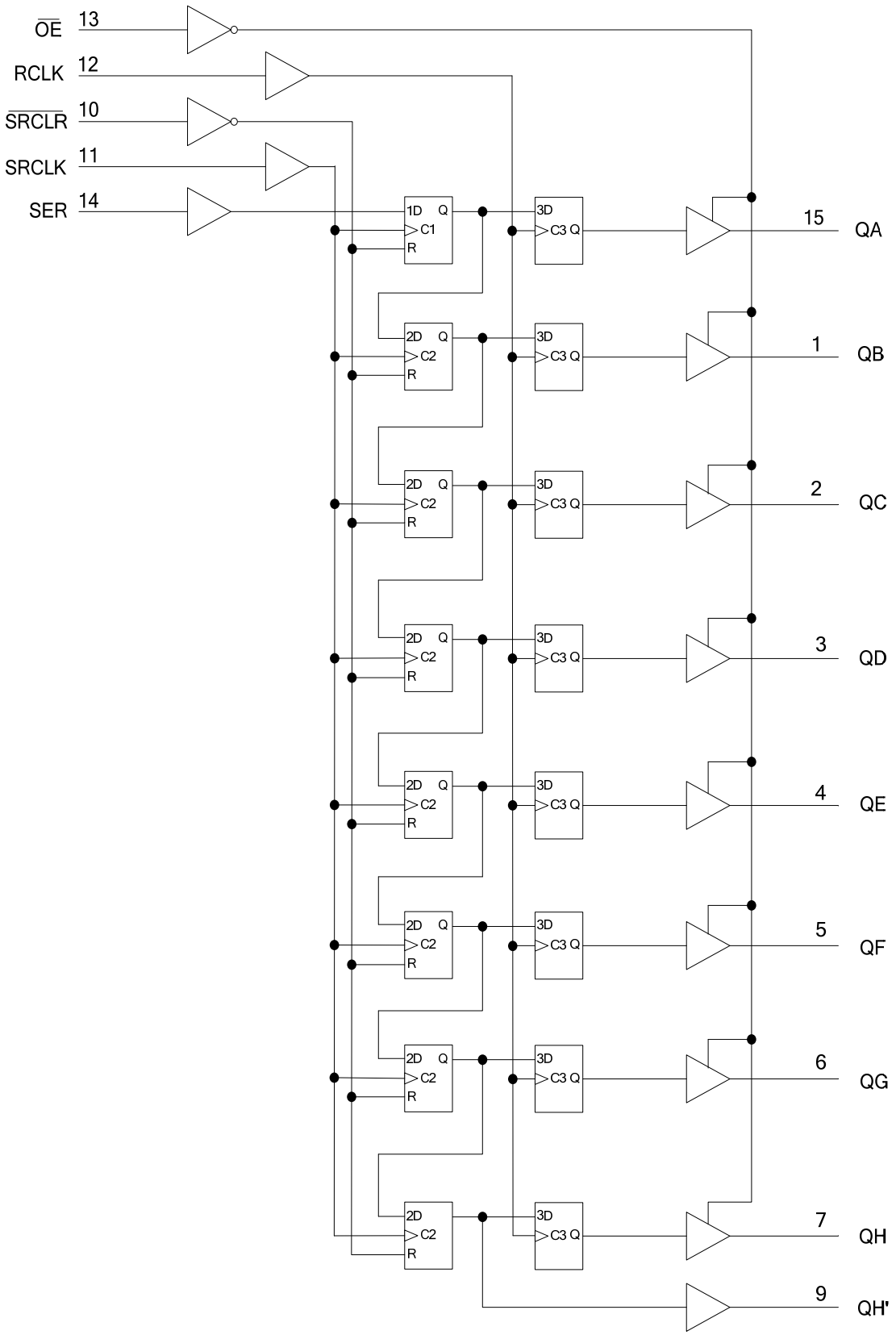


■ FUNCTION TABLE

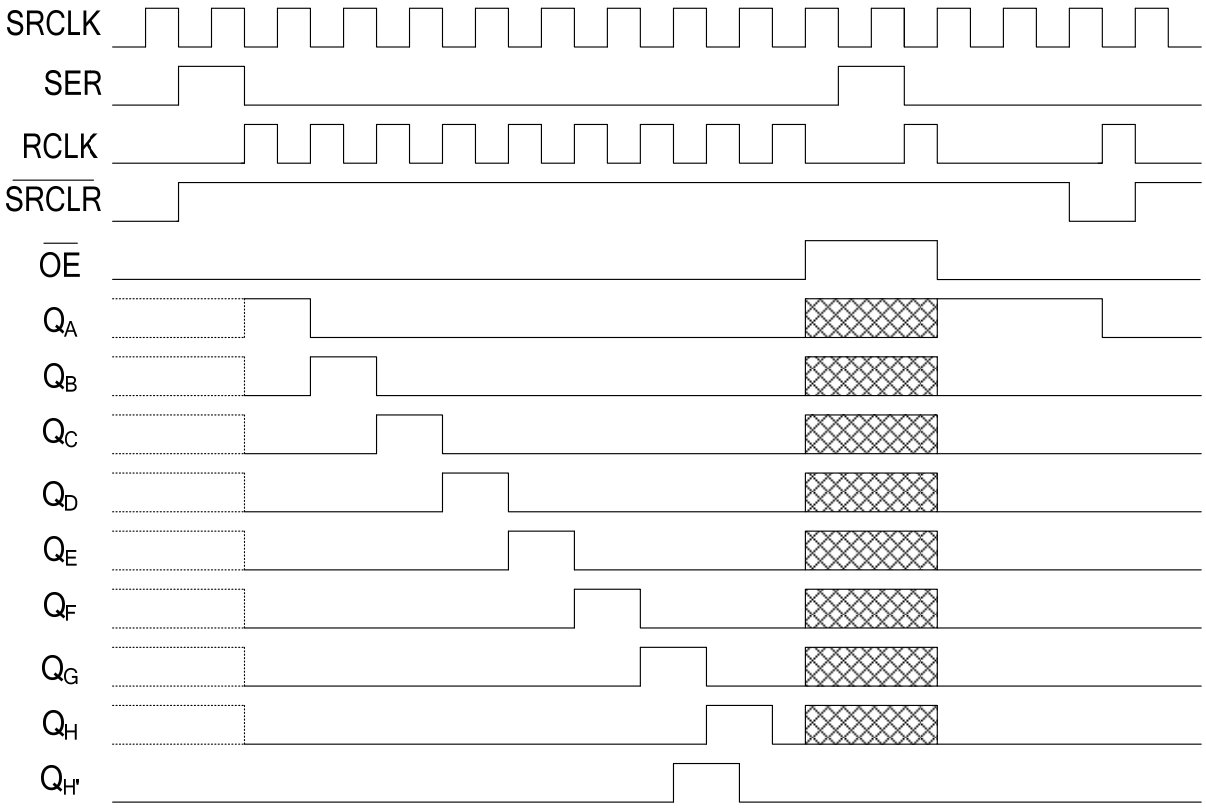
INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A-Q_H are disabled.
X	X	X	X	L	Outputs Q_A-Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored into the storage register.

L: low voltage level; H: high voltage level; ↑: low-to-high; X: don't care

■ LOGIC DIAGRAM (POSITIVE LOGIC)



■ TIMING DIAGRAM



Note: Implies that the outputs is in 3-State mode.

■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7.0	V
Input Voltage	V_{IN}	-0.5~7.0	V
Output Voltage(active mode)	V_{OUT}	-0.5~V_{CC}+0.5	V
Input Clamp Current (V_{iN}<0)	I_{IK}	-20	mA
Output Clamp Current (V_{OUT}<0)	I_{OK}	±20	mA
Output Current	I_{OUT}	±25	mA
V_{CC} or GND Current	I_{CC}	±75	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-16	θ_{JA}	73	°C/W
	SSOP-16		82	

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	2		5.5	V
Input Voltage		V_{IN}	0		5.5	V
Output Voltage		V_{OUT}	0		V_{CC}	V
Operating free-air temperature		T_A	-40		125	°C
Input Transition Rise or Fall Rate	V_{CC} =3.3±0.3V	Δt/Δv			100	ns/V
	V_{CC} =5±0.5V				20	

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-level input voltage	V_{IH}	V_{CC}=2V	1.5			V
		V_{CC}=3V	2.1			
		V_{CC}=5.5V	3.85			
LOW-lever output voltage	V_{IL}	V_{CC}=2V			0.5	V
		V_{CC}=3V			0.9	
		V_{CC}=5.5V			1.65	
High-Level Output Voltage	V_{OH}	V_{CC}=2V, I_{OH}=-50μA	1.9	2		V
		V_{CC}=3V, I_{OH}=-50μA	2.9	3		
		V_{CC}=4.5V, I_{OH}=-50μA	4.4	4.5		
		V_{CC}=3V, I_{OH}=-4mA	2.58			
		V_{CC}=4.5V, I_{OH}=-8mA	3.94			
Low-Level Output Voltage	V_{OL}	V_{CC}=2V, I_{OL}=50μA			0.1	V
		V_{CC}=3V, I_{OL}=50μA			0.1	
		V_{CC}=4.5V, I_{OL}=50μA			0.1	
		V_{CC}=3V, I_{OL}=4mA			0.36	
		V_{CC}=4.5V, I_{OH}=8mA			0.36	
Input Leakage Current	I_I	I_I=5.5V or GND, V_{CC}=0 to 5.5V			±0.1	μA
Output Off-state Current	I_{OZ}	V_I=V_{CC} or GND,V_O=V_{CC} or GND, $\overline{OE}$ =VIH or VIL, V_{CC}=5.5V			±0.25	μA
Quiescent Supply Current	I_{CC}	V_I=GND or V_{CC}, I_O=0, Vcc=5.5V			4	μA
Input Capacitance	C_I	V_I=V_{CC} or GND, V_{CC}=5V		3	10	pF
Output Capacitance	C_{OUT}	V_O=V_{CC} or GND, V_{CC}=5V		5.5		pF

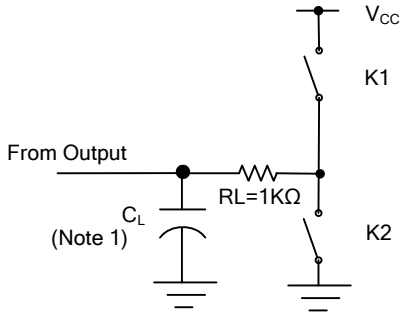
■ DYNAMIC CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Maximum Clock Frequency	f_{max}	V_{CC}=3.3±0.3V,C_L=15pF		80	120		MHz
		V_{CC}=3.3±0.3V,C_L=50pF		55	105		
		V_{CC}=5±0.5V,C_L=15pF		135	170		
		V_{CC}=5±0.5V,C_L=50pF		95	140		
From RCLK to Q_A-Q_H	t_{PLH}	V_{CC}=3.3±0.3V,	C_L=15pF		6	11.9	ns
			C_L=50pF		7.9	15.4	
		V_{CC}=5±0.5V	C_L=15pF		4.3	7.4	
			C_L=50pF		5.6	9.4	
	t_{PHL}	V_{CC}=3.3±0.3V	C_L=15pF		6	11.9	
			C_L=50pF		7.9	15.4	
		V_{CC}=5±0.5V	C_L=15pF		4.3	7.4	
			C_L=50pF		5.6	9.4	
From SRCLK to QH'	t_{PLH}	V_{CC}=3.3±0.3V	C_L=15pF		6.6	13	ns
			C_L=50pF		9.2	16.5	
		V_{CC}=5±0.5V	C_L=15pF		4.5	8.2	
			C_L=50pF		6.4	10.2	
	t_{PHL}	V_{CC}=3.3±0.3V	C_L=15pF		6.6	13	
			C_L=50pF		9.2	16.5	
		V_{CC}=5±0.5V	C_L=15pF		4.5	8.2	
			C_L=50pF		6.4	10.2	
From $\overline{SRCLR}$ to QH'	t_{PHL}	V_{CC}=3.3±0.3V	C_L=15pF		6.2	12.8	ns
			C_L=50pF		9	16.3	
		V_{CC}=5±0.5V	C_L=15pF		4.5	8	
			C_L=50pF		6.4	10	
From $\overline{OE}$ to Q_A-Q_H	t_{PZH}	V_{CC}=3.3±0.3V	C_L=15pF		6	11.5	ns
			C_L=50pF		7.8	15	
		V_{CC}=5±0.5V	C_L=15pF		4.3	8.6	
			C_L=50pF		5.7	10.6	
	t_{PZL}	V_{CC}=3.3±0.3V	C_L=15pF		7.8	11.5	
			C_L=50pF		9.6	15	
		V_{CC}=5±0.5V	C_L=15pF		5.4	8.6	
			C_L=50pF		6.8	10.6	
From $\overline{OE}$ to Q_A-Q_H	t_{PHZ}	V_{CC}=3.3±0.3V,C_L=50pF			8.1	15.7	ns
		V_{CC}=5±0.5V,C_L=50pF			3.5	10.3	
	t_{PLZ}	V_{CC}=3.3±0.3V,C_L=50pF			9.3	15.7	
		V_{CC}=5±0.5V,C_L=50pF			3.4	10.3	

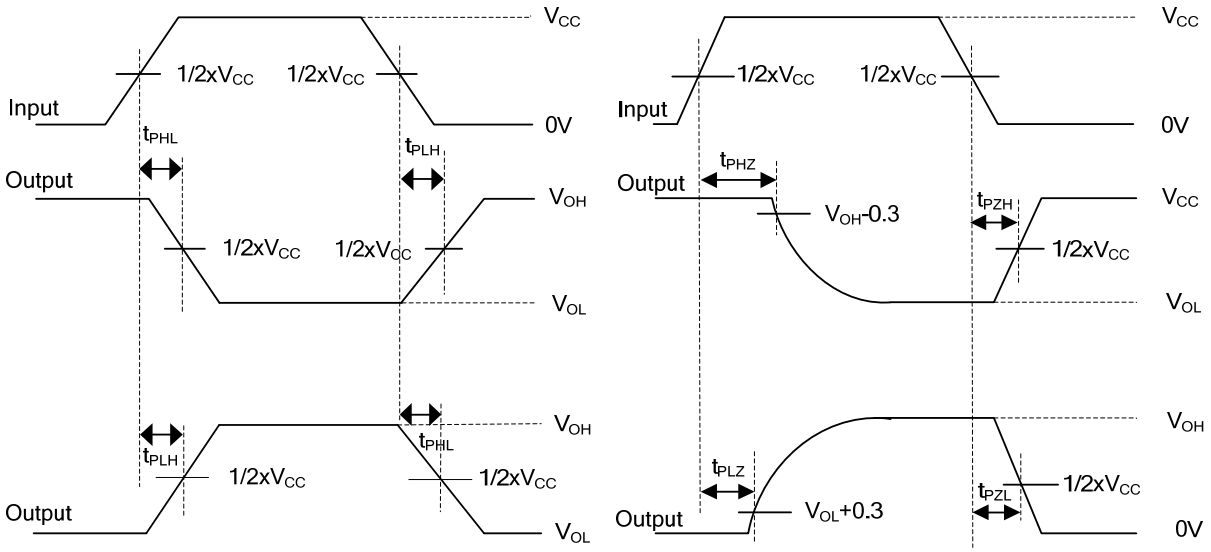
■ OPERATING CHARACTERISTICS (V_{CC}=5V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load, f=1MHz		25.2		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open



PROPAGATION DELAY TIMES ENABLE AND DISABLE TIMES

Note: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:
PRR ≤1MHZ, Z_O=50Ω, t_r ≤3ns, t_f ≤3ns.
3. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms