

Programmable Rambus™ XDR™ Clock Generator

ICS9220B

General Description

The **ICS9220** clock generator provides Programmable clock signals to support the Rambus XDR™ memory subsystem and Redwood logic interface. The **ICS9220** has been optimized for 100MHz reference input that may or may not be modulated for spread spectrum. The **ICS9220** provides 2 differential clock pairs in a space saving 28-pin TSSOP package and provides an off-the-shelf high-performance interface solution.

Figure 1 shows the major components of the **ICS9220** XDR Clock Generator. These include the a PLL, a Bypass Multiplexer and two differential output buffers. The outputs can be disabled by a logic low on the OE pin. An output is enabled by the combination of the OE pin being high, and 1 in its SMBus Output control register bit.

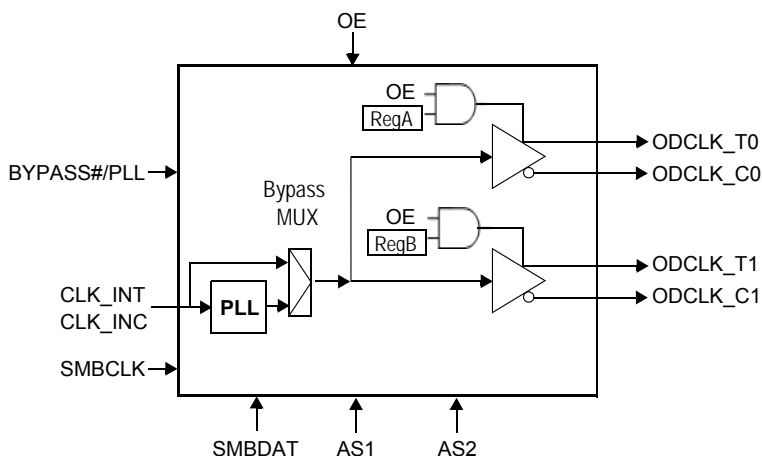
The PLL receives a reference clock, CLK_INT/C and outputs a clock signal at a frequency equal to the input frequency times a multiplier. Table 2 shows the multipliers selectable via the SMBus interface. This clock signal is then fed to the differential output buffers to drive the enabled clocks. Disabled outputs are set to Hi-Z. The Bypass mode routes the input clock, CLK_INT/C, directly to the differential output buffers, bypassing the PLL.

Up to four **ICS9220** devices can be cascaded on the same SMBus. Table 3 shows the SMBus addressing and control for the four devices.

Features

- 300 - 700 MHz clock source
- 2 open-drain differential output drives with short term jitter < 40ps
- Spread spectrum compatible
- Reference clock is differential or single-ended 100MHz
- SMBus programmability for:
 - frequency multiplier
 - output enable
 - operating mode
- Support systems where XDR subsystem is asynchronous to other system clocks
- 2.5V power supply

Block Diagram



Pin Configuration

AVDD2.5	1	ICS9220	28	VDD2.5
AGND	2		27	GND
IREFY	3		26	GND
AGND	4		25	ODCLK_T0
CLK_INT	5		24	ODCLK_C0
CLK_INC	6		23	GND
VDD2.5	7		22	VDD2.5
GND	8		21	VDD2.5
SMBCLK	9		20	GND
SMBDAT	10		19	ODCLK_T1
OE	11		18	ODCLK_C1
AS1	12		17	GND
AS2	13		16	GND
BYPASS#/PLL	14		15	VDD2.5

28-Pin 4.4mm TSSOP

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	AVDD2.5	PWR	2.5V Analog Power pin for Core PLL
2	AGND	PWR	Analog Ground pin for Core PLL
3	IREFY	IN	This pin establishes the reference current for the differential clock pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
4	AGND	PWR	Analog Ground pin for Core PLL
5	CLK_INT	IN	"True" reference clock input.
6	CLK_INC	IN	"Complementary" reference clock input.
7	VDD2.5	PWR	Power supply, nominal 2.5V
8	GND	PWR	Ground pin.
9	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
10	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
11	OE	IN	Active high input for enabling outputs. 0 = tri-state outputs, 1= enable outputs
12	AS1	IN	Default SMBus Address Select.
13	AS2	IN	Default SMBus Address Select.
14	BYPASS#/PLL	IN	Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode
15	VDD2.5	PWR	Power supply, nominal 2.5V
16	GND	PWR	Ground pin.
17	GND	PWR	Ground pin.
18	ODCLK_C1	OUT	"Complementary" side of open drain differential clock output. This open drain output needs an external resistor network..
19	ODCLK_T1	OUT	"True" side of open drain differential clock output. This open drain output needs an external resistor network..
20	GND	PWR	Ground pin.
21	VDD2.5	PWR	Power supply, nominal 2.5V
22	VDD2.5	PWR	Power supply, nominal 2.5V
23	GND	PWR	Ground pin.
24	ODCLK_C0	OUT	"Complementary" side of open drain differential clock output. This open drain output needs an external resistor network..
25	ODCLK_T0	OUT	"True" side of open drain differential clock output. This open drain output needs an external resistor network..
26	GND	PWR	Ground pin.
27	GND	PWR	Ground pin.
28	VDD2.5	PWR	Power supply, nominal 2.5V

General SMBus serial interface information for the ICS9220B

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address per table 3
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address per table 3
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address per table 3
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation			
Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address table 3			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
Data Byte Count = X			
		ACK	
Beginning Byte N		X Byte	
			ACK
◊			◊
◊			◊
◊			◊
Byte N + X - 1			
		ACK	
P	stoP bit		

Index Block Read Operation			
Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address table 3			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address table 3			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
ACK		X Byte	
			Beginning Byte N
◊			◊
◊			◊
◊			◊
		Byte N + X - 1	
N	Not acknowledge		
P	stoP bit		

I²C Table: Output Enable Control Register

Byte 0		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Test Mode	Reserved For Vendor	RW	Disable	Enable	0
Bit 6	-		Reserved	Reserved	RW	-	-	0
Bit 5	-		Reserved	Reserved	RW	-	-	0
Bit 4	-		Reserved	Reserved	RW	-	-	0
Bit 3	-		Reserved	Reserved	RW	-	-	0
Bit 2	-		Reserved	Reserved	RW	-	-	0
Bit 1	-		ODCLK_T/C1	Output Control	RW	Disable	Enable	1
Bit 0	-		ODCLK_T/C0	Output Control	RW	Disable	Enable	1

I²C Table: Frequency Multiplier Control Register

Byte 1		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Reserved	Reserved	R	-	-	0
Bit 6	-		AS1	SMBus Address Select	R	See Table 2		x
Bit 5	-		AS2	SMBus Address Select	R			x
Bit 4	-		Reserved	Reserved	R	-	-	0
Bit 3	-		Reserved	Reserved	R	-	-	0
Bit 2	-		Reserved	Reserved	R	-	-	0
Bit 1	-		Reserved	Reserved	R	-	-	0
Bit 0	-		Reserved	Reserved	R	-	-	0

I²C Table: Vendor & Revision ID Register

Byte 2		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		RID 3	Revision ID	R	-	-	0
Bit 6	-		RID 2		R	-	-	0
Bit 5	-		RID 1		R	-	-	0
Bit 4	-		RID 0		R	-	-	0
Bit 3	-		VID 3	Vendor ID	R	-	-	0
Bit 2	-		VID 2		R	-	-	0
Bit 1	-		VID 1		R	-	-	0
Bit 0	-		VID 0		R	-	-	1

I²C Table: Frequency Control Register

Byte 3		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Reserved	Reserved	RW	-	-	0
Bit 6	-		Reserved	Reserved	RW	-	-	0
Bit 5	-		Reserved	Reserved	RW	-	-	0
Bit 4	-		Reserved	Reserved	RW	-	-	0
Bit 3	-		Reserved	Reserved	RW	-	-	0
Bit 2	-		Reserved	Reserved	RW	-	-	0
Bit 1	-		Reserved	Reserved	RW	-	-	0
Bit 0	-		Reserved	Reserved	RW	-	-	0

I²C Table: Frequency Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: VCO Frequency Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	M DIV3	M Divider Programming b(3:0)	RW	The decimal representation of M and N Divider in Byte 5 and 6 will configure the PLL VCO frequency. VCO frequency = 100 x {[NDIV(5:0)+2]/[MDIV(3:0)+2]}		0
Bit 2	-	M DIV2		RW			0
Bit 1	-	M DIV1		RW			1
Bit 0	-	M DIV0		RW			0

I²C Table: VCO Frequency Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	N Divider Programming b(5:0)	RW	-	-	0
Bit 6	-	Reserved		RW	-	-	0
Bit 5	-	N DIV5		RW	The decimal representation of M and N Divider in Byte 5 and 6 will configure the PLL VCO frequency. VCO frequency = 100 x {[NDIV(5:0)+2]/[MDIV(3:0)+2]}		0
Bit 4	-	N DIV4		RW			0
Bit 3	-	N DIV3		RW			1
Bit 2	-	N DIV2		RW			0
Bit 1	-	N DIV1		RW			1
Bit 0	-	N DIV0		RW			0

I²C Table: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD	
Bit 7			Reserved					0
Bit 6			Reserved					0
Bit 5			Reserved					0
Bit 4	-	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is 07 = 7 bytes			0
Bit 3	-	BC3		RW				0
Bit 2	-	BC2		RW				1
Bit 1	-	BC1		RW				1
Bit 0	-	BC0		RW				1

PLL Multiplier

Table 2 shows the frequency multipliers in the PLL, selectable by programming the MULT0, MULT1 and MULT2 bits in the SMBus Multiplier Control register. Power up default is 4.

Table 2. PLL Multiplier Programming Selection

OUTPUT	PostDiv B5b7	VCO	M B5b(3:0)	N B6b(5:0)	Byte 5 Hex	Byte 6 Hex	ASIC Multiplier		
							4	6	8
300.00000	4	1200.0000	6	18	84	10	1200.00	1800.00	2400.00
325.00000	4	1300.0000	4	13	82	0B	1300.00	1950.00	2600.00
350.00000	4	1400.0000	6	21	84	13	1400.00	2100.00	2800.00
366.66667	4	1466.6667	6	22	84	14	1466.67	2200.00	2933.33
375.00000	4	1500.0000	4	15	82	0D	1500.00	2250.00	3000.00
383.33333	4	1533.3333	6	23	84	15	1533.33	2300.00	3066.67
400.00000	4	1600.0000	6	24	84	16	1600.00	2400.00	3200.00
416.66667	4	1666.6667	6	25	84	17	1666.67	2500.00	3333.33
425.00000	2	850.0000	4	17	02	0F	1700.00	2550.00	3400.00
433.33333	2	866.6667	6	26	04	18	1733.33	2600.00	3466.67
450.00000	2	900.0000	6	27	04	19	1800.00	2700.00	3600.00
466.66667	2	933.3333	6	28	04	1A	1866.67	2800.00	3733.33
475.00000	2	950.0000	4	19	02	11	1900.00	2850.00	3800.00
483.33333	2	966.6667	6	29	04	1B	1933.33	2900.00	3866.67
500.00000	2	1000.0000	6	30	04	1C	2000.00	3000.00	4000.00
516.66667	2	1033.3333	6	31	04	1D	2066.67	3100.00	4133.33
533.33333	2	1066.6667	6	32	04	1E	2133.33	3200.00	4266.67
550.00000	2	1100.0000	6	33	04	1F	2200.00	3300.00	4400.00
566.66667	2	1133.3333	6	34	04	20	2266.67	3400.00	4533.33
583.33333	2	1166.6667	6	35	04	21	2333.33	3500.00	4666.67
600.00000	2	1200.0000	6	36	04	22	2400.00	3600.00	4800.00
616.66667	2	1233.3333	6	37	04	23	2466.67	3700.00	4933.33
633.33333	2	1266.6667	6	38	04	24	2533.33	3800.00	5066.67
650.00000	2	1300.0000	6	39	04	25	2600.00	3900.00	5200.00
666.66667	2	1333.3333	6	40	04	26	2666.67	4000.00	5333.33

NOTE: All output values based on 100.000000MHz input clock

Device ID and SMBus Device Address

The device ID (SMB_A(2:1)) is part of the SMBus device address. The least significant bit of the address designates a write or read operation. Table 3 shows the addresses for four ICS9220 devices on the same SMBus.

Table 3. SMBus Device Addresses

ICS 9220		Hex Address	8 bit SMBus Device Address Including Oper.			
Device	Operation		Control Function	AS2	AS1	Wr#/Rd
0	Write	D8	11011	0	0	0
	Read	D9				1
1	Write	DA		0	1	0
	Read	DB				1
2	Write	DC		1	0	0
	Read	DD				1
3	Write	DE		1	1	0
	Read	DF				1

Operating Modes

Table 4: Operating Modes

OE	BYPASS#/ PLL	Byte 1	Byte 0		ODCLK_T/C1	ODCLK_T/C0
		Bit 7	Bit 1	Bit 0		
L	X	X	X	X	Z	Z
H	X	1	X	X	Reserved for Vendor Test	
H	L	0	X	X	CLK_INT/C	
H	H	0	0	0	Z	Z
H	H	0	0	1	Z	CLK_INT/C
H	H	0	1	0	CLK_INT/C	Z
H	H	0	1	1	CLK_INT/C	CLK_INT/C

Notes

- 1 Bypass Mode
- 2 Power up default mode

Absolute Maximum Ratings

Supply Voltage	4.0 V
Logic Inputs	GND -0.5 V to V _{DD} +0.5 V
Ambient Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Characteristics - Outputs

TA = -40°C to +85°C; Supply Voltage AVDD2.5, VDD2.5 = 2.5 V +/- 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power up latency	t _{PU}	Power within spec to outputs within spec			3	ms
State transition latency ¹	t _{CO}	SMBus or Mode Select transition to outputs valid and within spec			3	ms
Differential output crossing voltage	V _{OX}	Measured as shown in Fig. 3	0.9		1.1	V
Output Voltage Swing (peak-to-peak singled ended)	V _{COS}	Measured as shown in Fig. 3. Excludes over and undershoot.	300		350	mV
Absolute output low voltage	V _{OL, ABS}	Measured at ODCLK_T/C pins	0.85			V
Reference Voltage for swing control current	V _{ISET}	V _{DD} = 2.3V, V _{OUT} = 1V	0.98		1.02	V
Ratio of output low current to reference current at typical V _{DD2.5}	I _{OL} /I _{REF}	I _{REF} is equal to V _{ISET} /R _{RC} . Tolerance of R _{RC} <= +/-1%.	6.8	7	7.2	-
Minimum current at V _{OLABS}	I _{OL, ABS}	Measured at ODCLK_T/C pins with termination per Figure 3.	45		-	mA
Low-level output voltage SMBus	V _{OLSMB}	I _{OL} = 4 mA	-		0.4	V
Low-level output current SMBus	I _{OLSMB}	V _{OL} = 0.8 V	6		-	mA
Tristate output current	I _{OZ}	Differential clock output pins	-		50	μA

Notes:

- 1 There is no output latency or glitches if a value written to an output register is the same as its current contents.

DC Characteristics - Inputs

TA = -40°C to +85°C; Supply Voltage AVDD2.5, VDD2.5 = 2.5 V +/- 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V _{DD2.5} , A _{VDD}		2.375		2.625	V
High-level input voltage	V _{IHCLK}	CLK_INT, CLK_INC	0.6		0.95	V
Low-level input voltage	V _{ILCLK}		-0.15		0.15	V
Crossing point voltage	V _{IXCLK}		0.2		0.55	V
Difference in crossing point voltage	V _{IXCLK}				0.15	V
Input threshold voltage	V _{TH}	Singled-ended CLK_IN ¹	0.35		0.5V _{DD2.5}	V
High-level input voltage for single-ended CLK_IN	V _{IHSE}		V _{TH} + 0.3		2.625	V
Low-level input voltage for single-ended CLK_IN	V _{ILSE}		-0.15		V _{TH} - 0.3	V
High-level input voltage	V _{IH}	OE, AS1, AS2, BYPASS#/PLL	1.4		2.625	V
Low-level input voltage	V _{IL}		-0.15		0.8	V
High-level input voltage - SMBus	V _{IHSMB}	SMBCLK, SMBDAT	1.4		3.465 ²	V
Low-level input voltage - SMBus	V _{ILSMB}		-0.15		0.8	V

Notes:

- 1 When using singled-ended clock input, V_{TH} is supplied to CLK_INTC as shown in Figure 2. Duty cycle of singled-ended CLK_IN is measured at V_{TH}.
- 2 This range of SMBus input high voltages allows the 9220 to co-exist with 3.3V, 2.5V and 1.8V devices on the same SMBus.

AC Characteristics-Outputs

T_A = -40°C to +85°C; Supply Voltage AVDD2.5, VDD2.5 = 2.5 V +/- 5% (unless otherwise stated)

PARAMETER ¹	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Short term jitter (over 1 to 6 clock cycles)	t _J ²	f = 400 to 635 MHz	-		40	ps
		f = 635 to 800 MHz	-		30	ps
Cycle-to-cycle Jitter	T _{Jcyc-cyc}				100	ps
Duty cycle	DC		45		55	%
Output rise and fall times	t _R , t _F	20% to 80% of output voltage	140		300	ps
Difference between output rise and fall time on same pin of a single device	t _{R-F}	20% to 80% of output voltage	-		100	ps
Dynamic output impedance	Z _{OUT} ²	V _{OL} = 0.9 V	1000		-	Ω

Notes:

- 1 Guaranteed by design and characterization, not 100% tested in production
- 2 Z_{out} is defined at the output pins.

AC Characteristics-Inputs

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$; Supply Voltage AVDD2.5, VDD2.5 = 2.5 V +/- 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
CLK_INT/CLK_INC cycle time ¹	t_{CYCLEIN}		9	10	11	ns
Cycle-to-Cycle Jitter	$t_{\text{cyc}}-t_{\text{cyc}}^2$				185	ps
Input clock duty cycle	d_{tin}	over 10,000 cycles	40		60	%
CLK_INT/CLK_INC rise and fall time	$t_{\text{R}}, t_{\text{F}}$	20% to 80% of input voltage	175		700	ps
Difference between input rise and fall time on same pin of a single device	$t_{\text{R-F}}$	20% to 80% of input voltage	-		150	ps
Spread spectrum modulation frequency	f_{INM}^3		30		33	kHz
Spread spectrum modulation index	m_{INDEX}^3	Triangular modulation			0.6	%
		Non-triangular modulation			0.54	%
Input clock slew rate	$t_{\text{sl(l)}}$	20% to 80% of input voltage	1		4	V/ns
Input Capacitance ⁵	C_{INCLK}	CLK_INT, CLK_INC			7	pF
Input Capacitance ⁵	C_{IN}	VI = V _{DD2.5} or GND			10	pF
CLK_INT cycle time	t_{CYCLETST}	Bypass Mode	4		40	ns
SMBus clock frequency	f_{SMB}		10		100	kHz

Notes:

- 1 Measured at $(V_{\text{IH(nom)}} - V_{\text{IL(nom)}})/2$ and is the absolute value of the worst case deviation.
- 2 Measured at crossing points for differential clock input or at V_{TH} for single-ended clock input.
- 3 If input modulation is used. Input modulation is not necessary.
- 4 The amount of allowed spreading for non-triangular modulation is determined by the induced downstream tracking skew.
- 5 Capacitance measured at $f = 1$ MHz, DC bias = 0.9V, V_{AC} < 100mV.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		$^{\circ}\text{C/W}$
	θ_{JA}	1 m/s air flow		95		$^{\circ}\text{C/W}$
	θ_{JA}	3 m/s air flow		80		$^{\circ}\text{C/W}$
Thermal Resistance Junction to Case	θ_{JC}			20		$^{\circ}\text{C/W}$
Thermal Resistance Junction to Top of Case	Ψ_{JT}	Still Air		4.5		$^{\circ}\text{C/W}$
Maximum Case Temp					120	$^{\circ}\text{C}$

Clock Output Drivers

Figure 2 shows the clock driver equivalent circuit. The differential driver produces a specified voltage swing on the channel by switching the currents going into ODCLK_T and ODCLK_C. The external resistor R_{RC} at the IREFY pin sets the maximum current. The minimum current is zero.

The voltage at the IREFY pin, V_{IREFY} , is by design equal to 1 V nominally, and the driver current is seven times the current flowing through R_{RC} . So, the output low current can be estimated as $I_{OL} = 7 / R_{RC}$.

The driver output characteristics are defined together with the external resistors, R_1 , R_2 , and R_3 . The output clock signals are specified at the measurement points indicated in Figure 2. Table 5 shows example values for the resistors.

R_1 , R_2 , and R_3 and the clock driver output impedance, Z_{OUT} , must match the impedance of the channel, Z_{CH} , to minimize secondary reflections. Z_{OUT} is specified as 1000 Ohms, minimum to accomplish this. The effective impedance can be estimated by:

$$(1000R_1/(1000+R_1)+R_2) R_3/(1000R_1/(1000+R_1)+R_2+R_3)$$

Pull-up resistor R_T terminates the transmission line at the load to minimize clock signal reflection signal reflections. Table 5 shows the resistor values for establishing and effective source termination impedance of 49.2 Ohms to match a 50 Ohm channel. The termination voltages are 2.5 V for V_{TS} and 1.2 V for V_T . The resistor values $R_1 = 38.3$ Ohms, $R_2 = 19.1$ Ohms, $R_3 = 54.9$ Ohms and $R_{RC} = 200$ Ohms can be used to match a 28 Ohm channel.

Table 5. Example Resistor Values and Termination Voltages for a 50 Ohm Channel¹

Symbol	Parameter	Value	Tolerance	Unit
R_1	Termination resistor	39.2	+/- 1%	Ω
R_2	Termination resistor	66.5	+/- 1%	Ω
R_3	Termination resistor	93.1	+/- 1%	Ω
R_T	Termination resistor	49.9	+/- 1%	Ω
R_{RC}	Swing control resistor	200	+/- 1%	Ω
V_{TS}	Source termination voltage	2.5	+/-5%	V
V_T	Termination voltage	1.2	+/-5%	V

Notes:

- 1 A different set of resistors is used in Figure 2 when testing for maximum output current of the clock driver (I_{OLABS}). These resistors are: $R_1 = 23\Omega$, $R_2 = 36.5\Omega$, $R_3 = 52.3\Omega$, $R_T=28\Omega$, $R_{RC} = 118\Omega$

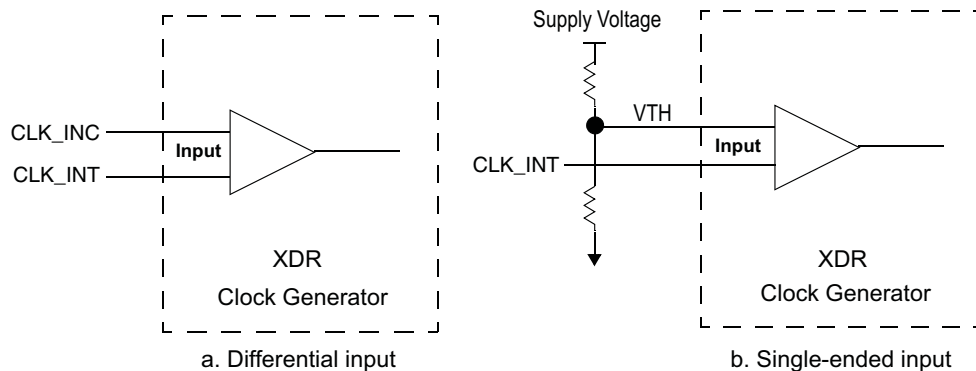


Figure 1. Differential and single-ended reference clock inputs

Input Clock Signal

The ICS9220 receives either a differential or single-ended reference clock (CLK_INT/C). When the reference input clock is from a differential clock source, it must meet the voltage levels and timing requirements listed in the **DC Characteristics – Inputs** and **AC Characteristics – Inputs** tables.

For a single-ended clock input, an external voltage divider and a supply voltage, as shown in Figure 2, provide a reference voltage V_{TH} at the CLK_INC pin to determine the proper switching point for CLK_INT. The range of V_{TH} is specified in the **DC Characteristics – Inputs** table.

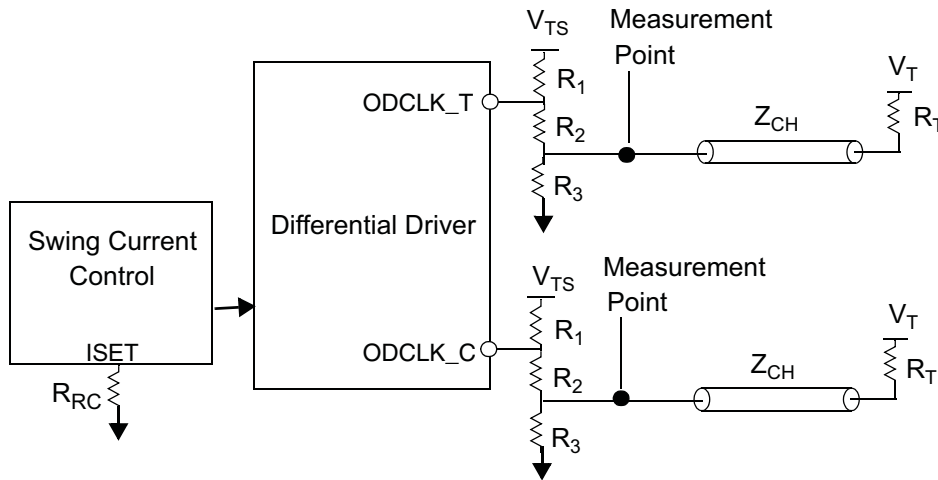


Figure 2. Example System Clock Driver Equivalent Circuit

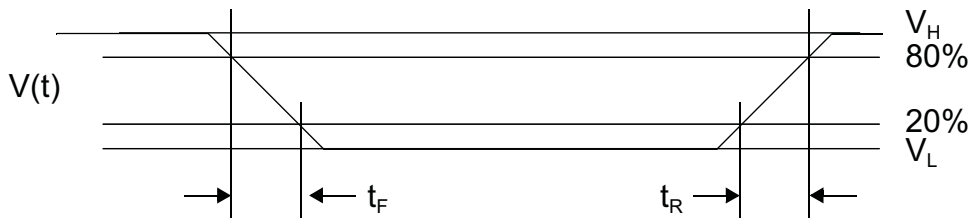


Figure 3. Input and Output Voltage Waveforms

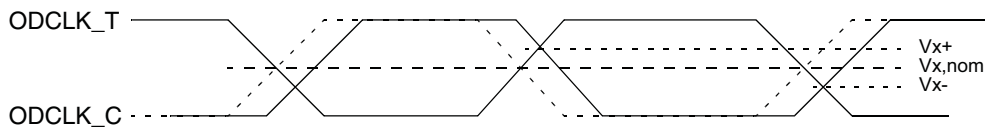


Figure 4. Crossing-point Voltage

Power Sequencing

Supply voltages for the ICS9220 must be applied before, or at the same time and external input and output signals.

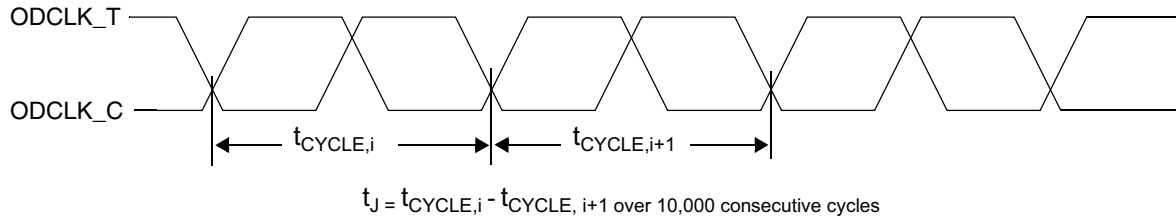


Figure 5. Cycle-to-cycle Jitter

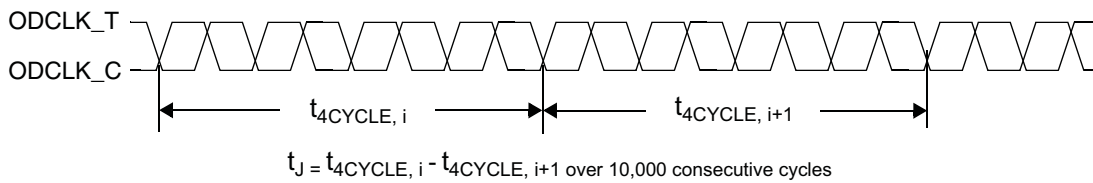


Figure 6. Short-term Jitter

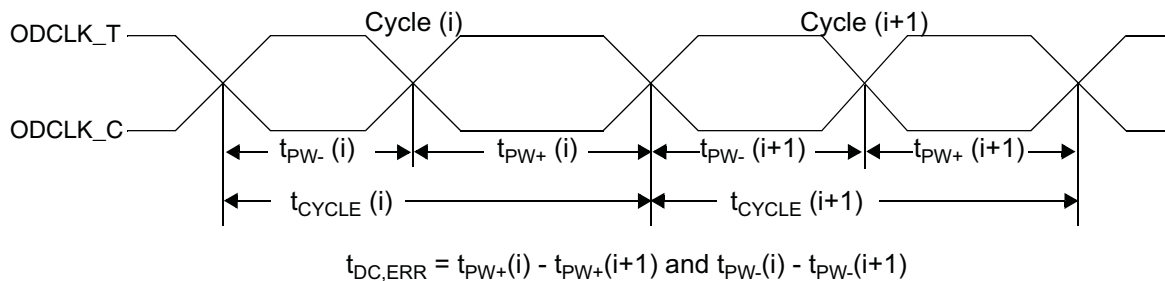
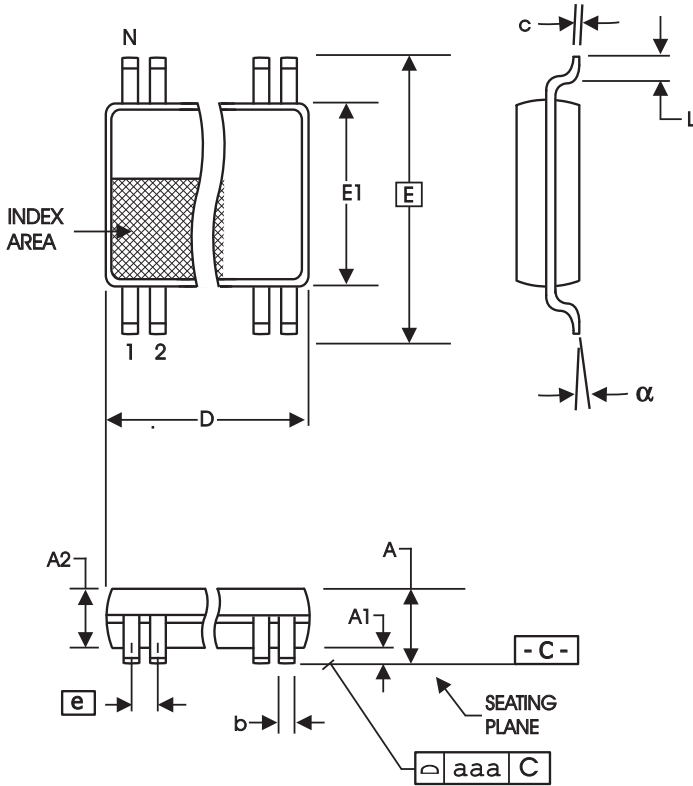


Figure 7. Cycle-to-cycle Duty Cycle Error



4.40 mm. Body, 0.65 mm. Pitch TSSOP
 (173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9220BGILF	Tubes	28-pin TSSOP	-40 to +85°C
9220BGILFT	Tape and Reel	28-pin TSSOP	-40 to +85°C

"LF" suffix to the part numbers are the Pb-Free configuration and are RoHS compliant.

"B" is the device revision designator (will not correlate to the datasheet revision).

Revision History

Rev.	Issue Date	Description	Page #
0.1	12/10/2007	Initial release	-
0.2	11/9/2009	Removed "Advanced Information" banner	-
A	1/26/2010	Removed watermarks; updated ordering information; released to final	-