2A High Side Load Switches

Features

- **70mΩ High Side MOSFET**
- **Wide Supply Voltage Range: 2.7V to 5.5V**
- **Current-Limit and Short-Circuit Protections**
- **Over-Temperature Protection**
- **Fault Indication Output**
- **Logic Level Enable Pin**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

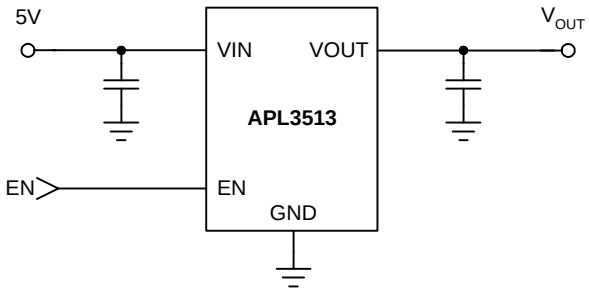
- **Cellular Telephones**
- **Digital Still Cameras**
- **Hot Swap Supplies**
- **Notebook Computers**
- **Personal Communication Devices**
- **Personal Digital Assistants (PDAs)**

General Description

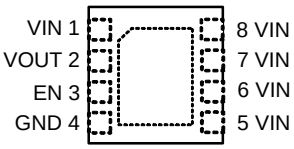
The APL3513 is a power-distribution switch with some protection that can deliver current up to 2A. The device incorporates a 70mΩ N-channel MOSFET power switch that is controlled by an enable logic pin.

The protection features include current-limit protection, short-circuit protection, and over-temperature protection. The device limits the output current at current limit threshold level. When V_{OUT} drops below V_{IN}-1V, the devices limit the current to a lower and safer level. The over-temperature protection limits the junction temperature below 140°C in case of short circuit or over load conditions.

Simplified Application Circuit



Pin Configuration



APL3513
TDFN2x2-8(Top View)

= Exposed Pad
(connected to ground plane for better heat dissipation)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APL3513 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN2x2-8 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL3513 QB: 	X - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Input Voltage (VIN to GND)	-0.3 ~ 7	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ 7	V
V_{ENB}, V_{EN}	EN, ENB to GND Voltage	-0.3 ~ 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) TDFN2x2-8	80	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TDFN2x2-8 is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	2.7 ~ 5.5	V
I_{OUT}	OUT Output Current	0 ~2	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit

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Electrical Characteristics

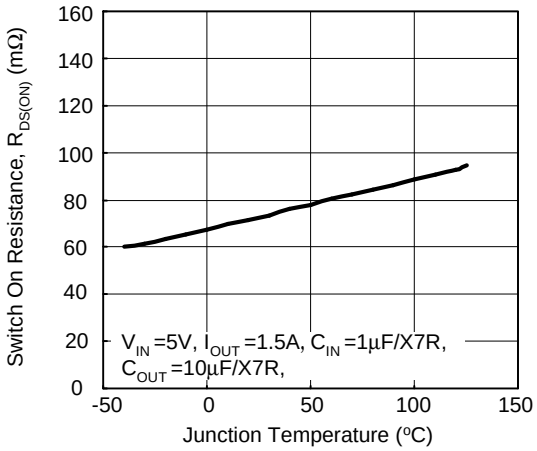
Unless otherwise specified, these specifications apply over V_{IN}=5V, V_{EN} =5V or V_{ENB}=0V and T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3513			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	VIN Supply Current	No load, V_{EN}=0V	-	-	1	µA
		No load, V_{EN}=5V	-	65	100	µA
	Leakage Current	VOUT=GND, V_{EN}=0V	-	-	1	µA
	Reverse Leakage Current	VIN=GND, V_{OUT}=5V, V_{EN}=0V	-	-	1	µA
POWER SWITCH						
$R_{DS(ON)}$	Power Switch On Resistance	I_{OUT}=1.5A, T_A= 25 °C	-	70	90	mΩ
UNDER-VOLTAGE LOCKOUT (UVLO)						
	VIN UVLO Threshold Voltage	V_{IN} rising, T_A= -40 ~ 85 °C	2.3	-	2.65	V
	VIN UVLO Hysteresis		-	0.2	-	V
CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTIONS						
I_{LIM}	Current Limit Threshold	V_{IN}=2.7V to 5.5V, T_A= -40 ~ 85 °C	2.1	2.5	3.6	A
I_{SHORT}	Short-Circuit Output Current	V_{IN}=2.7V to 5.5V	-	0.8	-	A
EN INPUT PIN						
V_{IH}	Input Logic HIGH	V_{IN}=2.7V to 5V	2	-	-	V
V_{IL}	Input Logic LOW	V_{IN}=2.7V to 5V	-	-	0.8	V
	Input Current		-	-	1	µA
	VOUT Discharge Resistance	V_{EN}=0V	-	150	-	Ω
$t_{D(ON)}$	Turn on Delay Time		-	30	-	µs
$t_{D(OFF)}$	Turn off Delay Time		-	30	-	µs
t_{SS}	Soft-Start Time	No load, C_{OUT}=1µF, V_{IN}=5V	-	400	-	µs
OVER-TEMPERATURE PROTECTION (OTP)						
T_{OTP}	Over-Temperature Threshold	T_J rising	-	140	-	°C
	Over-Temperature Hysteresis		-	20	-	°C

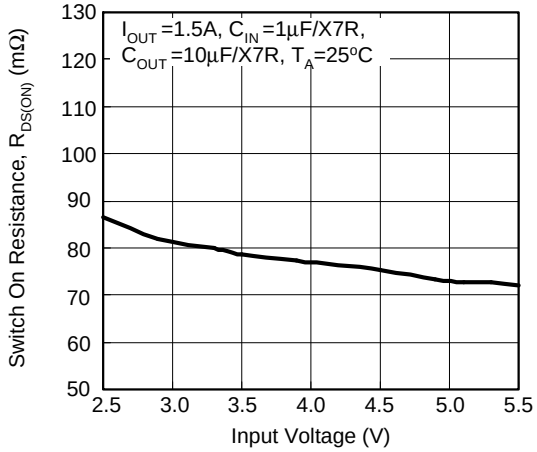
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Typical Operating Characteristics

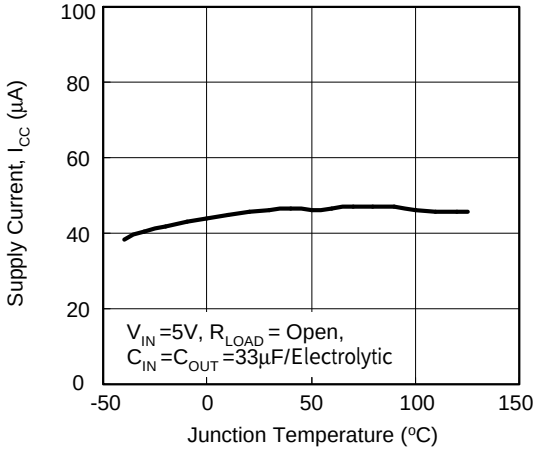
Switch On Resistance vs. Junction Temperature



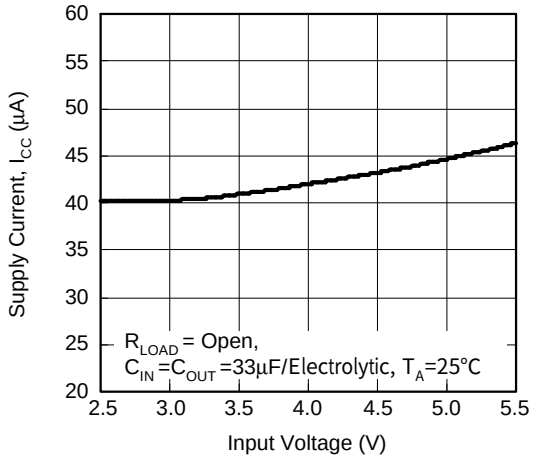
Switch On Resistance vs. Input Voltage



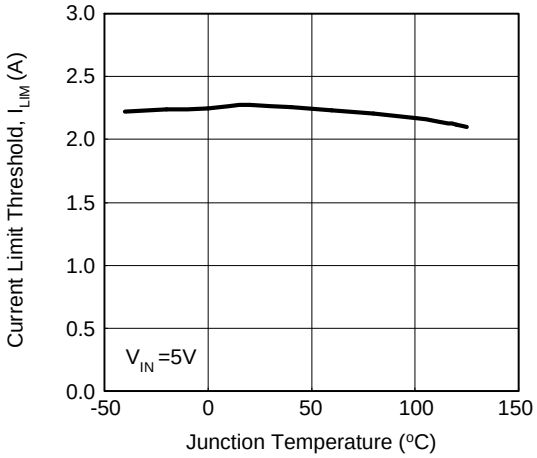
Supply Current vs. Junction Temperature



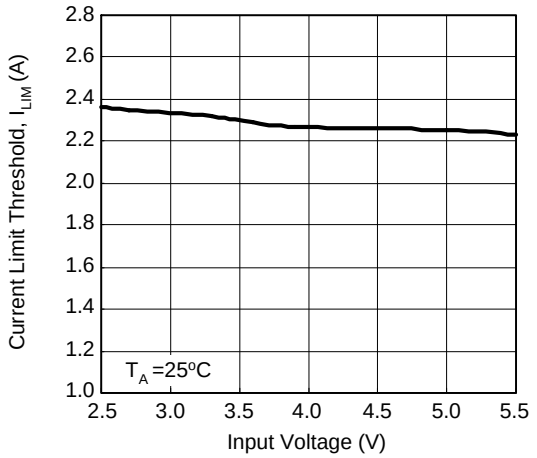
Supply Current vs. Input Voltage



Current Limit Threshold vs. Junction Temperature

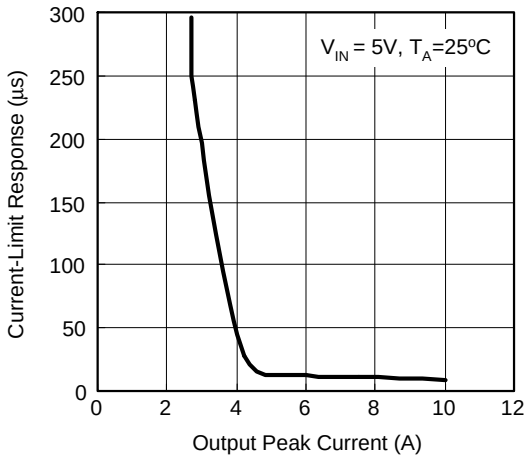


Current Limit Threshold vs. Input Voltage

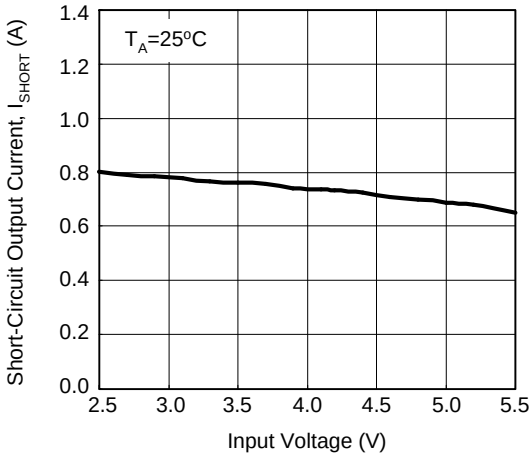


Typical Operating Characteristics (Cont.)

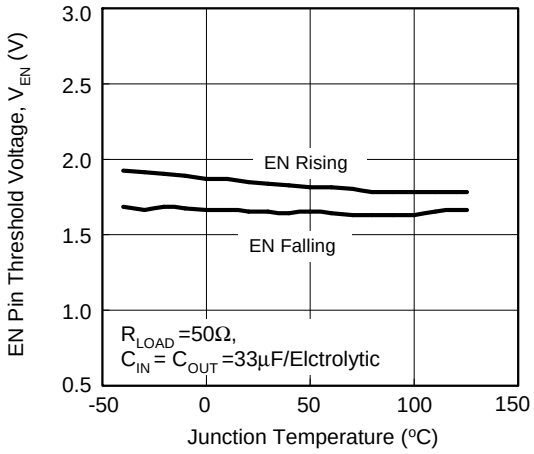
Current-Limit Response vs. Output Peak Current



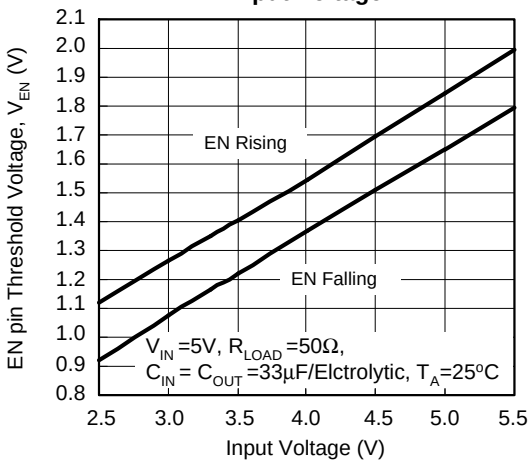
Short-Circuit Output Current vs. Input Voltage



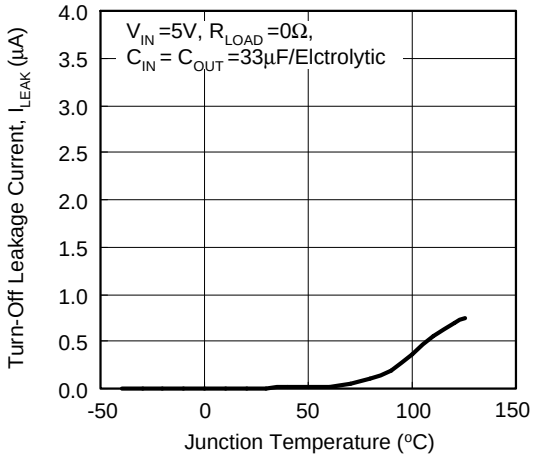
EN Pin Threshold Voltage vs. Junction Temperature



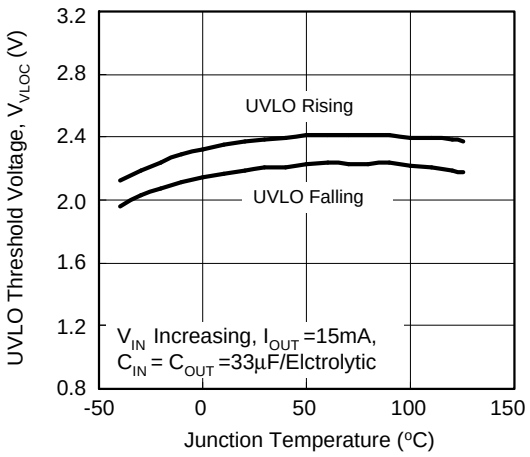
EN Pin Threshold Voltage vs. Input Voltage



Turn-Off Leakage Current vs. Junction Temperature



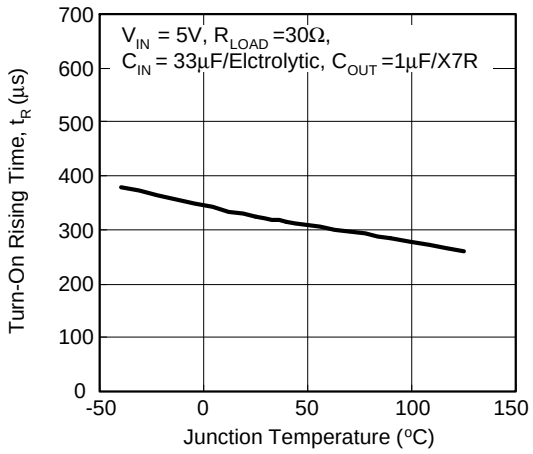
UVLO Threshold Voltage vs. Junction Temperature



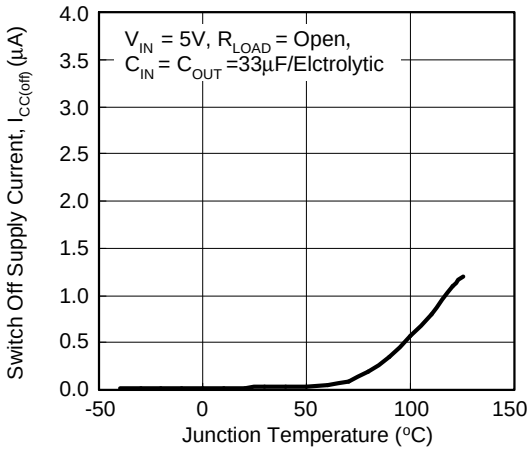
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Typical Operating Characteristics (Cont.)

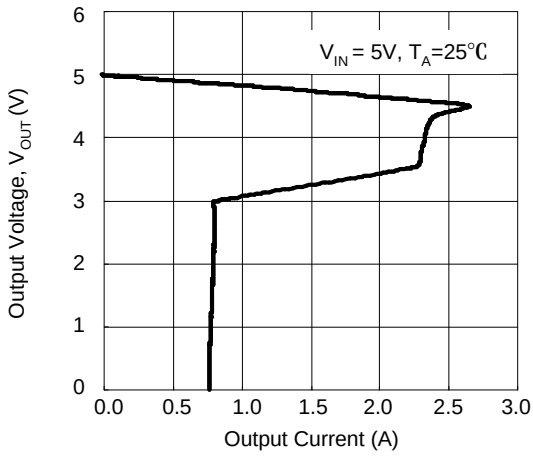
Turn-On Rising Time vs. Junction Temperature



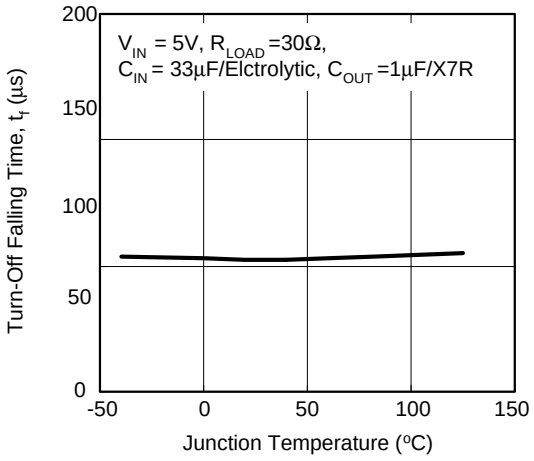
Switch Off Supply Current vs. Junction Temperature



Output Voltage vs. Output Current



Turn-Off Falling Time vs. Junction Temperature

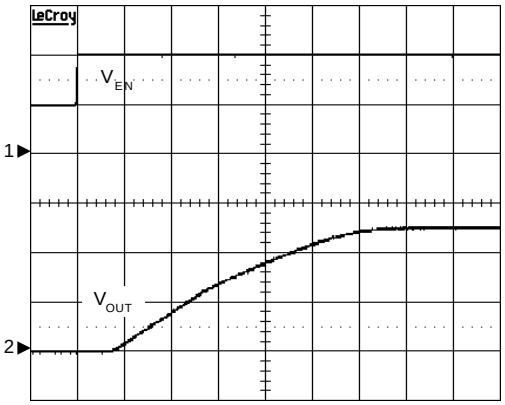


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Operating Waveforms

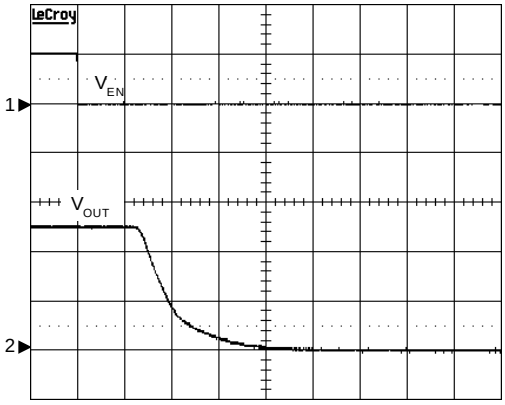
The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Turn On Response



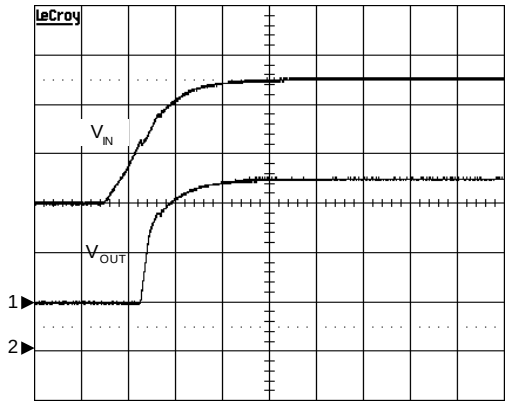
V_{IN} =5V, R_{LOAD} =30Ω, C_{IN} =1μF/Electrolytic,
C_{OUT} =0.1μF/Electrolytic
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
TIME: 100μs/Div

Turn Off Response



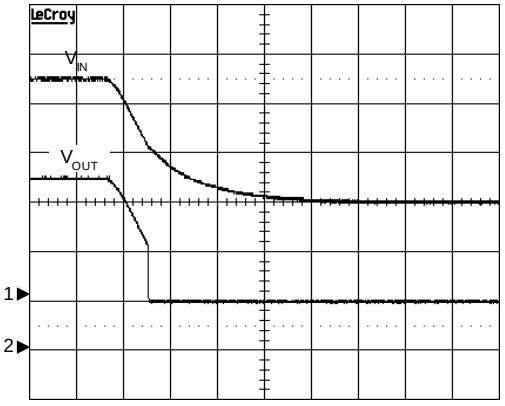
V_{IN} =5V, R_{LOAD} =30Ω, C_{IN} =1μF/Electrolytic,
C_{OUT} =0.1μF/Electrolytic
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
TIME: 10μs/Div

Power On



V_{IN} =5V, R_{LOAD} =30Ω, C_{IN} =1μF/Electrolytic,
C_{OUT} =0.1μF/Electrolytic
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
TIME:5ms/Div

Power Off



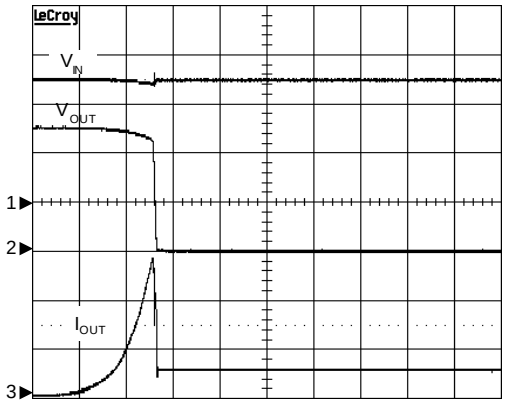
V_{IN} =5V, R_{LOAD} =30Ω, C_{IN} =1μF/Electrolytic,
C_{OUT} =0.1μF/Electrolytic
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
TIME:10ms/Div

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Operating Waveforms (Cont.)

The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Over Load Response



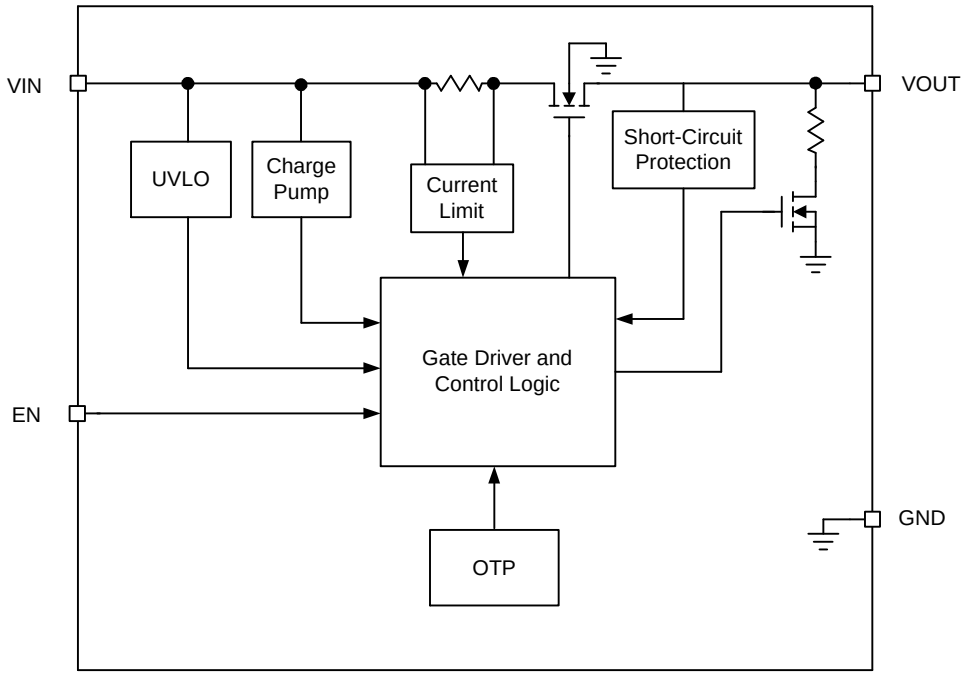
V_{IN} =5V, C_{IN} =1µF/Electrolytic, C_{OUT} =0.1µF/ Electrolytic
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 1ms/Div

Pin Description

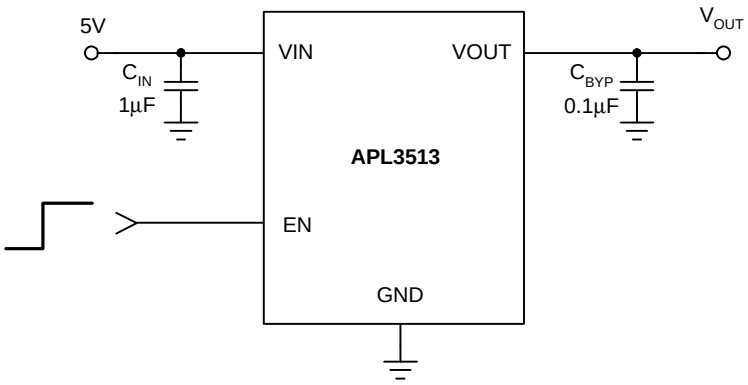
PIN		FUNCTION
NO.	NAME	
1,5,6,7,8	VIN	Power Supply Input. Connect this pin to external DC supply.
2	VOUT	Output Voltage Pin. The output voltage follows the input voltage. When ENB is high or EN is low, the output voltage is discharged by an internal resistor.
3	EN	Enable control input. Pulling this pin to high will enable the device and pulling this pin to low will disable device. The EN pin cannot be left floating.
4	GND	Ground.

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Block Diagram



Typical Application Circuit



Function Description

VIN Under-Voltage Lockout (UVLO)

The APL3513 series of power switches have a built-in under-voltage lockout circuit to keep the output shutting off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Power Switch

The power switch is an N-channel MOSFET with a low $R_{DS(ON)}$. The internal power MOSFET does not have the body diode. When IC is off, the MOSFET prevents a current flowing from the VOUT back to VIN and VIN to VOUT.

Current-Limit Protection

The APL3513 series of power switches provide the current-limit protection function. During current limit, the devices limit output current at current limit threshold. For reliable operation, the device should not be operated in current limit for extended period.

Short-Circuit Protection

When the output voltage drops below V_{IN}-1V, which is caused by an over-load or a short-circuit, the devices limit the output current down to a safe level. The short-circuit current limit is used to reduce the power dissipation during short-circuit conditions. If the junction temperature reaches over-temperature threshold, the device will enter the thermal shutdown.

Enable/Disable

Pull the EN below 0.8V will disable the device, and EN above 2V will enable the device. When the IC is disabled, the supply current is reduced to less than 1μA. The enable input is compatible with both TTL and CMOS logic levels. The EN pin cannot be left floating.

Over-Temperature Protection

When the junction temperature exceeds 140°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 20°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

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Application Information

Input Capacitor

A 1µF ceramic bypass capacitor from V_{IN} to GND, located near the APL3513, is strongly recommended to suppress the ringing during short circuit fault event. Without the bypass capacitor, the output short may cause sufficient ringing on the input (from supply lead inductance) to damage internal control circuitry.

Output Capacitor

A bypassing 0.1µF ceramic capacitor improves the immunity of the device to short-circuit transients. A low-ESR high capacitance between V_{OUT} and GND is suggested to reduce the voltage droop during load transient.

Layout Consideration

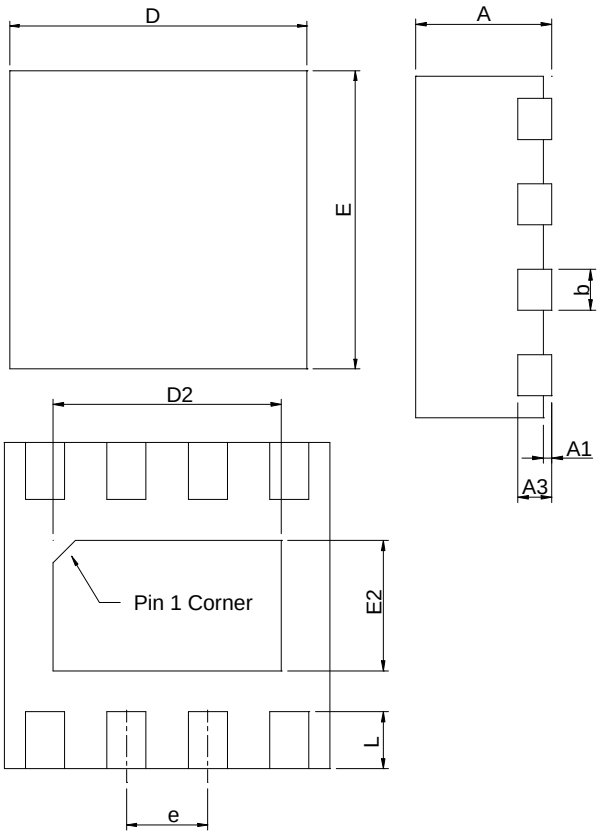
The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

1. Please place the input capacitors near the VIN pin as close as possible.
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high-frequency ripples.
3. Locate APL3513 and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
5. Keep V_{IN} and V_{OUT} traces as wide and short as possible.

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Package Information

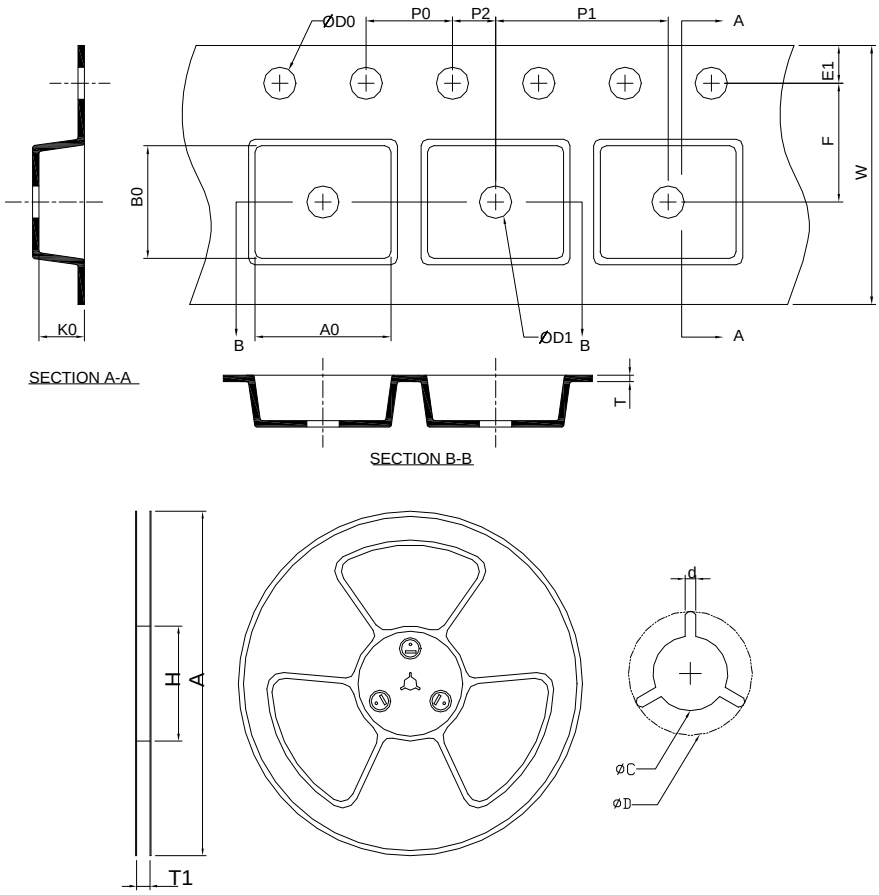
TDFN2x2-8



SYMBOL	TDFN2x2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018

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Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	3.35 MIN	3.35 MIN	1.30±0.20

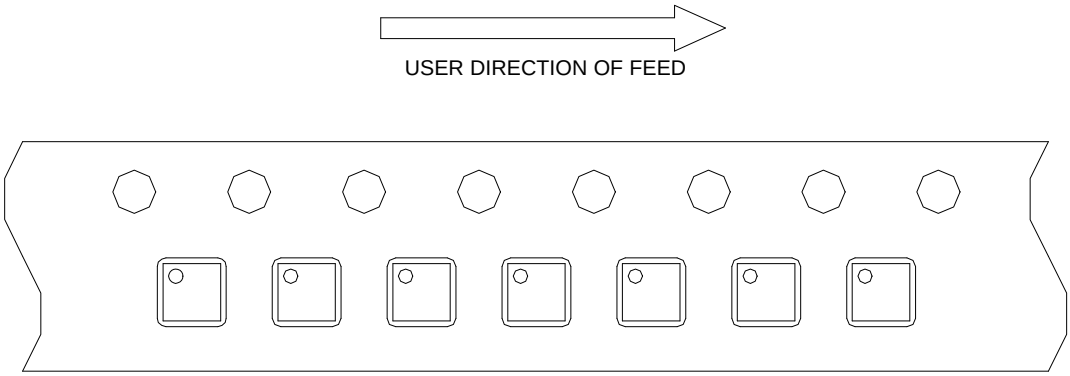
(mm)

Devices Per Unit

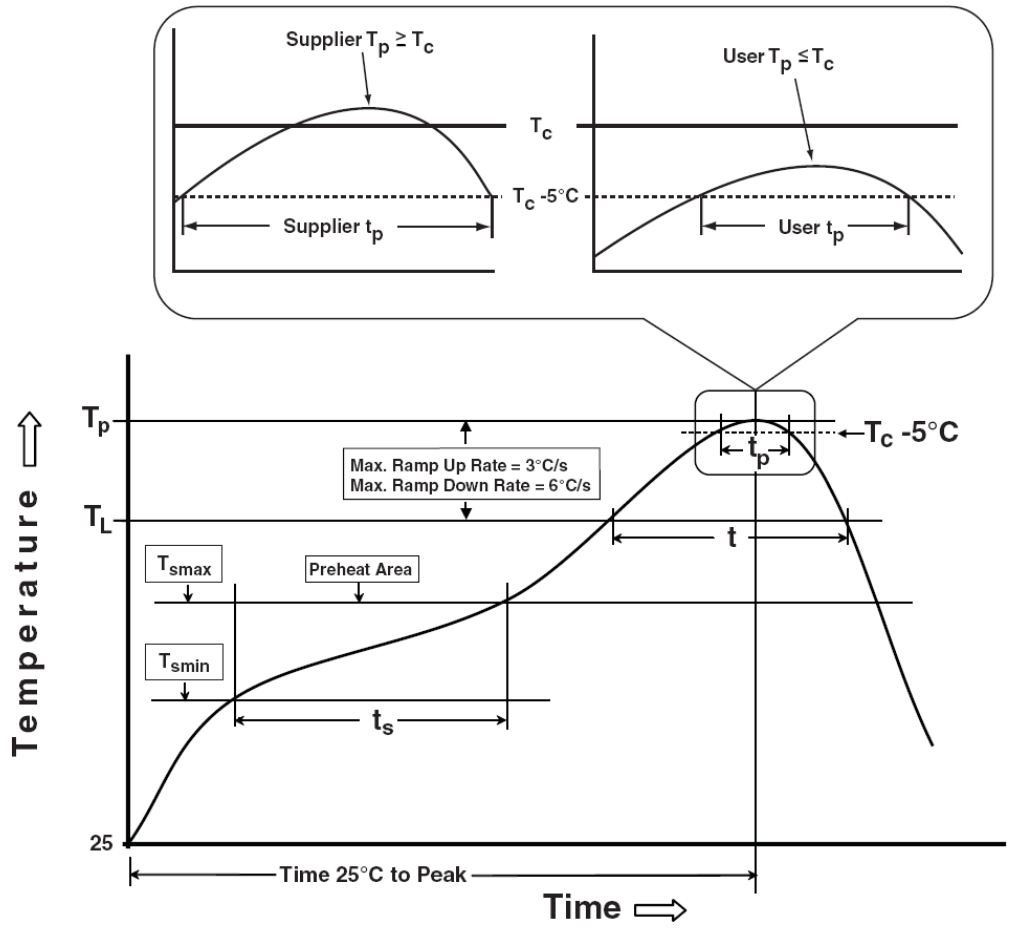
Package Type	Unit	Quantity
TDFN2x2-8	Tape & Reel	3000

Taping Direction Information

TDFN2x2-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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