



A23L2617/A23L26171 Series

4M X 16 / 8M X 8 BIT CMOS MASK ROM WITH PAGE MODE

Preliminary

Document Title

4M X 16 / 8M X 8 BIT CMOS MASK ROM WITH PAGE MODE

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.0	Initial issue	August 18, 2005	Preliminary



A23L2617/A23L26171 Series

Preliminary

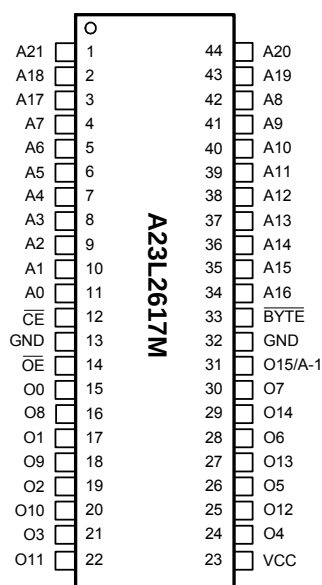
4M X 16 / 8M X 8 BIT CMOS MASK ROM

Features

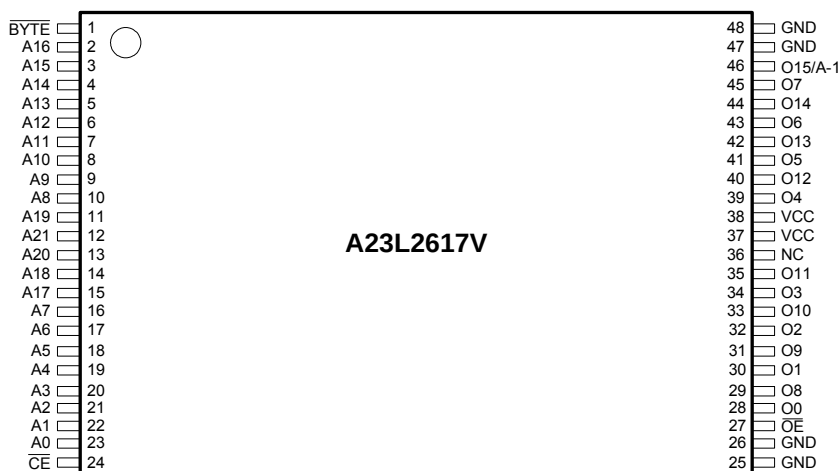
- 4M x 16 bit or 8M x 8 bit organization
- Supply voltage range: 2.7V~3.6V
- Random access time: 70ns (max.)/3.0V~3.6V
80ns (max.)/2.7V~3.6V
- Current: Operating: 30mA
Standby: 30 μ A
- Page Size:
 - 8 words per page
 - Page access: 30ns (max.)/2.7V~3.6V
- Three-state outputs for wired-OR expansion
- Full static operation
- All inputs and outputs are directly TTL-compatible
- Available in 44-pin SOP, 48-pin TSOP (forward, reverse type and flash memory's pinouts compatible)
- Pinout compatible with flash type (A23L26171)

Pin Configurations

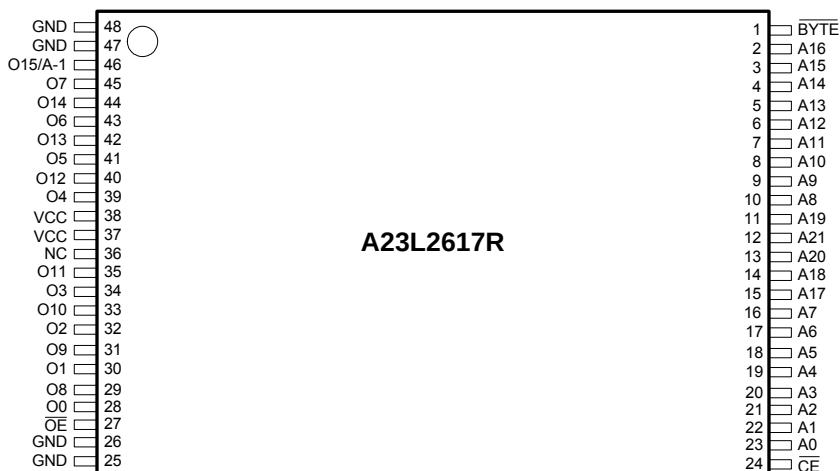
■ SOP

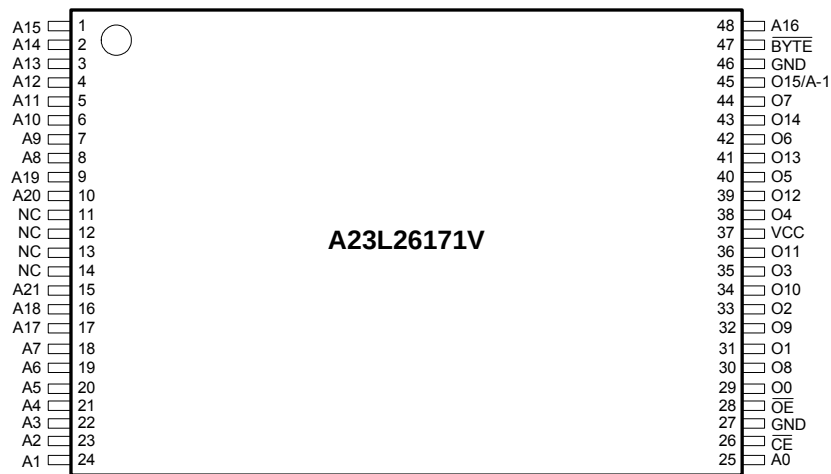
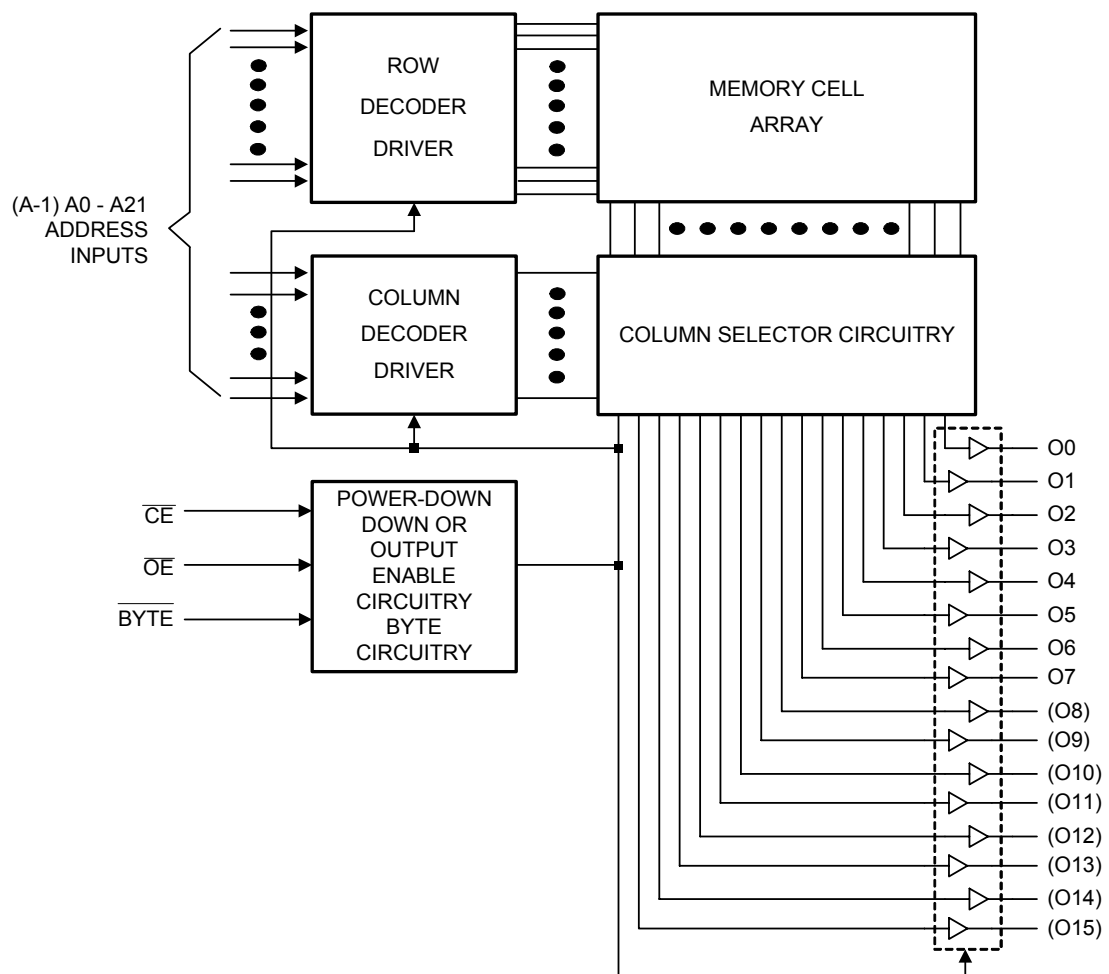


■ TSOP (forward type)



■ TSOP (reverse type)



Pin Configurations (continued)
■ TSOP (forward type)

Block Diagram


Pin Descriptions

Pin No.			Symbol	Description
44L SOP (A23L2617) (8M X 8 only)	48L TSOP (A23L2617)	48L TSOP (A23L26171)		
1-11, 34-44	2-23	1-10, 15-25, 48	A0-A21	Address Inputs
15-22, 24-30	28-35, 39-45	29-36, 38-44	O0-O14	Data Outputs
31	46	45	O15/A-1	Output 15(WORD mode) /LSB Address (BYTE mode)
12	24	26	$\overline{CE}$	Chip Enable Input
14	27	28	$\overline{OE}$	Output Enable Input
33	1	47	$\overline{BYTE}$	BYTE or WORD mode Selection
23	37-38	37	VCC	Power Supply
13, 32	25-26, 47-48	27, 46	GND	Ground
1	36	11-14	NC	No Connection

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply Voltage	2.7	3.6	V
GND	Ground	0	0	V
V _{IH}	Input High Voltage	2.2	VCC+0.3	V
V _{IL}	Input Low Voltage	- 0.3	0.6	V

Absolute Maximum Ratings*

Ambient Operating Temperature 0°C to + 70°C
 Storage Temperature -65°C to + 125°C
 Output Voltage -0.5V to VCC + 0.5V
 Input Voltage -0.5V to VCC + 0.5V

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0°C to + 70°C, VCC = 2.7V~3.6V, GND = 0V for -80, VCC = 3.0V~3.6V, GND = 0 for -70)

Symbol	Parameter	Min.	Max.	Unit	Conditions	Note
V _{OH}	Output High Voltage	2.4		V	I _{OH} = -0.4mA (3V)	
V _{OL}	Output Low Voltage		0.4	V	I _{OL} = 1.6mA (3V)	
V _{IH}	Input High Voltage	2.2	VCC + 0.3	V		
V _{IL}	Input Low Voltage	-0.3	0.6	V		
I _{LI}	Input Leakage Current		+10	μA	VCC = max. V _{IN} = VCC to GND	
I _{LO}	Output Leakage Current		+10	μA	VCC = max. V _{OUT} = VCC to GND	1
I _{CC}	Operating Supply Current		50	mA	t _{cy} = min.	2
I _{SB}	Standby Supply Current (TTL)		1.5	mA	$\overline{CE} = V_{IH}$	
I _{SB1}	Standby Supply Current (CMOS)		30	μA	$\overline{CE} \geq VCC - 0.2V$	

Capacitance

Symbol	Parameter	Min.	Max.	Unit	Test Conditions	Note
C _i	Input Capacitance		10	pF	T _A = 25°C f = 1.0MHz	3
C _o	Output Capacitance		10	pF		

AC Characteristics (T_A = 0°C to +70°C, VCC = 2.7V~3.6V for -80, VCC = 3.0V~3.6V for -70, GND = 0V)

Symbol	Parameter	A23L2617/ A23L26171-70		A23L2617/ A23L26171-80		Unit	Note
		Min.	Max.	Min.	Max.		
t _{cyc}	Cycle Time	70		80		ns	
t _{AA}	Address Access Time		70		80	ns	
t _{ACE}	Chip Enable Access Time		70		80	ns	
t _{PC}	Page Cycle Time	30		30		ns	
t _{PAC}	Page Access Time		30		30	ns	
t _{AOE}	Output Enable Access Time		30		30	ns	
t _{OH}	Output Hold after Address Change	10		10		ns	
t _{LZ}	Output Low Z Delay	10		10		ns	4, 6
t _{HZ}	Output High Z Delay*		20		20	ns	5, 6

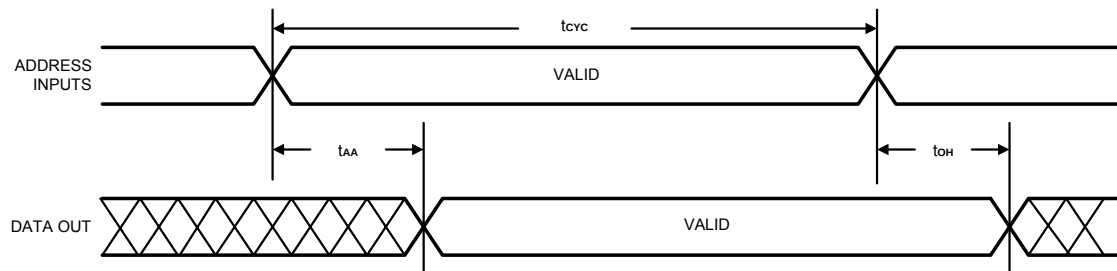
* t_{HZ} is specified from either $\overline{OE}$ or $\overline{CE}$ going disabled, whichever occurs first.

Notes:

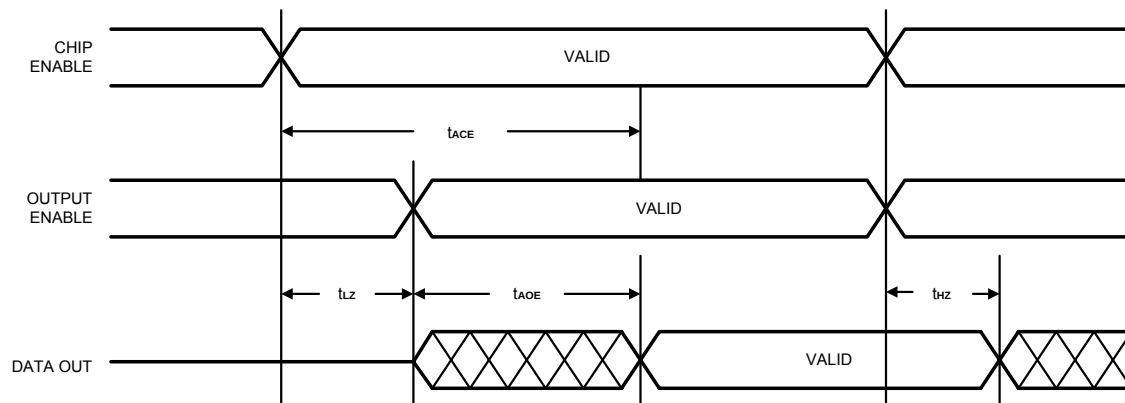
1. $\overline{OE} / \overline{CE} = V_{IH}$ (Output is unloaded)
2. $V_{IN} = V_{IH}/V_{IL}$, $\overline{OE} / \overline{CE} = V_{IL}$ (Output is unloaded)
3. This parameter is periodically sampled and is not 100% tested. All pins, except pins under test, are tied to AC ground.
4. Output LOW impedance delay (t_{LZ}) is measured from $\overline{CE}$ or $\overline{OE}$ going active.
5. Output HIGH impedance delay (t_{HZ}) is measured from $\overline{CE}$ or $\overline{OE}$ going inactive.
6. This parameter is sampled and not 100% tested.

Timing Waveforms

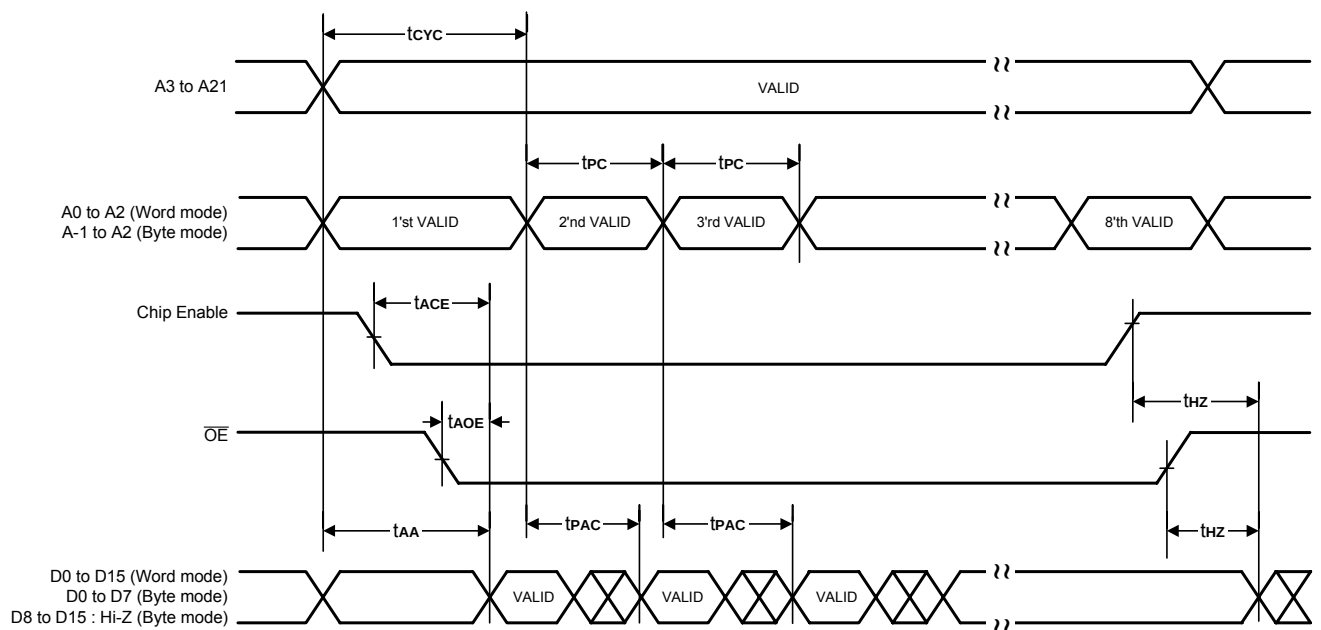
Propagation Delay from Address ($\overline{CE}$ = Active, $\overline{OE}$ = Active)



Propagation Delay from Chip Enable or Output Enable (Address Valid)



Page Access Mode Read Cycle



AC Test Conditions

Part No.	A23L2617/ A23L26171-70	A23L2617/ A23L26171-80
Applied Voltage	3.0V~3.6V	2.7V~3.6V
Input Pulse Levels	0.4V to 2.4V	0.4V to 2.4V
Input Rise and Fall Time	10 ns	10 ns
Timing Measurement Reference Level	$V_{IN} = 1.4V$, $V_{OUT} = 1.4V$	$V_{IN} = 1.4V$, $V_{OUT} = 1.4V$
Output Load	1 TTL gate and $C_L = 100pF$	1 TTL gate and $C_L = 100pF$

Function Table

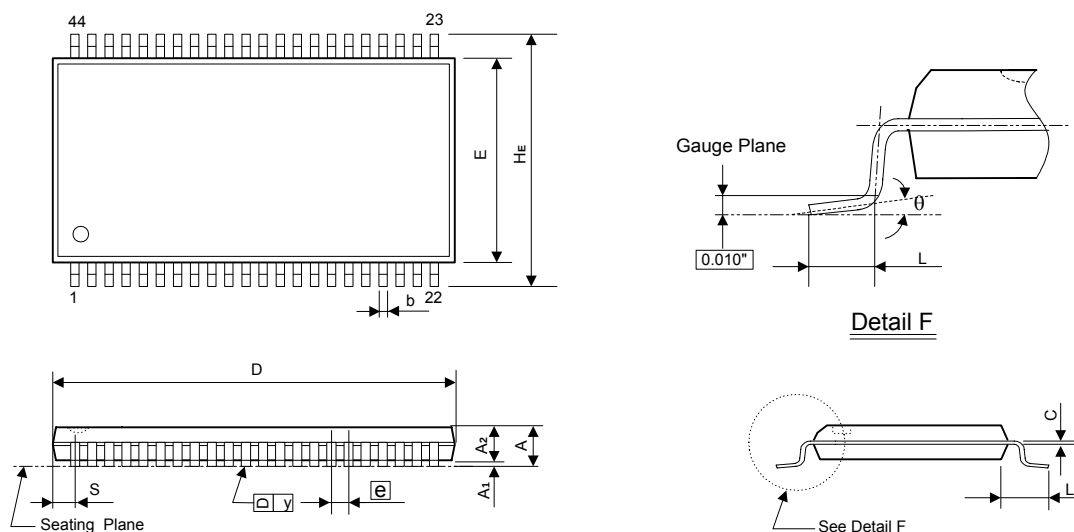
$\overline{CE}$	$\overline{OE}/NC$	$\overline{BYTE}$	O15/A-1	O0 - O7	O8 - O15	Mode
L	L	H	Data Pin O15	Data Out	Data out	Word
L	L	L	LSB Address A-1	Data Out	Hi - Z	Byte
H	X	X	X	Hi - Z	Hi - Z	Power-down
L	H	X	X	Hi - Z	Hi - Z	Output Disable

**Ordering Information**

Part No.	Access Time (ns)	Package
A23L2617M-70 (8M X 8 only)	70	44L SOP
A23L2617M-80 (8M X 8 only)	80	44L SOP
A23L2617V-70	70	48L TSOP (Forward)
A23L2617V-80	80	48L TSOP (Forward)
A23L2617R-70	70	48L TSOP (Reverse)
A23L2617R-80	80	48L TSOP (Reverse)
A23L26171V-70	70	48L TSOP (Flash Compatible)
A23L26171V-80	80	48L TSOP (Flash Compatible)

Package Information
SOP 44L Outline Dimensions

unit: inches/mm



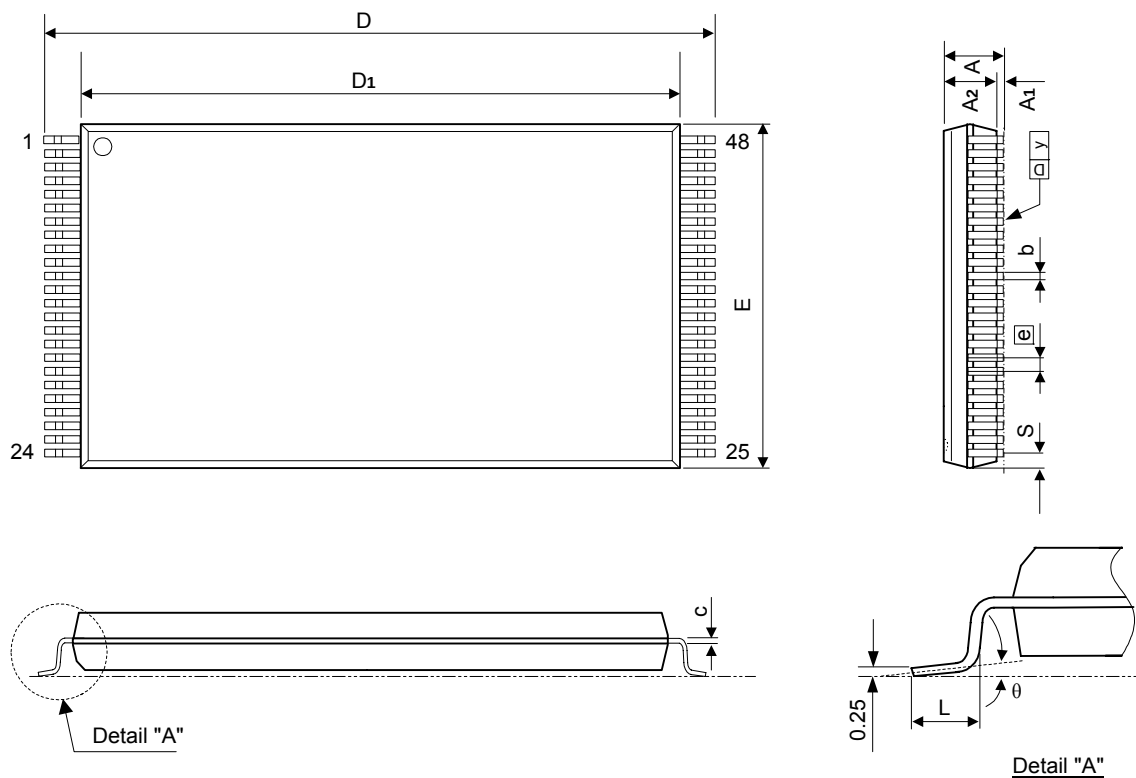
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.118	-	-	3.00
A1	0.004	-	-	0.10	-	-
A2	0.103	0.106	0.109	2.62	2.69	2.77
b	0.013	0.016	0.020	0.33	0.40	0.50
C	0.007	0.008	0.010	0.18	0.20	0.25
D	-	1.122	1.130	-	28.50	28.70
E	0.490	0.496	0.500	12.45	12.60	12.70
e	-	0.050	-	-	1.27	-
HE	0.620	0.631	0.643	15.75	16.03	16.33
L	0.024	0.032	0.040	0.61	0.80	1.02
L1	-	0.0675	-	-	1.71	-
S	-	-	0.045	-	-	1.14
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information
TSOP 48L (Type I) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A ₁	0.002	-	0.006	0.05	-	0.15
A ₂	0.037	0.039	0.042	0.94	1.00	1.06
b	0.007	0.009	0.011	0.18	0.22	0.27
c	0.004	-	0.008	0.12	-	0.20
D	0.779	0.787	0.795	19.80	20.00	20.20
D ₁	0.720	0.724	0.728	18.30	18.40	18.50
E	-	0.472	0.476	-	12.00	12.10
e	0.020 BASIC			0.50 BASIC		
L	0.016	0.020	0.024	0.40	0.50	0.60
S	0.011 Typ.			0.28 Typ.		
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.