

# Am186™EM/EMLV and Am188™EM/EMLV

## High Performance, 80C186-/80C188-Compatible and 80L186-/80L188-Compatible, 16-Bit Embedded Microcontrollers

### DISTINCTIVE CHARACTERISTICS

- **E86™ family 80C186- and 80C188-compatible microcontrollers with enhanced bus interface**
  - Lower system cost with higher performance
  - 3.3-V  $\pm$  3-V operation (Am186EMLV and Am188EMLV microcontrollers)
- **High performance**
  - 20-, 25-, 33-, and 40-MHz operating frequencies
  - Supports zero-wait-state operation at 25 MHz with 110-ns static memory (Am186™EMLV and Am188™EMLV microcontrollers) and 40 MHz with 70-ns static memory (Am186™EM and Am188™EM microcontrollers)
  - 1-Mbyte memory address space
  - 64-Kbyte I/O space
- **New features provide faster access to memory and remove the requirement for a 2x clock input**
  - Nonmultiplexed address bus
  - Phase-locked loop (PLL) allows processor to operate at the clock input frequency
- **New integrated peripherals provide increased functionality while reducing system cost**
  - Thirty-two programmable I/O (PIO) pins
  - Asynchronous serial port allows full-duplex, 7-bit or 8-bit data transfers
  - Synchronous serial interface allows half-duplex, bidirectional data transfer to and from ASICs
  - Pseudo static RAM (PSRAM) controller includes auto refresh capability
  - Reset configuration register
- **Familiar 80C186/80L186 peripherals**
  - Two independent DMA channels
  - Programmable interrupt controller with six external interrupts
  - Three programmable 16-bit timers—timer 1 can be used as a watchdog interrupt timer
  - Programmable memory and peripheral chip-select logic
  - Programmable wait state generator
  - Power-save clock divider
- **Software-compatible with the 80C186/80C188 and 80L186 /80L188 microcontrollers**
- **Widely available native development tools, applications, and system software**
- **Available in the following packages:**
  - 100-pin, thin quad flat pack (TQFP)
  - 100-pin, plastic quad flat pack (PQFP)

### GENERAL DESCRIPTION

The Am186™EM/EMLV and Am188™EM/EMLV microcontrollers are the ideal upgrade for 80C186/188 and 80L186/188 microcontroller designs requiring 80C186/188 and 80L186/188 microcontroller compatibility, increased performance, serial communications, and a direct bus interface. The Am186EM/EMLV and Am188EM/EMLV microcontrollers increase the performance of existing 80C186/188 and 80L186/188 systems while decreasing their cost.

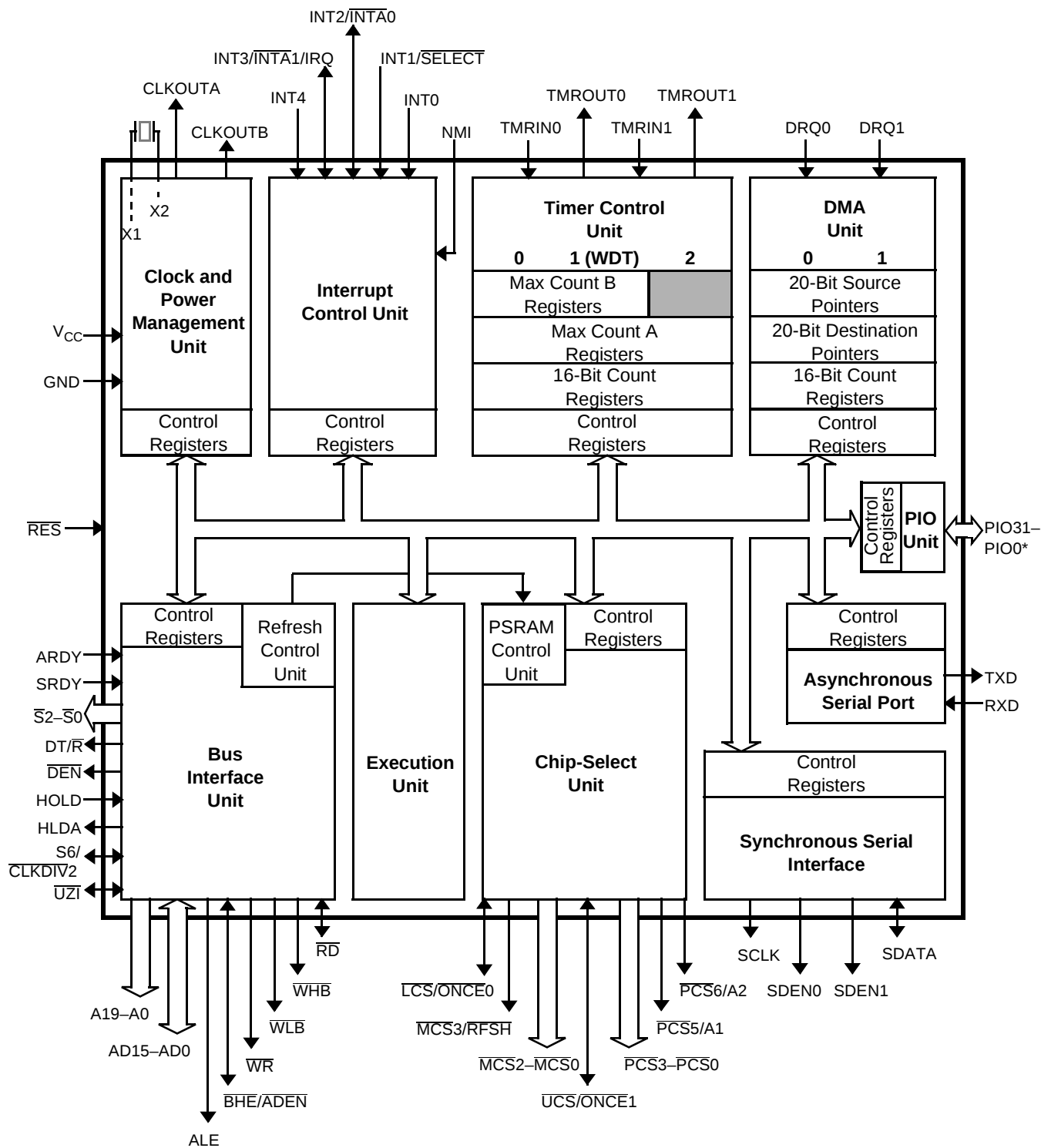
The Am186EM/EMLV and Am188EM/EMLV microcontrollers are part of the AMD E86 family of embedded microcontrollers and microprocessors based on the x86 architecture. The E86 family includes the 16- and 32-bit microcontrollers and microprocessors described on page 8

The Am186EM/EMLV and Am188EM/EMLV microcontrollers integrate the functions of the CPU, nonmultiplexed address bus, timers, chip selects, interrupt

controller, DMA controller, PSRAM controller, asynchronous serial port, synchronous serial interface, and programmable I/O (PIO) pins on one chip. Compared to the 80C186/188 and 80L186/188 microcontrollers, the Am186EM/EMLV and Am188EM/EMLV microcontrollers enable designers to reduce the size, power consumption, and cost of embedded systems, while increasing functionality and performance.

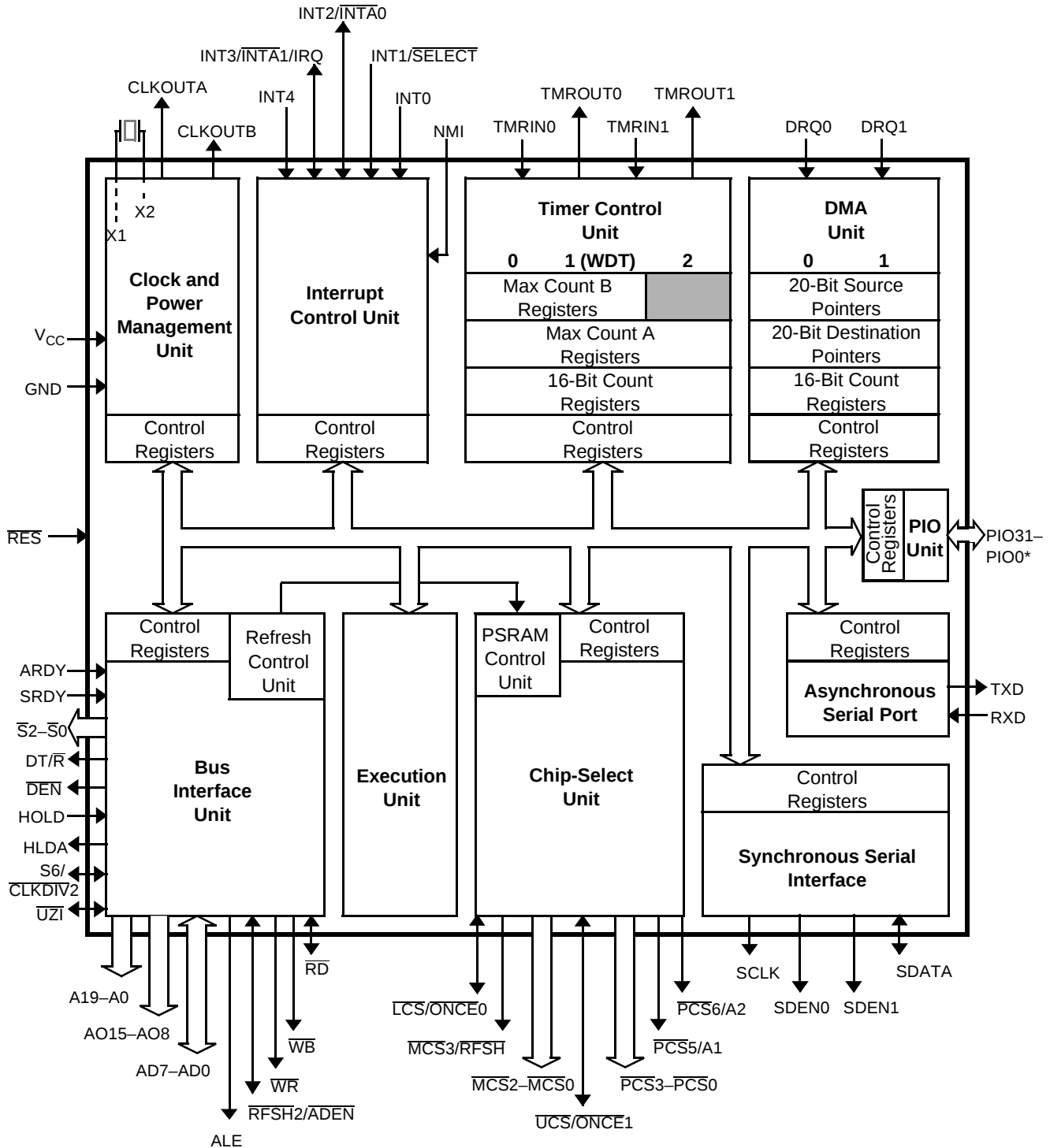
The Am186EM/EMLV and Am188EM/EMLV microcontrollers have been designed to meet the most common requirements of embedded products developed for the office automation, mass storage, communications, and general embedded markets. Specific applications include disk drives, hand-held terminals and desktop terminals, fax machines, printers, photocopiers, feature phones, cellular phones, PBXs, multiplexers, modems, and industrial controls.

## Am186EM MICROCONTROLLER BLOCK DIAGRAM

**Note:**

\* All PIO signals are shared with other physical pins. See the pin descriptions beginning on page 25 and Table 2 on page 30 for information on shared functions.

## Am188EM MICROCONTROLLER BLOCK DIAGRAM

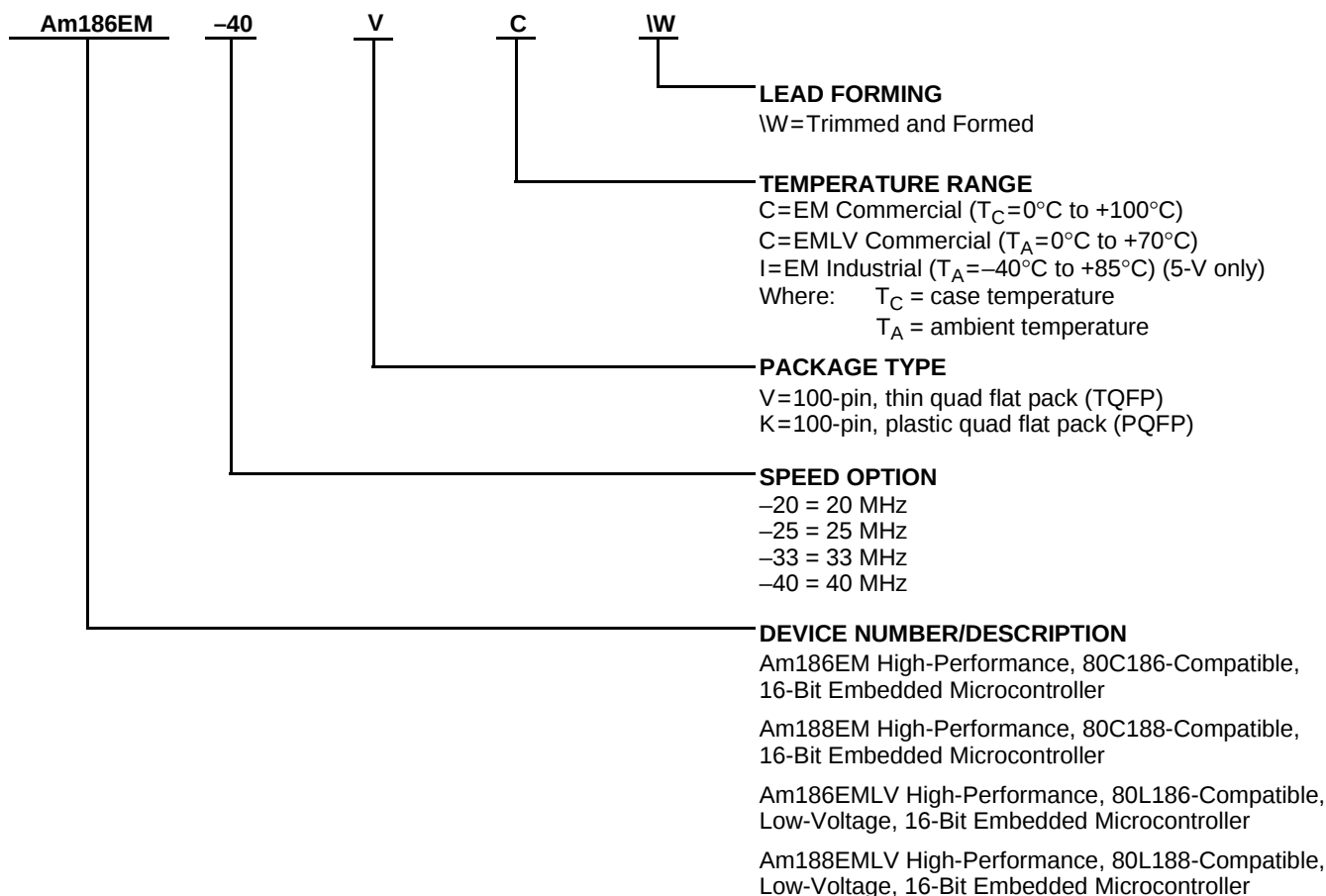
**Note:**

\* All PIO signals are shared with other physical pins. See the pin descriptions beginning on page 25 and Table 2 on page 30 for information on shared functions.

## ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order numbers (valid combinations) are formed by a combination of the elements below.



| Valid Combinations                                   |                 |
|------------------------------------------------------|-----------------|
| Am186EM-20<br>Am186EM-25<br>Am186EM-33<br>Am186EM-40 | VCIW or<br>KCIW |
| Am188EM-20<br>Am188EM-25<br>Am188EM-33<br>Am188EM-40 | VCIW or<br>KCIW |
| Am186EM-20<br>Am186EM-25                             | KIIW            |
| Am188EM-20<br>Am188EM-25                             | KIIW            |
| Am186EMLV-20<br>Am186EMLV-25                         | VCIW or<br>KCIW |
| Am188EMLV-20<br>Am188EMLV-25                         | VCIW or<br>KCIW |

## Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## Notes:

1. The Am186EM and Am188EM industrial microcontrollers, as well as the Am186EMLV and Am188EMLV commercial microcontrollers, are available in 20- and 25-MHz operating frequencies only.
2. The Am186EM and Am188EM industrial microcontrollers are not offered in a low-voltage operating range.
3. The Am186EM, Am188EM, Am186EMLV, and Am188EMLV microcontrollers are all functionally the same except for their DC characteristics and available frequencies.

**TABLE OF CONTENTS**

|                                                                                       |    |
|---------------------------------------------------------------------------------------|----|
| Distinctive Characteristics .....                                                     | 1  |
| General Description .....                                                             | 1  |
| Am186EM Microcontroller Block Diagram .....                                           | 2  |
| Am188EM Microcontroller Block Diagram .....                                           | 3  |
| Ordering Information .....                                                            | 4  |
| Related AMD Products .....                                                            | 8  |
| Key Features and Benefits .....                                                       | 10 |
| TQFP Connection Diagrams and Pinouts .....                                            | 11 |
| PQFP Connection Diagrams and Pinouts .....                                            | 17 |
| Logic Symbol—Am186EM Microcontroller .....                                            | 23 |
| Logic Symbol—Am188EM Microcontroller .....                                            | 24 |
| Pin Descriptions                                                                      |    |
| Pins that Are Used by Emulators .....                                                 | 25 |
| A19–A0 .....                                                                          | 25 |
| AD7–AD0 .....                                                                         | 25 |
| AD15–AD8 (Am186EM Microcontroller) .....                                              | 25 |
| AO15–AO8 (Am188EM Microcontroller) .....                                              | 25 |
| ALE .....                                                                             | 25 |
| ARDY .....                                                                            | 25 |
| $\overline{\text{BHE}}/\overline{\text{ADEN}}$ (Am186EM Microcontroller Only) .....   | 26 |
| CLKOUTA .....                                                                         | 26 |
| CLKOUTB .....                                                                         | 26 |
| $\overline{\text{DEN}}/\text{PIO5}$ .....                                             | 26 |
| DRQ1–DRQ0 .....                                                                       | 26 |
| DT/ $\overline{\text{R}}/\text{PIO4}$ .....                                           | 26 |
| GND .....                                                                             | 27 |
| HLDA .....                                                                            | 27 |
| HOLD .....                                                                            | 27 |
| INT0 .....                                                                            | 27 |
| INT1/ $\overline{\text{SELECT}}$ .....                                                | 27 |
| INT2/ $\overline{\text{INTA0}}/\text{PIO31}$ .....                                    | 27 |
| INT3/ $\overline{\text{INTA1}}/\text{IRQ}$ .....                                      | 27 |
| INT4/PIO30 .....                                                                      | 28 |
| $\overline{\text{LCS}}/\overline{\text{ONCE0}}$ .....                                 | 28 |
| $\overline{\text{MCS3}}/\overline{\text{RFSH}}/\text{PIO25}$ .....                    | 28 |
| $\overline{\text{MCS2}}\text{--}\overline{\text{MCS0}}$ .....                         | 28 |
| NMI .....                                                                             | 28 |
| $\overline{\text{PCS3}}\text{--}\overline{\text{PCS0}}$ .....                         | 29 |
| $\overline{\text{PCS5}}/\text{A1}/\text{PIO3}$ .....                                  | 29 |
| $\overline{\text{PCS6}}/\text{A2}/\text{PIO2}$ .....                                  | 29 |
| PIO31–PIO0 (Shared) .....                                                             | 29 |
| $\overline{\text{RD}}$ .....                                                          | 31 |
| $\overline{\text{RES}}$ .....                                                         | 31 |
| $\overline{\text{RFSH2}}/\overline{\text{ADEN}}$ (Am188EM Microcontroller Only) ..... | 31 |
| RXD/PIO28 .....                                                                       | 31 |
| $\overline{\text{S2}}\text{--}\overline{\text{S0}}$ .....                             | 31 |
| S6/ $\overline{\text{CLKDIV2}}/\text{PIO29}$ .....                                    | 31 |
| SCLK/PIO20 .....                                                                      | 32 |
| SDATA/PIO21 .....                                                                     | 32 |
| SDEN1/PIO23, SDEN0/PIO22 .....                                                        | 32 |
| SRDY/PIO6 .....                                                                       | 32 |
| TMRIN0/PIO11 .....                                                                    | 32 |

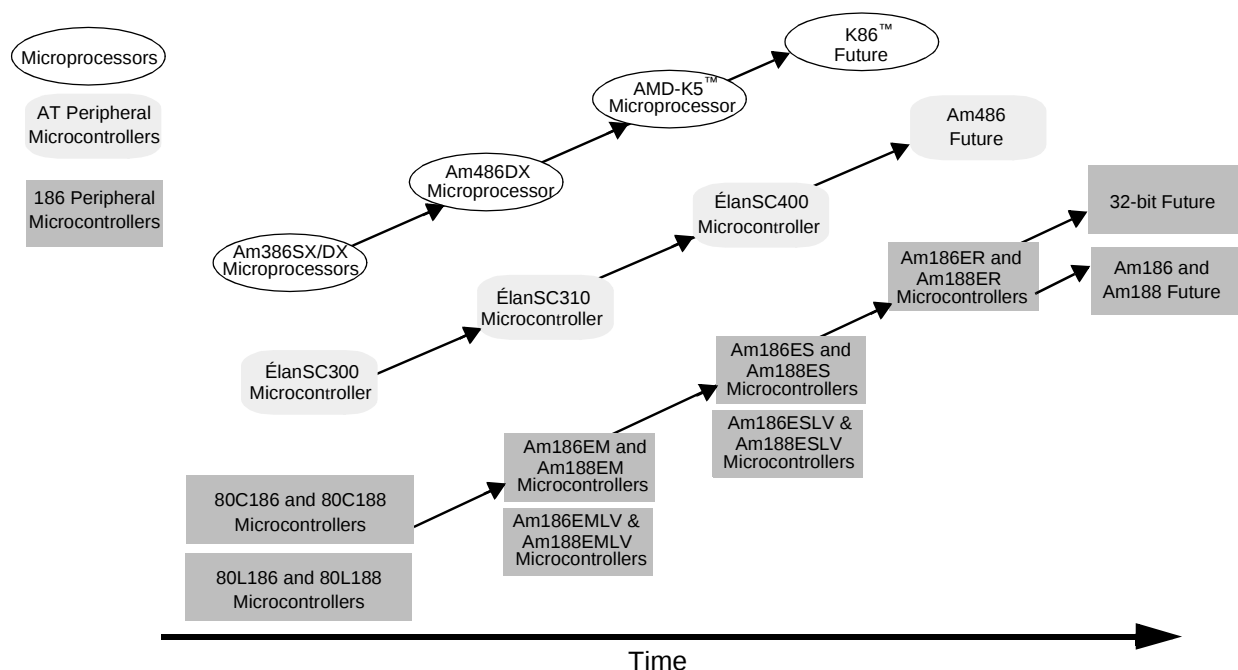
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|----------------------------------------------------------|----|
| TMRIN1/PIO0 .....                                        | 32 |
| TMROUT0/PIO10 .....                                      | 32 |
| TMROUT1/PIO1 .....                                       | 32 |
| TXD/PIO27 .....                                          | 32 |
| UCS/ONCE1 .....                                          | 32 |
| $\overline{UZI}$ /PIO26 .....                            | 33 |
| $V_{CC}$ .....                                           | 33 |
| $\overline{WHB}$ (Am186EM Microcontroller Only) .....    | 33 |
| $\overline{WLB}$ (Am186EM Microcontroller Only) .....    | 33 |
| $\overline{WB}$ (Am188EM Microcontroller Only) .....     | 33 |
| WR .....                                                 | 33 |
| X1 .....                                                 | 33 |
| X2 .....                                                 | 33 |
| Functional Description .....                             | 34 |
| Bus Operation .....                                      | 35 |
| Bus Interface Unit .....                                 | 37 |
| Peripheral Control Block (PCB) .....                     | 38 |
| Clock and Power Management .....                         | 41 |
| Chip-Select Unit .....                                   | 43 |
| Refresh Control Unit .....                               | 45 |
| Interrupt Control Unit .....                             | 45 |
| Timer Control Unit .....                                 | 46 |
| Direct Memory Access (DMA) .....                         | 46 |
| Asynchronous Serial Port .....                           | 48 |
| Synchronous Serial Interface .....                       | 48 |
| Programmable I/O (PIO) Pins .....                        | 50 |
| Absolute Maximum Ratings .....                           | 51 |
| Operating Ranges .....                                   | 51 |
| DC Characteristics Over Commercial Operating Range ..... | 51 |
| Commercial Switching Characteristics and Waveforms ..... | 60 |

**LIST OF FIGURES**

|            |                                                                                    |    |
|------------|------------------------------------------------------------------------------------|----|
| Figure 1.  | Example System Design .....                                                        | 10 |
| Figure 2.  | Two-Component Address .....                                                        | 34 |
| Figure 3.  | Am186EM Microcontroller Address Bus—Normal Read and Write Operation .....          | 35 |
| Figure 4.  | Am186EM Microcontroller—Read and Write with Address Bus<br>Disable In Effect ..... | 36 |
| Figure 5.  | Am188EM Microcontroller Address Bus—Normal Read and Write Operation .....          | 36 |
| Figure 6.  | Am188EM Microcontroller—Read and Write with Address Bus<br>Disable In Effect ..... | 37 |
| Figure 7.  | Peripheral Control Block Register Map .....                                        | 39 |
| Figure 8.  | Am186EM and Am188EM Microcontrollers Oscillator Configurations .....               | 41 |
| Figure 9.  | Clock Organization .....                                                           | 42 |
| Figure 10. | DMA Unit Block Diagram .....                                                       | 47 |
| Figure 11. | Synchronous Serial Interface Multiple Write .....                                  | 49 |
| Figure 12. | Synchronous Serial Interface Multiple Read .....                                   | 49 |
| Figure 13. | Typical $I_{CC}$ Versus Frequency for the Am186EMLV and Am188EMLV .....            | 53 |
| Figure 14. | Typical $I_{CC}$ Versus Frequency for the Am186EM and Am188EM .....                | 53 |
| Figure 15. | Thermal Resistance( $^{\circ}\text{C}/\text{Watt}$ ) .....                         | 54 |
| Figure 16. | Thermal Characteristics Equations .....                                            | 54 |
| Figure 17. | Typical Ambient Temperatures for PQFP with 2-Layer Board .....                     | 56 |
| Figure 18. | Typical Ambient Temperatures for TQFP with 2-Layer Board .....                     | 57 |
| Figure 19. | Typical Ambient Temperatures for PQFP with 4-Layer to 6-Layer Board .....          | 58 |
| Figure 20. | Typical Ambient Temperatures for TQFP with 4-Layer to 6-Layer Board .....          | 59 |

**LIST OF TABLES**

|           |                                                                                |    |
|-----------|--------------------------------------------------------------------------------|----|
| Table 1.  | Data Byte Encoding .....                                                       | 26 |
| Table 2.  | Numeric PIO Pin Assignments .....                                              | 30 |
| Table 3.  | Alphabetic PIO Pin Assignments .....                                           | 30 |
| Table 4.  | Bus Cycle Encoding .....                                                       | 31 |
| Table 5.  | Segment Register Selection Rules .....                                         | 34 |
| Table 6.  | Am186EM Microcontroller Maximum DMA Transfer Rates .....                       | 46 |
| Table 7.  | Typical Power Consumption Calculation for the<br>Am186EMLV and Am188EMLV ..... | 53 |
| Table 8.  | Thermal Characteristics ( $^{\circ}\text{C}/\text{Watt}$ ) .....               | 54 |
| Table 9.  | Typical Power Consumption Calculation .....                                    | 55 |
| Table 10. | Junction Temperature Calculation .....                                         | 55 |
| Table 11. | Typical Ambient Temperatures for PQFP with 2-Layer Board .....                 | 56 |
| Table 12. | Typical Ambient Temperatures for TQFP with 2-Layer Board .....                 | 57 |
| Table 13. | Typical Ambient Temperatures for PQFP with 4-Layer to 6-Layer Board .....      | 58 |
| Table 14. | Typical Ambient Temperatures for TQFP with 4-Layer to 6-Layer Board .....      | 59 |



The E6 Family of Embedded Microprocessors and Microcontrollers

## RELATED AMD PRODUCTS

### E86™ Family Devices

| Device      | Description                                                                                                                                 |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 80C186      | 16-bit microcontroller                                                                                                                      |
| 80C188      | 16-bit microcontroller with 8-bit external data bus                                                                                         |
| 80L186      | Low-voltage, 16-bit microcontroller                                                                                                         |
| 80L188      | Low-voltage, 16-bit microcontroller with 8-bit external data bus                                                                            |
| Am186EM     | High-performance, 80C186-compatible, 16-bit embedded microcontroller                                                                        |
| Am188EM     | High-performance, 80C188-compatible, 16-bit embedded microcontroller with 8-bit external data bus                                           |
| Am186EMLV   | High-performance, 80C186-compatible, low-voltage, 16-bit embedded microcontroller                                                           |
| Am188EMLV   | High-performance, 80C188-compatible, low-voltage, 16-bit embedded microcontroller with 8-bit external data bus                              |
| Am186ES     | High-performance, 80C186-compatible, 16-bit embedded microcontroller                                                                        |
| Am188ES     | High-performance, 80C188-compatible, 16-bit embedded microcontroller with 8-bit external data bus                                           |
| Am186ESLV   | High-performance, 80C186-compatible, low-voltage, 16-bit embedded microcontroller                                                           |
| Am188ESLV   | High-performance, 80C188-compatible, low-voltage, 16-bit embedded microcontroller with 8-bit external data bus                              |
| Am186ER     | High-performance, 80C186-compatible, low-voltage, 16-bit embedded microcontroller with 32 Kbyte of internal RAM                             |
| Am188ER     | High-performance, 80C188-compatible, low-voltage, 16-bit embedded microcontroller with 8-bit external data bus and 32 Kbyte of internal RAM |
| Élan™ SC300 | High-performance, highly integrated, low-voltage, 32-bit embedded microcontroller                                                           |
| ÉlanSC310   | High-performance, single-chip, 32-bit embedded PC/AT microcontroller                                                                        |
| ÉlanSC400   | Single-chip, low-power, PC/AT-compatible microcontroller                                                                                    |
| Am386®DX    | High-performance, 32-bit embedded microprocessor with 32-bit external data bus                                                              |
| Am386SX     | High-performance, 32-bit embedded microprocessor with 16-bit external data bus                                                              |
| Am486®DX    | High-performance, 32-bit embedded microprocessor with 32-bit external data bus                                                              |

## Related Documents

The following documents provide additional information regarding the Am186EM and Am188EM microcontrollers.

- The Am186EM and Am188EM Microcontrollers User's Manual, order# 19713
- The Am186 and Am188 Family Instruction Set Manual, order# 21267
- The FusionE86<sup>SM</sup> Catalog, order# 19255

## Third-Party Development Support Products

The FusionE86 Program of Partnerships for Application Solutions provides the customer with an array of products designed to meet critical time-to-market needs. Products and solutions available from the AMD FusionE86 partners include emulators, hardware and software debuggers, board-level products, and software development tools, among others.

In addition, mature development tools and applications for the x86 platform are widely available in the general marketplace.

## Customer Service

The AMD customer service network includes U.S. offices, international offices, and a customer training center. Expert technical assistance is available from the AMD worldwide staff of field application engineers and factory support staff who can answer E86 family hardware and software development questions.

## Hotline and World Wide Web Support

For answers to technical questions, AMD provides a toll-free number for direct access to our corporate applications hotline. Also available is the AMD World Wide Web home page and FTP site, which provides the latest E86 family product information, including technical information and data on upcoming product releases.

## Corporate Applications Hotline

800-222-9323

Toll-free for U.S. and Canada

44-(0) 1276-803-299

U.K. and Europe hotline

## World Wide Web Home Page and FTP Site

To access the AMD home page go to <http://www.amd.com>.

To download documents and software, ftp to <ftp://ftp.amd.com> and log on as anonymous using your E-mail address as a password. Or via your web browser, go to <ftp://ftp.amd.com>.

Questions, requests, and input concerning AMD's WWW pages can be sent via E-mail to [webmaster@amd.com](mailto:webmaster@amd.com).

## Documentation and Literature

Free E86 family information such as data books, user's manuals, data sheets, application notes, the FusionE86 Partner Solutions Catalog, and other literature is available with a simple phone call. Internationally, contact your local AMD sales office for complete E86 family literature.

## Literature Ordering

800-222-9323

Toll-free for U.S. and Canada

512-602-5651

Direct dial worldwide

800-222-9323

AMD Facts-On-Demand<sup>TM</sup> fax information service, toll-free for U.S. and Canada

## KEY FEATURES AND BENEFITS

The Am186EM and Am188EM microcontrollers extend the AMD family of microcontrollers based on the industry-standard x86 architecture. The Am186EM and Am188EM microcontrollers are higher-performance, more integrated versions of the 80C186/188 microprocessors, offering a migration path that was previously unavailable. Upgrading to the Am186EM and Am188EM microcontrollers is an attractive solution for several reasons:

- **Minimized total system cost**—New peripherals and on-chip system interface logic on the Am186EM and Am188EM microcontrollers reduce the cost of existing 80C186/188 designs.
- **X86 software compatibility**—80C186/188-compatible and upward-compatible with the other members of the AMD E86 family.
- **Enhanced performance**—The Am186EM and Am188EM microcontrollers increase the performance of 80C186/188 systems, and the demultiplexed address bus offers faster, unbuffered access to memory.
- **Enhanced functionality**—The new and enhanced on-chip peripherals of the Am186EM and Am188EM microcontrollers include an asynchronous serial port, 32 PIOs, a watchdog timer, an additional interrupt pin, a synchronous serial interface, a PSRAM controller, a 16-bit reset configuration register, and enhanced chip-select functionality.

## Application Considerations

The integration enhancements of the Am186EM and Am188EM microcontrollers provide a high-performance, low-system-cost solution for 16-bit embedded microcontroller designs. The nonmultiplexed address bus eliminates the need for system-support logic to interface memory devices, while the multiplexed address/data bus maintains the value of previously engineered, customer-specific peripherals and circuits within the upgraded design.

Figure 1 illustrates an example system design that uses the integrated peripheral set to achieve high performance with reduced system cost.

### Clock Generation

The integrated clock generation circuitry of the Am186EM and Am188EM microcontrollers allows the use of a times-one crystal frequency. The design in Figure 1 achieves 40-MHz CPU operation while using a 40-MHz crystal.

### Memory Interface

The integrated memory controller logic of the Am186EM and Am188EM microcontrollers provides a direct address bus interface to memory devices. The use of an external address latch controlled by the address latch enable (ALE) signal is no longer needed.

Individual byte-write-enable signals are provided to eliminate the need for external high/low byte-write-enable circuitry. The maximum bank size that is programmable for the memory chip-select signals has been increased to facilitate the use of high-density memory devices.

The improved memory timing specifications for the Am186EM and Am188EM microcontrollers allow no wait-state operation with 70-ns memory access times at a 40-MHz CPU clock speed. This reduces overall system cost significantly by allowing the use of a more commonly available memory speed and technology.

### Direct Memory Interface Example

Figure 1 illustrates the Am186EM microcontroller direct memory interface. The processor A19–A0 bus connects to the memory address inputs, the AD bus connects to the data inputs and outputs, and the chip selects connect to the memory chip-select inputs.

The  $\overline{RD}$  output connects to the SRAM Output Enable ( $\overline{OE}$ ) pin for read operations. Write operations use the byte write enables connected to the SRAM Write Enable ( $\overline{WE}$ ) pins.

The example design uses 2-Mbit memory technology (256 Kbytes) to fully populate the available address space. Two flash PROM devices provide 512 Kbytes of nonvolatile program storage and two static RAM devices provide 512 Kbytes of data storage area.

Figure 1 also shows an implementation of an RS-232 console or modem communications port. The RS-232-to-CMOS voltage-level converter is required for the electrical interface with the external device.

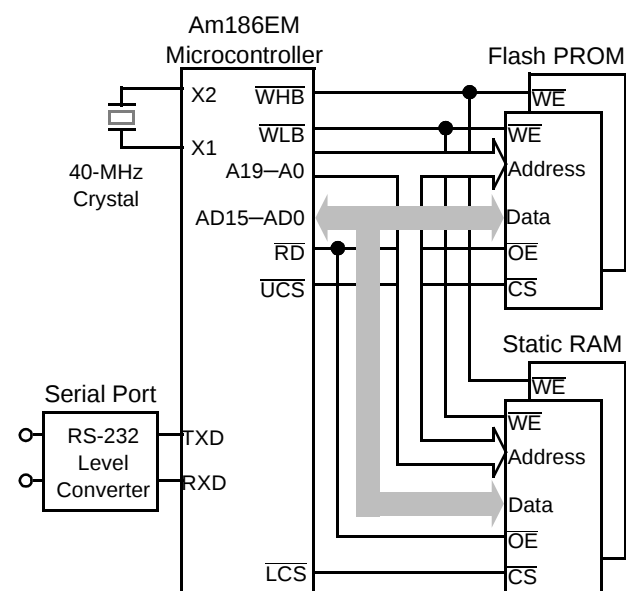
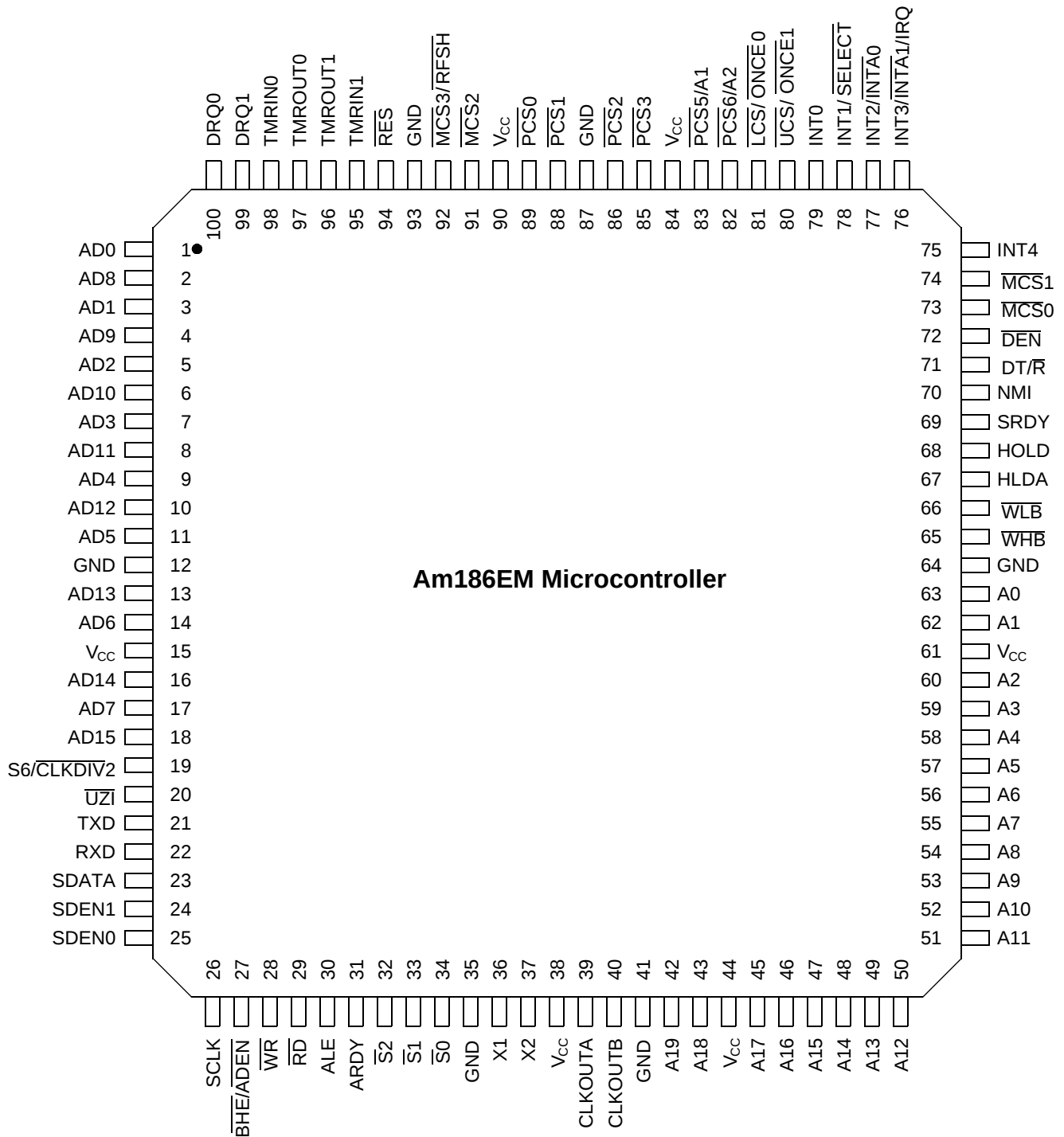


Figure 1. Example System Design

## TQFP CONNECTION DIAGRAMS AND PINOUTS

## Am186EM Microcontroller

## Top Side View—100-Pin Thin Quad Flat Pack (TQFP)

**Note:**

Pin 1 is marked for orientation.

# **TQFP PIN ASSIGNMENTS—Am186EM Microcontroller** **(Sorted by Pin Number)**

| Pin No. | Name             | Pin No. | Name            | Pin No. | Name            | Pin No. | Name            |
|---------|------------------|---------|-----------------|---------|-----------------|---------|-----------------|
| 1       | AD0              | 26      | SCLK/PIO20      | 51      | A11             | 76      | INT3/INTA1/IRQ  |
| 2       | AD8              | 27      | BHE/ADEN        | 52      | A10             | 77      | INT2/INTA0      |
| 3       | AD1              | 28      | WR              | 53      | A9              | 78      | INT1/SELECT     |
| 4       | AD9              | 29      | RD              | 54      | A8              | 79      | INT0            |
| 5       | AD2              | 30      | ALE             | 55      | A7              | 80      | UCS/ONCE1       |
| 6       | AD10             | 31      | ARDY            | 56      | A6              | 81      | LCS/ONCE0       |
| 7       | AD3              | 32      | S2              | 57      | A5              | 82      | PCS6/A2/PIO2    |
| 8       | AD11             | 33      | S1              | 58      | A4              | 83      | PCS5/A1/PIO3    |
| 9       | AD4              | 34      | S0              | 59      | A3              | 84      | V <sub>CC</sub> |
| 10      | AD12             | 35      | GND             | 60      | A2              | 85      | PCS3/PIO19      |
| 11      | AD5              | 36      | X1              | 61      | V <sub>CC</sub> | 86      | PCS2/PIO18      |
| 12      | GND              | 37      | X2              | 62      | A1              | 87      | GND             |
| 13      | AD13             | 38      | V <sub>CC</sub> | 63      | A0              | 88      | PCS1/PIO17      |
| 14      | AD6              | 39      | CLKOUTA         | 64      | GND             | 89      | PCS0/PIO16      |
| 15      | V <sub>CC</sub>  | 40      | CLKOUTB         | 65      | WHB             | 90      | V <sub>CC</sub> |
| 16      | AD14             | 41      | GND             | 66      | WLB             | 91      | MCS2            |
| 17      | AD7              | 42      | A19/PIO9        | 67      | HLDA            | 92      | MCS3/RFSH       |
| 18      | AD15             | 43      | A18/PIO8        | 68      | HOLD            | 93      | GND             |
| 19      | S6/CLKDIV2/PIO29 | 44      | V <sub>CC</sub> | 69      | SRDY/PIO6       | 94      | RES             |
| 20      | UZI/PIO26        | 45      | A17/PIO7        | 70      | NMI             | 95      | TMRIN1/PIO0     |
| 21      | TXD              | 46      | A16             | 71      | DT/R/PIO4       | 96      | TMROUT1/PIO1    |
| 22      | RXD              | 47      | A15             | 72      | DEN/PIO5        | 97      | TMROUT0/PIO10   |
| 23      | SDATA/PIO21      | 48      | A14             | 73      | MCS0/PIO14      | 98      | TMRIN0/PIO11    |
| 24      | SDEN1/PIO23      | 49      | A13             | 74      | MCS1/PIO15      | 99      | DRQ1/PIO13      |
| 25      | SDEN0/PIO22      | 50      | A12             | 75      | INT4            | 100     | DRQ0/PIO12      |

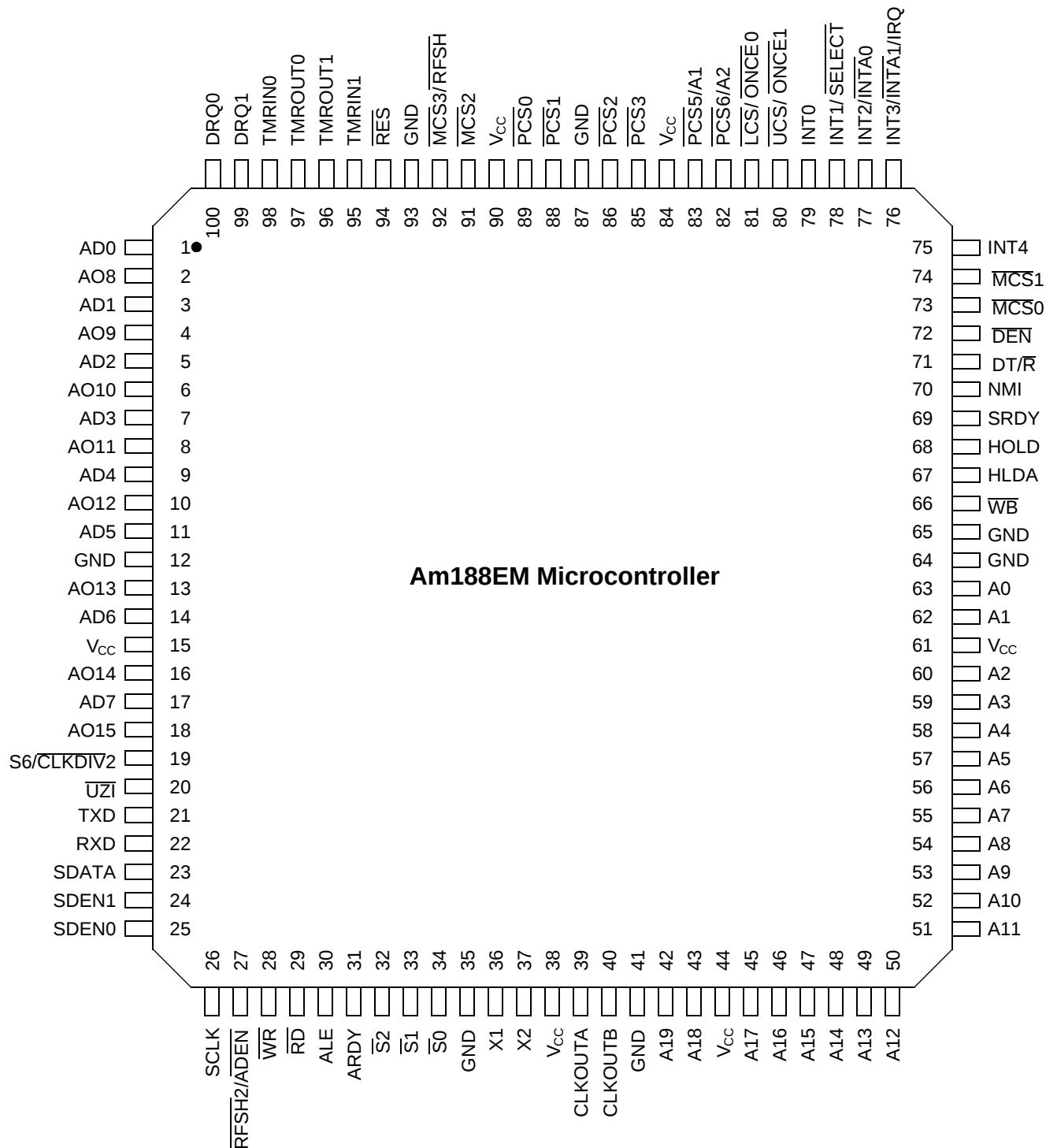
# TQFP PIN ASSIGNMENTS—Am186EM Microcontroller (Sorted by Pin Name)

| Pin Name | No. | Pin Name                         | No. | Pin Name                              | No. | Pin Name                          | No. |
|----------|-----|----------------------------------|-----|---------------------------------------|-----|-----------------------------------|-----|
| A0       | 63  | AD5                              | 11  | GND                                   | 93  | $\overline{S}2$                   | 32  |
| A1       | 62  | AD6                              | 14  | HLDA                                  | 67  | S6/ $\overline{CLKDIV}2$ /PIO29   | 19  |
| A2       | 60  | AD7                              | 17  | HOLD                                  | 68  | SCLK/PIO20                        | 26  |
| A3       | 59  | AD8                              | 2   | INT0                                  | 79  | SDATA/PIO21                       | 23  |
| A4       | 58  | AD9                              | 4   | INT1/ $\overline{SELECT}$             | 78  | SDEN0/PIO22                       | 25  |
| A5       | 57  | AD10                             | 6   | INT2/ $\overline{INTA}0$              | 77  | SDEN1/PIO23                       | 24  |
| A6       | 56  | AD11                             | 8   | INT3/ $\overline{INTA}1$ /IRQ         | 76  | SRDY/PIO6                         | 69  |
| A7       | 55  | AD12                             | 10  | INT4                                  | 75  | TMRIN0/PIO11                      | 98  |
| A8       | 54  | AD13                             | 13  | $\overline{LCS}/\overline{ONCE}0$     | 81  | TMRIN1/PIO0                       | 95  |
| A9       | 53  | AD14                             | 16  | $\overline{MCS}0$ /PIO14              | 73  | TMROUT0/PIO10                     | 97  |
| A10      | 52  | AD15                             | 18  | $\overline{MCS}1$ /PIO15              | 74  | TMROUT1/PIO1                      | 96  |
| A11      | 51  | ALE                              | 30  | $\overline{MCS}2$                     | 91  | TXD                               | 21  |
| A12      | 50  | ARDY                             | 31  | $\overline{MCS}3$ / $\overline{RFSH}$ | 92  | $\overline{UCS}/\overline{ONCE}1$ | 80  |
| A13      | 49  | $\overline{BHE}/\overline{ADEN}$ | 27  | NMI                                   | 70  | $\overline{UZI}/\overline{PIO}26$ | 20  |
| A14      | 48  | CLKOUTA                          | 39  | $\overline{PCS}0$ /PIO16              | 89  | V <sub>CC</sub>                   | 15  |
| A15      | 47  | CLKOUTB                          | 40  | $\overline{PCS}1$ /PIO17              | 88  | V <sub>CC</sub>                   | 38  |
| A16      | 46  | $\overline{DEN}$ /PIO5           | 72  | $\overline{PCS}2$ /PIO18              | 86  | V <sub>CC</sub>                   | 44  |
| A17/PIO7 | 45  | DRQ0/PIO12                       | 100 | $\overline{PCS}3$ /PIO19              | 85  | V <sub>CC</sub>                   | 61  |
| A18/PIO8 | 43  | DRQ1/PIO13                       | 99  | $\overline{PCS}5$ /A1/PIO3            | 83  | V <sub>CC</sub>                   | 84  |
| A19/PIO9 | 42  | DT/ $\overline{R}$ /PIO4         | 71  | $\overline{PCS}6$ /A2/PIO2            | 82  | V <sub>CC</sub>                   | 90  |
| AD0      | 1   | GND                              | 12  | $\overline{RD}$                       | 29  | $\overline{WHB}$                  | 65  |
| AD1      | 3   | GND                              | 35  | $\overline{RES}$                      | 94  | $\overline{WLB}$                  | 66  |
| AD2      | 5   | GND                              | 41  | RXD                                   | 22  | $\overline{WR}$                   | 28  |
| AD3      | 7   | GND                              | 64  | $\overline{S}0$                       | 34  | X1                                | 36  |
| AD4      | 9   | GND                              | 87  | $\overline{S}1$                       | 33  | X2                                | 37  |

## CONNECTION DIAGRAM

## Am188EM Microcontroller

## Top Side View—100-Pin Thin Quad Flat Pack (TQFP)

**Note:**

Pin 1 is marked for orientation.

# **TQFP PIN ASSIGNMENTS—Am188EM Microcontroller** **(Sorted by Pin Number)**

| Pin No. | Name             | Pin No. | Name            | Pin No. | Name            | Pin No. | Name             |
|---------|------------------|---------|-----------------|---------|-----------------|---------|------------------|
| 1       | AD0              | 26      | SCLK/PIO20      | 51      | A11             | 76      | INT3/INTA1/IRQ   |
| 2       | AO8              | 27      | RFSH2/ADEN      | 52      | A10             | 77      | INT2/INTA0/PIO31 |
| 3       | AD1              | 28      | WR              | 53      | A9              | 78      | INT1/SELECT      |
| 4       | AO9              | 29      | RD              | 54      | A8              | 79      | INT0             |
| 5       | AD2              | 30      | ALE             | 55      | A7              | 80      | UCS/ONCE1        |
| 6       | AO10             | 31      | ARDY            | 56      | A6              | 81      | LCS/ONCE0        |
| 7       | AD3              | 32      | S2              | 57      | A5              | 82      | PCS6/A2/PIO2     |
| 8       | AO11             | 33      | S1              | 58      | A4              | 83      | PCS5/A1/PIO3     |
| 9       | AD4              | 34      | S0              | 59      | A3              | 84      | V <sub>CC</sub>  |
| 10      | AO12             | 35      | GND             | 60      | A2              | 85      | PCS3/PIO19       |
| 11      | AD5              | 36      | X1              | 61      | V <sub>CC</sub> | 86      | PCS2/PIO18       |
| 12      | GND              | 37      | X2              | 62      | A1              | 87      | GND              |
| 13      | AO13             | 38      | V <sub>CC</sub> | 63      | A0              | 88      | PCS1/PIO17       |
| 14      | AD6              | 39      | CLKOUTA         | 64      | GND             | 89      | PCS0/PIO16       |
| 15      | V <sub>CC</sub>  | 40      | CLKOUTB         | 65      | GND             | 90      | V <sub>CC</sub>  |
| 16      | AO14             | 41      | GND             | 66      | WB              | 91      | MCS2/PIO24       |
| 17      | AD7              | 42      | A19/PIO9        | 67      | HLDA            | 92      | MCS3/RFSH/PIO25  |
| 18      | AO15             | 43      | A18/PIO8        | 68      | HOLD            | 93      | GND              |
| 19      | S6/CLKDIV2/PIO29 | 44      | V <sub>CC</sub> | 69      | SRDY/PIO6       | 94      | RES              |
| 20      | UZI/PIO26        | 45      | A17/PIO7        | 70      | NMI             | 95      | TMRIN1/PIO0      |
| 21      | TXD/PIO27        | 46      | A16             | 71      | DT/R/PIO4       | 96      | TMROUT1/PIO1     |
| 22      | RXD/PIO28        | 47      | A15             | 72      | DEN/PIO5        | 97      | TMROUT0/PIO10    |
| 23      | SDATA/PIO21      | 48      | A14             | 73      | MCS0/PIO14      | 98      | TMRIN0/PIO11     |
| 24      | SDEN1/PIO23      | 49      | A13             | 74      | MCS1/PIO15      | 99      | DRQ1/PIO13       |
| 25      | SDEN0/PIO22      | 50      | A12             | 75      | INT4/PIO30      | 100     | DRQ0/PIO12       |

# TQFP PIN ASSIGNMENTS—Am188EM Microcontroller

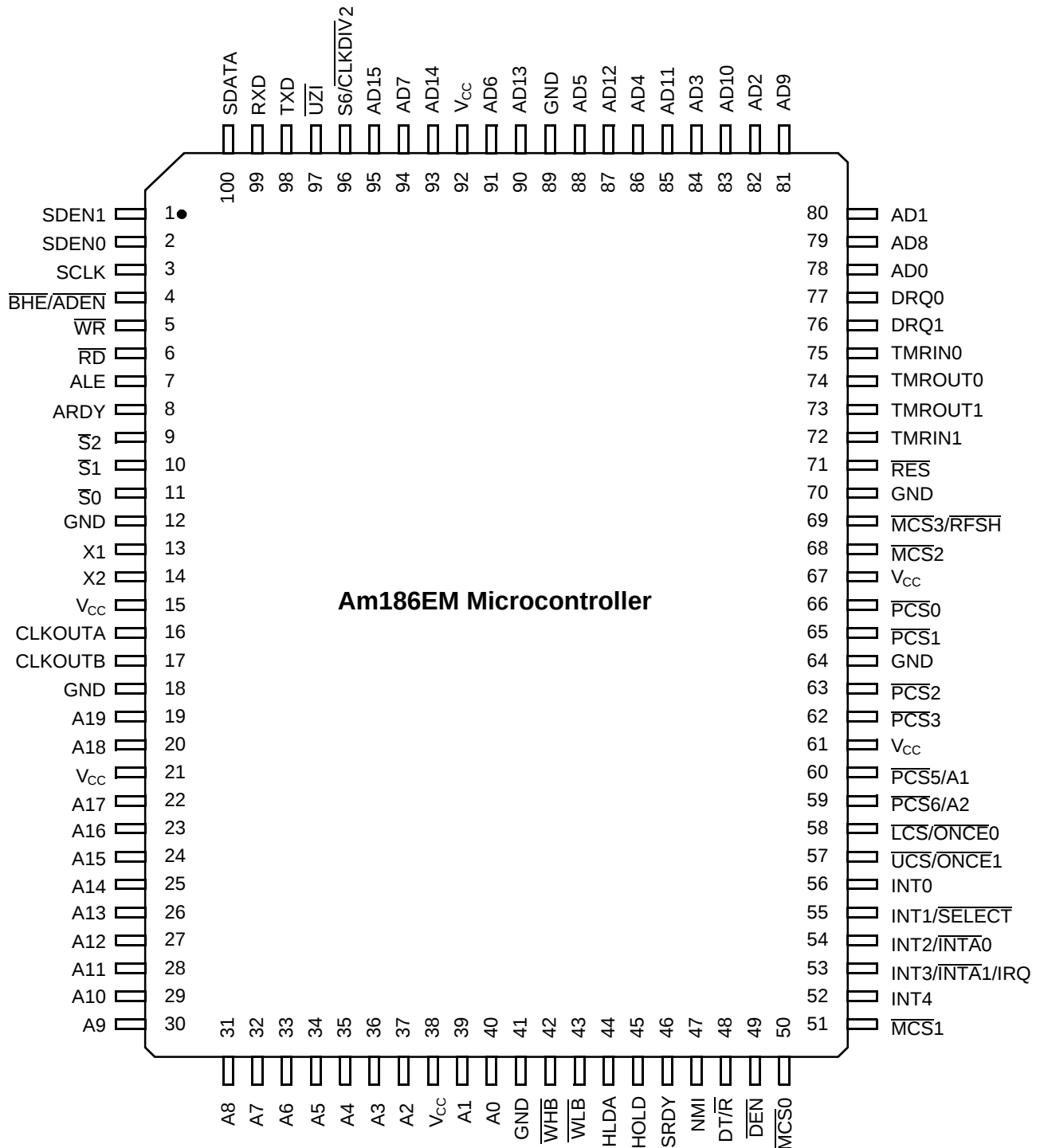
(Sorted by Pin Name)

| Pin Name | No. | Pin Name                 | No. | Pin Name                                     | No. | Pin Name                          | No. |
|----------|-----|--------------------------|-----|----------------------------------------------|-----|-----------------------------------|-----|
| A0       | 63  | AD5                      | 11  | GND                                          | 93  | $\overline{S}1$                   | 33  |
| A1       | 62  | AD6                      | 14  | HLDA                                         | 67  | $\overline{S}2$                   | 32  |
| A2       | 60  | AD7                      | 17  | HOLD                                         | 68  | S6/ $\overline{CLKDIV}2$ /PIO29   | 19  |
| A3       | 59  | ALE                      | 30  | INT0                                         | 79  | SCLK/PIO20                        | 26  |
| A4       | 58  | AO8                      | 2   | INT1/ $\overline{SELECT}$                    | 78  | SDATA/PIO21                       | 23  |
| A5       | 57  | AO9                      | 4   | INT2/ $\overline{INTA}0$ /PIO31              | 77  | SDEN0/PIO22                       | 25  |
| A6       | 56  | AO10                     | 6   | INT3/ $\overline{INTA}1$ /IRQ                | 76  | SDEN1/PIO23                       | 24  |
| A7       | 55  | AO11                     | 8   | INT4/PIO30                                   | 75  | SRDY/PIO6                         | 69  |
| A8       | 54  | AO12                     | 10  | $\overline{LCS}/\overline{ONCE}0$            | 81  | TMRIN0/PIO11                      | 98  |
| A9       | 53  | AO13                     | 13  | $\overline{MCS}0$ /PIO14                     | 73  | TMRIN1/PIO0                       | 95  |
| A10      | 52  | AO14                     | 16  | $\overline{MCS}1$ /PIO15                     | 74  | TMROUT0/PIO10                     | 97  |
| A11      | 51  | AO15                     | 18  | $\overline{MCS}2$ /PIO24                     | 91  | TMROUT1/PIO1                      | 96  |
| A12      | 50  | ARDY                     | 31  | $\overline{MCS}3$ / $\overline{RFSH}$ /PIO25 | 92  | TXD/PIO27                         | 21  |
| A13      | 49  | CLKOUTA                  | 39  | NMI                                          | 70  | $\overline{UCS}/\overline{ONCE}1$ | 80  |
| A14      | 48  | CLKOUTB                  | 40  | $\overline{PCS}0$ /PIO16                     | 89  | $\overline{UZI}$ /PIO26           | 20  |
| A15      | 47  | $\overline{DEN}$ /PIO5   | 72  | $\overline{PCS}1$ /PIO17                     | 88  | V <sub>CC</sub>                   | 15  |
| A16      | 46  | DRQ0/PIO12               | 100 | $\overline{PCS}2$ /PIO18                     | 86  | V <sub>CC</sub>                   | 38  |
| A17/PIO7 | 45  | DRQ1/PIO13               | 99  | $\overline{PCS}3$ /PIO19                     | 85  | V <sub>CC</sub>                   | 44  |
| A18/PIO8 | 43  | DT/ $\overline{R}$ /PIO4 | 71  | $\overline{PCS}5$ /A1/PIO3                   | 83  | V <sub>CC</sub>                   | 61  |
| A19/PIO9 | 42  | GND                      | 12  | $\overline{PCS}6$ /A2/PIO2                   | 82  | V <sub>CC</sub>                   | 84  |
| AD0      | 1   | GND                      | 35  | $\overline{RD}$                              | 29  | V <sub>CC</sub>                   | 90  |
| AD1      | 3   | GND                      | 41  | $\overline{RES}$                             | 94  | $\overline{WB}$                   | 66  |
| AD2      | 5   | GND                      | 64  | $\overline{RFSH}2$ / $\overline{ADEN}$       | 27  | $\overline{WR}$                   | 28  |
| AD3      | 7   | GND                      | 65  | RXD/PIO28                                    | 22  | X1                                | 36  |
| AD4      | 9   | GND                      | 87  | $\overline{S}0$                              | 34  | X2                                | 37  |

## PQFP CONNECTION DIAGRAMS AND PINOUTS

## Am186EM Microcontroller

## Top Side View—100-Pin Plastic Quad Flat Pack (PQFP)

**Note:**

Pin 1 is marked for orientation.

# **PQFP PIN ASSIGNMENTS—Am186EM Microcontroller** **(Sorted by Pin Number)**

| Pin No. | Name                                | Pin No. | Name                                  | Pin No. | Name                                              | Pin No. | Name                                         |
|---------|-------------------------------------|---------|---------------------------------------|---------|---------------------------------------------------|---------|----------------------------------------------|
| 1       | SDEN1/PIO23                         | 26      | A13                                   | 51      | $\overline{\text{MCS}}1/\text{PIO15}$             | 76      | DRQ1/PIO13                                   |
| 2       | SDEN0/PIO22                         | 27      | A12                                   | 52      | INT4/PIO30                                        | 77      | DRQ0/PIO12                                   |
| 3       | SCLK/PIO20                          | 28      | A11                                   | 53      | INT3/ $\overline{\text{INTA}}1/\text{IRQ}$        | 78      | AD0                                          |
| 4       | $\overline{\text{BHE}}/\text{ADEN}$ | 29      | A10                                   | 54      | INT2/ $\overline{\text{INTA}}0/\text{PIO31}$      | 79      | AD8                                          |
| 5       | $\overline{\text{WR}}$              | 30      | A9                                    | 55      | INT1/ $\overline{\text{SELECT}}$                  | 80      | AD1                                          |
| 6       | $\overline{\text{RD}}$              | 31      | A8                                    | 56      | INT0                                              | 81      | AD9                                          |
| 7       | ALE                                 | 32      | A7                                    | 57      | $\overline{\text{UCS}}/\text{ONCE}1$              | 82      | AD2                                          |
| 8       | ARDY                                | 33      | A6                                    | 58      | $\overline{\text{LCS}}/\text{ONCE}0$              | 83      | AD10                                         |
| 9       | $\overline{\text{S}}2$              | 34      | A5                                    | 59      | $\overline{\text{PCS}}6/\text{A2}/\text{PIO2}$    | 84      | AD3                                          |
| 10      | $\overline{\text{S}}1$              | 35      | A4                                    | 60      | $\overline{\text{PCS}}5/\text{A1}/\text{PIO3}$    | 85      | AD11                                         |
| 11      | $\overline{\text{S}}0$              | 36      | A3                                    | 61      | V <sub>CC</sub>                                   | 86      | AD4                                          |
| 12      | GND                                 | 37      | A2                                    | 62      | $\overline{\text{PCS}}3/\text{PIO19}$             | 87      | AD12                                         |
| 13      | X1                                  | 38      | V <sub>CC</sub>                       | 63      | $\overline{\text{PCS}}2/\text{PIO18}$             | 88      | AD5                                          |
| 14      | X2                                  | 39      | A1                                    | 64      | GND                                               | 89      | GND                                          |
| 15      | V <sub>CC</sub>                     | 40      | A0                                    | 65      | $\overline{\text{PCS}}1/\text{PIO17}$             | 90      | AD13                                         |
| 16      | CLKOUTA                             | 41      | GND                                   | 66      | $\overline{\text{PCS}}0/\text{PIO16}$             | 91      | AD6                                          |
| 17      | CLKOUTB                             | 42      | $\overline{\text{WHB}}$               | 67      | V <sub>CC</sub>                                   | 92      | V <sub>CC</sub>                              |
| 18      | GND                                 | 43      | $\overline{\text{WLB}}$               | 68      | $\overline{\text{MCS}}2/\text{PIO24}$             | 93      | AD14                                         |
| 19      | A19/PIO9                            | 44      | HLDA                                  | 69      | $\overline{\text{MCS}}3/\text{RFSH}/\text{PIO25}$ | 94      | AD7                                          |
| 20      | A18/PIO8                            | 45      | HOLD                                  | 70      | GND                                               | 95      | AD15                                         |
| 21      | V <sub>CC</sub>                     | 46      | SRDY/PIO6                             | 71      | $\overline{\text{RES}}$                           | 96      | S6/ $\overline{\text{CLKDIV}}2/\text{PIO29}$ |
| 22      | A17/PIO7                            | 47      | NMI                                   | 72      | TMRIN1/PIO0                                       | 97      | $\overline{\text{UZI}}/\text{PIO26}$         |
| 23      | A16                                 | 48      | DT/ $\overline{\text{R}}/\text{PIO4}$ | 73      | TMROUT1/PIO1                                      | 98      | TXD/PIO27                                    |
| 24      | A15                                 | 49      | $\overline{\text{DEN}}/\text{PIO5}$   | 74      | TMROUT0/PIO10                                     | 99      | RXD/PIO28                                    |
| 25      | A14                                 | 50      | $\overline{\text{MCS}}0/\text{PIO14}$ | 75      | TMRIN0/PIO11                                      | 100     | SDATA/PIO21                                  |

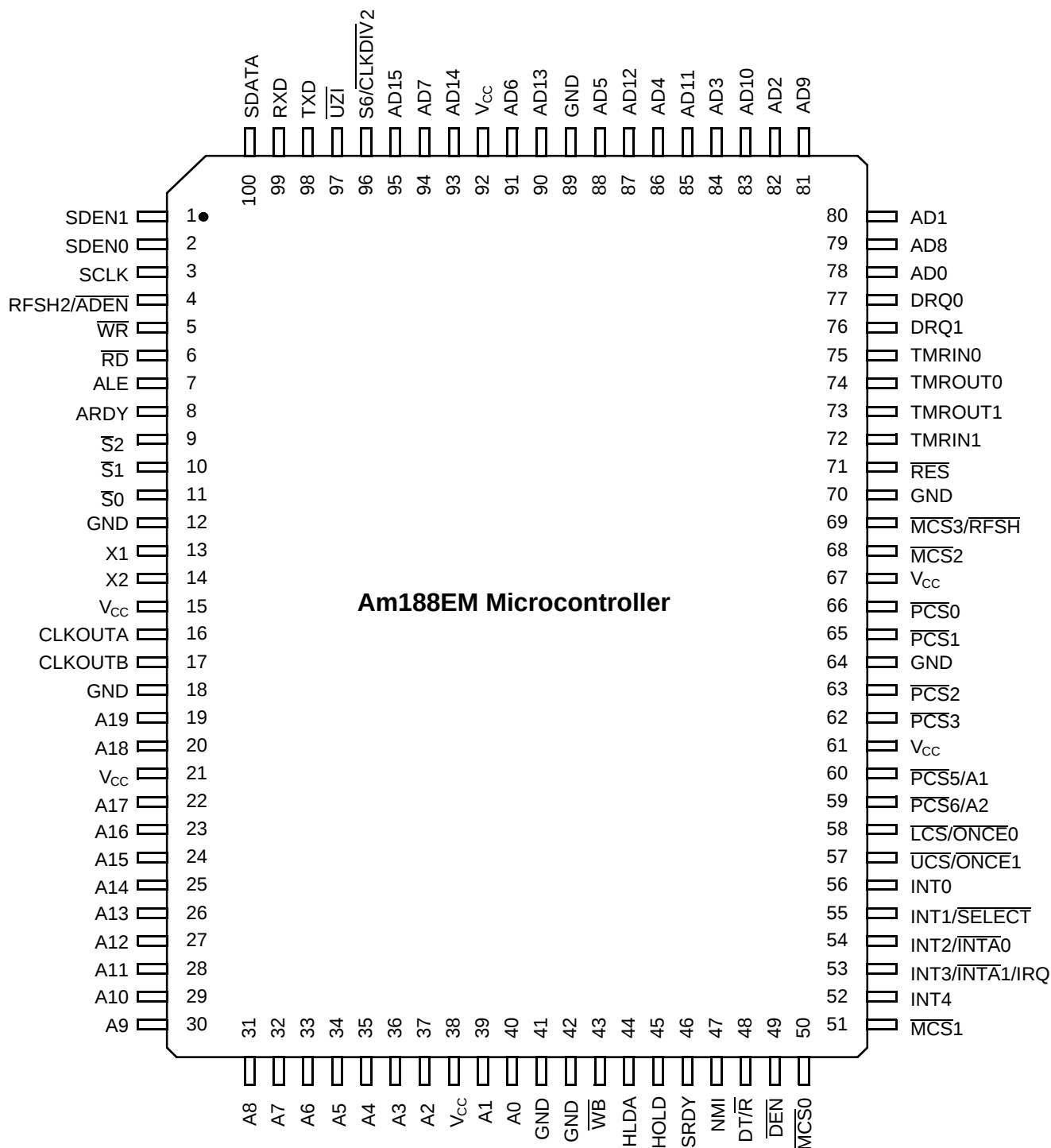
**PQFP PIN ASSIGNMENTS—Am186EM Microcontroller**  
**(Sorted by Pin Name)**

| Pin Name | No. | Pin Name                            | No. | Pin Name                                           | No. | Pin Name                             | No. |
|----------|-----|-------------------------------------|-----|----------------------------------------------------|-----|--------------------------------------|-----|
| A0       | 40  | AD5                                 | 88  | GND                                                | 89  | $\overline{S}2$                      | 9   |
| A1       | 39  | AD6                                 | 91  | HLDA                                               | 44  | $S6/\overline{CLKDIV}2/\text{PIO}29$ | 96  |
| A2       | 37  | AD7                                 | 94  | HOLD                                               | 45  | SCLK/PIO20                           | 3   |
| A3       | 36  | AD8                                 | 79  | INT0                                               | 56  | SDATA/PIO21                          | 100 |
| A4       | 35  | AD9                                 | 81  | $\text{INT}1/\overline{\text{SELECT}}$             | 55  | SDEN0/PIO22                          | 2   |
| A5       | 34  | AD10                                | 83  | $\text{INT}2/\overline{\text{INTA}}0/\text{PIO}31$ | 54  | SDEN1/PIO23                          | 1   |
| A6       | 33  | AD11                                | 85  | $\text{INT}3/\overline{\text{INTA}}1/\text{IRQ}$   | 53  | SRDY/PIO6                            | 46  |
| A7       | 32  | AD12                                | 87  | INT4/PIO30                                         | 52  | TMRIN0/PIO11                         | 75  |
| A8       | 31  | AD13                                | 90  | $\overline{\text{LCS}}/\text{ONCE}0$               | 58  | TMRIN1/PIO0                          | 72  |
| A9       | 30  | AD14                                | 93  | $\overline{\text{MCS}}0/\text{PIO}14$              | 50  | TMROUT0/PIO10                        | 74  |
| A10      | 29  | AD15                                | 95  | $\overline{\text{MCS}}1/\text{PIO}15$              | 51  | TMROUT1/PIO1                         | 73  |
| A11      | 28  | ALE                                 | 7   | $\overline{\text{MCS}}2/\text{PIO}24$              | 68  | TXD/PIO27                            | 98  |
| A12      | 27  | ARDY                                | 8   | $\overline{\text{MCS}}3/\text{RFSH}/\text{PIO}25$  | 69  | $\overline{\text{UCS}}/\text{ONCE}1$ | 57  |
| A13      | 26  | $\overline{\text{BHE}}/\text{ADEN}$ | 4   | NMI                                                | 47  | $\overline{\text{UZI}}/\text{PIO}26$ | 97  |
| A14      | 25  | CLKOUTA                             | 16  | $\overline{\text{PCS}}0/\text{PIO}16$              | 66  | $V_{CC}$                             | 15  |
| A15      | 24  | CLKOUTB                             | 17  | $\overline{\text{PCS}}1/\text{PIO}17$              | 65  | $V_{CC}$                             | 21  |
| A16      | 23  | $\overline{\text{DEN}}/\text{PIO}5$ | 49  | $\overline{\text{PCS}}2/\text{PIO}18$              | 63  | $V_{CC}$                             | 38  |
| A17/PIO7 | 22  | DRQ0/PIO12                          | 77  | $\overline{\text{PCS}}3/\text{PIO}19$              | 62  | $V_{CC}$                             | 61  |
| A18/PIO8 | 20  | DRQ1/PIO13                          | 76  | $\overline{\text{PCS}}5/\text{A}1/\text{PIO}3$     | 60  | $V_{CC}$                             | 67  |
| A19/PIO9 | 19  | DT/ $\overline{\text{R}}$ /PIO4     | 48  | $\overline{\text{PCS}}6/\text{A}2/\text{PIO}2$     | 59  | $V_{CC}$                             | 92  |
| AD0      | 78  | GND                                 | 12  | $\overline{\text{RD}}$                             | 6   | $\overline{\text{WHB}}$              | 42  |
| AD1      | 80  | GND                                 | 18  | $\overline{\text{RES}}$                            | 71  | $\overline{\text{WLB}}$              | 43  |
| AD2      | 82  | GND                                 | 41  | RXD/PIO28                                          | 99  | $\overline{\text{WR}}$               | 5   |
| AD3      | 84  | GND                                 | 64  | $\overline{S}0$                                    | 11  | X1                                   | 13  |
| AD4      | 86  | GND                                 | 70  | $\overline{S}1$                                    | 10  | X2                                   | 14  |

# CONNECTION DIAGRAM

## Am188EM Microcontroller

### Top Side View—100-Pin Plastic Quad Flat Pack (PQFP)



**Note:**

Pin 1 is marked for orientation.

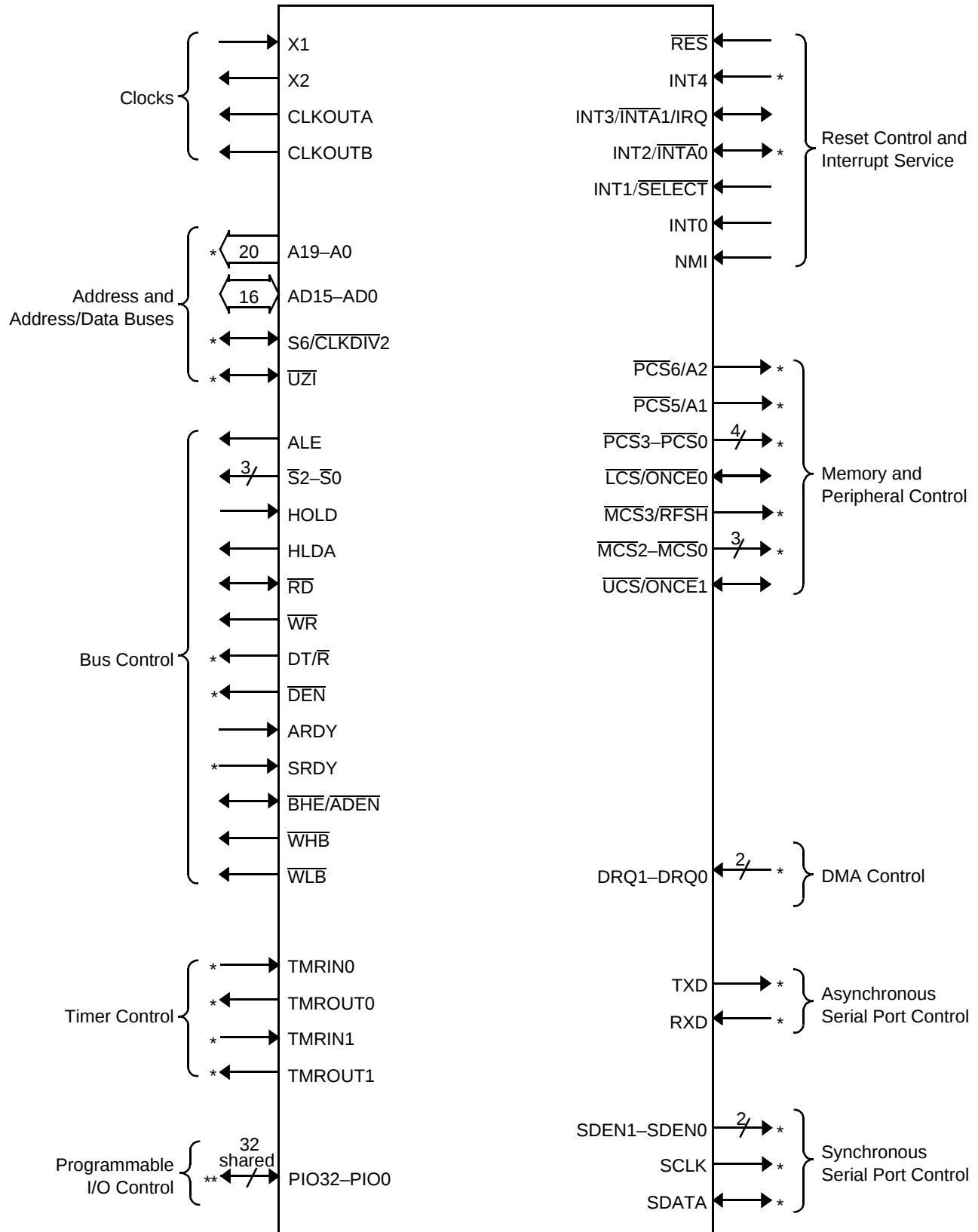
# **PQFP PIN ASSIGNMENTS—Am188EM Microcontroller** **(Sorted by Pin Number)**

| Pin No. | Name                                  | Pin No. | Name                                  | Pin No. | Name                                              | Pin No. | Name                                         |
|---------|---------------------------------------|---------|---------------------------------------|---------|---------------------------------------------------|---------|----------------------------------------------|
| 1       | SDEN1/PIO23                           | 26      | A13                                   | 51      | $\overline{\text{MCS}}1/\text{PIO15}$             | 76      | DRQ1/PIO13                                   |
| 2       | SDEN0/PIO22                           | 27      | A12                                   | 52      | INT4/PIO30                                        | 77      | DRQ0/PIO12                                   |
| 3       | SCLK/PIO20                            | 28      | A11                                   | 53      | INT3/ $\overline{\text{INTA}}1/\text{IRQ}$        | 78      | AD0                                          |
| 4       | $\overline{\text{RFSH}}2/\text{ADEN}$ | 29      | A10                                   | 54      | INT2/ $\overline{\text{INTA}}0/\text{PIO31}$      | 79      | AO8                                          |
| 5       | $\overline{\text{WR}}$                | 30      | A9                                    | 55      | INT1/ $\overline{\text{SELECT}}$                  | 80      | AD1                                          |
| 6       | $\overline{\text{RD}}$                | 31      | A8                                    | 56      | INT0                                              | 81      | AO9                                          |
| 7       | ALE                                   | 32      | A7                                    | 57      | $\overline{\text{UCS}}/\text{ONCE}1$              | 82      | AD2                                          |
| 8       | ARDY                                  | 33      | A6                                    | 58      | $\overline{\text{LCS}}/\text{ONCE}0$              | 83      | AO10                                         |
| 9       | $\overline{\text{S}}2$                | 34      | A5                                    | 59      | $\overline{\text{PCS}}6/\text{A2}/\text{PIO2}$    | 84      | AD3                                          |
| 10      | $\overline{\text{S}}1$                | 35      | A4                                    | 60      | $\overline{\text{PCS}}5/\text{A1}/\text{PIO3}$    | 85      | AO11                                         |
| 11      | $\overline{\text{S}}0$                | 36      | A3                                    | 61      | V <sub>CC</sub>                                   | 86      | AD4                                          |
| 12      | GND                                   | 37      | A2                                    | 62      | $\overline{\text{PCS}}3/\text{PIO19}$             | 87      | AO12                                         |
| 13      | X1                                    | 38      | V <sub>CC</sub>                       | 63      | $\overline{\text{PCS}}2/\text{PIO18}$             | 88      | AD5                                          |
| 14      | X2                                    | 39      | A1                                    | 64      | GND                                               | 89      | GND                                          |
| 15      | V <sub>CC</sub>                       | 40      | A0                                    | 65      | $\overline{\text{PCS}}1/\text{PIO17}$             | 90      | AO13                                         |
| 16      | CLKOUTA                               | 41      | GND                                   | 66      | $\overline{\text{PCS}}0/\text{PIO16}$             | 91      | AD6                                          |
| 17      | CLKOUTB                               | 42      | GND                                   | 67      | V <sub>CC</sub>                                   | 92      | V <sub>CC</sub>                              |
| 18      | GND                                   | 43      | $\overline{\text{WB}}$                | 68      | $\overline{\text{MCS}}2/\text{PIO24}$             | 93      | AO14                                         |
| 19      | A19/PIO9                              | 44      | HLDA                                  | 69      | $\overline{\text{MCS}}3/\text{RFSH}/\text{PIO25}$ | 94      | AD7                                          |
| 20      | A18/PIO8                              | 45      | HOLD                                  | 70      | GND                                               | 95      | AO15                                         |
| 21      | V <sub>CC</sub>                       | 46      | SRDY/PIO6                             | 71      | $\overline{\text{RES}}$                           | 96      | S6/ $\overline{\text{CLKDIV}}2/\text{PIO29}$ |
| 22      | A17/PIO7                              | 47      | NMI                                   | 72      | TMRIN1/PIO0                                       | 97      | $\overline{\text{UZI}}/\text{PIO26}$         |
| 23      | A16                                   | 48      | DT/ $\overline{\text{R}}/\text{PIO4}$ | 73      | TMROUT1/PIO1                                      | 98      | TXD/PIO27                                    |
| 24      | A15                                   | 49      | $\overline{\text{DEN}}/\text{PIO5}$   | 74      | TMROUT0/PIO10                                     | 99      | RXD/PIO28                                    |
| 25      | A14                                   | 50      | $\overline{\text{MCS}}0/\text{PIO14}$ | 75      | TMRIN0/PIO11                                      | 100     | SDATA/PIO21                                  |

# **PQFP PIN ASSIGNMENTS—Am188EM Microcontroller** **(Sorted by Pin Name)**

| Pin Name | No. | Pin Name                 | No. | Pin Name                                     | No. | Pin Name                          | No. |
|----------|-----|--------------------------|-----|----------------------------------------------|-----|-----------------------------------|-----|
| A0       | 40  | AD5                      | 88  | GND                                          | 89  | $\overline{S}1$                   | 10  |
| A1       | 39  | AD6                      | 91  | HLDA                                         | 44  | $\overline{S}2$                   | 9   |
| A2       | 37  | AD7                      | 94  | HOLD                                         | 45  | S6/ $\overline{CLKDIV}2$ /PIO29   | 96  |
| A3       | 36  | ALE                      | 7   | INT0                                         | 56  | SCLK/PIO20                        | 3   |
| A4       | 35  | AO8                      | 79  | INT1/ $\overline{SELECT}$                    | 55  | SDATA/PIO21                       | 100 |
| A5       | 34  | AO9                      | 81  | INT2/ $\overline{INTA}0$ /PIO31              | 54  | SDEN0/PIO22                       | 2   |
| A6       | 33  | AO10                     | 83  | INT3/ $\overline{INTA}1$ /IRQ                | 53  | SDEN1/PIO23                       | 1   |
| A7       | 32  | AO11                     | 85  | INT4/PIO30                                   | 52  | SRDY/PIO6                         | 46  |
| A8       | 31  | AO12                     | 87  | $\overline{LCS}/\overline{ONCE}0$            | 58  | TMRIN0/PIO11                      | 75  |
| A9       | 30  | AO13                     | 90  | $\overline{MCS}0$ /PIO14                     | 50  | TMRIN1/PIO0                       | 72  |
| A10      | 29  | AO14                     | 93  | $\overline{MCS}1$ /PIO15                     | 51  | TMROUT0/PIO10                     | 74  |
| A11      | 28  | AO15                     | 95  | $\overline{MCS}2$ /PIO24                     | 68  | TMROUT1/PIO1                      | 73  |
| A12      | 27  | ARDY                     | 8   | $\overline{MCS}3$ / $\overline{RFSH}$ /PIO25 | 69  | TXD/PIO27                         | 98  |
| A13      | 26  | CLKOUTA                  | 16  | NMI                                          | 47  | $\overline{UCS}/\overline{ONCE}1$ | 57  |
| A14      | 25  | CLKOUTB                  | 17  | $\overline{PCS}0$ /PIO16                     | 66  | $\overline{UZI}$ /PIO26           | 97  |
| A15      | 24  | $\overline{DEN}$ /PIO5   | 49  | $\overline{PCS}1$ /PIO17                     | 65  | V <sub>CC</sub>                   | 15  |
| A16      | 23  | DRQ0/PIO12               | 77  | $\overline{PCS}2$ /PIO18                     | 63  | V <sub>CC</sub>                   | 21  |
| A17/PIO7 | 22  | DRQ1/PIO13               | 76  | $\overline{PCS}3$ /PIO19                     | 62  | V <sub>CC</sub>                   | 38  |
| A18/PIO8 | 20  | DT/ $\overline{R}$ /PIO4 | 48  | $\overline{PCS}5$ /A1/PIO3                   | 60  | V <sub>CC</sub>                   | 61  |
| A19/PIO9 | 19  | GND                      | 12  | $\overline{PCS}6$ /A2/PIO2                   | 59  | V <sub>CC</sub>                   | 67  |
| AD0      | 78  | GND                      | 18  | $\overline{RD}$                              | 6   | V <sub>CC</sub>                   | 92  |
| AD1      | 80  | GND                      | 41  | $\overline{RES}$                             | 71  | $\overline{WB}$                   | 43  |
| AD2      | 82  | GND                      | 42  | $\overline{RFSH}2$ /ADEN                     | 4   | $\overline{WR}$                   | 5   |
| AD3      | 84  | GND                      | 64  | RXD/PIO28                                    | 99  | X1                                | 13  |
| AD4      | 86  | GND                      | 70  | $\overline{S}0$                              | 11  | X2                                | 14  |

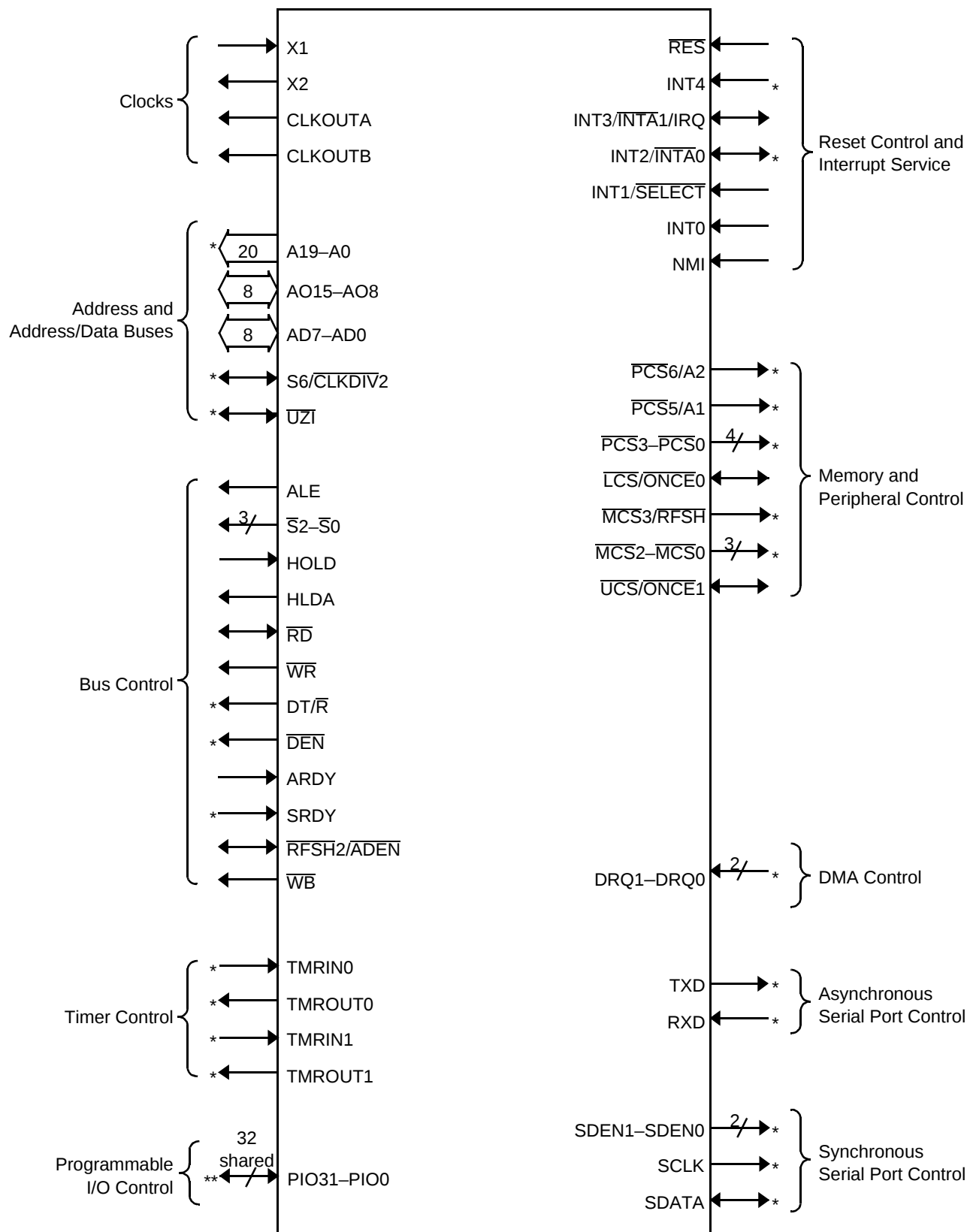
## LOGIC SYMBOL—Am186EM MICROCONTROLLER

**Notes:**

\* These signals are the normal function of a pin that can be used as a PIO. See the pin descriptions beginning on page 25 and Table 2 on page 30 for information on shared function.

\*\* All PIO signals are shared with other physical pins.

## LOGIC SYMBOL—Am188EM MICROCONTROLLER

**Notes:**

\* These signals are the normal function of a pin that can be used as a PIO. See the pin descriptions beginning on page 25 and Table 2 on page 30 for information on shared function.

\*\* All PIO signals are shared with other physical pins.

## PIN DESCRIPTIONS

### Pins That Are Used by Emulators

The following pins are used by emulators: A19–A0, AO15–AO8, AD7–AD0, ALE,  $\overline{\text{BHE}}/\overline{\text{ADEN}}$  (on the Am186EM), CLKOUTA,  $\overline{\text{RFSH2}}/\overline{\text{ADEN}}$  (on the Am188EM),  $\overline{\text{RD}}$ ,  $\overline{\text{S2}}\text{--}\overline{\text{S0}}$ , S6/CLKDIV2, and  $\overline{\text{UZI}}$ .

Emulators require that S6/CLKDIV2 and  $\overline{\text{UZI}}$  be configured in their normal functionality, that is as S6 and  $\overline{\text{UZI}}$ .

If  $\overline{\text{BHE}}/\overline{\text{ADEN}}$  (on the 186) or  $\overline{\text{RFSH2}}/\overline{\text{ADEN}}$  (on the 188) is held Low during the rising edge of  $\overline{\text{RES}}$ , S6 and  $\overline{\text{UZI}}$  are configured in their normal functionality.

### Pin Terminology

The following terms are used to describe the pins:

**Input**—An input-only pin.

**Output**—An output-only pin.

**Input/Output**—A pin that can be either input or output.

**Synchronous**—Synchronous inputs must meet setup and hold times in relation to CLKOUTA. Synchronous outputs are synchronous to CLKOUTA.

**Asynchronous**—Inputs or outputs that are asynchronous to CLKOUTA.

### A19–A0

#### (A19/PIO9, A18/PIO8, A17/PIO7)

##### Address Bus (output, three-state, synchronous)

These pins supply nonmultiplexed memory or I/O addresses to the system one-half of a CLKOUTA period earlier than the multiplexed address and data bus (AD15–AD0 on the 186 or AO15–AO8 and AD7–AD0 on the 188). During a bus hold or reset condition, the address bus is in a high-impedance state.

### AD7–AD0

##### Address and Data Bus (input/output, three-state, synchronous, level-sensitive)

These time-multiplexed pins supply partial memory or I/O addresses, as well as data, to the system. This bus supplies the low-order 8 bits of an address to the system during the first period of a bus cycle ( $t_1$ ), and it supplies data to the system during the remaining periods of that cycle ( $t_2$ ,  $t_3$ , and  $t_4$ ).

The address phase of these pins can be disabled. See the  $\overline{\text{ADEN}}$  description with the  $\overline{\text{BHE}}/\overline{\text{ADEN}}$  pin. When  $\overline{\text{WLB}}$  is negated, these pins are three-stated during  $t_2$ ,  $t_3$ , and  $t_4$ .

During a bus hold or reset condition, the address and data bus is in a high-impedance state.

During a power-on reset, the address and data bus pins (AD15–AD0 for the 186, AO15–AO8 and AD7–AD0 for the 188) can also be used to load system configuration information into the internal reset configuration register.

### AD15–AD8 (Am186EM Microcontroller) AO15–AO8 (Am188EM Microcontroller)

##### Address and Data Bus (input/output, three-state, synchronous, level-sensitive)

##### Address-Only Bus (output, three-state, synchronous, level-sensitive)

**AD15–AD8**—On the Am186EM microcontroller, these time-multiplexed pins supply memory or I/O addresses and data to the system. This bus can supply an address to the system during the first period of a bus cycle ( $t_1$ ). It supplies data to the system during the remaining periods of that cycle ( $t_2$ ,  $t_3$ , and  $t_4$ ).

The address phase of these pins can be disabled. See the  $\overline{\text{ADEN}}$  description with the  $\overline{\text{BHE}}/\overline{\text{ADEN}}$  pin. When  $\overline{\text{WHB}}$  is negated, these pins are three-stated during  $t_2$ ,  $t_3$ , and  $t_4$ .

During a bus hold or reset condition, the address and data bus is in a high-impedance state.

During a power-on reset, the address and data bus pins (AD15–AD0 for the 186, AO15–AO8 and AD7–AD0 for the 188) can also be used to load system configuration information into the internal reset configuration register.

**AO15–AO8**—On the Am188EM microcontroller, the address-only bus (AO15–AO8) contains valid high-order address bits from bus cycles  $t_1$ – $t_4$ . These outputs are floated during a bus hold or reset.

On the Am188EM microcontroller, AO15–AO8 combine with AD7–AD0 to form a complete multiplexed address bus while AD7–AD0 is the 8-bit data bus.

### ALE

##### Address Latch Enable (output, synchronous)

This pin indicates to the system that an address appears on the address and data bus (AD15–AD0 for the 186 or AO15–AO8 and AD7–AD0 for the 188). The address is guaranteed valid on the trailing edge of ALE. This pin is three-stated during ONCE mode. This pin is not three-stated during a bus hold or reset.

### ARDY

##### Asynchronous Ready (input, asynchronous, level-sensitive)

This pin indicates to the microcontroller that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUTA and is active High. The

falling edge of ARDY must be synchronized to CLK-OUTA. To always assert the ready condition to the microcontroller, tie ARDY High. If the system does not use ARDY, tie the pin Low to yield control to SRDY.

## **BHE/ADEN**

### **(Am186EM Microcontroller Only)**

#### **Bus High Enable (three-state, output, synchronous) Address Enable (input, internal pullup)**

**BHE**—During a memory access, this pin and the least-significant address bit (AD0 or A0) indicate to the system which bytes of the data bus (upper, lower, or both) participate in a bus cycle. The  $\overline{\text{BHE/ADEN}}$  and AD0 pins are encoded as shown in Table 1.

$\overline{\text{BHE}}$  is asserted during  $t_1$  and remains asserted through  $t_3$  and  $t_w$ .  $\overline{\text{BHE}}$  does not need to be latched.  $\overline{\text{BHE}}$  floats during bus hold and reset.

On the Am186EM and Am188EM microcontrollers,  $\overline{\text{WLB}}$  and  $\overline{\text{WHB}}$  implement the functionality of  $\overline{\text{BHE}}$  and AD0 for high and low byte write enables.

**Table 1. Data Byte Encoding**

| <b>BHE</b> | <b>AD0</b> | <b>Type of Bus Cycle</b>       |
|------------|------------|--------------------------------|
| 0          | 0          | Word Transfer                  |
| 0          | 1          | High Byte Transfer (Bits 15–8) |
| 1          | 0          | Low Byte Transfer (Bits 7–0)   |
| 1          | 1          | Refresh                        |

$\overline{\text{BHE/ADEN}}$  also signals DRAM refresh cycles when using the multiplexed address and data (AD) bus. A refresh cycle is indicated when both  $\overline{\text{BHE/ADEN}}$  and AD0 are High. During refresh cycles, the A bus and the AD bus are not guaranteed to provide the same address during the address phase of the AD bus cycle. For this reason, the A0 signal cannot be used in place of the AD0 signal to determine refresh cycles. PSRAM refreshes also provide an additional  $\overline{\text{RFSH}}$  signal (see the  $\overline{\text{MCS3/RFSH}}$  pin description on page 28).

**ADEN**—If  $\overline{\text{BHE/ADEN}}$  is held High or left floating during power-on reset, the address portion of the AD bus (AD15–AD0 for the 186 or AO15–AO8 and AD7–AD0 for the 188) is enabled or disabled during LCS and UCS bus cycles based on the DA bit in the LMCS and UMCS registers. If the DA bit is set, the memory address is accessed on the A19–A0 pins. There is a weak internal pullup resistor on  $\overline{\text{BHE/ADEN}}$  so no external pullup is required. This mode of operation reduces power consumption.

If  $\overline{\text{BHE/ADEN}}$  is held Low on power-on reset, the AD bus drives both addresses and data, regardless of the DA bit setting. This pin is sampled on the rising edge of  $\overline{\text{RES}}$ . (S6 and  $\overline{\text{UZI}}$  also assume their normal functionality in this instance. See Table 2 on page 30.)

**Note:** On the Am188EM microcontroller, AO15–AO8 are driven during the entire bus cycle, regardless of the setting of the DA bit in the UMCS and LMCS registers.

## **CLKOUTA**

### **Clock Output A (output, synchronous)**

This pin supplies the internal clock to the system. Depending on the value of the power-save control register (PDCON), CLKOUTA operates at either the crystal input frequency (X1), the power-save frequency, or is three-stated. CLKOUTA remains active during reset and bus hold conditions.

## **CLKOUTB**

### **Clock Output B (output, synchronous)**

This pin supplies an additional clock to the system. Depending upon the value of the power-save control register (PDCON), CLKOUTB operates at either the crystal input frequency (X1), the power-save frequency, or is three-stated. CLKOUTB remains active during reset and bus hold conditions.

## **DEN/PIO5**

### **Data Enable (output, three-state, synchronous)**

This pin supplies an output enable to an external data-bus transceiver.  $\overline{\text{DEN}}$  is asserted during memory, I/O, and interrupt acknowledge cycles.  $\overline{\text{DEN}}$  is deasserted when DT/ $\overline{\text{R}}$  changes state.  $\overline{\text{DEN}}$  floats during a bus hold or reset condition.

## **DRQ1–DRQ0 (DRQ1/PIO13, DRQ0/PIO12)**

### **DMA Requests (input, synchronous, level-sensitive)**

These pins indicate to the microcontroller that an external device is ready for DMA channel 1 or channel 0 to perform a transfer. DRQ1–DRQ0 are level-triggered and internally synchronized.

The DRQ signals are not latched and must remain active until serviced.

## **DT/ $\overline{\text{R}}$ /PIO4**

### **Data Transmit or Receive (output, three-state, synchronous)**

This pin indicates which direction data should flow through an external data-bus transceiver. When DT/ $\overline{\text{R}}$  is asserted High, the microcontroller transmits data. When this pin is deasserted Low, the microcontroller receives data. DT/ $\overline{\text{R}}$  floats during a bus hold or reset condition.

**GND****Ground**

The ground pins connect the system ground to the microcontroller.

**HLDA****Bus Hold Acknowledge (output, synchronous)**

This pin is asserted High to indicate to an external bus master that the microcontroller has released control of the local bus. When an external bus master requests control of the local bus (by asserting HOLD), the microcontroller completes the bus cycle in progress and then relinquishes control of the bus to the external bus master by asserting HLDA and floating  $\overline{\text{DEN}}$ ,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ ,  $\overline{\text{S2-S0}}$ , AD15–AD0, S6, A19–A0,  $\overline{\text{BHE}}$ ,  $\overline{\text{WHB}}$ ,  $\overline{\text{WLB}}$ , and  $\overline{\text{DT/R}}$ , and then driving the chip selects  $\overline{\text{UCS}}$ ,  $\overline{\text{LCS}}$ ,  $\overline{\text{MCS3-MCS0}}$ ,  $\overline{\text{PCS6-PCS5}}$ , and  $\overline{\text{PCS3-PCS0}}$  High.

When the external bus master has finished using the local bus, it indicates this to the microcontroller by deasserting HOLD. The microcontroller responds by deasserting HLDA.

If the microcontroller requires access to the bus (i.e. for refresh), it will deassert HLDA before the external bus master deasserts HOLD. The external bus master must be able to deassert HOLD and allow the microcontroller access to the bus. See the timing diagrams for bus hold on page 92.

**HOLD****Bus Hold Request (input, synchronous, level-sensitive)**

This pin indicates to the microcontroller that an external bus master needs control of the local bus.

The Am186EM and Am188EM microcontrollers' HOLD latency time is a function of the activity occurring in the processor when the HOLD request is received. A DRAM request will delay a HOLD request when both requests are made at the same time. In addition, if locked transfers are performed, the HOLD latency time is increased by the length of the locked transfer.

For more information, see the HLDA pin description.

**INT0****Maskable Interrupt Request 0 (input, asynchronous)**

This pin indicates to the microcontroller that an interrupt request has occurred. If the INT0 pin is not masked, the microcontroller transfers program execution to the location specified by the INT0 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT0 until the request is acknowledged.

**INT1/SELECT****Maskable Interrupt Request 1 (input, asynchronous)****Slave Select (input, asynchronous)**

**INT1**—This pin indicates to the microcontroller that an interrupt request has occurred. If INT1 is not masked, the microcontroller transfers program execution to the location specified by the INT1 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT1 until the request is acknowledged.

**SELECT**—When the microcontroller interrupt control unit is operating as a slave to an external interrupt controller, this pin indicates to the microcontroller that an interrupt type appears on the address and data bus. The INT0 pin must indicate to the microcontroller that an interrupt has occurred before the **SELECT** pin indicates to the microcontroller that the interrupt type appears on the bus.

**INT2/ $\overline{\text{INTA0}}$ /PIO31****Maskable Interrupt Request 2 (input, asynchronous)****Interrupt Acknowledge 0 (output, synchronous)**

**INT2**—This pin indicates to the microcontroller that an interrupt request has occurred. If the INT2 pin is not masked, the microcontroller transfers program execution to the location specified by the INT2 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT2 until the request is acknowledged. INT2 becomes  $\overline{\text{INTA0}}$  when INT0 is configured in cascade mode.

**INTA0**—When the microcontroller interrupt control unit is operating in cascade mode, this pin indicates to the system that the microcontroller needs an interrupt type to process the interrupt request on INT0. The peripheral issuing the interrupt request must provide the microcontroller with the corresponding interrupt type.

**INT3/ $\overline{\text{INTA1}}$ /IRQ****Maskable Interrupt Request 3 (input, asynchronous)****Interrupt Acknowledge 1 (output, synchronous)****Slave Interrupt Request (output, synchronous)**

**INT3**—This pin indicates to the microcontroller that an interrupt request has occurred. If the INT3 pin is not masked, the microcontroller then transfers program execution to the location specified by the INT3 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally, and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT3 until the request is acknowledged. INT3 becomes  $\overline{\text{INTA}}1$  when INT1 is configured in cascade mode.

**$\overline{\text{INTA}}1$** —When the microcontroller interrupt control unit is operating in cascade mode or special fully-nested mode, this pin indicates to the system that the microcontroller needs an interrupt type to process the interrupt request on INT1. In both modes, the peripheral issuing the interrupt request must provide the microcontroller with the corresponding interrupt type.

**IRQ**—When the microcontroller interrupt control unit is operating as a slave to an external master interrupt controller, this pin lets the microcontroller issue an interrupt request to the external master interrupt controller.

### INT4/PIO30

**Maskable Interrupt Request 4 (input, asynchronous)**

This pin indicates to the microcontroller that an interrupt request has occurred. If the INT4 pin is not masked, the microcontroller then transfers program execution to the location specified by the INT4 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally, and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT4 until the request is acknowledged.

### $\overline{\text{LCS}}/\overline{\text{ONCE}}0$

**Lower Memory Chip Select (output, synchronous, internal pullup)**

**ONCE Mode Request 0 (input)**

**$\overline{\text{LCS}}$** —This pin indicates to the system that a memory access is in progress to the lower memory block. The base address and size of the lower memory block are programmable up to 512 Kbytes.  $\overline{\text{LCS}}$  is held High during a bus hold condition.

**$\overline{\text{ONCE}}0$** —During reset this pin and  $\overline{\text{ONCE}}1$  indicate to the microcontroller the mode in which it should operate.  $\overline{\text{ONCE}}0$  and  $\overline{\text{ONCE}}1$  are sampled on the rising edge of  $\overline{\text{RES}}$ . If both pins are asserted Low, the microcontroller enters ONCE mode; otherwise, it operates normally.

In ONCE mode, all pins assume a high-impedance state and remain in that state until a subsequent reset occurs. To guarantee that the microcontroller does not inadvertently enter ONCE mode,  $\overline{\text{ONCE}}0$  has a weak internal pullup resistor that is active only during reset. This pin is not three-stated during a bus hold condition.

### $\overline{\text{MCS}}3/\overline{\text{RFSH}}/\text{PIO}25$

**Midrange Memory Chip Select 3**

**(output, synchronous, internal pullup)**

**Automatic Refresh (output, synchronous)**

**$\overline{\text{MCS}}3$** —This pin indicates to the system that a memory access is in progress to the fourth region of the midrange memory block. The base address and size of the midrange memory block are programmable.  $\overline{\text{MCS}}3$  is held High during a bus hold condition. In addition, this pin has a weak internal pullup resistor that is active during reset.

**$\overline{\text{RFSH}}$** —This pin provides a signal timed for auto refresh to PSRAM devices. It is only enabled to function as a refresh pulse when the PSRAM mode bit is set in the LMCS Register. An active Low pulse is generated for 1.5 clock cycles with an adequate deassertion period to ensure that overall auto refresh cycle time is met. This pin is not three-stated during a bus hold condition.

### $\overline{\text{MCS}}2\text{--}\overline{\text{MCS}}0$

**( $\overline{\text{MCS}}2/\text{PIO}24$ ,  $\overline{\text{MCS}}1/\text{PIO}15$ ,  $\overline{\text{MCS}}0/\text{PIO}14$ )**

**Midrange Memory Chip Selects (output, synchronous, internal pullup)**

These pins indicate to the system that a memory access is in progress to the corresponding region of the midrange memory block. The base address and size of the midrange memory block are programmable.  $\overline{\text{MCS}}2\text{--}\overline{\text{MCS}}0$  are held High during a bus hold condition. In addition, they have weak internal pullup resistors that are active during reset.

### NMI

**Nonmaskable Interrupt (input, synchronous, edge-sensitive)**

This pin indicates to the microcontroller that an interrupt request has occurred. The NMI signal is the highest priority hardware interrupt and, unlike the INT4–INT0 pins, cannot be masked. The microcontroller always transfers program execution to the location specified by the nonmaskable interrupt vector in the microcontroller interrupt vector table when NMI is asserted.

Although NMI is the highest priority interrupt source, it does not participate in the priority resolution process of the maskable interrupts. There is no bit associated with NMI in the interrupt in-service or interrupt request registers. This means that a new NMI request can interrupt an executing NMI interrupt service routine. As with all hardware interrupts, the IF (interrupt flag) is cleared when the processor takes the interrupt, disabling the maskable interrupt sources. However, if maskable interrupts are re-enabled by software in the NMI interrupt service routine, via the STI instruction for example, the fact that an NMI is currently in service will not have any

effect on the priority resolution of maskable interrupt requests. For this reason, it is strongly advised that the interrupt service routine for NMI does not enable the maskable interrupts.

An NMI transition from Low to High is latched and synchronized internally, and it initiates the interrupt at the next instruction boundary. To guarantee that the interrupt is recognized, the NMI pin must be asserted for at least one CLKOUTA period.

### **$\overline{PCS3}$ – $\overline{PCS0}$ ( $\overline{PCS3}$ /PIO19, $\overline{PCS2}$ /PIO18, $\overline{PCS1}$ /PIO17, $\overline{PCS0}$ /PIO16)**

#### **Peripheral Chip Selects (output, synchronous)**

These pins indicate to the system that a memory access is in progress to the corresponding region of the peripheral memory block (either I/O or memory address space). The base address of the peripheral memory block is programmable.  $\overline{PCS3}$ – $\overline{PCS0}$  are held High during a bus hold condition. They are also held High during reset.

$\overline{PCS4}$  is not available on the Am186EM and Am188EM microcontrollers.

Unlike the  $\overline{UCS}$  and  $\overline{LCS}$  chip selects, the  $\overline{PCS}$  outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers.

### **$\overline{PCS5}$ /A1/PIO3**

#### **Peripheral Chip Select 5 (output, synchronous) Latched Address Bit 1 (output, synchronous)**

**$\overline{PCS5}$** —This pin indicates to the system that a memory access is in progress to the sixth region of the peripheral memory block (either I/O or memory address space). The base address of the peripheral memory block is programmable.  $\overline{PCS5}$  is held High during a bus hold condition. It is also held High during reset.

Unlike the  $\overline{UCS}$  and  $\overline{LCS}$  chip selects, the  $\overline{PCS}$  outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers.

**A1**—When the EX bit in the  $\overline{MCS}$  and  $\overline{PCS}$  auxiliary register is 0, this pin supplies an internally latched ad-

dress bit 1 to the system. During a bus hold condition, A1 retains its previously latched value.

### **$\overline{PCS6}$ /A2/PIO2**

#### **Peripheral Chip Select 6 (output, synchronous) Latched Address Bit 2 (output, synchronous)**

**$\overline{PCS6}$** —This pin indicates to the system that a memory access is in progress to the seventh region of the peripheral memory block (either I/O or memory address space). The base address of the peripheral memory block is programmable.  $\overline{PCS6}$  is held High during a bus hold condition or reset.

Unlike the  $\overline{UCS}$  and  $\overline{LCS}$  chip selects, the  $\overline{PCS}$  outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers.

**A2**—When the EX bit in the  $\overline{MCS}$  and  $\overline{PCS}$  Auxiliary Register is 0, this pin supplies an internally latched address bit 2 to the system. During a bus hold condition, A2 retains its previously latched value.

### **PIO31–PIO0 (Shared)**

#### **Programmable I/O Pins (input/output, asynchronous, open-drain)**

The Am186EM and Am188EM microcontrollers provide 32 individually programmable I/O pins. Each PIO can be programmed with the following attributes: PIO function (enabled/disabled), direction (input/output), and weak pullup or pulldown.

The pins that are multiplexed with PIO31–PIO0 are listed in Table 2 and Table 3.

After power-on reset, the PIO pins default to various configurations. The column titled *Power-On Reset Status* in Table 2 and Table 3 lists the defaults for the PIOs. The system initialization code must reconfigure any PIOs as required.

The A19–A17 address pins default to normal operation on power-on reset, allowing the processor to correctly begin fetching instructions at the boot address FFFF0h. The  $\overline{DT/R}$ ,  $\overline{DEN}$ , and SRDY pins also default to normal operation on power-on reset.

Table 2. Numeric PIO Pin Assignments

| PIO No              | Associated Pin                  | Power-On Reset Status           |
|---------------------|---------------------------------|---------------------------------|
| 0                   | TMRIN1                          | Input with pullup               |
| 1                   | TMROUT1                         | Input with pulldown             |
| 2                   | $\overline{\text{PCS6/A2}}$     | Input with pullup               |
| 3                   | $\overline{\text{PCS5/A1}}$     | Input with pullup               |
| 4                   | $\text{DT}/\overline{\text{R}}$ | Normal operation <sup>(3)</sup> |
| 5                   | $\overline{\text{DEN}}$         | Normal operation <sup>(3)</sup> |
| 6                   | SRDY                            | Normal operation <sup>(4)</sup> |
| 7 <sup>(1)</sup>    | A17                             | Normal operation <sup>(3)</sup> |
| 8 <sup>(1)</sup>    | A18                             | Normal operation <sup>(3)</sup> |
| 9 <sup>(1)</sup>    | A19                             | Normal operation <sup>(3)</sup> |
| 10                  | TMROUT0                         | Input with pulldown             |
| 11                  | TMRIN0                          | Input with pullup               |
| 12                  | DRQ0                            | Input with pullup               |
| 13                  | DRQ1                            | Input with pullup               |
| 14                  | $\overline{\text{MCS0}}$        | Input with pullup               |
| 15                  | $\overline{\text{MCS1}}$        | Input with pullup               |
| 16                  | $\overline{\text{PCS0}}$        | Input with pullup               |
| 17                  | $\overline{\text{PCS1}}$        | Input with pullup               |
| 18                  | $\overline{\text{PCS2}}$        | Input with pullup               |
| 19                  | $\overline{\text{PCS3}}$        | Input with pullup               |
| 20                  | SCLK                            | Input with pullup               |
| 21                  | SDATA                           | Input with pullup               |
| 22                  | SDEN0                           | Input with pulldown             |
| 23                  | SDEN1                           | Input with pulldown             |
| 24                  | $\overline{\text{MCS2}}$        | Input with pullup               |
| 25                  | $\overline{\text{MCS3/RFSH}}$   | Input with pullup               |
| 26 <sup>(1,2)</sup> | $\overline{\text{UZI}}$         | Input with pullup               |
| 27                  | TXD                             | Input with pullup               |
| 28                  | RXD                             | Input with pullup               |
| 29 <sup>(1,2)</sup> | S6/CLKDIV2                      | Input with pullup               |
| 30                  | INT4                            | Input with pullup               |
| 31                  | INT2                            | Input with pullup               |

**Notes:**

1. These pins are used by emulators. (Emulators also use  $\overline{\text{S2-S0}}$ ,  $\overline{\text{RES}}$ , NMI, CLKOUTA, BHE, ALE, AD15-AD0, and A16-A0.)
2. These pins revert to normal operation if  $\overline{\text{BHE/ADEN}}$  (186) or  $\overline{\text{RFSH2/ADEN}}$  (188) is held Low during power-on reset.
3. When used as a PIO, input with pullup option available.
4. When used as a PIO, input with pulldown option available.

Table 3. Alphabetic PIO Pin Assignments

| Associated Pin                           | PIO No | Power-On Reset Status           |
|------------------------------------------|--------|---------------------------------|
| A17 <sup>(1)</sup>                       | 7      | Normal operation <sup>(3)</sup> |
| A18 <sup>(1)</sup>                       | 8      | Normal operation <sup>(3)</sup> |
| A19 <sup>(1)</sup>                       | 9      | Normal operation <sup>(3)</sup> |
| DEN                                      | 5      | Normal operation <sup>(3)</sup> |
| DRQ0                                     | 12     | Input with pullup               |
| DRQ1                                     | 13     | Input with pullup               |
| $\text{DT}/\overline{\text{R}}$          | 4      | Normal operation <sup>(3)</sup> |
| INT2                                     | 31     | Input with pullup               |
| INT4                                     | 30     | Input with pullup               |
| $\overline{\text{MCS0}}$                 | 14     | Input with pullup               |
| $\overline{\text{MCS1}}$                 | 15     | Input with pullup               |
| $\overline{\text{MCS2}}$                 | 24     | Input with pullup               |
| $\overline{\text{MCS3/RFSH}}$            | 25     | Input with pullup               |
| $\overline{\text{PCS0}}$                 | 16     | Input with pullup               |
| $\overline{\text{PCS1}}$                 | 17     | Input with pullup               |
| $\overline{\text{PCS2}}$                 | 18     | Input with pullup               |
| $\overline{\text{PCS3}}$                 | 19     | Input with pullup               |
| $\overline{\text{PCS5/A1}}$              | 3      | Input with pullup               |
| $\overline{\text{PCS6/A2}}$              | 2      | Input with pullup               |
| RXD                                      | 28     | Input with pullup               |
| S6/CLKDIV2 <sup>(1,2)</sup>              | 29     | Input with pullup               |
| SCLK                                     | 20     | Input with pullup               |
| SDATA                                    | 21     | Input with pullup               |
| SDEN0                                    | 22     | Input with pulldown             |
| SDEN1                                    | 23     | Input with pulldown             |
| SRDY                                     | 6      | Normal operation <sup>(4)</sup> |
| TMRIN0                                   | 11     | Input with pullup               |
| TMRIN1                                   | 0      | Input with pullup               |
| TMROUT0                                  | 10     | Input with pulldown             |
| TMROUT1                                  | 1      | Input with pulldown             |
| TXD                                      | 27     | Input with pullup               |
| $\overline{\text{UZI}}$ <sup>(1,2)</sup> | 26     | Input with pullup               |

**Notes:**

1. These pins are used by emulators. (Emulators also use  $\overline{\text{S2-S0}}$ ,  $\overline{\text{RES}}$ , NMI, CLKOUTA, BHE, ALE, AD15-AD0, and A16-A0.)
2. These pins revert to normal operation if  $\overline{\text{BHE/ADEN}}$  (186) or  $\overline{\text{RFSH2/ADEN}}$  (188) is held Low during power-on reset.
3. When used as a PIO, input with pullup option available.
4. When used as a PIO, input with pulldown option available.

**$\overline{RD}$** **Read Strobe (output, synchronous, three-state)**

This pin indicates to the system that the microcontroller is performing a memory or I/O read cycle.  $\overline{RD}$  is guaranteed not to be asserted before the address and data bus is floated during the address-to-data transition.  $\overline{RD}$  floats during a bus hold condition.

 **$\overline{RES}$** **Reset (input, asynchronous, level-sensitive)**

This pin requires the microcontroller to perform a reset. When  $\overline{RES}$  is asserted, the microcontroller immediately terminates its present activity, clears its internal logic, and CPU control is transferred to the reset address FFFF0h.

$\overline{RES}$  must be held Low for at least 1 ms.

$\overline{RES}$  can be asserted asynchronously to CLKOUTA because  $\overline{RES}$  is synchronized internally. For proper initialization,  $V_{CC}$  must be within specifications, and CLKOUTA must be stable for more than four CLKOUTA periods during which  $\overline{RES}$  is asserted.

The microcontroller begins fetching instructions approximately 6.5 CLKOUTA periods after  $\overline{RES}$  is deasserted. This input is provided with a Schmitt trigger to facilitate power-on  $\overline{RES}$  generation via an RC network.

 **$\overline{RFSH2/ADEN}$** **(Am188EM Microcontroller Only)****Refresh 2 (three-state, output, synchronous)  
Address Enable (input, internal pullup)**

**$\overline{RFSH2}$** —Asserted Low to signify a DRAM refresh bus cycle. The use of  $\overline{RFSH2/ADEN}$  to signal a refresh is not valid when PSRAM mode is selected. Instead, the  $\overline{MCS3/RFSH}$  signal is provided to the PSRAM.

**$\overline{ADEN}$** —If  $\overline{RFSH2/ADEN}$  is held High or left floating on power-on reset, the AD bus (AO15–AO8 and AD7–AD0) is enabled or disabled during the address portion of LCS and UCS bus cycles based on the DA bit in the LMCS and UMCS registers. If the DA bit is set, the memory address is accessed on the A19–A0 pins. This mode of operation reduces power consumption. For more information, see the “Bus Operation” section on page 37. There is a weak internal pullup resistor on  $\overline{RFSH2/ADEN}$  so no external pullup is required.

If  $\overline{RFSH2/ADEN}$  is held Low on power-on reset, the AD bus drives both addresses and data regardless of the DA bit setting. The pin is sampled one crystal clock cycle after the rising edge of  $\overline{RES}$ .  $\overline{RFSH2/ADEN}$  is three-stated during bus holds and ONCE mode.

**RXD/PIO28****Receive Data (input, asynchronous)**

This pin supplies asynchronous serial receive data from the system to the internal UART of the microcontroller.

 **$\overline{S2}\text{--}\overline{S0}$** **Bus Cycle Status (output, three-state, synchronous)**

These pins indicate to the system the type of bus cycle in progress.  $\overline{S2}$  can be used as a logical memory or I/O indicator, and  $\overline{S1}$  can be used as a data transmit or receive indicator.  $\overline{S2}\text{--}\overline{S0}$  float during bus hold and hold acknowledge conditions. The  $\overline{S2}\text{--}\overline{S0}$  pins are encoded as shown in Table 4.

**Table 4. Bus Cycle Encoding**

| $\overline{S2}$ | $\overline{S1}$ | $\overline{S0}$ | Bus Cycle             |
|-----------------|-----------------|-----------------|-----------------------|
| 0               | 0               | 0               | Interrupt acknowledge |
| 0               | 0               | 1               | Read data from I/O    |
| 0               | 1               | 0               | Write data to I/O     |
| 0               | 1               | 1               | Halt                  |
| 1               | 0               | 0               | Instruction fetch     |
| 1               | 0               | 1               | Read data from memory |
| 1               | 1               | 0               | Write data to memory  |
| 1               | 1               | 1               | None (passive)        |

 **$\overline{S6/CLKDIV2/PIO29}$** **Bus Cycle Status Bit 6 (output, synchronous)  
Clock Divide by 2 (input, internal pullup)**

**$\overline{S6}$** —During the second and remaining periods of a cycle ( $t_2$ ,  $t_3$ , and  $t_4$ ), this pin is asserted High to indicate a DMA-initiated bus cycle. During a bus hold or reset condition,  $\overline{S6}$  floats.

**$\overline{CLKDIV2}$** —If  $\overline{S6/CLKDIV2/PIO29}$  is held Low during power-on reset, the chip enters clock divided by 2 mode where the processor clock is derived by dividing the external clock input by 2. If this mode is selected, the PLL is disabled. The pin is sampled on the rising edge of  $\overline{RES}$ .

If  $\overline{S6}$  is to be used as PIO29 in input mode, the device driving PIO29 must not drive the pin Low during power-on reset.  $\overline{S6/CLKDIV2/PIO29}$  defaults to a PIO input with pullup, so the pin does not need to be driven High externally.

**SCLK/PIO20****Serial Clock (output, synchronous)**

This pin supplies the synchronous serial interface (SSI) clock to a slave device, allowing transmit and receive operations to be synchronized between the microcontroller and the slave. SCLK is derived from the microcontroller internal clock and then divided by 2, 4, 8, or 16 depending on register settings.

An access to any of the SSR or SSD registers activates SCLK for eight SCLK cycles (see Figure 11 and Figure 12 on page 49). When SCLK is inactive, it is held High by the microcontroller.

**SDATA/PIO21****Serial Data (input/output, synchronous)**

This pin transmits synchronous serial interface (SSI) data to and from a slave device. When SDATA is inactive, a weak keeper holds the last value of SDATA on the pin.

**SDEN1/PIO23, SDEN0/PIO22****Serial Data Enables (output, synchronous)**

These pins enable data transfers on port 1 and port 0 of the synchronous serial interface (SSI). The microcontroller asserts either SDEN1 or SDEN0 at the beginning of a transfer and deasserts it after the transfer is complete. When SDEN1–SDEN0 are inactive, they are held Low by the microcontroller.

**SRDY/PIO6****Synchronous Ready (input, synchronous, level-sensitive)**

This pin indicates to the microcontroller that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active High input synchronized to CLKOUTA.

Using SRDY instead of ARDY allows a relaxed system timing because of the elimination of the one-half clock period required to internally synchronize ARDY. To always assert the ready condition to the microcontroller, tie SRDY High. If the system does not use SRDY, tie the pin Low to yield control to ARDY.

**TMRIN0/PIO11****Timer Input 0 (input, synchronous, edge-sensitive)**

This pin supplies a clock or control signal to the internal microcontroller timer 0. After internally synchronizing a Low-to-High transition on TMRIN0, the microcontroller increments the timer. TMRIN0 must be tied High if not being used.

**TMRIN1/PIO0****Timer Input 1 (input, synchronous, edge-sensitive)**

This pin supplies a clock or control signal to the internal microcontroller timer 1. After internally synchronizing a Low-to-High transition on TMRIN1, the microcontroller increments the timer. TMRIN1 must be tied High if not being used.

**TMROUT0/PIO10****Timer Output 0 (output, synchronous)**

This pin supplies the system with either a single pulse or a continuous waveform with a programmable duty cycle. TMROUT0 is floated during a bus hold or reset.

**TMROUT1/PIO1****Timer Output 1 (output, synchronous)**

This pin supplies the system with either a single pulse or a continuous waveform with a programmable duty cycle. TMROUT1 can also be programmed as a watchdog timer. TMROUT1 is floated during a bus hold or reset.

**TXD/PIO27****Transmit Data (output, asynchronous)**

This pin supplies asynchronous serial transmit data to the system from the internal UART of the microcontroller.

**UCS/ONCE1****Upper Memory Chip Select (output, synchronous)  
ONCE Mode Request 1 (input, internal pullup)**

**UCS**—This pin indicates to the system that a memory access is in progress to the upper memory block. The base address and size of the upper memory block are programmable up to 512 Kbytes.  $\overline{\text{UCS}}$  is held High during a bus hold condition.

After power-on reset,  $\overline{\text{UCS}}$  is asserted because the processor begins executing at FFFF0h and the default configuration for the  $\overline{\text{UCS}}$  chip select is 64 Kbytes from F0000h to FFFFFh.

**ONCE1**—During reset, this pin and  $\overline{\text{ONCE0}}$  indicate to the microcontroller the mode in which it should operate.  $\overline{\text{ONCE0}}$  and  $\overline{\text{ONCE1}}$  are sampled on the rising edge of  $\overline{\text{RES}}$ . If both pins are asserted Low, the microcontroller enters ONCE mode. Otherwise, it operates normally. In ONCE mode, all pins assume a high-impedance state and remain in that state until a subsequent reset occurs. To guarantee that the microcontroller does not inadvertently enter ONCE mode,  $\overline{\text{ONCE1}}$  has a weak internal pullup resistor that is active only during a reset. This pin is not three-stated during a bus hold condition.

**UZI/PIO26****Upper Zero Indicate (output, synchronous)**

$\overline{UZI}$ —This pin lets the designer determine if an access to the interrupt vector table is in progress by ORing it with bits 15–10 of the address and data bus (AD15–AD10 on the 186 and AO15–AO10 on the 188).  $\overline{UZI}$  is the logical OR of the inverted A19–A16 bits, and it asserts in the first period of a bus cycle and is held throughout the cycle.

This signal should be pulled High or allowed to float at reset. If this pin is Low at the negation of reset, the Am186EM and Am188EM microcontrollers will enter a reserved clock test mode.

**V<sub>CC</sub>****Power Supply (input)**

These pins supply power (+5 V) to the microcontroller.

 **$\overline{WHB}$  (Am186EM Microcontroller Only)****Write High Byte (output, three-state, synchronous)**

This pin and  $\overline{WLB}$  indicate to the system which bytes of the data bus (upper, lower, or both) participate in a write cycle. In 80C186 designs, this information is provided by  $\overline{BHE}$ , AD0, and  $\overline{WR}$ . However, by using  $\overline{WHB}$  and  $\overline{WLB}$ , the standard system interface logic and external address latch that were required are eliminated.

$\overline{WHB}$  is asserted with AD15–AD8.  $\overline{WHB}$  is the logical OR of  $\overline{BHE}$  and  $\overline{WR}$ . This pin floats during reset.

 **$\overline{WLB}$  (Am186EM Microcontroller Only)** **$\overline{WB}$  (Am188EM Microcontroller Only)****Write Low Byte (output, three-state, synchronous)****Write Byte (output, three-state, synchronous)**

$\overline{WLB}$ —This pin and  $\overline{WHB}$  indicate to the system which bytes of the data bus (upper, lower, or both) participate in a write cycle. In 80C186 designs, this information is provided by  $\overline{BHE}$ , AD0, and  $\overline{WR}$ . However, by using  $\overline{WHB}$  and  $\overline{WLB}$ , the standard system interface logic and external address latch that were required are eliminated.

$\overline{WLB}$  is asserted with AD7–AD0.  $\overline{WLB}$  is the logical OR of AD0 and  $\overline{WR}$ . This pin floats during reset.

$\overline{WB}$ —On the Am188EM microcontroller, this pin indicates a write to the bus.  $\overline{WB}$  uses the same early timing as the nonmultiplexed address bus.  $\overline{WB}$  is associated with AD7–AD0. This pin floats during reset.

 **$\overline{WR}$** **Write Strobe (output, synchronous)**

This pin indicates to the system that the data on the bus is to be written to a memory or I/O device.  $\overline{WR}$  floats during a bus hold or reset condition.

**X1****Crystal Input (input)**

This pin and the X2 pin provide connections for a fundamental mode or third-overtone parallel-resonant crystal used by the internal oscillator circuit. To provide the microcontroller with an external clock source, connect the source to the X1 pin and leave the X2 pin unconnected.

**X2****Crystal Output (output)**

This pin and the X1 pin provide connections for a fundamental mode or third-overtone parallel-resonant crystal used by the internal oscillator circuit. To provide the microcontroller with an external clock source, leave the X2 pin unconnected and connect the source to the X1 pin.

## FUNCTIONAL DESCRIPTION

AMD's Am186 and Am188 family of microcontrollers and microprocessors is based on the architecture of the original 8086 and 8088 microcontrollers and currently includes the 80C186, 80C188, 80L186, 80L188, Am186EM, Am188EM, Am186EMLV, Am188EMLV, Am186ES, Am188ES, Am186ESLV, Am188ESLV, Am186ER, and Am188ER microcontrollers.

All family members contain the same basic set of registers, instructions, and addressing modes and are compatible with the industry-standard 80C186/188 microcontrollers.

A full description of all the Am186EM and Am188EM microcontroller registers is included in the *Am186EM and Am188EM Microcontrollers User's Manual*, order# 19713. The instruction set for the Am186EM and Am188EM microcontrollers is documented in the *Am186 and Am188 Family Instruction Set Manual*, order# 21267.

## Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of 64K ( $2^{16}$ ) 8-bit bytes. Memory is addressed using a two-component address that consists of a 16-bit segment value and a 16-bit offset. The 16-bit segment values are contained in one of four internal segment registers (CS, DS, SS, or ES). The physical address is calculated by shifting the segment value left by 4 bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 3). This allows for a 1-Mbyte physical address size.

All instructions that address operands in memory must specify the segment value and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 5).

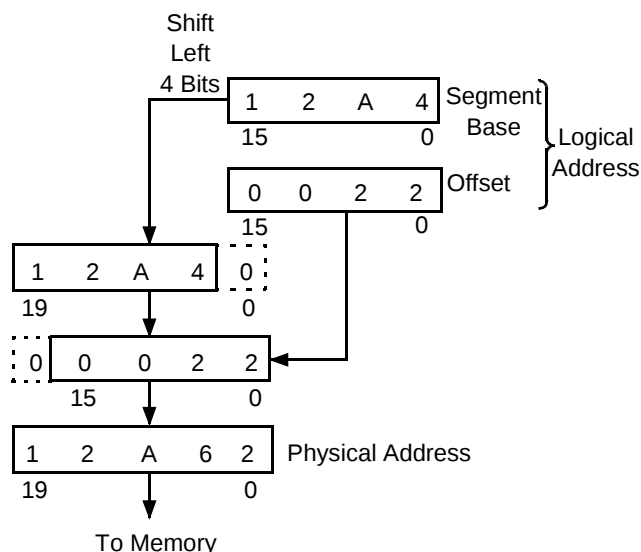


Figure 2. Two-Component Address

## I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions (IN, INS and OUT, OUTS) address the I/O space with either an 8-bit port address specified in the instruction, or a 16-bit port address in the DX register. Eight-bit port addresses are zero-extended so that A15–A8 are Low. I/O port addresses 00F8h through 00FFh are reserved. The Am186EM and Am188EM microcontrollers provide specific instructions for addressing I/O space.

Table 5. Segment Register Selection Rules

| Memory Reference Needed | Segment Register Used | Implicit Segment Selection Rule                                          |
|-------------------------|-----------------------|--------------------------------------------------------------------------|
| Instructions            | Code (CS)             | Instructions (including immediate data)                                  |
| Local Data              | Data (DS)             | All data references                                                      |
| Stack                   | Stack (SS)            | All stack pushes and pops;<br>any memory references that use BP Register |
| External Data (Global)  | Extra (ES)            | All string instruction references that use the DI Register as an index   |

## BUS OPERATION

The industry-standard 80C186 and 80C188 microcontrollers use a multiplexed address and data (AD) bus. The address is present on the AD bus only during the  $t_1$  clock phase. The Am186EM and Am188EM microcontrollers continue to provide the multiplexed AD bus and, in addition, provide a nonmultiplexed address (A) bus. The A bus provides an address to the system for the complete bus cycle ( $t_1$ – $t_4$ ).

For systems where power consumption is a concern, it is possible to disable the address from being driven on the AD bus on the Am186EM microcontroller and on the AD and AO buses on the Am188EM microcontroller during the normal address portion of the bus cycle for accesses to UCS and/or LCS address spaces. In this mode, the affected bus is placed in a high impedance state during the address portion of the bus cycle. This feature is enabled through the DA bits in the UMCS and LMCS registers. When address disable is in effect, the number of signals that assert on the bus during all normal bus cycles to the associated address space is reduced, decreasing power consumption and reducing processor switching noise. On the Am188EM microcontroller, the address is driven on A015–A08 during the data portion of the bus cycle, regardless of the setting of the DA bits.

If the  $\overline{\text{ADEN}}$  pin is pulled Low during processor reset, the value of the DA bits in the UMCS and LMCS registers is ignored and the address is driven on the AD bus for all ac-

cesses, thus preserving the industry-standard 80C186 and 80C188 microcontrollers' multiplexed address bus and providing support for existing emulation tools.

The following diagrams show the Am186EM and Am188EM microcontroller bus cycles when the address bus disable feature is in effect.

Figure 3 shows the affected signals during a normal read or write operation for an Am186EM microcontroller. The address and data will be multiplexed onto the AD bus.

Figure 4 shows an Am186EM microcontroller bus cycle when address bus disable is in effect. This results in having the AD bus operate in a nonmultiplexed address/data mode. The A bus will have the address during a read or write operation.

Figure 5 shows the affected signals during a normal read or write operation for an Am188EM microcontroller. The multiplexed address/data mode is compatible with the 80C186 and 80C188 microcontrollers and might be used to take advantage of existing logic or peripherals.

Figure 6 shows an Am188EM microcontroller bus cycle when address bus disable is in effect. The address and data is not multiplexed. The AD7–AD0 signals will have only data on the bus, while the AO bus will have the address during a read or write operation.

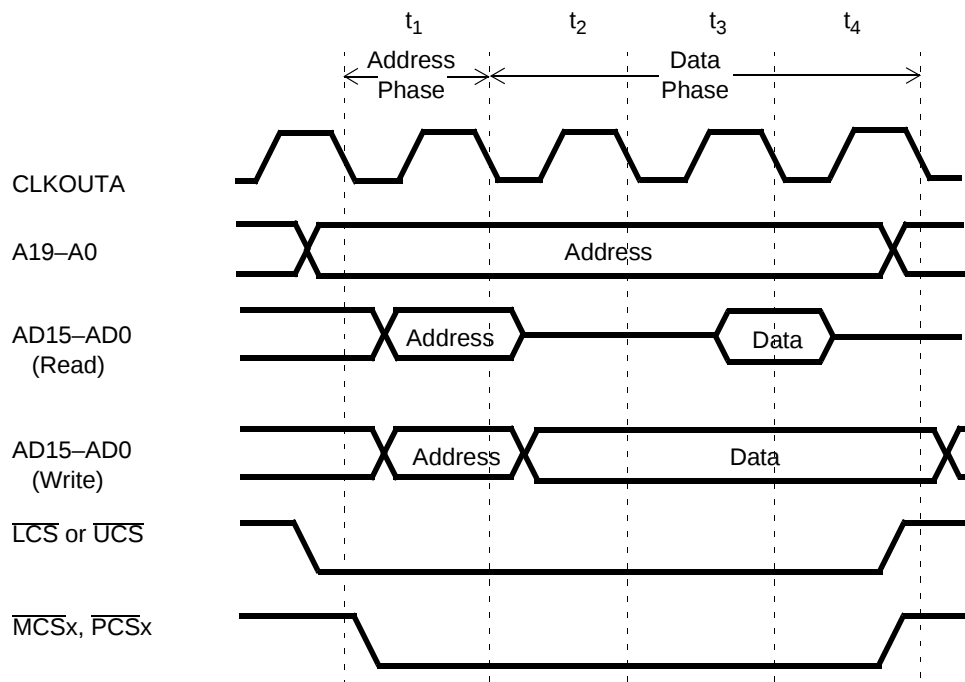


Figure 3. Am186EM Microcontroller Address Bus—Normal Read and Write Operation

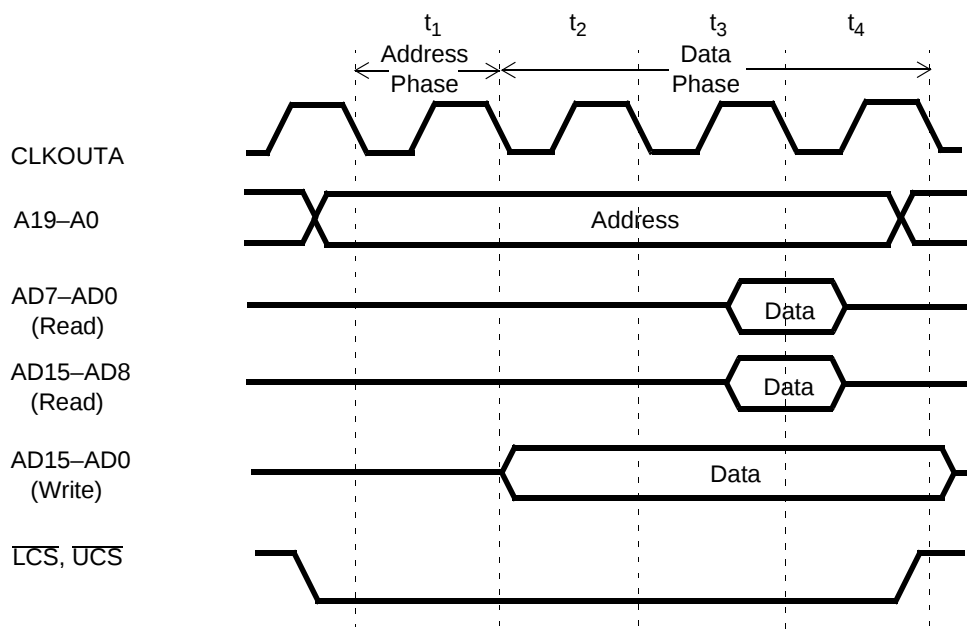


Figure 4. Am186EM Microcontroller—Read and Write with Address Bus Disable In Effect

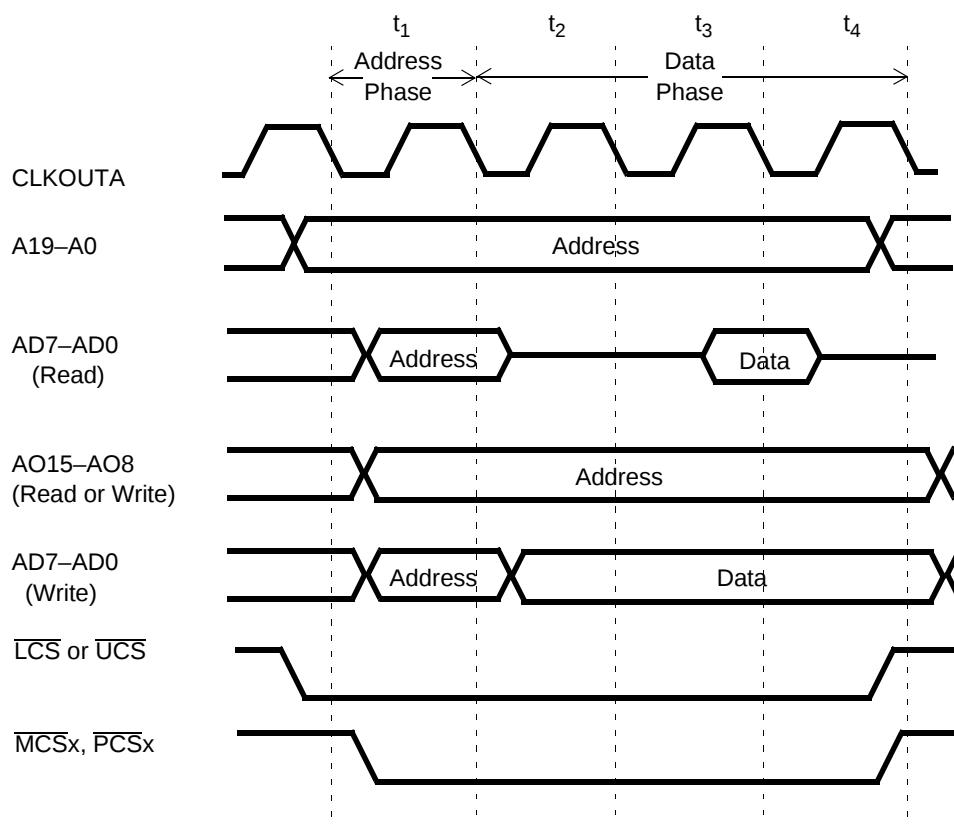


Figure 5. Am188EM Microcontroller Address Bus—Normal Read and Write Operation

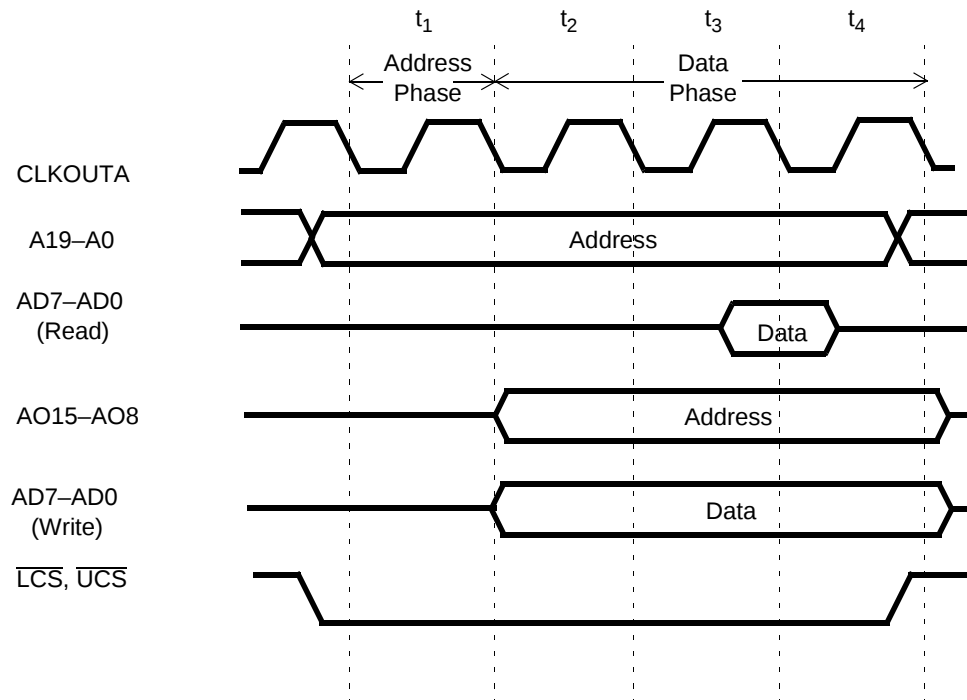


Figure 6. Am188EM Microcontroller—Read and Write with Address Bus Disable In Effect

## BUS INTERFACE UNIT

The bus interface unit controls all accesses to external peripherals and memory devices. External accesses include those to memory devices, as well as those to memory-mapped and I/O-mapped peripherals and the peripheral control block. The Am186EM and Am188EM microcontrollers provide an enhanced bus interface unit with the following features:

- A nonmultiplexed address bus
- Separate byte write enables for high and low bytes in the Am186EM microcontroller only
- Pseudo Static RAM (PSRAM) support

The standard 80C186/188 multiplexed address and data bus requires system interface logic and an external address latch. On the Am186EM and Am188EM microcontrollers, new byte write enables, PSRAM control logic, and a new nonmultiplexed address bus can reduce design costs by eliminating this external logic.

## Nonmultiplexed Address Bus

The nonmultiplexed address bus (A19-A0) is valid one-half CLKOUTA cycle in advance of the address on the AD bus. When used in conjunction with the modified UCS and LCS outputs and the byte write enable signals, the A19-A0 bus provides a seamless interface to SRAM, PSRAM, and Flash/EPROM memory systems.

## Byte Write Enables

The Am186EM microcontroller provides the  $\overline{WHB}$  (Write High Byte) and  $\overline{WLB}$  (Write Low Byte) signals, which act as byte write enables.

$\overline{WHB}$  is the logical OR of  $\overline{BHE}$  and  $\overline{WR}$ .  $\overline{WHB}$  is Low when  $\overline{BHE}$  and  $\overline{WR}$  are both Low.  $\overline{WLB}$  is the logical OR of AD0 and  $\overline{WR}$ .  $\overline{WLB}$  is Low when AD0 and  $\overline{WR}$  are both Low.  $\overline{WB}$  is Low whenever a byte is written on the Am188EM microcontroller.

The byte write enables are driven in conjunction with the nonmultiplexed address bus as required for the write timing requirements of common SRAMs.

## Pseudo Static RAM (PSRAM) Support

The Am186EM and Am188EM microcontrollers support the use of PSRAM devices in low memory chip-select (LCS) space only. When PSRAM mode is enabled, the timing for the  $\overline{\text{LCS}}$  signal is modified by the chip-select control unit to provide a  $\overline{\text{CS}}$  precharge period during PSRAM accesses. The 40-MHz timing of the Am186EM and Am188EM microcontrollers is appropriate to allow 70-ns PSRAM to run with one wait state. PSRAM mode is enabled through a bit in the Low Memory Chip-Select (LMCS) Register. The PSRAM feature is disabled on CPU reset.

In addition to the  $\overline{\text{LCS}}$  timing changes for PSRAM precharge, the PSRAM devices also require periodic refresh of all internal row addresses to retain their data. Although refresh of PSRAM can be accomplished several ways, the Am186EM and Am188EM microcontrollers implement auto refresh only.

The Am186EM and Am188EM microcontrollers generate  $\overline{\text{RFSH}}$ , a refresh signal, to the PSRAM devices when PSRAM mode is enabled. No refresh address is required by the PSRAM when using the auto refresh mechanism. The  $\overline{\text{RFSH}}$  signal is multiplexed with the  $\overline{\text{MCS3}}$  signal pin. When PSRAM mode is enabled,  $\overline{\text{MCS3}}$  is not available for use as a chip-select signal.

The refresh control unit must be programmed before accessing PSRAM in LCS space. The refresh counter in the Clock Prescaler (CDRAM) Register must be configured with the required refresh interval value. The ending address of LCS space and the ready and wait-state generation in the LMCS Register must also be programmed. The refresh counter reload value in the CDRAM Register should not be set to less than 18 (12h) in order to provide time for processor cycles within refresh. The refresh address counter must be set to 000000h to prevent another chip select from asserting.

$\overline{\text{LCS}}$  is held High during a refresh cycle. The A bus is not used during refresh cycles. The LMCS Register must be configured to external ready ignored (R2=1) with one wait state (R1–R0=01b), and the PSRAM mode enable bit (SE) must be set.

## PERIPHERAL CONTROL BLOCK (PCB)

The integrated peripherals of the Am186EM and Am188EM microcontrollers are controlled by 16-bit read/write registers. The peripheral registers are contained within an internal 256-byte control block. The registers are physically located in the peripheral devices they control, but they are addressed as a single 256-byte block. Figure 7 shows a map of these registers.

### Reading and Writing the PCB

Code that is intended to execute on the Am188EM microcontroller should perform all writes to the PCB registers as byte writes. These writes will transfer 16 bits of data to the PCB register even if an 8-bit register is named in the instruction. For example, `out dx, al` results in the value of `ax` being written to the port address in `dx`. Reads to the PCB should be done as word reads. Code written in this manner will run correctly on the Am188EM microcontroller and on the Am186EM microcontroller.

Unaligned reads and writes to the PCB result in unpredictable behavior on both the Am186EM and Am188EM microcontrollers.

For a complete description of all the registers in the PCB, see the *Am186EM and Am188EM Microcontrollers User's Manual*, order# 19713.

| Offset<br>(Hexadecimal) | Register Name                                                          |
|-------------------------|------------------------------------------------------------------------|
| FE                      | Peripheral Control Block Relocation Register                           |
| F6                      | Reset Configuration Register                                           |
| F4                      | Processor Release Level Register                                       |
| F0                      | PDCON Register                                                         |
| E4                      | Enable RCU Register                                                    |
| E2                      | Clock Prescaler Register                                               |
| E0                      | Memory Partition Register                                              |
| DA                      | DMA 1 Control Register                                                 |
| D8                      | DMA 1 Transfer Count Register                                          |
| D6                      | DMA 1 Destination Address High Register                                |
| D4                      | DMA 1 Destination Address Low Register                                 |
| D2                      | DMA 1 Source Address High Register                                     |
| D0                      | DMA 1 Source Address Low Register                                      |
| CA                      | DMA 0 Control Register                                                 |
| C8                      | DMA 0 Transfer Count Register                                          |
| C6                      | DMA 0 Destination Address High Register                                |
| C4                      | DMA 0 Destination Address Low Register                                 |
| C2                      | DMA 0 Source Address High Register                                     |
| C0                      | DMA 0 Source Address Low Register                                      |
| A8                      | $\overline{\text{PCS}}$ and $\overline{\text{MCS}}$ Auxiliary Register |
| A6                      | Midrange Memory Chip Select Register                                   |
| A4                      | Peripheral Chip Select Register                                        |
| A2                      | Low Memory Chip Select Register                                        |
| A0                      | Upper Memory Chip Select Register                                      |
| 88                      | Serial Port Baud Rate Divisor Register                                 |
| 86                      | Serial Port Receive Register                                           |
| 84                      | Serial Port Transmit Register                                          |
| 82                      | Serial Port Status Register                                            |
| 80                      | Serial Port Control Register                                           |

 Changed from 80C186 microcontroller.

**Note:** Gaps in offset addresses indicate reserved registers.

**Figure 7. Peripheral Control Block Register Map**

| Offset<br>(Hexadecimal) | Register Name                          |
|-------------------------|----------------------------------------|
| 7A                      | PIO Data 1 Register                    |
| 78                      | PIO Direction 1 Register               |
| 76                      | PIO Mode 1 Register                    |
| 74                      | PIO Data 0 Register                    |
| 72                      | PIO Direction 0 Register               |
| 70                      | PIO Mode 0 Register                    |
| 66                      | Timer 2 Mode/Control Register          |
| 62                      | Timer 2 Maxcount Compare A Register    |
| 60                      | Timer 2 Count Register                 |
| 5E                      | Timer 1 Mode/Control Register          |
| 5C                      | Timer 1 Maxcount Compare B Register    |
| 5A                      | Timer 1 Maxcount Compare A Register    |
| 58                      | Timer 1 Count Register                 |
| 56                      | Timer 0 Mode/Control Register          |
| 54                      | Timer 0 Maxcount Compare B Register    |
| 52                      | Timer 0 Maxcount Compare A Register    |
| 50                      | Timer 0 Count Register                 |
| 44                      | Serial Port Interrupt Control Register |
| 42                      | Watchdog Timer Control Register        |
| 40                      | INT4 Control Register                  |
| 3E                      | INT3 Control Register                  |
| 3C                      | INT2 Control Register                  |
| 3A                      | INT1 Control Register                  |
| 38                      | INT0 Control Register                  |
| 36                      | DMA 1 Interrupt Control Register       |
| 34                      | DMA 0 Interrupt Control Register       |
| 32                      | Timer Interrupt Control Register       |
| 30                      | Interrupt Status Register              |
| 2E                      | Interrupt Request Register             |
| 2C                      | In-service Register                    |
| 2A                      | Priority Mask Register                 |
| 28                      | Interrupt Mask Register                |
| 26                      | Poll Status Register                   |
| 24                      | Poll Register                          |
| 22                      | End-of-Interrupt Register              |
| 20                      | Interrupt Vector Register              |
| 18                      | Synchronous Serial Receive Register    |
| 16                      | Synchronous Serial Transmit 0 Register |
| 14                      | Synchronous Serial Transmit 1 Register |
| 12                      | Synchronous Serial Enable Register     |
| 10                      | Synchronous Serial Status Register     |

 Changed from 80C186 microcontroller.

**Note:** Gaps in offset addresses indicate reserved registers.

Figure 7. Peripheral Control Block Register Map (continued)

## CLOCK AND POWER MANAGEMENT

The clock and power management unit of the Am186EM and Am188EM microcontrollers includes a phase-locked loop (PLL) and a second programmable system clock output (CLKOUTB).

### Phase-Locked Loop (PLL)

In a traditional 80C186/188 design, the crystal frequency is twice that of the desired internal clock. Because of the internal PLL on the Am186EM and Am188EM microcontrollers, the internal clock generated by the Am186EM and Am188EM microcontrollers (CLKOUTA) is the same frequency as the crystal. The PLL takes the crystal inputs (X1 and X2) and generates a 45/55% (worst case) duty cycle intermediate system clock of the same frequency. This removes the need for an external 2x oscillator, reducing system cost. The PLL is reset by an on-chip power-on reset (POR) circuit.

### Crystal-Driven Clock Source

The internal oscillator circuit of the Am186EM and Am188EM microcontrollers is designed to function with a parallel-resonant fundamental or third-overtone crystal. Because of the PLL, the crystal frequency should be equal to the processor frequency. Do not replace a crystal with an LC or RC equivalent.

The signals X1 and X2 are connected to an internal inverting amplifier (oscillator) which provides, along with the external feedback loading, the necessary phase shift (Figure 8). In such a positive feedback circuit, the inverting amplifier has an output signal (X2) 180 degrees out of phase of the input signal (X1).

The external feedback network provides an additional 180-degree phase shift. In an ideal system, the input to X1 will have 360 or zero degrees of phase shift. The external feedback network is designed to be as close to ideal as possible. If the feedback network is not providing necessary phase shift, negative feedback will dampen the output of the amplifier and negatively af-

fect the operation of the clock generator. Values for the loading on X1 and X2 must be chosen to provide the necessary phase shift and crystal operation.

### Selecting a Crystal

When selecting a crystal, the load capacitance should always be specified ( $C_L$ ). This value can cause variance in the oscillation frequency from the desired specified value (resonance). The load capacitance and the loading of the feedback network have the following relationship:

$$C_L = \frac{(C_1 \cdot C_2)}{(C_1 + C_2)} + C_S$$

where  $C_S$  is the stray capacitance of the circuit. Placing the crystal and  $C_L$  in series across the inverting amplifier and tuning these values ( $C_1$ ,  $C_2$ ) allows the crystal to oscillate at resonance. This relationship is true for both fundamental and third-overtone operation. Finally, there is a relationship between  $C_1$  and  $C_2$ . To enhance the oscillation of the inverting amplifier, these values need to be off-set with the larger load on the output (X2). Equal values of these loads will tend to balance the poles of the inverting amplifier.

The characteristics of the inverting amplifier set limits on the following parameters for crystals:

ESR (Equivalent Series Resistance)..... 80 ohm max

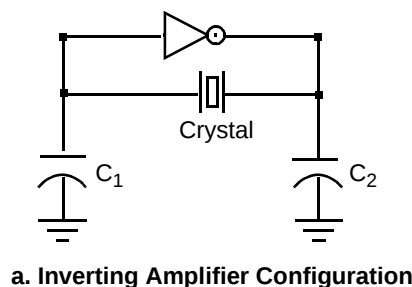
Drive Level..... 1 mW max

The recommended range of values for  $C_1$  and  $C_2$  are as follows:

$C_1$ ..... 15 pF  $\pm$  20%

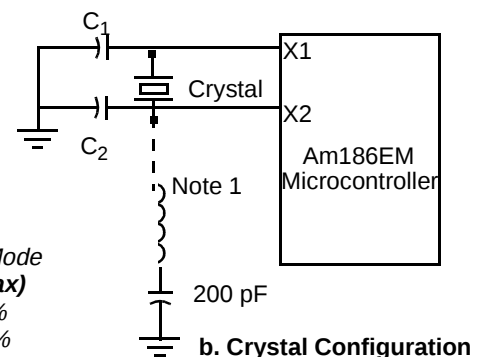
$C_2$ ..... 22 pF  $\pm$  20%

The specific values for  $C_1$  and  $C_2$  must be determined by the designer and are dependent on the characteristics of the chosen crystal and board design.



**Note 1: Use for Third Overtone Mode**

| XTAL Frequency | L1 Value (Max)        |
|----------------|-----------------------|
| 20 MHz         | 12 $\mu$ H $\pm$ 20%  |
| 25 MHz         | 8.2 $\mu$ H $\pm$ 20% |
| 33 MHz         | 4.7 $\mu$ H $\pm$ 20% |
| 40 MHz         | 3.0 $\mu$ H $\pm$ 20% |



**Figure 8. Am186EM and Am188EM Microcontrollers Oscillator Configurations**

## External Source Clock

Alternately, the internal oscillator can be driven from an external clock source. This source should be connected to the input of the inverting amplifier (X1), with the output (X2) not connected.

## System Clocks

The base system clock of the 80C186 and 80C188 microcontrollers is renamed CLKOUTA and the additional output is called CLKOUTB. CLKOUTA and

CLKOUTB operate at either the processor frequency or the crystal input frequency. The output drivers for both clocks are individually programmable for disable. Figure 9 shows the organization of the clocks.

The second clock output (CLKOUTB) allows one clock to run at the crystal input frequency and the other clock to run at the power-save frequency. Individual drive enable bits allow selective enabling of just one or both of these clock outputs.

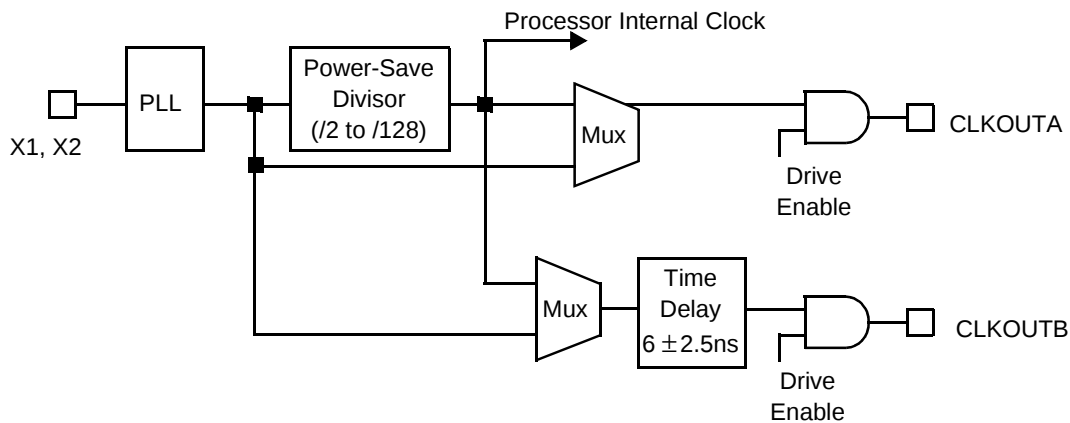


Figure 9. Clock Organization

## Power-Save Operation

The power-save mode of the Am186EM and Am188EM microcontrollers reduces power consumption and heat dissipation, thereby extending battery life in portable systems. In power-save mode, operation of the CPU and internal peripherals continues at a slower clock frequency. When an interrupt occurs, the microcontroller automatically returns to its normal operating frequency on the internal clock's next rising edge of  $t_3$ . In order for an interrupt to be recognized, it must be valid before the internal clock's rising edge of  $t_3$ .

**Note:** Power-save operation requires that clock-dependent devices be reprogrammed for clock frequency changes. Software drivers must be aware of clock frequency.

## Initialization and Processor Reset

Processor initialization or startup is accomplished by driving the  $\overline{RES}$  input pin Low.  $\overline{RES}$  must be held Low for 1 ms during power-up to ensure proper device initialization.  $\overline{RES}$  forces the Am186EM and Am188EM microcontrollers to terminate all execution and local bus activity. No instruction or bus activity occurs as long as  $\overline{RES}$  is active.

After  $\overline{RES}$  becomes inactive and an internal processing interval elapses, the microcontroller begins execution with the instruction at physical location FFFF0h.  $\overline{RES}$  also sets some registers to predefined values.

## The Reset Configuration Register

When the  $\overline{RES}$  input is asserted Low, the contents of the address/data bus (AD15–AD0) are written into the Reset Configuration register. The system can place configuration information on the address/data bus using weak external pullup or pulldown resistors, or using an external driver that is enabled during reset. The processor does not drive the address/data bus during reset.

For example, the Reset Configuration register could be used to provide the software with the position of a configuration switch in the system. Using weak external pullup and pulldown resistors on the address and data bus, the system would provide the microcontroller with a value corresponding to the position of the jumper during a reset.

## CHIP-SELECT UNIT

The Am186EM and Am188EM microcontrollers contain logic that provides programmable chip-select generation for both memories and peripherals. The logic can be programmed to provide ready and wait-state generation and latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they are generated by the CPU or by the integrated DMA unit.

The Am186EM and Am188EM microcontrollers provide six chip-select outputs for use with memory devices and six more for use with peripherals in either memory space or I/O space. The six chip selects for memory devices can be used to address three memory ranges. Each of the six peripheral chip selects addresses a 256-byte block that is offset from a programmable base address. A read or write access to the corresponding chip select register activates the chip selects.

### Chip-Select Timing

The timing for the  $\overline{UCS}$  and  $\overline{LCS}$  outputs is modified from the original 80C186 microcontroller. These outputs now assert in conjunction with the nonmultiplexed address bus for normal memory timing. To allow these outputs to be available earlier in the bus cycle, the number of programmable memory size selections has been reduced.

### Ready and Wait-State Programming

The Am186EM and Am188EM microcontrollers can be programmed to sense a ready signal for each of the peripheral or memory chip-select lines. The ready signal can be either the ARDY or SRDY signal. Each chip-select control register (UMCS, LMCS, MMCS, PACS, and MPCS) contains a single-bit field that determines whether the external ready signal is required or ignored.

The number of wait states to be inserted for each access to a peripheral or memory region is programmable. The chip-select control registers for  $\overline{UCS}$ ,  $\overline{LCS}$ ,  $\overline{MCS3}$ – $\overline{MCS0}$ ,  $\overline{PCS6}$ , and  $\overline{PCS5}$  contain a two-bit field that determines the number of wait states from zero to three to be inserted.  $\overline{PCS3}$ – $\overline{PCS0}$  use three bits to provide additional values of 5, 7, 9, and 15 wait states.

When external ready is required, internally programmed wait states will always complete before external ready can terminate or extend a bus cycle. For example, if the internal wait states are set to insert two wait states, the processor samples the external ready pin during the first wait cycle. If external ready is asserted at that time, the access completes after six cycles (four cycles plus two wait states). If external ready is not asserted during the first wait state, the access is extended until ready is asserted, which is followed by one more wait state followed by  $t_4$ .

## Chip-Select Overlap

Although programming the various chip selects on the Am186EM and Am188EM microcontrollers so that multiple chip select signals are asserted for the same physical address is not recommended, it may be unavoidable in some systems. In such systems, the chip selects whose assertions overlap must have the same configuration for ready (external ready required or not required) and the number of wait states to be inserted into the cycle by the processor.

The peripheral control block (PCB) is accessed using internal signals. These internal signals function as chip selects configured with zero wait states and no external ready. Therefore, the PCB can be programmed to addresses that overlap external chip select signals if those external chip selects are programmed to zero wait states with no external ready required.

When overlapping an additional chip select with either the  $\overline{LCS}$  or  $\overline{UCS}$  chip selects, it must be noted that setting the Disable Address (DA) bit in the LMCS or UMCS register will disable the address from being driven on the AD bus for all accesses for which the associated chip select is asserted, including any accesses for which multiple chip selects assert.

The  $\overline{MCS}$  and  $\overline{PCS}$  chip select pins can be configured as either chip selects (normal function) or as PIO inputs or outputs. It should be noted; however, that the ready and wait state generation logic for these chip selects is in effect regardless of their configurations as chip selects or PIOs. This means that if these chip selects are enabled (by a read or write to the MMCS and MPCS for the  $\overline{MCS}$  chip selects, or by a read or write to the PACS and MPCS registers for the  $\overline{PCS}$  chip selects), the ready and wait state programming for these signals must agree with the programming for any other chip selects with which their assertion would overlap if they were configured as chip selects.

Although the  $\overline{PCS4}$  signal is not available on an external pin, the ready and wait state logic for this signal still exists internal to the part. For this reason, the  $\overline{PCS4}$  address space must follow the rules for overlapping chip selects. The ready and wait-state logic for  $\overline{PCS6}$ – $\overline{PCS5}$  is disabled when these signals are configured as address bits A2–A1.

Failure to configure overlapping chip selects with the same ready and wait state requirements may cause the processor to hang with the appearance of waiting for a ready signal. This behavior may occur even in a system in which ready is always asserted (ARDY or SRDY tied High).

Configuring  $\overline{PCS}$  in I/O space with  $\overline{LCS}$  or any other chip select configured for memory address 0 is not considered overlapping of the chip selects. Overlapping chip selects refers to configurations where more than one chip select asserts for the same physical address.

### Upper Memory Chip Select

The Am186EM and Am188EM microcontrollers provide a  $\overline{UCS}$  chip select for the top of memory. On reset, the Am186EM and Am188EM microcontrollers begin fetching and executing instructions starting at memory location FFFF0h. Therefore, upper memory is usually used as instruction memory. To facilitate this usage,  $\overline{UCS}$  defaults to active on reset, with a default memory range of 64 Kbytes from F0000h to FFFFFh, with external ready required and three wait states automatically inserted. The  $\overline{UCS}$  memory range always ends at FFFFFh. The lower boundary is programmable.

### Low Memory Chip Select

The Am186EM and Am188EM microcontrollers provide an  $\overline{LCS}$  chip select for the bottom of memory. Since the interrupt vector table is located at the bottom of memory starting at 00000h, the  $\overline{LCS}$  pin is usually used to control data memory. The  $\overline{LCS}$  pin is not active on reset.

### Midrange Memory Chip Selects

The Am186EM and Am188EM microcontrollers provide four chip selects,  $\overline{MCS3}$ – $\overline{MCS0}$ , for use in a user-locatable memory block. The base address of the memory block can be located anywhere within the 1-Mbyte memory address space, exclusive of the areas associated with the  $\overline{UCS}$  and  $\overline{LCS}$  chip selects, as well as the address range of the Peripheral Chip Selects,  $\overline{PCS6}$ ,  $\overline{PCS5}$ , and  $\overline{PCS3}$ – $\overline{PCS0}$ , if they are mapped to memory. The  $\overline{MCS}$  address range can overlap the  $\overline{PCS}$  address range if the  $\overline{PCS}$  chip selects are mapped to I/O space.

Unlike the  $\overline{UCS}$  and  $\overline{LCS}$  chip selects, the  $\overline{MCS}$  outputs assert with the multiplexed AD address bus.

### Peripheral Chip Selects

The Am186EM and Am188EM microcontrollers provide six chip selects,  $\overline{PCS6}$ – $\overline{PCS5}$  and  $\overline{PCS3}$ – $\overline{PCS0}$ , for use within a user-locatable memory or I/O block.  $\overline{PCS4}$  is not available on the Am186EM and Am188EM microcontrollers. The base address of the memory block can be located anywhere within the 1-Mbyte memory address space, exclusive of the areas associated with the  $\overline{UCS}$ ,  $\overline{LCS}$ , and  $\overline{MCS}$  chip selects, or they can be configured to access the 64 Kbyte I/O space.

The  $\overline{PCS}$  pins are not active on reset.  $\overline{PCS6}$ – $\overline{PCS5}$  can have from zero to three wait states.  $\overline{PCS3}$ – $\overline{PCS0}$  can have four additional wait-state values—5, 7, 9, and 15.

Unlike the  $\overline{UCS}$  and  $\overline{LCS}$  chip selects, the  $\overline{PCS}$  outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers.

## REFRESH CONTROL UNIT

The Refresh Control Unit (RCU) automatically generates refresh bus cycles. After a programmable period of time, the RCU generates a memory read request to the bus interface unit. The RCU is fixed to three wait states for the PSRAM auto refresh mode.

If the HLDA pin is active when a refresh request is generated (indicating a bus hold condition), then the Am186EM and Am188EM microcontrollers deactivate the HLDA pin in order to perform a refresh cycle. The external bus master must remove the HOLD signal for at least one clock in order to allow the refresh cycle to execute. The sequence of HLDA going inactive while HOLD is being held active can be used to signal a pending refresh request.

## INTERRUPT CONTROL UNIT

The Am186EM and Am188EM microcontrollers can receive interrupt requests from a variety of sources, both internal and external. The internal interrupt controller arranges these requests by priority and presents them one at a time to the CPU.

There are six external interrupt sources on the Am186EM and Am188EM microcontrollers—five maskable interrupt pins and one nonmaskable interrupt pin. In addition, there are six total internal interrupt sources—three timers, two DMA channels, and the asynchronous serial port—that are not connected to external pins.

The Am186EM and Am188EM microcontrollers provide three interrupt sources not present on the Am186 and Am188 microcontrollers. The first is an additional external interrupt pin (INT4). This pin operates much like the already existing interrupt pins (INT3–INT0). The second is an internal watchdog timer interrupt. The third is an internal interrupt from the asynchronous serial port.

The five maskable interrupt request pins can be used as direct interrupt requests, or they can be cascaded with an 82C59A-compatible external interrupt controller if more inputs are needed. An external interrupt controller can be used as the system master by programming the internal interrupt controller to operate in slave mode. In all cases, nesting can be enabled so that interrupt service routines for lower priority interrupts are interrupted by a higher priority interrupt.

## TIMER CONTROL UNIT

There are three 16-bit programmable timers in the Am186EM and Am188EM microcontrollers. Timer 0 and timer 1 are connected to four external pins (each one has an input and an output). These two timers can be used to count or time external events, or to generate nonrepetitive or variable-duty-cycle waveforms. In addition, timer 1 can be configured as a watchdog timer interrupt.

The watchdog timer interrupt provides a mechanism for detecting software crashes or hangs. The TMROUT1 output is internally connected to the watchdog timer interrupt. The TIMER1 count register must then be reloaded at intervals less than the TIMER1 max count to assure the watchdog interrupt is not taken. If the code crashes or hangs, the TIMER1 countdown will cause a watchdog interrupt.

Timer 2 is not connected to any external pins. It can be used for real-time coding and time-delay applications. It can also be used as a prescale to timers 0 and 1 or as a DMA request source.

The timers are controlled by eleven 16-bit registers in the peripheral control block. A timer's timer-count register contains the current value of that timer. The timer-count register can be read or written with a value at any time, regardless of whether the timer is running. The microcontroller increments the value of the timer-count register each time a timer event occurs.

Each timer also has a maximum-count register that defines the maximum value the timer will reach. When the timer reaches the maximum value, it resets to 0 during the same clock cycle—the value in the maximum-count register is never stored in the timer-count register. Also, timers 0 and 1 have a secondary maximum-count register. Using both the primary and secondary maximum-count registers lets the timer alternate between two maximum values.

If the timer is programmed to use only the primary maximum-count register, the timer output pin switches Low for one clock cycle after the maximum value is reached. If the timer is programmed to use both of its maximum-count registers, the output pin indicates which maximum-count register is currently in control, thereby creating a waveform. The duty cycle of the waveform depends on the values in the maximum-count registers.

Each timer is serviced every fourth clock cycle, so a timer can operate at a speed of up to one-quarter the internal clock frequency. A timer can be clocked externally at this same frequency; however, because of internal synchronization and pipelining of the timer circuitry, the timer output may take up to six clock cycles to respond to the clock or gate input.

## DIRECT MEMORY ACCESS (DMA)

Direct memory access (DMA) permits transfer of data between memory and peripherals without CPU involvement. The DMA unit in the Am186EM and Am188EM microcontrollers, shown in Figure 10, provides two high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., memory to I/O) or within the same space (e.g., memory-to-memory or I/O-to-I/O). In addition, either bytes or words can be transferred to or from even or odd addresses on the Am186EM microcontroller. The Am188EM microcontroller does not support word transfers. Only two bus cycles (a minimum of eight clocks) are necessary for each data transfer.

Each channel accepts a DMA request from one of three sources—the channel request pin (DRQ1–DRQ0), timer 2, or the system software. The channels can be programmed with different priorities in the event of a simultaneous DMA request or if there is a need to interrupt transfers on the other channel.

### DMA Operation

Each channel has six registers in the peripheral control block that define specific channel operations. The DMA registers consist of a 20-bit source address (2 registers), a 20-bit destination address (2 registers), a 16-bit transfer count register, and a 16-bit control register.

The DMA transfer count register (DTC) specifies the number of DMA transfers to be performed. Up to 64K byte or word transfers can be performed with automatic termination. The DMA control registers define the channel operation. All registers can be modified during any DMA activity. Any changes made to the DMA registers are reflected immediately in DMA operation.

**Table 6. Am186EM Microcontroller Maximum DMA Transfer Rates**

| Type of Synchronization Selected          | Maximum DMA Transfer Rate (Mbyte/s) |        |        |        |
|-------------------------------------------|-------------------------------------|--------|--------|--------|
|                                           | 40 MHz                              | 33 MHz | 25 MHz | 20 MHz |
| Unsynchronized                            | 10                                  | 8.25   | 6.25   | 5      |
| Source Synch                              | 10                                  | 8.25   | 6.25   | 5      |
| Destination Synch (CPU needs bus)         | 6.6                                 | 5.5    | 4.16   | 3.3    |
| Destination Synch (CPU does not need bus) | 8                                   | 6.6    | 5      | 4      |

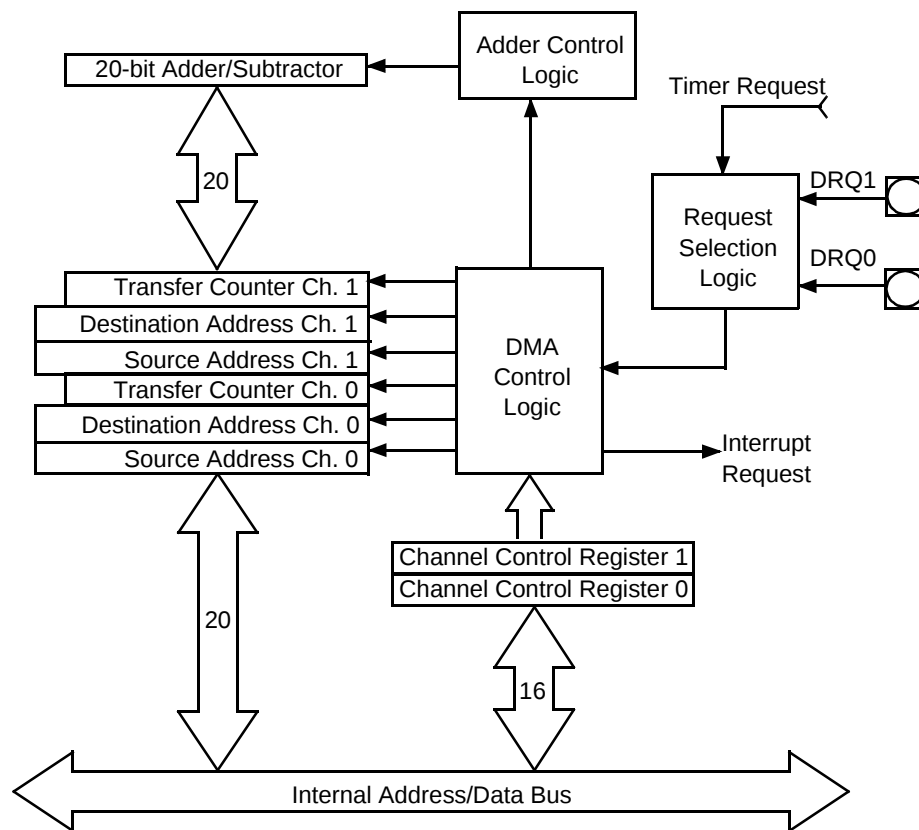


Figure 10. DMA Unit Block Diagram

### DMA Channel Control Registers

Each DMA control register determines the mode of operation for the particular DMA channel. This register specifies the following:

- The mode of synchronization
- Whether bytes or words are transferred
- If an interrupt is generated after the last transfer
- If DMA activity ceases after a programmed number of DMA cycles
- The relative priority of the DMA channel with respect to the other DMA channel
- Whether the source address is incremented, decremented, or maintained constant after each transfer
- Whether the source address addresses memory or I/O space
- Whether the destination address is incremented, decremented, or maintained constant after transfers
- Whether the destination address addresses memory or I/O space

### DMA Priority

The DMA channels can be programmed so that one channel is always given priority over the other, or they can be programmed to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles, except between locked memory accesses or word accesses to odd memory locations. However, an external bus hold takes priority over an internal DMA cycle.

Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time suffers during sequences of continuous DMA cycles. An NMI request, however, causes all internal DMA activity to halt. This allows the CPU to respond quickly to the NMI request.

## ASYNCHRONOUS SERIAL PORT

The Am186EM and Am188EM microcontrollers provide an asynchronous serial port. The asynchronous serial port is a two-pin interface that permits full-duplex bidirectional data transfer. The asynchronous serial port supports the following features:

- Full-duplex operation
- 7-bit or 8-bit data transfers
- Odd, even, or no parity
- 1 or 2 stop bits

If additional RS-232 signals are required, they can be created with available PIO pins. The asynchronous serial port transmit and receive sections are double buffered. Break character, framing, parity, and overrun error detection are provided. Exception interrupt generation is programmable by the user.

The transmit/receive clock is based on the internal processor clock, which is divided down internally to the serial port operating frequency. The serial port permits 7-bit and 8-bit data transfers. DMA transfers through the serial port are not supported.

The serial port generates one interrupt for any of three serial port events—transmit complete, data received, and error.

The serial port can be used in power-save mode, but the software must adjust the transfer rate to correctly reflect the new internal operating frequency and must ensure that the serial port does not receive any information while the frequency is being changed.

## SYNCHRONOUS SERIAL INTERFACE

The synchronous serial interface (SSI) lets the Am186EM and Am188EM microcontrollers communicate with application-specific integrated circuits (ASICs) that require reprogrammability but are short on pins. This four-pin interface permits half-duplex, bidirectional data transfer at speeds of up to 20 Mbits/sec.

Unlike the asynchronous serial port, the SSI operates in a master/slave configuration. The Am186EM and Am188EM microcontrollers are the master port.

The SSI interface provides four pins for communicating with system components: two enables (SDEN0 and SDEN1), a clock (SCLK), and a data pin (SDATA). Five registers are used to control and monitor the interface.

### Four-Pin Interface

The two enable pins SDEN1–SDEN0 can be used directly as enables for up to two peripheral devices.

Transmit and receive operations are synchronized between the master (Am186EM and Am188EM microcontrollers) and slave (peripheral) by means of the SCLK output. SCLK is derived from the internal processor clock and is the processor clock divided by 2, 4, 8, or 16.

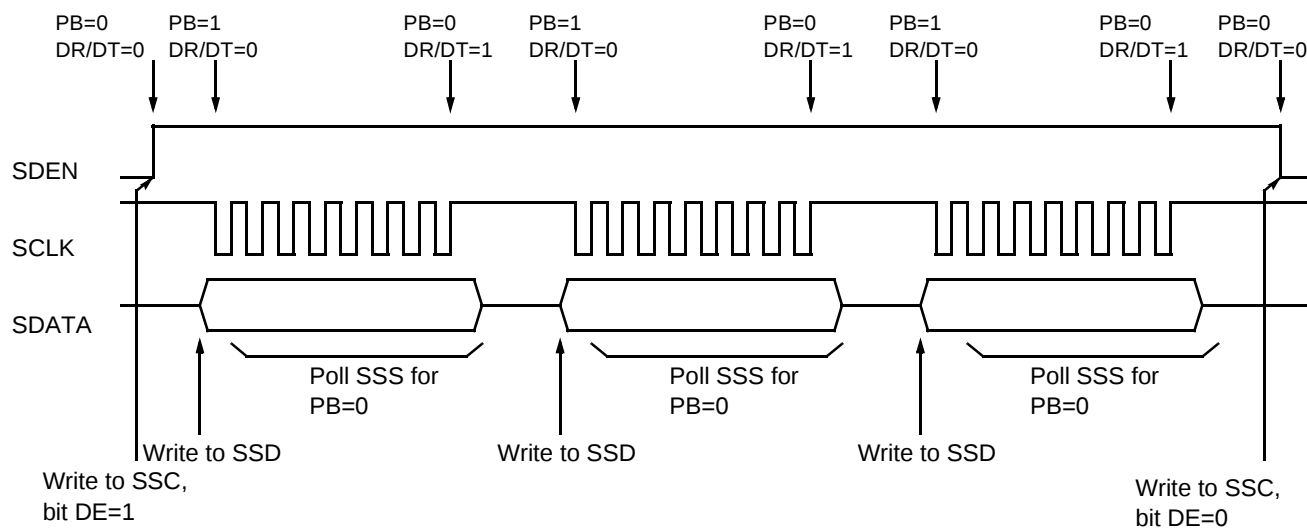


Figure 11. Synchronous Serial Interface Multiple Write

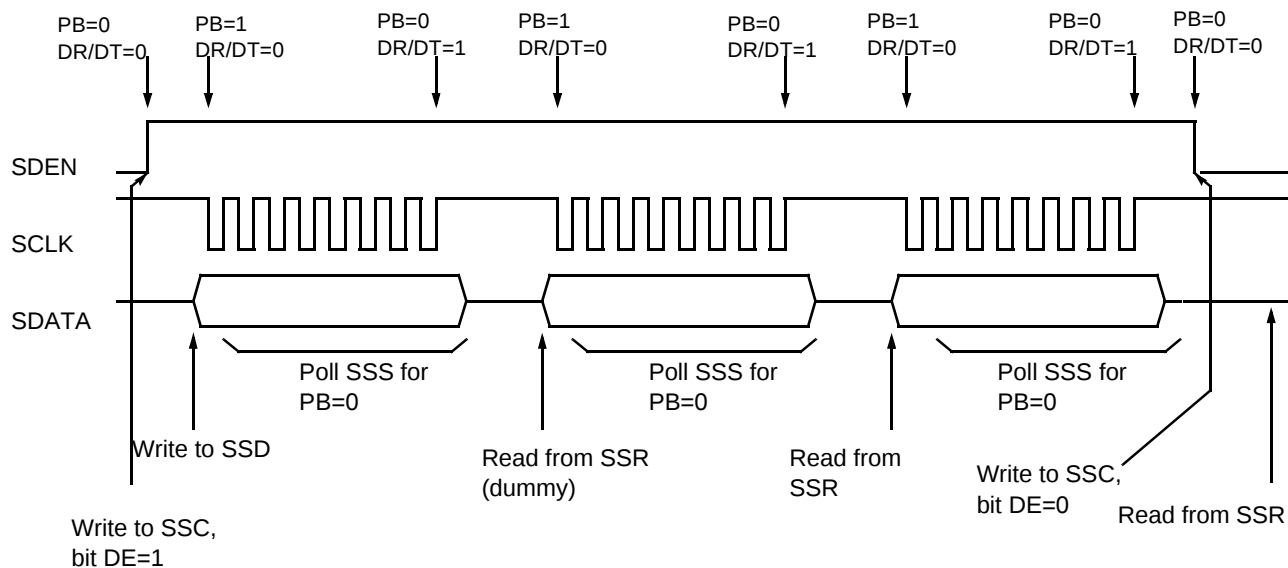


Figure 12. Synchronous Serial Interface Multiple Read

## PROGRAMMABLE I/O (PIO) PINS

There are 32 pins on the Am186EM and Am188EM microcontrollers that are available as user multipurpose signals. Table 2 and Table 3 on page 30 list the PIO pins. Each of these pins can be used as a user-programmable input or output signal if the normal shared function is not needed.

If a pin is enabled to function as a PIO signal, the pre-assigned signal function is disabled and does not affect the level on the pin. A PIO signal can be configured to operate as an input or output with or without a weak pullup or pulldown, or as an open-drain output.

After power-on reset, the PIO pins default to various configurations. The column titled *Power-On Reset Status* in Table 2 and Table 3 on page 30 lists the defaults for the PIOs. The system initialization code must reconfigure the PIOs as required.

The A19–A17 address pins default to normal operation on power-on reset, allowing the processor to correctly begin fetching instructions at the boot address FFFF0h. The DT/ $\overline{R}$ ,  $\overline{DEN}$ , and SRDY pins also default to normal operation on power-on reset.

Note that emulators use A19, A18, A17, S6, and  $\overline{UZI}$ .

If the AD15–AD0 bus override is enabled on power-on reset, then S6/ $\overline{CLKDIV2}$  and  $\overline{UZI}$  revert to normal operation instead of PIO input with pullup. If  $\overline{BHE/ADEN}$  (186) or  $\overline{RFSH2/ADEN}$  (188) is held Low during power-on reset the AD15–AD0 bus override is enabled.

**ABSOLUTE MAXIMUM RATINGS****Storage temperature**

Am186EM/Am188EM ..... -65°C to +125°C

Am186EMLV/Am188EMLV ..... -65°C to +125°C

**Voltage on any pin with respect to ground**Am186/188EM ..... -0.5 V to  $V_{CC} + 0.5$  VAm186/188EMLV ..... -0.5 V to  $V_{CC} + 0.5$  V

**Note:** Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**OPERATING RANGES**

Operating Ranges define those limits between which

the functionality of the device is guaranteed.

**Am186EM/Am188EM Microcontrollers**Commercial ( $T_C$ ) ..... 0°C to +100°CIndustrial\* ( $T_A$ ) ..... -40°C to +85°C $V_{CC}$  up to 33 MHz ..... 5 V  $\pm$  10% $V_{CC}$  greater than 33 MHz ..... 5 V  $\pm$  5%**Am186EMLV/Am188EMLV Microcontrollers**Commercial ( $T_A$ ) ..... 0°C to +70°C $V_{CC}$  up to 25 MHz ..... 3.3 V  $\pm$  0.3 VWhere:  $T_C$  = case temperature $T_A$  = ambient temperature

\*Industrial versions of Am186EM and Am188EM microcontrollers are available in 20 and 25 MHz operating frequencies only.

**DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE**

| Symbol    | Parameter Description                               | Test Conditions                                                   | Preliminary    |                | Unit       |
|-----------|-----------------------------------------------------|-------------------------------------------------------------------|----------------|----------------|------------|
|           |                                                     |                                                                   | Min            | Max            |            |
| $V_{IL}$  | Input Low Voltage (Except X1)                       |                                                                   | -0.5           | 0.8            | V          |
| $V_{IL1}$ | Clock Input Low Voltage (X1)                        |                                                                   | -0.5           | 0.8            | V          |
| $V_{IH}$  | Input High Voltage (Except $\overline{RES}$ and X1) |                                                                   | 2.0            | $V_{CC} + 0.5$ | V          |
| $V_{IH1}$ | Input High Voltage ( $\overline{RES}$ )             |                                                                   | 2.4            | $V_{CC} + 0.5$ | V          |
| $V_{IH2}$ | Clock Input High Voltage (X1)                       |                                                                   | $V_{CC} - 0.8$ | $V_{CC} + 0.5$ | V          |
| $V_{OL}$  | <b>Output Low Voltage</b>                           |                                                                   |                |                |            |
|           | Am186EM and Am188EM                                 | $I_{OL} = 2.5$ mA ( $S_2$ - $S_0$ )<br>$I_{OL} = 2.0$ mA (others) |                | 0.45           | V          |
|           | Am186EMLV and Am188EMLV                             | $I_{OL} = 1.5$ mA ( $S_2$ - $S_0$ )<br>$I_{OL} = 1.0$ mA (others) |                | 0.45           | V          |
| $V_{OH}$  | <b>Output High Voltage<sup>(a)</sup></b>            |                                                                   |                |                |            |
|           | Am186EM and Am188EM                                 | $I_{OH} = -2.4$ mA @ 2.4 V                                        | 2.4            | $V_{CC} + 0.5$ | V          |
|           |                                                     | $I_{OH} = -200$ $\mu$ A @ $V_{CC} - 0.5$                          | $V_{CC} - 0.5$ | $V_{CC}$       | V          |
|           | Am186EMLV and Am188EMLV                             | $I_{OH} = -200$ $\mu$ A @ $V_{CC} - 0.5$                          | $V_{CC} - 0.5$ | $V_{CC}$       | V          |
| $I_{CC}$  | <b>Power Supply Current @ 0°C</b>                   |                                                                   |                |                |            |
|           | Am186EM and Am188EM                                 | $V_{CC} = 5.5$ V <sup>(b)</sup>                                   |                | 5.9            | mA/<br>MHz |
|           | Am186EMLV and Am188EMLV                             | $V_{CC} = 3.6$ V <sup>(b)</sup>                                   |                | 2.75           | mA/<br>MHz |
| $V_{OL}$  | Output Low Voltage                                  | $I_{OL} = 2.5$ mA ( $S_2$ - $S_0$ )<br>$I_{OL} = 2.0$ mA (others) |                | 0.45           | V          |
| $I_{LI}$  | Input Leakage Current @ 0.5 MHz                     | $0.45$ V $\leq V_{IN} \leq V_{CC}$                                |                | $\pm 10$       | $\mu$ A    |
| $I_{LO}$  | Output Leakage Current @ 0.5 MHz                    | $0.45$ V $\leq V_{OUT} \leq V_{CC}$ <sup>(d)</sup>                |                | $\pm 10$       | $\mu$ A    |
| $V_{CLO}$ | Clock Output Low                                    | $I_{CLO} = 4.0$ mA                                                |                | 0.45           | V          |
| $V_{CHO}$ | Clock Output High                                   | $I_{CHO} = -500$ $\mu$ A                                          | $V_{CC} - 0.5$ |                | V          |

**Notes:**

a The  $\overline{LCS}/\overline{ONCE0}$ ,  $\overline{MCS3}$ - $\overline{MCS0}$ ,  $\overline{UCS}/\overline{ONCE1}$ , and  $\overline{RD}$  pins have weak internal pullup resistors. Loading the  $\overline{LCS}/\overline{ONCE0}$  and  $\overline{UCS}/\overline{ONCE1}$  pins in excess of  $I_{OH} = -200$   $\mu$ A during reset can cause the device to go into ONCE mode.

b Current is measured with the device in RESET with X1 and X2 driven, and all other non-power pins open but held High or Low.

c Power supply current for the Am186EMLV and Am188EMLV microcontrollers, which are available in 20 and 25 MHz operating frequencies only.

d Testing is performed with the pins floating, either during HOLD or by invoking the ONCE mode.

## DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE (continued)

| Symbol           | Parameter Description                                       | Test Conditions                   | Preliminary | Unit       |
|------------------|-------------------------------------------------------------|-----------------------------------|-------------|------------|
|                  |                                                             |                                   | Typical     |            |
| Nominal $I_{CC}$ | Typical Power Supply Current @ 25°C                         | $V_{CC} = 5.5\text{ V}^{(a)}$     | 4.5         | mA/<br>MHz |
| Nominal $I_{CC}$ | Am186EMLV and Am188EMLV Typical Power Supply Current @ 25°C | $V_{CC} = 3.6\text{ V}^{(a) (b)}$ | 3.0         | mA/<br>MHz |
| Peak $I_{CC}$    | Measured Peak $I_{CC}$                                      | $V_{CC} = 5.5\text{ V}^{(c)}$     | 5.9         | mA/<br>MHz |
| Peak $I_{CC}$    | Am186EMLV and Am188EMLV Measured Peak $I_{CC}$              | $V_{CC} = 3.6\text{ V}^{(b) (c)}$ | 4.0         | mA/<br>MHz |

*a Measured with a device running. Not tested and not guaranteed.*

*b Power supply current for the Am186EMLV and Am188EMLV microcontrollers, which are available in 20 and 25 MHz operating frequencies only.*

*c Power is measured while device is operating. Not tested and not guaranteed.*

## Capacitance

| Symbol   | Parameter Description     | Test Conditions | Preliminary |     | Unit |
|----------|---------------------------|-----------------|-------------|-----|------|
|          |                           |                 | Min         | Max |      |
| $C_{IN}$ | Input Capacitance         | @ 1 MHz         |             | 10  | pF   |
| $C_{IO}$ | Output or I/O Capacitance | @ 1 MHz         |             | 20  | pF   |

**Note:**

*Capacitance limits are guaranteed by characterization.*

## Power Supply Current

For the typical system specification shown in Figure 13,  $I_{CC}$  has been measured at 3.0 mA per MHz of system clock. For the typical system specification shown in Figure 14,  $I_{CC}$  has been measured at 4.5 mA per MHz of system clock. The typical system is measured while the system is executing code in a typical application with maximum voltage and at room temperature. Actual power supply current is dependent on system design and may be greater or less than the typical  $I_{CC}$  figure presented here.

Typical current in Figure 13 is given by:

.....  $I_{CC} = 3.0 \text{ mA} \cdot \text{freq}(\text{MHz})$ .

Typical current in Figure 14 is given by:

.....  $I_{CC} = 4.5 \text{ mA} \cdot \text{freq}(\text{MHz})$ .

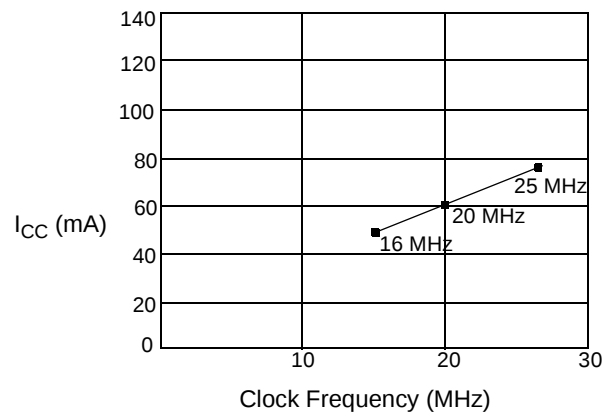
Please note that dynamic  $I_{CC}$  measurements are dependent upon chip activity, operating frequency, output buffer logic, and capacitive/resistive loading of the outputs. For these  $I_{CC}$  measurements, the devices were set to the following modes:

- No DC loads on the output buffers
- Output capacitive load set to 35 pF
- AD bus set to data only
- PIOs are disabled
- Timer, serial port, refresh, and DMA are enabled

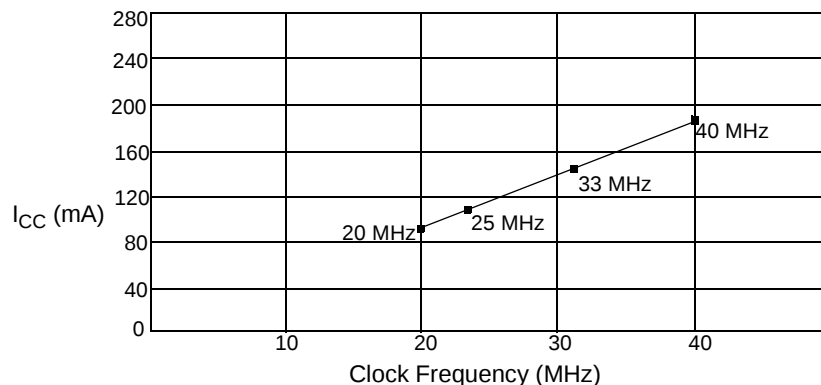
Table 7 shows the variables that are used to calculate the typical power consumption value for each version of the Am186EMLV and Am188EMLV microcontrollers.

**Table 7. Typical Power Consumption Calculation for the Am186EMLV and Am188EMLV**

| $\text{MHz} \cdot I_{CC} \cdot \text{Volts} / 1000 = P$ |                  |       | Typical Power<br>in Watts |
|---------------------------------------------------------|------------------|-------|---------------------------|
| MHz                                                     | Typical $I_{CC}$ | Volts |                           |
| 16                                                      | 3.0              | 3.6   | 0.173                     |
| 20                                                      | 3.0              | 3.6   | 0.216                     |
| 25                                                      | 3.0              | 3.6   | 0.270                     |



**Figure 13. Typical  $I_{CC}$  Versus Frequency for the Am186EMLV and Am188EMLV**



**Figure 14. Typical  $I_{CC}$  Versus Frequency for the Am186EM and Am188EM**

## THERMAL CHARACTERISTICS

### TQFP Package

The Am186EM and Am188EM microcontrollers are specified for operation with case temperature ranges from 0°C to +100°C for a commercial temperature device. Case temperature is measured at the top center of the package as shown in Figure 15. The various temperatures and thermal resistances can be determined using the equations in Figure 16 with information given in Table 8.

$\theta_{JA}$  is the sum of  $\theta_{JC}$  and  $\theta_{CA}$ .  $\theta_{JC}$  is the internal thermal resistance of the assembly.  $\theta_{CA}$  is the case to ambient thermal resistance.

The variable P is power in watts. Typical power supply current ( $I_{CC}$ ) for the Am186EM and Am188EM microcontrollers is 5.9 mA per MHz of clock frequency.

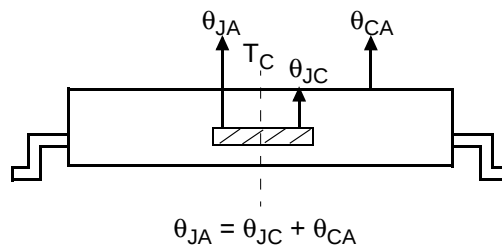


Figure 15. Thermal Resistance(°C/Watt)

$$\begin{aligned}\theta_{JA} &= \theta_{JC} + \theta_{CA} \\ P &= 5.9 \text{ mA} \cdot \text{freq (MHz)} \cdot V_{CC} \\ T_J &= T_C + (P \cdot \theta_{JC}) \\ T_J &= T_A + (P \cdot \theta_{JA}) \\ T_C &= T_J - (P \cdot \theta_{JC}) \\ T_C &= T_A + (P \cdot \theta_{CA}) \\ T_A &= T_J - (P \cdot \theta_{JA}) \\ T_A &= T_C - (P \cdot \theta_{CA})\end{aligned}$$

Figure 16. Thermal Characteristics Equations

Table 8. Thermal Characteristics (°C/Watt)

| Package/Board              | Airflow<br>(Linear Feet<br>per Minute) | $\theta_{JC}$ | $\theta_{CA}$ | $\theta_{JA}$ |
|----------------------------|----------------------------------------|---------------|---------------|---------------|
| PQFP/2-Layer               | 0 fpm                                  | 7             | 38            | 45            |
|                            | 200 fpm                                | 7             | 32            | 39            |
|                            | 400 fpm                                | 7             | 28            | 35            |
|                            | 600 fpm                                | 7             | 26            | 33            |
| TQFP/2-Layer               | 0 fpm                                  | 10            | 46            | 56            |
|                            | 200 fpm                                | 10            | 36            | 46            |
|                            | 400 fpm                                | 10            | 30            | 40            |
|                            | 600 fpm                                | 10            | 28            | 38            |
| PQFP/4-Layer<br>to 6-Layer | 0 fpm                                  | 5             | 18            | 23            |
|                            | 200 fpm                                | 5             | 16            | 21            |
|                            | 400 fpm                                | 5             | 14            | 19            |
|                            | 600 fpm                                | 5             | 12            | 17            |
| TQFP/4-Layer<br>to 6-Layer | 0 fpm                                  | 6             | 24            | 30            |
|                            | 200 fpm                                | 6             | 22            | 28            |
|                            | 400 fpm                                | 6             | 20            | 26            |
|                            | 600 fpm                                | 6             | 18            | 24            |

## Typical Ambient Temperatures

The typical ambient temperature specifications are based on the following assumptions and calculations:

The commercial operating range of the Am186EM and Am188EM microcontrollers is a case temperature  $T_C$  of 0 to 100 degrees Centigrade.  $T_C$  is measured at the top center of the package. An increase in the ambient temperature causes a proportional increase in  $T_C$ .

The 40-MHz microcontroller is specified as 5.0 V, plus or minus 5%. Therefore, 5.25 V is used for calculating typical power consumption on the 40-MHz microcontroller.

Microcontrollers up to 33 MHz are specified as 5.0 V, plus or minus 10%. Therefore, 5.5 V is used for calculating typical power consumption up to 33 MHz.

Typical power supply current ( $I_{CC}$ ) in normal usage is estimated at 5.9 mA per MHz of microcontroller clock rate.

Typical power consumption (watts) = (5.9 mA/MHz) times microcontroller clock rate times voltage divided by 1000.

Table 9 shows the variables that are used to calculate the typical power consumption value for each version of the Am186EM and Am188EM microcontrollers.

**Table 9. Typical Power Consumption Calculation**

| $P = \text{MHz} \cdot I_{CC} \cdot \text{Volts} / 1000$ |                  |       | Typical Power (P) in Watts |
|---------------------------------------------------------|------------------|-------|----------------------------|
| MHz                                                     | Typical $I_{CC}$ | Volts |                            |
| 40                                                      | 5.9              | 5.25  | 1.239                      |
| 33                                                      | 5.9              | 5.5   | 1.07085                    |
| 25                                                      | 5.9              | 5.5   | 0.81125                    |
| 20                                                      | 5.9              | 5.5   | 0.649                      |

Thermal resistance is a measure of the ability of a package to remove heat from a semiconductor device. A safe operating range for the device can be calculated using the following formulas from Figure 16 and the variables in Table 8.

By using the maximum case rating  $T_C$ , the typical power consumption value from Table 9, and  $\theta_{JC}$  from Table 8, the junction temperature  $T_J$  can be calculated by using the following formula from Figure 16.

$$T_J = T_C + (P \cdot \theta_{JC})$$

Table 10 shows  $T_J$  values for the various versions of the Am186EM and Am188EM microcontrollers. The column titled *Speed/Pkg/Board* in Table 10 indicates the clock speed in MHz, the type of package (P for PQFP and T for TQFP), and the type of board (2 for 2-layer and 4–6 for 4-layer to 6-layer).

**Table 10. Junction Temperature Calculation**

| Speed/<br>Pkg/<br>Board | $T_J = T_C + (P \cdot \theta_{JC})$ |         |               | $T_J$ |
|-------------------------|-------------------------------------|---------|---------------|-------|
|                         | $T_C$                               | P       | $\theta_{JC}$ |       |
| 40/P2                   | 100                                 | 1.239   | 7             | 108.7 |
| 40/T2                   | 100                                 | 1.239   | 10            | 112.4 |
| 40/P4–6                 | 100                                 | 1.239   | 5             | 106.2 |
| 40/T4–6                 | 100                                 | 1.239   | 6             | 107.4 |
| 33/P2                   | 100                                 | 1.07085 | 7             | 107.5 |
| 33/T2                   | 100                                 | 1.07085 | 10            | 110.7 |
| 33/P4–6                 | 100                                 | 1.07085 | 5             | 105.3 |
| 33/T4–6                 | 100                                 | 1.07085 | 6             | 106.4 |
| 25/P2                   | 100                                 | 0.81125 | 7             | 105.7 |
| 25/T2                   | 100                                 | 0.81125 | 10            | 108.1 |
| 25/P4–6                 | 100                                 | 0.81125 | 5             | 104.1 |
| 25/T4–6                 | 100                                 | 0.81125 | 6             | 104.9 |
| 20/P2                   | 100                                 | 0.649   | 7             | 104.5 |
| 20/T2                   | 100                                 | 0.649   | 10            | 106.5 |
| 20/P4–6                 | 100                                 | 0.649   | 5             | 103.2 |
| 20/T4–6                 | 100                                 | 0.649   | 6             | 103.9 |

By using  $T_J$  from Table 10, the typical power consumption value from Table 9, and a  $\theta_{JA}$  value from Table 8, the typical ambient temperature  $T_A$  can be calculated using the following formula from Figure 16.

$$T_A = T_J - (P \cdot \theta_{JA})$$

For example,  $T_A$  for a 40-MHz PQFP design with a 2-layer board and 0 fpm airflow is calculated as follows:

$$T_A = 108.673 - (1.239 \cdot 45)$$

$$T_A = 52.918$$

In this calculation,  $T_J$  comes from Table 10, P comes from Table 9, and  $\theta_{JA}$  comes from Table 8. See Table 11.

$T_A$  for a 33-MHz TQFP design with a 4-layer to 6-layer board and 200 fpm airflow is calculated as follows:

$$T_A = 106.4251 - (1.07085 \cdot 28)$$

$$T_A = 76.4413$$

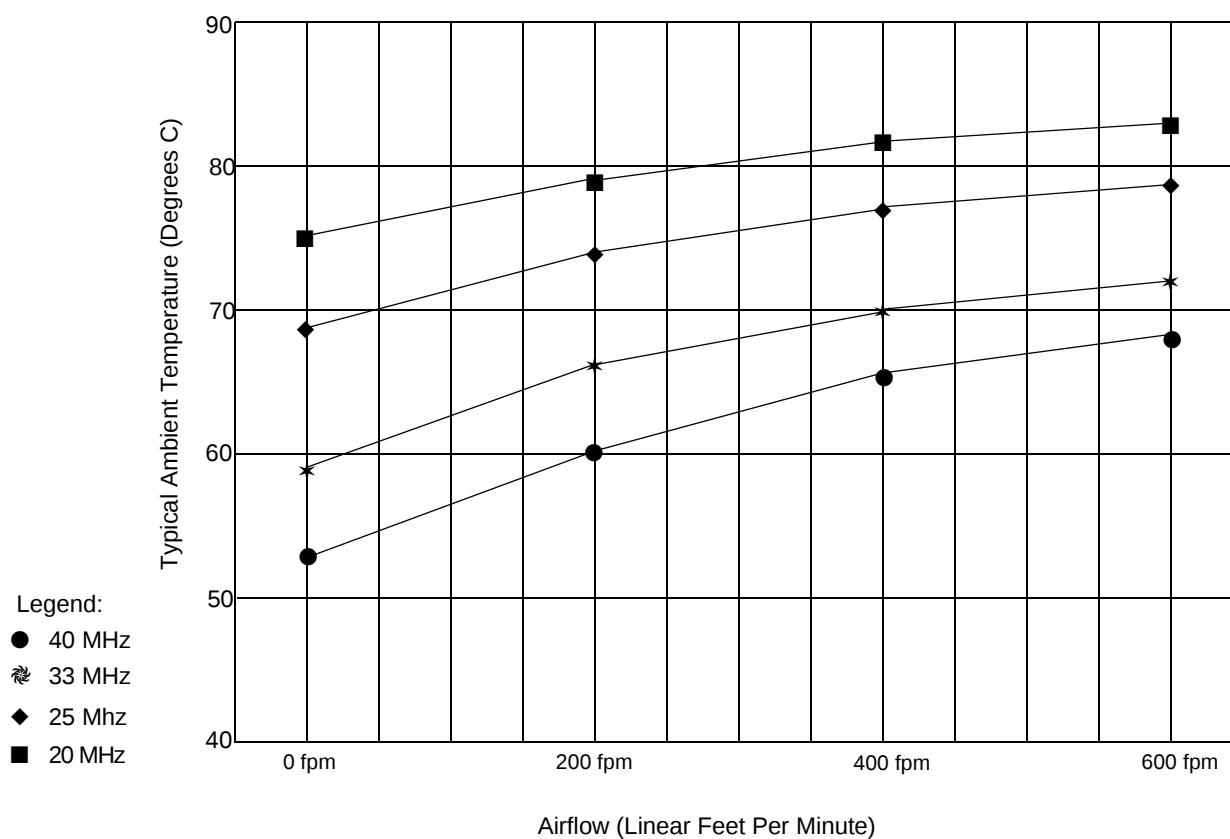
See Table 14 for the result of this calculation.

Table 11 through Table 14 and Figure 17 through Figure 20 show  $T_A$  based on the preceding assumptions and calculations for a range of  $\theta_{JA}$  values with airflow from 0 linear feet per minute to 600 linear feet per minute.

Table 11 shows typical maximum ambient temperatures in degrees Centigrade for a PQFP package used with a 2-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 17 illustrates the typical temperatures in Table 11.

**Table 11. Typical Ambient Temperatures for PQFP with 2-Layer Board**

| Microcontroller Speed | Typical Power (Watts) | Linear Feet per Minute Airflow |         |         |         |
|-----------------------|-----------------------|--------------------------------|---------|---------|---------|
|                       |                       | 0 fpm                          | 200 fpm | 400 fpm | 600 fpm |
| 40 MHz                | 1.239                 | 52.918                         | 60.352  | 65.308  | 67.786  |
| 33 MHz                | 1.07085               | 59.3077                        | 65.7328 | 70.0162 | 72.1579 |
| 25 MHz                | 0.81125               | 69.1725                        | 74.04   | 77.285  | 78.9075 |
| 20 MHz                | 0.649                 | 75.338                         | 79.232  | 81.828  | 83.126  |

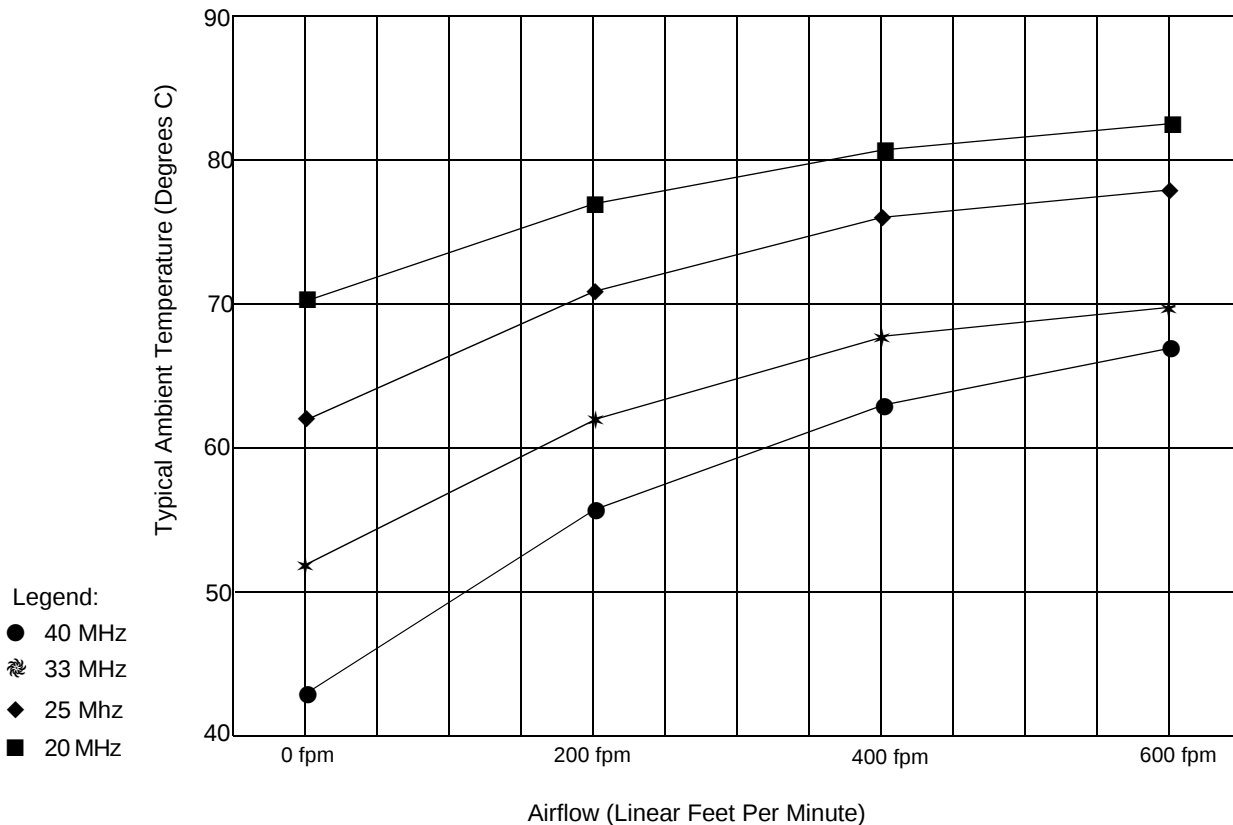


**Figure 17. Typical Ambient Temperatures for PQFP with 2-Layer Board**

Table 12 shows typical maximum ambient temperatures in degrees Centigrade for a TQFP package used with a 2-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 18 illustrates the typical temperatures in Table 12.

**Table 12. Typical Ambient Temperatures for TQFP with 2-Layer Board**

| Microcontroller Speed | Typical Power (Watts) | Linear Feet per Minute Airflow |         |         |         |
|-----------------------|-----------------------|--------------------------------|---------|---------|---------|
|                       |                       | 0 fpm                          | 200 fpm | 400 fpm | 600 fpm |
| 40 MHz                | 1.239                 | 43.006                         | 55.396  | 62.83   | 65.308  |
| 33 MHz                | 1.07085               | 50.7409                        | 61.4494 | 67.8745 | 70.0162 |
| 25 MHz                | 0.81125               | 62.6825                        | 70.795  | 75.6625 | 77.285  |
| 20 MHz                | 0.649                 | 70.146                         | 76.636  | 80.53   | 81.828  |

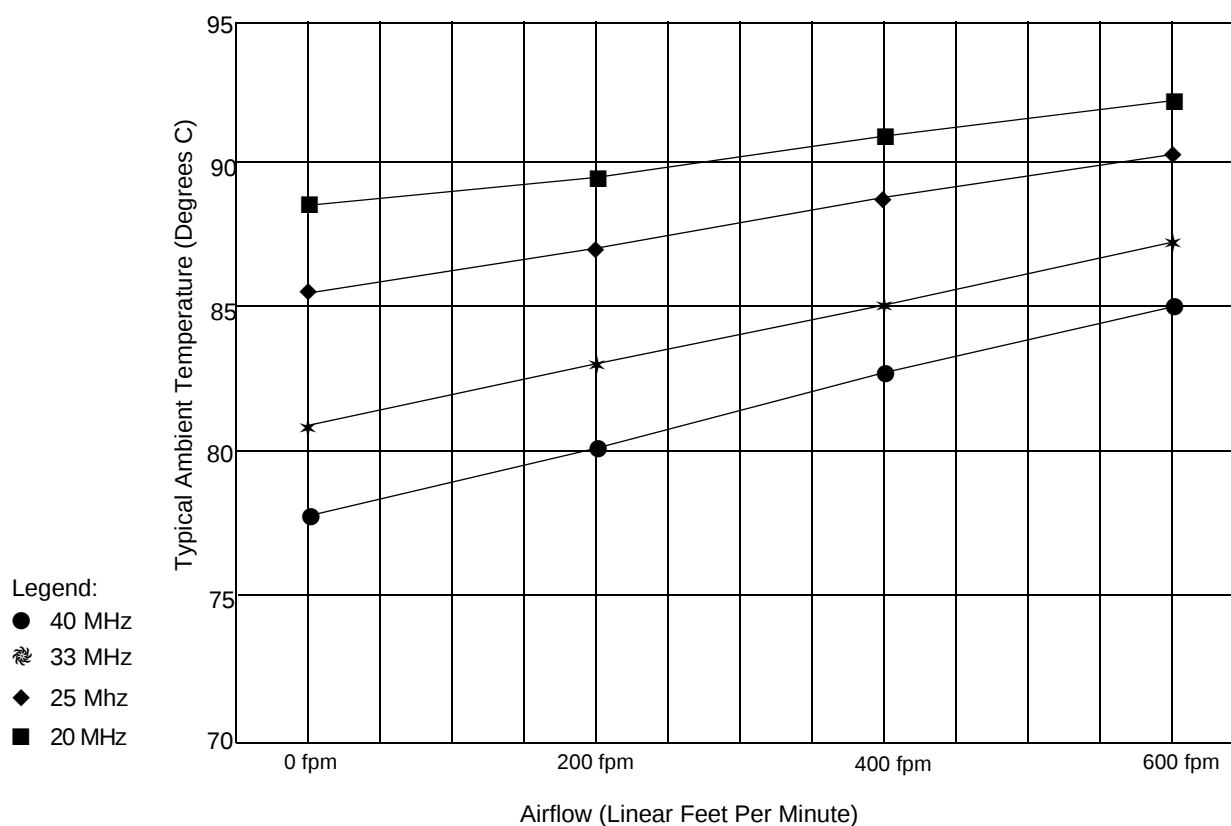


**Figure 18. Typical Ambient Temperatures for TQFP with 2-Layer Board**

Table 13 shows typical maximum ambient temperatures in degrees Centigrade for a PQFP package used with a 4-layer to 6-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 19 illustrates the typical temperatures in Table 13.

**Table 13. Typical Ambient Temperatures for PQFP with 4-Layer to 6-Layer Board**

| Microcontroller Speed | Typical Power (Watts) | Linear Feet per Minute Airflow |         |         |         |
|-----------------------|-----------------------|--------------------------------|---------|---------|---------|
|                       |                       | 0 fpm                          | 200 fpm | 400 fpm | 600 fpm |
| 40 MHz                | 1.239                 | 77.698                         | 80.176  | 82.654  | 85.132  |
| 33 MHz                | 1.07085               | 80.7247                        | 82.8664 | 85.0081 | 87.1498 |
| 25 MHz                | 0.81125               | 85.3975                        | 87.02   | 88.6425 | 90.265  |
| 20 MHz                | 0.649                 | 88.318                         | 89.616  | 90.914  | 92.212  |

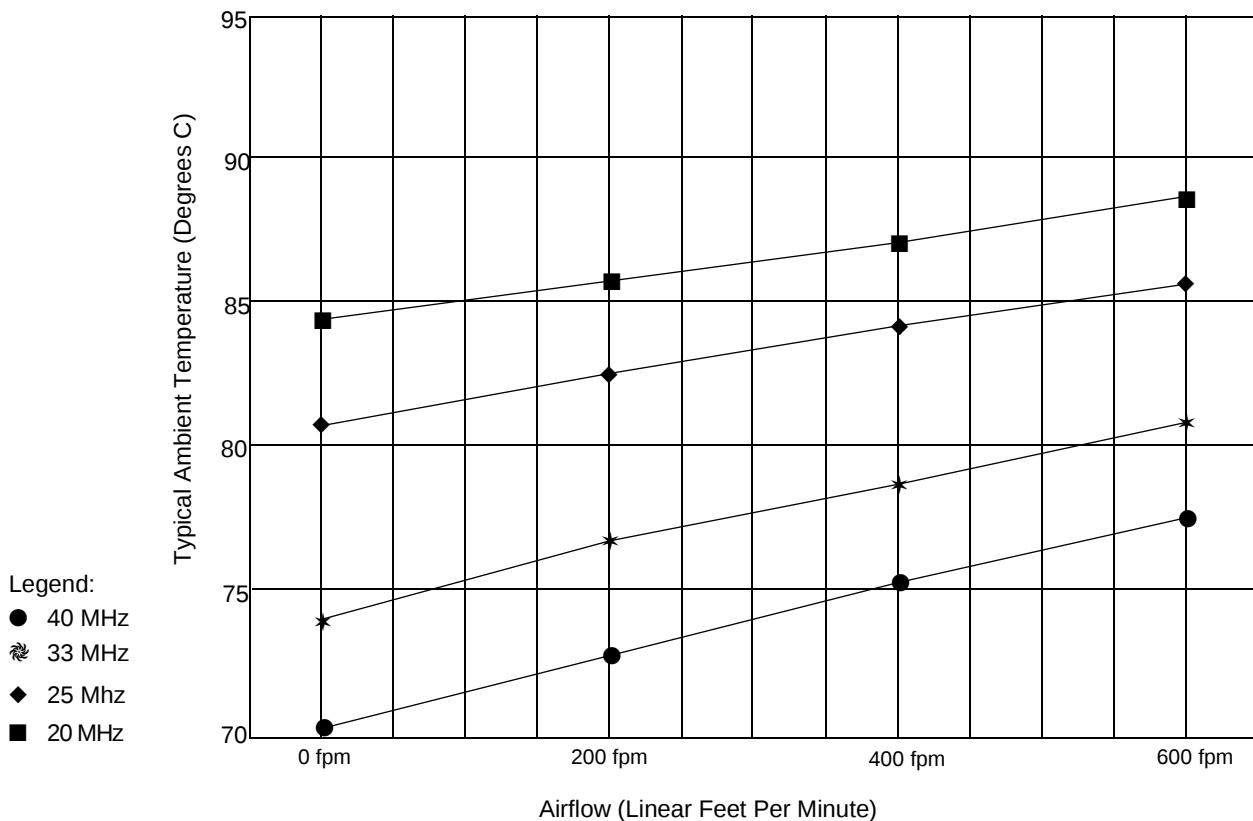


**Figure 19. Typical Ambient Temperatures for PQFP with 4-Layer to 6-Layer Board**

Table 14 shows typical maximum ambient temperatures in degrees Centigrade for a TQFP package used with a 4-layer to 6-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 20 illustrates the typical temperatures in Table 14.

**Table 14. Typical Ambient Temperatures for TQFP with 4-Layer to 6-Layer Board**

| Microcontroller Speed | Typical Power (Watts) | Linear Feet per Minute Airflow |         |         |         |
|-----------------------|-----------------------|--------------------------------|---------|---------|---------|
|                       |                       | 0 fpm                          | 200 fpm | 400 fpm | 600 fpm |
| 40 MHz                | 1.239                 | 70.264                         | 72.742  | 75.22   | 77.698  |
| 33 MHz                | 1.07085               | 74.2996                        | 76.4413 | 78.583  | 80.7247 |
| 25 MHz                | 0.81125               | 80.53                          | 82.1525 | 83.775  | 85.3975 |
| 20 MHz                | 0.649                 | 84.424                         | 85.722  | 87.02   | 88.318  |



**Figure 20. Typical Ambient Temperatures for TQFP with 4-Layer to 6-Layer Board**

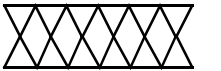
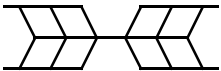
COMMERCIAL SWITCHING CHARACTERISTICS AND WAVEFORMS

In the switching waveforms that follow, several abbreviations are used to indicate the specific periods of a bus cycle. These periods are referred to as time states. A typical bus cycle is composed of four consecutive time states:  $t_1$ ,  $t_2$ ,  $t_3$ , and  $t_4$ . Wait states, which represent

multiple  $t_3$  states, are referred to as  $t_w$  states. When no bus cycle is pending, an idle ( $t_i$ ) state occurs.

In the switching parameter descriptions, the *multiplexed* address is referred to as the AD address bus; the *demultiplexed* address is referred to as the A address bus.

Key to Switching Waveforms

| WAVEFORM                                                                            | INPUT                            | OUTPUT                                  |
|-------------------------------------------------------------------------------------|----------------------------------|-----------------------------------------|
|    | Must be Steady                   | Will be Steady                          |
|    | May Change from H to L           | Will be Changing from H to L            |
|    | May Change from L to H           | Will be Changing from L to H            |
|   | Don't Care, Any Change Permitted | Changing, State Unknown                 |
|  | Does Not Apply                   | Center Line is High-Impedance Off State |
|  | Invalid                          | Invalid                                 |

## Alphabetical Key to Switching Parameter Symbols

| Parameter Symbol | No. | Description                                                | Parameter Symbol | No. | Description                                                 |
|------------------|-----|------------------------------------------------------------|------------------|-----|-------------------------------------------------------------|
| $t_{ARYCH}$      | 49  | ARDY Resolution Transition Setup Time                      | $t_{CLDX}$       | 2   | Data in Hold                                                |
| $t_{ARYCHL}$     | 51  | ARDY Inactive Holding Time                                 | $t_{CLEV}$       | 71  | CLKOUTA Low to SDEN Valid                                   |
| $t_{ARYLCL}$     | 52  | ARDY Setup Time                                            | $t_{CLHAV}$      | 62  | HLDA Valid Delay                                            |
| $t_{AVBL}$       | 87  | A Address Valid to $\overline{WHB}$ , $\overline{WLB}$ Low | $t_{CLRF}$       | 82  | CLKOUTA High to $\overline{RFSH}$ Invalid                   |
| $t_{AVCH}$       | 14  | AD Address Valid to Clock High                             | $t_{CLRH}$       | 27  | $\overline{RD}$ Inactive Delay                              |
| $t_{AVLL}$       | 12  | AD Address Valid to ALE Low                                | $t_{CLRL}$       | 25  | $\overline{RD}$ Active Delay                                |
| $t_{AVRL}$       | 66  | A Address Valid to $\overline{RD}$ Low                     | $t_{CLSH}$       | 4   | Status Inactive Delay                                       |
| $t_{AVWL}$       | 65  | A Address Valid to $\overline{WR}$ Low                     | $t_{CLSL}$       | 72  | CLKOUTA Low to SCLK Low                                     |
| $t_{AZRL}$       | 24  | AD Address Float to $\overline{RD}$ Active                 | $t_{CLSR}$       | 48  | SRDY Transition Hold Time                                   |
| $t_{CH1CH2}$     | 45  | CLKOUTA Rise Time                                          | $t_{CLTMV}$      | 55  | Timer Output Delay                                          |
| $t_{CHAV}$       | 68  | CLKOUTA High to A Address Valid                            | $t_{COAOB}$      | 83  | CLKOUTA to CLKOUTB Skew                                     |
| $t_{CHCK}$       | 38  | X1 High Time                                               | $t_{CVCTV}$      | 20  | Control Active Delay 1                                      |
| $t_{CHCL}$       | 44  | CLKOUTA High Time                                          | $t_{CVCTX}$      | 31  | Control Inactive Delay                                      |
| $t_{CHCSV}$      | 67  | CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid      | $t_{CVDEX}$      | 21  | $\overline{DEN}$ Inactive Delay                             |
| $t_{CHCSX}$      | 18  | $\overline{MCS}/\overline{PCS}$ Inactive Delay             | $t_{CXCSX}$      | 17  | $\overline{MCS}/\overline{PCS}$ Hold from Command Inactive  |
| $t_{CHCTV}$      | 22  | Control Active Delay 2                                     | $t_{DVCL}$       | 1   | Data in Setup                                               |
| $t_{CHCV}$       | 64  | Command Lines Valid Delay (after Float)                    | $t_{DVSH}$       | 75  | Data Valid to SCLK High                                     |
| $t_{CHCZ}$       | 63  | Command Lines Float Delay                                  | $t_{DXDL}$       | 19  | $\overline{DEN}$ Inactive to DT/ $\overline{R}$ Low         |
| $t_{CHDX}$       | 8   | Status Hold Time                                           | $t_{HVCL}$       | 58  | HOLD Setup                                                  |
| $t_{CHLH}$       | 9   | ALE Active Delay                                           | $t_{INVCH}$      | 53  | Peripheral Setup Time                                       |
| $t_{CHLL}$       | 11  | ALE Inactive Delay                                         | $t_{INVCL}$      | 54  | DRQ Setup Time                                              |
| $t_{CHRFD}$      | 79  | CLKOUTA High to $\overline{RFSH}$ valid                    | $t_{LCRF}$       | 86  | $\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay |
| $t_{CHSV}$       | 3   | Status Active Delay                                        | $t_{LHAV}$       | 23  | ALE High to Address Valid                                   |
| $t_{CICOA}$      | 69  | X1 to CLKOUTA Skew                                         | $t_{LHLL}$       | 10  | ALE Width                                                   |
| $t_{CICOB}$      | 70  | X1 to CLKOUTB Skew                                         | $t_{LLAX}$       | 13  | AD Address Hold from ALE Inactive                           |
| $t_{CKHL}$       | 39  | X1 Fall Time                                               | $t_{LOCK}$       | 61  | Maximum PLL Lock Time                                       |
| $t_{CKIN}$       | 36  | X1 Period                                                  | $t_{LRLL}$       | 84  | $\overline{LCS}$ Precharge Pulse Width                      |
| $t_{CKLH}$       | 40  | X1 Rise Time                                               | $t_{RESIN}$      | 57  | $\overline{RES}$ Setup Time                                 |
| $t_{CL2CL1}$     | 46  | CLKOUTA Fall Time                                          | $t_{RFCY}$       | 85  | $\overline{RFSH}$ Cycle Time                                |
| $t_{CLARX}$      | 50  | ARDY Active Hold Time                                      | $t_{RHAV}$       | 29  | $\overline{RD}$ Inactive to AD Address Active               |
| $t_{CLAV}$       | 5   | AD Address Valid Delay                                     | $t_{RHDX}$       | 59  | $\overline{RD}$ High to Data Hold on AD Bus                 |
| $t_{CLAX}$       | 6   | Address Hold                                               | $t_{RHLH}$       | 28  | $\overline{RD}$ Inactive to ALE High                        |
| $t_{CLAZ}$       | 15  | AD Address Float Delay                                     | $t_{RLRH}$       | 26  | $\overline{RD}$ Pulse Width                                 |
| $t_{CLCH}$       | 43  | CLKOUTA Low Time                                           | $t_{SHDX}$       | 77  | SCLK High to SPI Data Hold                                  |
| $t_{CLCK}$       | 37  | X1 Low Time                                                | $t_{SLDV}$       | 78  | SCLK Low to SPI Data Valid                                  |
| $t_{CLCL}$       | 42  | CLKOUTA Period                                             | $t_{SRYCL}$      | 47  | SRDY Transition Setup Time                                  |
| $t_{CLCLX}$      | 80  | $\overline{LCS}$ Inactive Delay                            | $t_{WHDEX}$      | 35  | $\overline{WR}$ Inactive to $\overline{DEN}$ Inactive       |
| $t_{CLCSL}$      | 81  | $\overline{LCS}$ Active Delay                              | $t_{WHDX}$       | 34  | Data Hold after $\overline{WR}$                             |
| $t_{CLCSV}$      | 16  | $\overline{MCS}/\overline{PCS}$ Active Delay               | $t_{WHLH}$       | 33  | $\overline{WR}$ Inactive to ALE High                        |
| $t_{CLDOX}$      | 30  | Data Hold Time                                             | $t_{WLWH}$       | 32  | $\overline{WR}$ Pulse Width                                 |
| $t_{CLDV}$       | 7   | Data Valid Delay                                           |                  |     |                                                             |

**Note:**

The following parameters are not defined or used as this time: 41, 56, 60, 73, 74, 76.

## Numerical Key to Switching Parameter Symbols

| Number | Parameter Symbol | Description                                                   | Number | Parameter Symbol | Description                                                 |
|--------|------------------|---------------------------------------------------------------|--------|------------------|-------------------------------------------------------------|
| 1      | $t_{DVCL}$       | Data in Setup                                                 | 43     | $t_{CLCH}$       | CLKOUTA Low Time                                            |
| 2      | $t_{CLDX}$       | Data in Hold                                                  | 44     | $t_{CHCL}$       | CLKOUTA High Time                                           |
| 3      | $t_{CHSV}$       | Status Active Delay                                           | 45     | $t_{CH1CH2}$     | CLKOUTA Rise Time                                           |
| 4      | $t_{CLSH}$       | Status Inactive Delay                                         | 46     | $t_{CL2CL1}$     | CLKOUTA Fall Time                                           |
| 5      | $t_{CLAV}$       | AD Address Valid Delay                                        | 47     | $t_{SRYCL}$      | SRDY Transition Setup Time                                  |
| 6      | $t_{CLAX}$       | Address Hold                                                  | 48     | $t_{CLSRV}$      | SRDY Transition Hold Time                                   |
| 7      | $t_{CLDV}$       | Data Valid Delay                                              | 49     | $t_{ARYCH}$      | ARDY Resolution Transition Setup Time                       |
| 8      | $t_{CHDX}$       | Status Hold Time                                              | 50     | $t_{CLARX}$      | ARDY Active Hold Time                                       |
| 9      | $t_{CHLH}$       | ALE Active Delay                                              | 51     | $t_{ARYCHL}$     | ARDY Inactive Holding Time                                  |
| 10     | $t_{LHLL}$       | ALE Width                                                     | 52     | $t_{ARYLCL}$     | ARDY Setup Time                                             |
| 11     | $t_{CHLL}$       | ALE Inactive Delay                                            | 53     | $t_{INVCH}$      | Peripheral Setup Time                                       |
| 12     | $t_{AVLL}$       | AD Address Valid to ALE Low                                   | 54     | $t_{INVCL}$      | DRQ Setup Time                                              |
| 13     | $t_{LLAX}$       | AD Address Hold from ALE Inactive                             | 55     | $t_{CLTMV}$      | Timer Output Delay                                          |
| 14     | $t_{AVCH}$       | AD Address Valid to Clock High                                | 57     | $t_{RESIN}$      | $\overline{RES}$ Setup Time                                 |
| 15     | $t_{CLAZ}$       | AD Address Float Delay                                        | 58     | $t_{HVCL}$       | HOLD Setup                                                  |
| 16     | $t_{CLCSV}$      | $\overline{MCS}/\overline{PCS}$ Active Delay                  | 59     | $t_{RHDX}$       | $\overline{RD}$ High to Data Hold on AD Bus                 |
| 17     | $t_{CXCSX}$      | $\overline{MCS}/\overline{PCS}$ Hold from Command Inactive    | 61     | $t_{LOCK}$       | Maximum PLL Lock Time                                       |
| 18     | $t_{CHCSX}$      | $\overline{MCS}/\overline{PCS}$ Inactive Delay                | 62     | $t_{CLHAV}$      | HLDA Valid Delay                                            |
| 19     | $t_{DXDL}$       | $\overline{DEN}$ Inactive to $\overline{DT}/\overline{R}$ Low | 63     | $t_{CHCZ}$       | Command Lines Float Delay                                   |
| 20     | $t_{CVCTV}$      | Control Active Delay 1                                        | 64     | $t_{CHCV}$       | Command Lines Valid Delay (after Float)                     |
| 21     | $t_{CVDEX}$      | $\overline{DEN}$ Inactive Delay                               | 65     | $t_{AVWL}$       | A Address Valid to $\overline{WR}$ Low                      |
| 22     | $t_{CHCTV}$      | Control Active Delay 2                                        | 66     | $t_{AVRL}$       | A Address Valid to $\overline{RD}$ Low                      |
| 23     | $t_{LHAV}$       | ALE High to Address Valid                                     | 67     | $t_{CHCSV}$      | CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid       |
| 24     | $t_{AZRL}$       | AD Address Float to $\overline{RD}$ Active                    | 68     | $t_{CHAV}$       | CLKOUTA High to Address Valid                               |
| 25     | $t_{CLRL}$       | $\overline{RD}$ Active Delay                                  | 69     | $t_{CICOA}$      | X1 to CLKOUTA Skew                                          |
| 26     | $t_{RLRH}$       | $\overline{RD}$ Pulse Width                                   | 70     | $t_{CICOB}$      | X1 to CLKOUTB Skew                                          |
| 27     | $t_{CLRH}$       | $\overline{RD}$ Inactive Delay                                | 71     | $t_{CLEV}$       | CLKOUTA Low to SDEN Valid                                   |
| 28     | $t_{RHLH}$       | $\overline{RD}$ Inactive to ALE High                          | 72     | $t_{CLSL}$       | CLKOUTA Low to SCLK Low                                     |
| 29     | $t_{RHAV}$       | $\overline{RD}$ Inactive to AD address Active                 | 75     | $t_{DVSH}$       | Data Valid to SCLK High                                     |
| 30     | $t_{CLDOX}$      | Data Hold Time                                                | 77     | $t_{SHDX}$       | SCLK High to SPI Data Hold                                  |
| 31     | $t_{CVCTX}$      | Control Inactive Delay                                        | 78     | $t_{SLDV}$       | SCLK Low to SPI Data Valid                                  |
| 32     | $t_{WLWH}$       | $\overline{WR}$ Pulse Width                                   | 79     | $t_{CHRFD}$      | CLKOUTA High to $\overline{RFSH}$ Valid                     |
| 33     | $t_{WHLH}$       | $\overline{WR}$ Inactive to ALE High                          | 80     | $t_{CLCLX}$      | $\overline{LCS}$ Inactive Delay                             |
| 34     | $t_{WHDX}$       | Data Hold after $\overline{WR}$                               | 81     | $t_{CLCSL}$      | $\overline{LCS}$ Active Delay                               |
| 35     | $t_{WHDEX}$      | $\overline{WR}$ Inactive to $\overline{DEN}$ Inactive         | 82     | $t_{CLRF}$       | CLKOUTA High to $\overline{RFSH}$ Invalid                   |
| 36     | $t_{CKIN}$       | X1 Period                                                     | 83     | $t_{COAOB}$      | CLKOUTA to CLKOUTB Skew                                     |
| 37     | $t_{CLCK}$       | X1 Low Time                                                   | 84     | $t_{LRLL}$       | $\overline{LCS}$ Precharge Pulse Width                      |
| 38     | $t_{CHCK}$       | X1 High Time                                                  | 85     | $t_{RFCY}$       | $\overline{RFSH}$ Cycle Time                                |
| 39     | $t_{CKHL}$       | X1 Fall Time                                                  | 86     | $t_{LCRF}$       | $\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay |
| 40     | $t_{CKLH}$       | X1 Rise Time                                                  | 87     | $t_{AVBL}$       | A Address Valid to $\overline{WHB}$ , $\overline{WLB}$ Low  |
| 42     | $t_{CLCL}$       | CLKOUTA Period                                                |        |                  |                                                             |

**Note:**

The following parameters are not defined or used at this time: 41, 56, 60, 73, 74, and 76.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

## Read Cycle (20 MHz and 25 MHz)

| Parameter                   |                    |                                                   | Preliminary               |     |                           |     | Unit |
|-----------------------------|--------------------|---------------------------------------------------|---------------------------|-----|---------------------------|-----|------|
|                             |                    |                                                   | 20 MHz                    |     | 25 MHz                    |     |      |
| No.                         | Symbol             | Description                                       | Min                       | Max | Min                       | Max |      |
| General Timing Requirements |                    |                                                   |                           |     |                           |     |      |
| 1                           | t <sub>DVCL</sub>  | Data in Setup                                     | 10                        |     | 10                        |     | ns   |
| 2                           | t <sub>CLDX</sub>  | Data in Hold <sup>(c)</sup>                       | 3                         |     | 3                         |     | ns   |
| General Timing Responses    |                    |                                                   |                           |     |                           |     |      |
| 3                           | t <sub>CHSV</sub>  | Status Active Delay                               | 0                         | 25  | 0                         | 20  | ns   |
| 4                           | t <sub>CLSH</sub>  | Status Inactive Delay                             | 0                         | 25  | 0                         | 20  | ns   |
| 5                           | t <sub>CLAV</sub>  | AD Address Valid Delay and BHE                    | 0                         | 25  | 0                         | 20  | ns   |
| 6                           | t <sub>CLAX</sub>  | Address Hold                                      | 0                         | 25  | 0                         | 20  | ns   |
| 8                           | t <sub>CHDX</sub>  | Status Hold Time                                  | 0                         |     | 0                         |     | ns   |
| 9                           | t <sub>CHLH</sub>  | ALE Active Delay                                  |                           | 25  |                           | 20  | ns   |
| 10                          | t <sub>LHLL</sub>  | ALE Width                                         | t <sub>CLCL</sub> −10=40  |     | t <sub>CLCL</sub> −10=30  |     | ns   |
| 11                          | t <sub>CHLL</sub>  | ALE Inactive Delay                                |                           | 25  |                           | 20  | ns   |
| 12                          | t <sub>AVLL</sub>  | AD Address Valid to ALE Low <sup>(a)</sup>        | t <sub>CLCH</sub> −2      |     | t <sub>CLCH</sub> −2      |     | ns   |
| 13                          | t <sub>LLAX</sub>  | AD Address Hold from ALE Inactive <sup>(a)</sup>  | t <sub>CHCL</sub> −2      |     | t <sub>CHCL</sub> −2      |     | ns   |
| 14                          | t <sub>AVCH</sub>  | AD Address Valid to Clock High                    | 0                         |     | 0                         |     | ns   |
| 15                          | t <sub>CLAZ</sub>  | AD Address Float Delay                            | t <sub>CLAX</sub> =0      | 25  | t <sub>CLAX</sub> =0      | 20  | ns   |
| 16                          | t <sub>CLCSV</sub> | MCS/PCS Active Delay                              | 0                         | 25  | 0                         | 20  | ns   |
| 17                          | t <sub>CXCSX</sub> | MCS/PCS Hold from Command Inactive <sup>(a)</sup> | t <sub>CLCH</sub> −2      |     | t <sub>CLCH</sub> −2      |     | ns   |
| 18                          | t <sub>CHCSX</sub> | MCS/PCS Inactive Delay                            | 0                         | 25  | 0                         | 20  | ns   |
| 19                          | t <sub>DXDL</sub>  | DEN Inactive to DT/R Low <sup>(a)</sup>           | 0                         |     | 0                         |     | ns   |
| 20                          | t <sub>CVCTV</sub> | Control Active Delay 1 <sup>(b)</sup>             | 0                         | 25  | 0                         | 20  | ns   |
| 21                          | t <sub>CVDEX</sub> | DEN Inactive Delay                                | 0                         | 25  | 0                         | 20  | ns   |
| 22                          | t <sub>CHCTV</sub> | Control Active Delay 2 <sup>(b)</sup>             | 0                         | 25  | 0                         | 20  | ns   |
| 23                          | t <sub>LHAV</sub>  | ALE High to Address Valid                         | 20                        |     | 15                        |     | ns   |
| Read Cycle Timing Responses |                    |                                                   |                           |     |                           |     |      |
| 24                          | t <sub>AZRL</sub>  | AD Address Float to RD Active                     | 0                         |     | 0                         |     | ns   |
| 25                          | t <sub>CLRL</sub>  | RD Active Delay                                   | 0                         | 25  | 0                         | 20  | ns   |
| 26                          | t <sub>RLRH</sub>  | RD Pulse Width                                    | 2t <sub>CLCL</sub> −15=85 |     | 2t <sub>CLCL</sub> −15=65 |     | ns   |
| 27                          | t <sub>CLRH</sub>  | RD Inactive Delay                                 | 0                         | 25  | 0                         | 20  | ns   |
| 28                          | t <sub>RHLH</sub>  | RD Inactive to ALE High <sup>(a)</sup>            | t <sub>CLCH</sub> −3      |     | t <sub>CLCH</sub> −3      |     | ns   |
| 29                          | t <sub>RHAV</sub>  | RD Inactive to AD Address Active <sup>(a)</sup>   | t <sub>CLCL</sub> −10=40  |     | t <sub>CLCL</sub> −10=30  |     | ns   |
| 59                          | t <sub>RHDX</sub>  | RD High to Data Hold on AD Bus <sup>(c)</sup>     | 0                         |     | 0                         |     | ns   |
| 66                          | t <sub>AVRL</sub>  | A Address Valid to RD Low <sup>(a)</sup>          | 2t <sub>CLCL</sub> −15=85 |     | 2t <sub>CLCL</sub> −15=65 |     | ns   |
| 67                          | t <sub>CHCSV</sub> | CLKOUTA High to LCS/UCS Valid                     | 0                         | 25  | 0                         | 20  | ns   |
| 68                          | t <sub>CHAV</sub>  | CLKOUTA High to A Address Valid                   | 0                         | 25  | 0                         | 20  | ns   |

**Note:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b This parameter applies to the  $\overline{DEN}$ ,  $\overline{INTA1}$ – $\overline{INTA0}$ ,  $\overline{WR}$ ,  $\overline{WHB}$ , and  $\overline{WLB}$  signals.

c If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

## Read Cycle (33 MHz and 40 MHz)

| Parameter                   |                     |                                                   | Preliminary               |     |                             |     |      |
|-----------------------------|---------------------|---------------------------------------------------|---------------------------|-----|-----------------------------|-----|------|
|                             |                     |                                                   | 33 MHz                    |     | 40 MHz                      |     |      |
| No.                         | Symbol              | Description                                       | Min                       | Max | Min                         | Max | Unit |
| General Timing Requirements |                     |                                                   |                           |     |                             |     |      |
| 1                           | t <sub>DVCL</sub>   | Data in Setup                                     | 8                         |     | 5                           |     | ns   |
| 2                           | t <sub>CLDX</sub>   | Data in Hold <sup>(c)</sup>                       | 3                         |     | 2                           |     | ns   |
| General Timing Responses    |                     |                                                   |                           |     |                             |     |      |
| 3                           | t <sub>CHSV</sub>   | Status Active Delay                               | 0                         | 15  | 0                           | 12  | ns   |
| 4                           | t <sub>CLSH</sub>   | Status Inactive Delay                             | 0                         | 15  | 0                           | 12  | ns   |
| 5                           | t <sub>CLAV</sub>   | AD Address Valid Delay and BHE                    | 0                         | 15  | 0                           | 12  | ns   |
| 6                           | t <sub>CLAX</sub>   | Address Hold                                      | 0                         | 25  | 0                           | 20  | ns   |
| 7                           | t <sub>CLDV</sub>   | Data Valid Delay                                  | 0                         | 15  | 0                           | 12  | ns   |
| 8                           | t <sub>CHDX</sub>   | Status Hold Time                                  | 0                         |     | 0                           |     | ns   |
| 9                           | t <sub>CHLH</sub>   | ALE Active Delay                                  |                           | 15  |                             | 12  | ns   |
| 10                          | t <sub>LHLL</sub>   | ALE Width                                         | t <sub>CLCL</sub> −10=20  |     | t <sub>CLCL</sub> −5<br>=20 |     | ns   |
| 11                          | t <sub>CHLL</sub>   | ALE Inactive Delay                                |                           | 15  |                             | 12  | ns   |
| 12                          | t <sub>AVLL</sub>   | AD Address Valid to ALE Low <sup>(a)</sup>        | t <sub>CLCH</sub> −2      |     | t <sub>CLCH</sub> −2        |     | ns   |
| 13                          | t <sub>LLAX</sub>   | AD Address Hold from ALE Inactive <sup>(a)</sup>  | t <sub>CHCL</sub> −2      |     | t <sub>CHCL</sub> −2        |     | ns   |
| 14                          | t <sub>AVCH</sub>   | AD Address Valid to Clock High                    | 0                         |     | 0                           |     | ns   |
| 15                          | t <sub>CLAZ</sub>   | AD Address Float Delay                            | t <sub>CLAX</sub> =0      | 15  | t <sub>CLAX</sub> =0        | 12  | ns   |
| 16                          | t <sub>CLCSV</sub>  | MCS/PCS Active Delay                              | 0                         | 15  | 0                           | 12  | ns   |
| 17                          | t <sub>CXCXSX</sub> | MCS/PCS Hold from Command Inactive <sup>(a)</sup> | t <sub>CLCH</sub> −2      |     | t <sub>CLCH</sub> −2        |     | ns   |
| 18                          | t <sub>CHCSX</sub>  | MCS/PCS Inactive Delay                            | 0                         | 15  | 0                           | 12  | ns   |
| 19                          | t <sub>DXDL</sub>   | DEN Inactive to DT/R Low <sup>(a)</sup>           | 0                         |     | 0                           |     | ns   |
| 20                          | t <sub>CVCTV</sub>  | Control Active Delay 1 <sup>(b)</sup>             | 0                         | 15  | 0                           | 12  | ns   |
| 21                          | t <sub>CVDEX</sub>  | DEN Inactive Delay                                | 0                         | 15  | 0                           | 12  | ns   |
| 22                          | t <sub>CHCTV</sub>  | Control Active Delay 2 <sup>(b)</sup>             | 0                         | 15  | 0                           | 12  | ns   |
| 23                          | t <sub>LHAV</sub>   | ALE High to Address Valid                         | 10                        |     | 7.5                         |     | ns   |
| Read Cycle Timing Responses |                     |                                                   |                           |     |                             |     |      |
| 24                          | t <sub>AZRL</sub>   | AD Address Float to RD Active                     | 0                         |     | 0                           |     | ns   |
| 25                          | t <sub>CLRL</sub>   | RD Active Delay                                   | 0                         | 15  | 0                           | 10  | ns   |
| 26                          | t <sub>RLRH</sub>   | RD Pulse Width                                    | 2t <sub>CLCL</sub> −15=45 |     | 2t <sub>CLCL</sub> −10=40   |     | ns   |
| 27                          | t <sub>CLRH</sub>   | RD Inactive Delay                                 | 0                         | 15  | 0                           | 12  | ns   |
| 28                          | t <sub>RHLH</sub>   | RD Inactive to ALE High <sup>(a)</sup>            | t <sub>CLCH</sub> −3      |     | t <sub>CLCH</sub> −2        |     | ns   |
| 29                          | t <sub>RHAV</sub>   | RD Inactive to AD Address Active <sup>(a)</sup>   | t <sub>CLCL</sub> −10=20  |     | t <sub>CLCL</sub> −5<br>=20 |     | ns   |
| 59                          | t <sub>RHDX</sub>   | RD High to Data Hold on AD Bus <sup>(c)</sup>     | 0                         |     | 0                           |     | ns   |
| 66                          | t <sub>AVRL</sub>   | A Address Valid to RD Low <sup>(a)</sup>          | 2t <sub>CLCL</sub> −15=45 |     | 2t <sub>CLCL</sub> −10=40   |     | ns   |
| 67                          | t <sub>CHCSV</sub>  | CLKOUTA High to LCS/UCS Valid                     | 0                         | 15  | 0                           | 10  | ns   |
| 68                          | t <sub>CHAV</sub>   | CLKOUTA High to A Address Valid                   | 0                         | 15  | 0                           | 10  | ns   |

**Notes:**

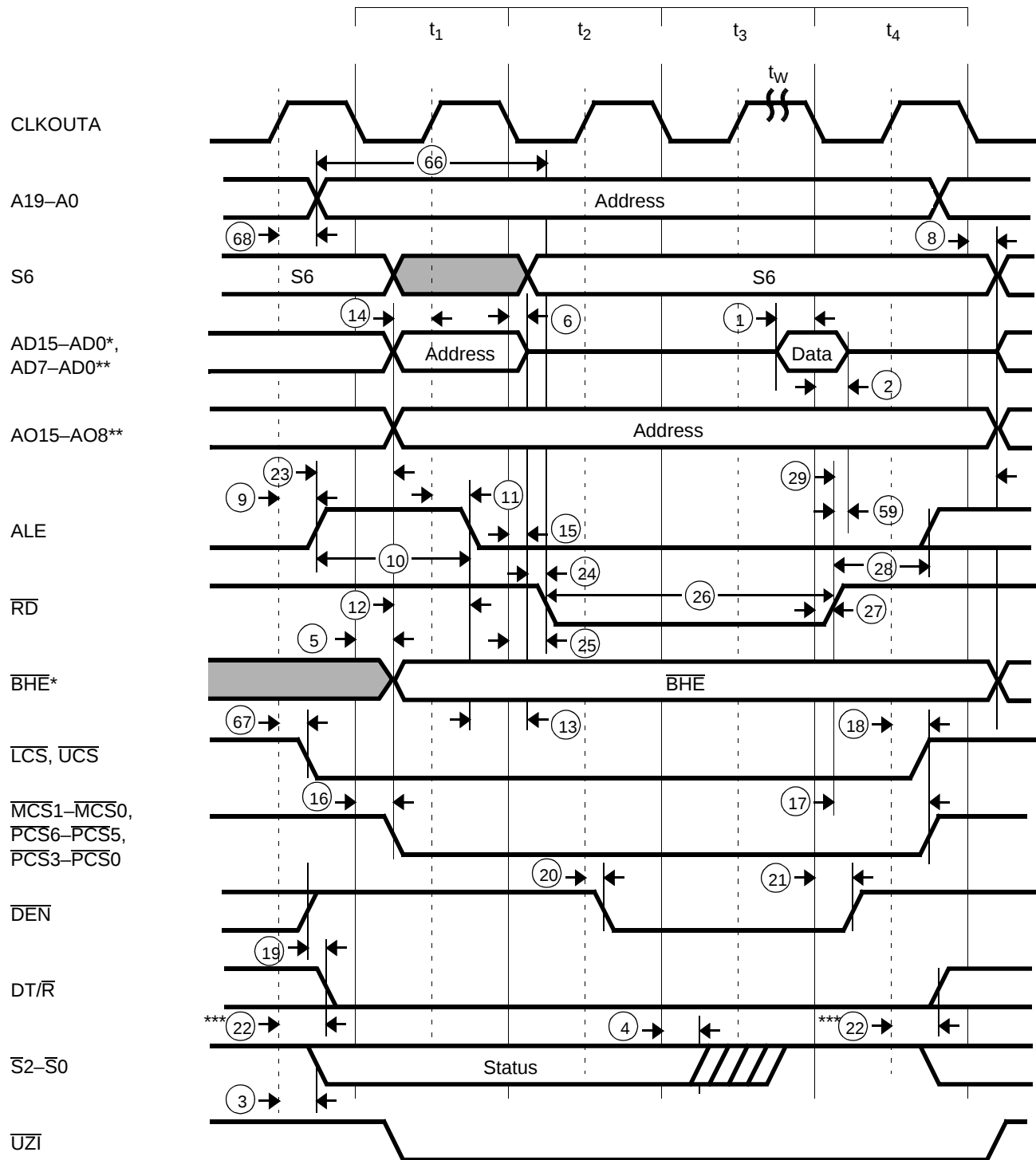
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b This parameter applies to the  $\overline{DEN}$ ,  $\overline{INTA1}$ – $\overline{INTA0}$ ,  $\overline{WR}$ ,  $\overline{WHB}$ , and  $\overline{WLB}$  signals.

c If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

## Read Cycle Waveforms

**Notes:**

\* Am186EM microcontroller only

\*\* Am188EM microcontroller only

\*\*\* Changes in  $t_4$  phase of the clock preceding next bus cycle if followed by read, INTA, or halt

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

## Write Cycle (20 MHz and 25 MHz)

| Parameter                    |                     |                                                   | Preliminary                                |     |                                            |     | Unit |
|------------------------------|---------------------|---------------------------------------------------|--------------------------------------------|-----|--------------------------------------------|-----|------|
|                              |                     |                                                   | 20 MHz                                     |     | 25 MHz                                     |     |      |
| No.                          | Symbol              | Description                                       | Min                                        | Max | Min                                        | Max |      |
| General Timing Responses     |                     |                                                   |                                            |     |                                            |     |      |
| 3                            | t <sub>CHSV</sub>   | Status Active Delay                               | 0                                          | 25  | 0                                          | 20  | ns   |
| 4                            | t <sub>CLSH</sub>   | Status Inactive Delay                             | 0                                          | 25  | 0                                          | 20  | ns   |
| 5                            | t <sub>CLAV</sub>   | AD Address Valid Delay and BHE                    | 0                                          | 25  | 0                                          | 20  | ns   |
| 6                            | t <sub>CLAX</sub>   | Address Hold                                      | 0                                          | 25  | 0                                          | 20  | ns   |
| 7                            | t <sub>CLDV</sub>   | Data Valid Delay                                  | 0                                          | 25  | 0                                          | 20  | ns   |
| 8                            | t <sub>CHDX</sub>   | Status Hold Time                                  | 0                                          |     | 0                                          |     | ns   |
| 9                            | t <sub>CHLH</sub>   | ALE Active Delay                                  |                                            | 25  |                                            | 20  | ns   |
| 10                           | t <sub>LHLL</sub>   | ALE Width                                         | t <sub>CLCL</sub> −10=<br>40               |     | t <sub>CLCL</sub> −10=<br>30               |     | ns   |
| 11                           | t <sub>CHLL</sub>   | ALE Inactive Delay                                |                                            | 25  |                                            | 20  | ns   |
| 12                           | t <sub>AVLL</sub>   | AD Address Valid to ALE Low <sup>(a)</sup>        | t <sub>CLCH</sub>                          |     | t <sub>CLCH</sub>                          |     | ns   |
| 13                           | t <sub>LLAX</sub>   | AD Address Hold from ALE Inactive <sup>(a)</sup>  | t <sub>CHCL</sub>                          |     | t <sub>CHCL</sub>                          |     | ns   |
| 14                           | t <sub>AVCH</sub>   | AD Address Valid to Clock High                    | 0                                          |     | 0                                          |     | ns   |
| 16                           | t <sub>CLCSV</sub>  | MCS/PCS Active Delay                              | 0                                          | 25  | 0                                          | 20  | ns   |
| 17                           | t <sub>CXCXSX</sub> | MCS/PCS Hold from Command Inactive <sup>(a)</sup> | t <sub>CLCH</sub>                          |     | t <sub>CLCH</sub>                          |     | ns   |
| 18                           | t <sub>CHCSX</sub>  | MCS/PCS Inactive Delay                            | 0                                          | 25  | 0                                          | 20  | ns   |
| 19                           | t <sub>DXDL</sub>   | DEN Inactive to DT/R Low <sup>(a)</sup>           | 0                                          |     | 0                                          |     | ns   |
| 20                           | t <sub>CVCTV</sub>  | Control Active Delay 1 <sup>(b)</sup>             | 0                                          | 25  | 0                                          | 20  | ns   |
| 22                           | t <sub>CHCTV</sub>  | Control Active Delay 2                            | 0                                          | 25  | 0                                          | 20  | ns   |
| 23                           | t <sub>LHAV</sub>   | ALE High to Address Valid                         | 20                                         |     | 15                                         |     | ns   |
| Write Cycle Timing Responses |                     |                                                   |                                            |     |                                            |     |      |
| 30                           | t <sub>CLDOX</sub>  | Data Hold Time                                    | 0                                          |     | 0                                          |     | ns   |
| 31                           | t <sub>CVCTX</sub>  | Control Inactive Delay <sup>(b)</sup>             | 0                                          | 25  | 0                                          | 20  | ns   |
| 32                           | t <sub>WLWH</sub>   | WR Pulse Width                                    | 2t <sub>CLCL</sub> −10<br>=90              |     | 2t <sub>CLCL</sub> −10<br>=70              |     | ns   |
| 33                           | t <sub>WHLH</sub>   | WR Inactive to ALE High <sup>(a)</sup>            | t <sub>CLCH</sub> −2                       |     | t <sub>CLCH</sub> −2                       |     | ns   |
| 34                           | t <sub>WHDX</sub>   | Data Hold after WR <sup>(a)</sup>                 | t <sub>CLCL</sub> −10=<br>40               |     | t <sub>CLCL</sub> −10=<br>30               |     | ns   |
| 35                           | t <sub>WHDEX</sub>  | WR Inactive to DEN Inactive <sup>(a)</sup>        | t <sub>CLCH</sub> −3                       |     | t <sub>CLCH</sub> −3                       |     | ns   |
| 65                           | t <sub>AVWL</sub>   | A Address Valid to WR Low                         | t <sub>CLCL</sub> +t <sub>CHCL</sub><br>−3 |     | t <sub>CLCL</sub> +t <sub>CHCL</sub><br>−3 |     | ns   |
| 67                           | t <sub>CHCSV</sub>  | CLKOUTA High to LCS/UCS Valid                     | 0                                          | 25  | 0                                          | 20  | ns   |
| 68                           | t <sub>CHAV</sub>   | CLKOUTA High to A Address Valid                   | 0                                          | 25  | 0                                          | 20  | ns   |
| 87                           | t <sub>AVBL</sub>   | A Address Valid to WHB, WLB Low                   | t <sub>CHCL</sub> −3                       | 25  | t <sub>CHCL</sub> −3                       | 20  | ns   |

**Notes:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b This parameter applies to the  $\overline{DEN}$ ,  $\overline{INTA1}$ – $\overline{INTA0}$ ,  $\overline{WR}$ ,  $\overline{WHB}$ , and  $\overline{WLB}$  signals.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

## Write Cycle (33 MHz and 40 MHz)

| Parameter                    |                     |                                                   | Preliminary                                |     |                                               |     | Unit |
|------------------------------|---------------------|---------------------------------------------------|--------------------------------------------|-----|-----------------------------------------------|-----|------|
|                              |                     |                                                   | 33 MHz                                     |     | 40 MHz                                        |     |      |
| No.                          | Symbol              | Description                                       | Min                                        | Max | Min                                           | Max |      |
| General Timing Responses     |                     |                                                   |                                            |     |                                               |     |      |
| 3                            | t <sub>CHSV</sub>   | Status Active Delay                               | 0                                          | 15  | 0                                             | 12  | ns   |
| 4                            | t <sub>CLSH</sub>   | Status Inactive Delay                             | 0                                          | 15  | 0                                             | 12  | ns   |
| 5                            | t <sub>CLAV</sub>   | AD Address Valid Delay and BHE                    | 0                                          | 15  | 0                                             | 12  | ns   |
| 6                            | t <sub>CLAX</sub>   | Address Hold                                      | 0                                          | 25  | 0                                             | 20  | ns   |
| 7                            | t <sub>CLDV</sub>   | Data Valid Delay                                  | 0                                          | 15  | 0                                             | 12  | ns   |
| 8                            | t <sub>CHDX</sub>   | Status Hold Time                                  | 0                                          |     | 0                                             |     | ns   |
| 9                            | t <sub>CHLH</sub>   | ALE Active Delay                                  |                                            | 15  |                                               | 12  | ns   |
| 10                           | t <sub>LHLL</sub>   | ALE Width                                         | t <sub>CLCL</sub> −10=<br>20               |     | t <sub>CLCL</sub> −5<br>=20                   |     | ns   |
| 11                           | t <sub>CHLL</sub>   | ALE Inactive Delay                                |                                            | 15  |                                               | 12  | ns   |
| 12                           | t <sub>AVLL</sub>   | AD Address Valid to ALE Low <sup>(a)</sup>        | t <sub>CLCH</sub>                          |     | t <sub>CLCH</sub>                             |     | ns   |
| 13                           | t <sub>LLAX</sub>   | AD Address Hold from ALE Inactive <sup>(a)</sup>  | t <sub>CHCL</sub>                          |     | t <sub>CHCL</sub>                             |     | ns   |
| 14                           | t <sub>AVCH</sub>   | AD Address Valid to Clock High                    | 0                                          |     | 0                                             |     | ns   |
| 16                           | t <sub>CLCSV</sub>  | MCS/PCS Active Delay                              | 0                                          | 15  | 0                                             | 12  | ns   |
| 17                           | t <sub>CXC SX</sub> | MCS/PCS Hold from Command Inactive <sup>(a)</sup> | t <sub>CLCH</sub>                          |     | t <sub>CLCH</sub>                             |     | ns   |
| 18                           | t <sub>CHCSX</sub>  | MCS/PCS Inactive Delay                            | 0                                          | 15  | 0                                             | 12  | ns   |
| 19                           | t <sub>DXDL</sub>   | DEN Inactive to DT/R Low <sup>(a)</sup>           | 0                                          |     | 0                                             |     | ns   |
| 20                           | t <sub>CVCTV</sub>  | Control Active Delay 1 <sup>(b)</sup>             | 0                                          | 15  | 0                                             | 12  | ns   |
| 22                           | t <sub>CHCTV</sub>  | Control Active Delay 2                            | 0                                          | 15  | 0                                             | 12  | ns   |
| 23                           | t <sub>LHAV</sub>   | ALE High to Address Valid                         | 10                                         |     | 7.5                                           |     | ns   |
| Write Cycle Timing Responses |                     |                                                   |                                            |     |                                               |     |      |
| 30                           | t <sub>CLDOX</sub>  | Data Hold Time                                    | 0                                          |     | 0                                             |     | ns   |
| 31                           | t <sub>CVCTX</sub>  | Control Inactive Delay <sup>(b)</sup>             | 0                                          | 15  | 0                                             | 12  | ns   |
| 32                           | t <sub>WLWH</sub>   | WR Pulse Width                                    | 2t <sub>CLCL</sub> −10<br>=50              |     | 2t <sub>CLCL</sub> −10<br>=40                 |     | ns   |
| 33                           | t <sub>WHLH</sub>   | WR Inactive to ALE High <sup>(a)</sup>            | t <sub>CLCH</sub> −2                       |     | t <sub>CLCH</sub> −2                          |     | ns   |
| 34                           | t <sub>WHDX</sub>   | Data Hold after WR <sup>(a)</sup>                 | t <sub>CLCL</sub> −10=<br>20               |     | t <sub>CLCL</sub> −10=<br>15                  |     | ns   |
| 35                           | t <sub>WHDEX</sub>  | WR Inactive to DEN Inactive <sup>(a)</sup>        | t <sub>CLCH</sub> −5                       |     | t <sub>CLCH</sub>                             |     | ns   |
| 65                           | t <sub>AVWL</sub>   | A Address Valid to WR Low                         | t <sub>CLCL</sub> +t <sub>CHCL</sub><br>−3 |     | t <sub>CLCL</sub> +t <sub>CHCL</sub><br>−1.25 |     | ns   |
| 67                           | t <sub>CHCSV</sub>  | CLKOUTA High to LCS/UCS Valid                     | 0                                          | 15  | 0                                             | 10  | ns   |
| 68                           | t <sub>CHAV</sub>   | CLKOUTA High to A Address Valid                   | 0                                          | 15  | 0                                             | 10  | ns   |
| 87                           | t <sub>AVBL</sub>   | A Address Valid to WHB, WLB Low                   | t <sub>CHCL</sub> −3                       | 15  | t <sub>CHCL</sub> −1.25                       | 12  | ns   |

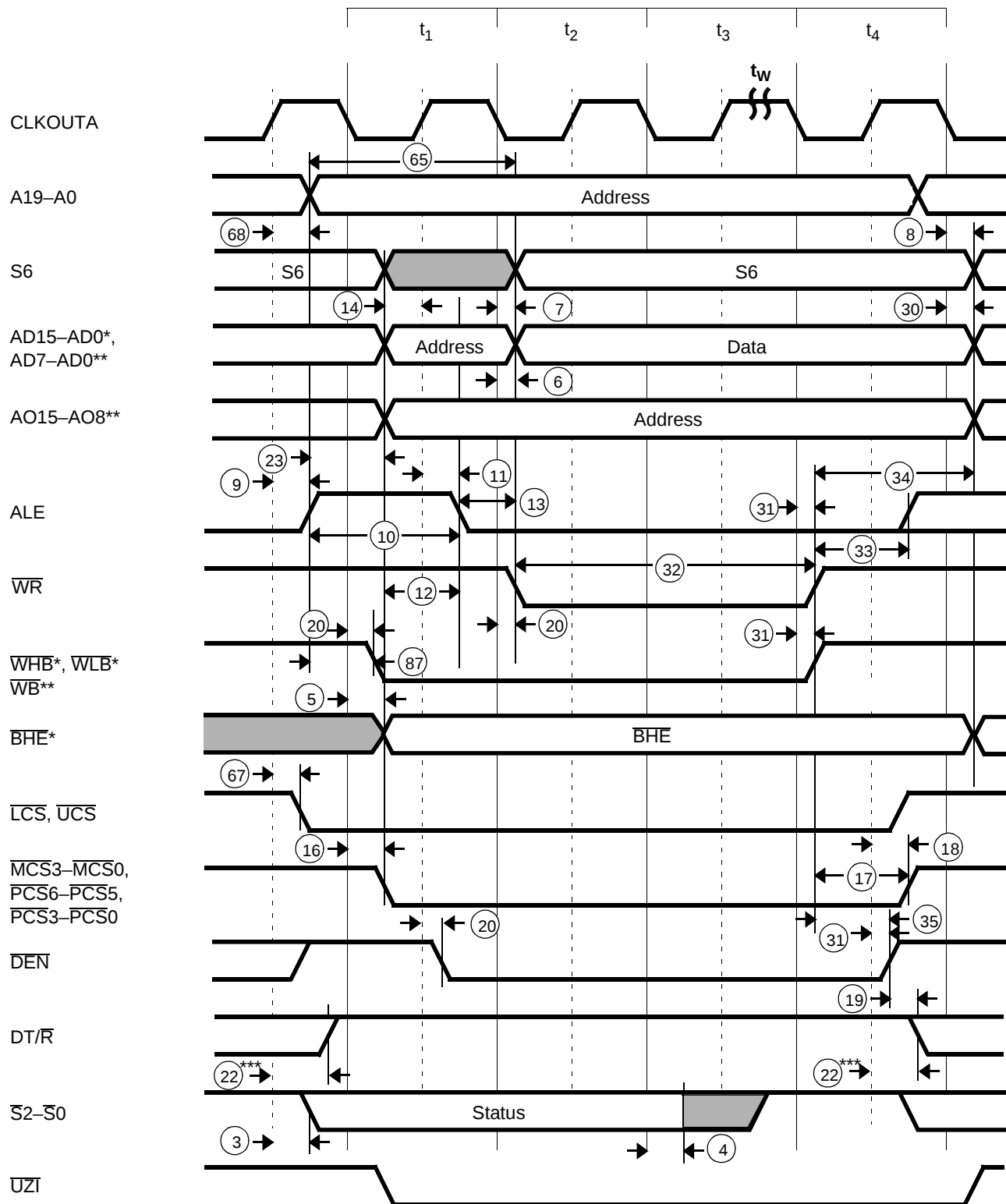
**Notes:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b This parameter applies to the  $\overline{DEN}$ ,  $\overline{INTA1}$ – $\overline{INTA0}$ ,  $\overline{WR}$ ,  $\overline{WHB}$ , and  $\overline{WLB}$  signals.

# Write Cycle Waveforms



**Note:**

\* Am186EM microcontroller only

\*\* Am188EM microcontroller only

\*\*\* Changes in  $t_4$  phase of the clock preceding next bus cycle if followed by read, INTA, or halt.

# SWITCHING CHARACTERISTICS over COMMERCIAL operating range

## PSRAM Read Cycle (20 MHz and 25 MHz)

| Parameter                   |                    |                                                                   | Preliminary                                 |     |                                             |     | Unit |
|-----------------------------|--------------------|-------------------------------------------------------------------|---------------------------------------------|-----|---------------------------------------------|-----|------|
|                             |                    |                                                                   | 20 MHz                                      |     | 25 MHz                                      |     |      |
| No.                         | Symbol             | Description                                                       | Min                                         | Max | Min                                         | Max |      |
| General Timing Requirements |                    |                                                                   |                                             |     |                                             |     |      |
| 1                           | t <sub>DVCL</sub>  | Data in Setup                                                     | 10                                          |     | 10                                          |     | ns   |
| 2                           | t <sub>CLDX</sub>  | Data in Hold <sup>(b)</sup>                                       | 3                                           |     | 3                                           |     | ns   |
| General Timing Responses    |                    |                                                                   |                                             |     |                                             |     |      |
| 5                           | t <sub>CLAV</sub>  | AD Address Valid Delay and BHE                                    | 0                                           | 25  | 0                                           | 20  | ns   |
| 7                           | t <sub>CLDV</sub>  | Data Valid Delay                                                  | 0                                           | 25  | 0                                           | 20  | ns   |
| 8                           | t <sub>CHDX</sub>  | Status Hold Time                                                  | 0                                           |     | 0                                           |     | ns   |
| 9                           | t <sub>CHLH</sub>  | ALE Active Delay                                                  |                                             | 25  |                                             | 20  | ns   |
| 10                          | t <sub>LHLL</sub>  | ALE Width                                                         | t <sub>CLCL</sub> −10=<br>40                |     | t <sub>CLCL</sub> −10=<br>30                |     | ns   |
| 11                          | t <sub>CHLL</sub>  | ALE Inactive Delay                                                |                                             | 25  |                                             | 20  | ns   |
| 23                          | t <sub>LHAV</sub>  | ALE High to Address Valid                                         | 20                                          |     | 15                                          |     | ns   |
| 80                          | t <sub>CLCLX</sub> | $\overline{\text{LCS}}$ Inactive Delay                            | 0                                           | 25  | 0                                           | 20  | ns   |
| 81                          | t <sub>CLCSL</sub> | $\overline{\text{LCS}}$ Active Delay                              | 0                                           | 25  | 0                                           | 20  | ns   |
| 84                          | t <sub>LRLL</sub>  | $\overline{\text{LCS}}$ Precharge Pulse Width                     | t <sub>CLCL</sub> + t <sub>CLCH</sub><br>−3 |     | t <sub>CLCL</sub> + t <sub>CLCH</sub><br>−3 |     | ns   |
| Read Cycle Timing Responses |                    |                                                                   |                                             |     |                                             |     |      |
| 24                          | t <sub>AZRL</sub>  | AD Address Float to $\overline{\text{RD}}$ Active                 | 0                                           |     | 0                                           |     | ns   |
| 25                          | t <sub>CLRL</sub>  | $\overline{\text{RD}}$ Active Delay                               | 0                                           | 25  | 0                                           | 20  | ns   |
| 26                          | t <sub>RLRH</sub>  | $\overline{\text{RD}}$ Pulse Width                                | 2t <sub>CLCL</sub> −15<br>=85               |     | 2t <sub>CLCL</sub> −15<br>=65               |     | ns   |
| 27                          | t <sub>CLRH</sub>  | $\overline{\text{RD}}$ Inactive Delay                             | 0                                           | 25  | 0                                           | 20  | ns   |
| 28                          | t <sub>RHLH</sub>  | $\overline{\text{RD}}$ Inactive to ALE High <sup>(a)</sup>        | t <sub>CLCH</sub> −3                        |     | t <sub>CLCH</sub> −3                        |     | ns   |
| 59                          | t <sub>RHDX</sub>  | $\overline{\text{RD}}$ High to Data Hold on AD Bus <sup>(b)</sup> | 0                                           |     | 0                                           |     | ns   |
| 66                          | t <sub>AVRL</sub>  | A Address Valid to $\overline{\text{RD}}$ Low                     | 2t <sub>CLCL</sub> −15<br>=85               |     | 2t <sub>CLCL</sub> −15<br>=65               |     | ns   |
| 68                          | t <sub>CHAV</sub>  | CLKOUTA High to A Address Valid                                   | 0                                           | 25  | 0                                           | 20  | ns   |

**Notes:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

## SWITCHING CHARACTERISTICS over Commercial operating range

### PSRAM Read Cycle (33 MHz and 40 MHz)

| Parameter                   |                    |                                               | Preliminary                                 |     |                                                |     | Unit |
|-----------------------------|--------------------|-----------------------------------------------|---------------------------------------------|-----|------------------------------------------------|-----|------|
|                             |                    |                                               | 33 MHz                                      |     | 40 MHz                                         |     |      |
| No.                         | Symbol             | Description                                   | Min                                         | Max | Min                                            | Max |      |
| General Timing Requirements |                    |                                               |                                             |     |                                                |     |      |
| 1                           | t <sub>DVCL</sub>  | Data in Setup                                 | 8                                           |     | 5                                              |     | ns   |
| 2                           | t <sub>CLDX</sub>  | Data in Hold <sup>(b)</sup>                   | 3                                           |     | 2                                              |     | ns   |
| General Timing Responses    |                    |                                               |                                             |     |                                                |     |      |
| 5                           | t <sub>CLAV</sub>  | AD Address Valid Delay and BHE                | 0                                           | 15  | 0                                              | 12  | ns   |
| 7                           | t <sub>CLDV</sub>  | Data Valid Delay                              | 0                                           | 15  | 0                                              | 12  | ns   |
| 8                           | t <sub>CHDX</sub>  | Status Hold Time                              | 0                                           |     | 0                                              |     | ns   |
| 9                           | t <sub>CHLH</sub>  | ALE Active Delay                              |                                             | 15  |                                                | 12  | ns   |
| 10                          | t <sub>LHLL</sub>  | ALE Width                                     | t <sub>CLCL</sub> −10=<br>20                |     | t <sub>CLCL</sub> −5=<br>20                    |     | ns   |
| 11                          | t <sub>CHLL</sub>  | ALE Inactive Delay                            |                                             | 15  |                                                | 12  | ns   |
| 23                          | t <sub>LHAV</sub>  | ALE High to Address Valid                     | 10                                          |     | 7.5                                            |     | ns   |
| 80                          | t <sub>CLCLX</sub> | LCS Inactive Delay                            | 0                                           | 15  | 0                                              | 12  | ns   |
| 81                          | t <sub>CLCSL</sub> | LCS Active Delay                              | 0                                           | 15  | 0                                              | 12  | ns   |
| 84                          | t <sub>LRLL</sub>  | LCS Precharge Pulse Width                     | t <sub>CLCL</sub> + t <sub>CLCH</sub><br>−3 |     | t <sub>CLCL</sub> + t <sub>CLCH</sub><br>−1.25 |     | ns   |
| Read Cycle Timing Responses |                    |                                               |                                             |     |                                                |     |      |
| 24                          | t <sub>AZRL</sub>  | AD Address Float to RD Active                 | 0                                           |     | 0                                              |     | ns   |
| 25                          | t <sub>CLRL</sub>  | RD Active Delay                               | 0                                           | 15  | 0                                              | 10  | ns   |
| 26                          | t <sub>RLRH</sub>  | RD Pulse Width                                | 2t <sub>CLCL</sub> −15<br>=45               |     | 2t <sub>CLCL</sub> −10<br>=40                  |     | ns   |
| 27                          | t <sub>CLRH</sub>  | RD Inactive Delay                             | 0                                           | 15  | 0                                              | 12  | ns   |
| 28                          | t <sub>RHLH</sub>  | RD Inactive to ALE High <sup>(a)</sup>        | t <sub>CLCH</sub> −3                        |     | t <sub>CLCH</sub> −1.25                        |     | ns   |
| 59                          | t <sub>RHDX</sub>  | RD High to Data Hold on AD Bus <sup>(b)</sup> | 0                                           |     | 0                                              |     | ns   |
| 66                          | t <sub>AVRL</sub>  | A Address Valid to RD Low                     | 2t <sub>CLCL</sub> −15<br>=45               |     | 2t <sub>CLCL</sub> −10<br>=40                  |     | ns   |
| 68                          | t <sub>CHAV</sub>  | CLKOUTA High to A Address Valid               | 0                                           | 15  | 0                                              | 10  | ns   |

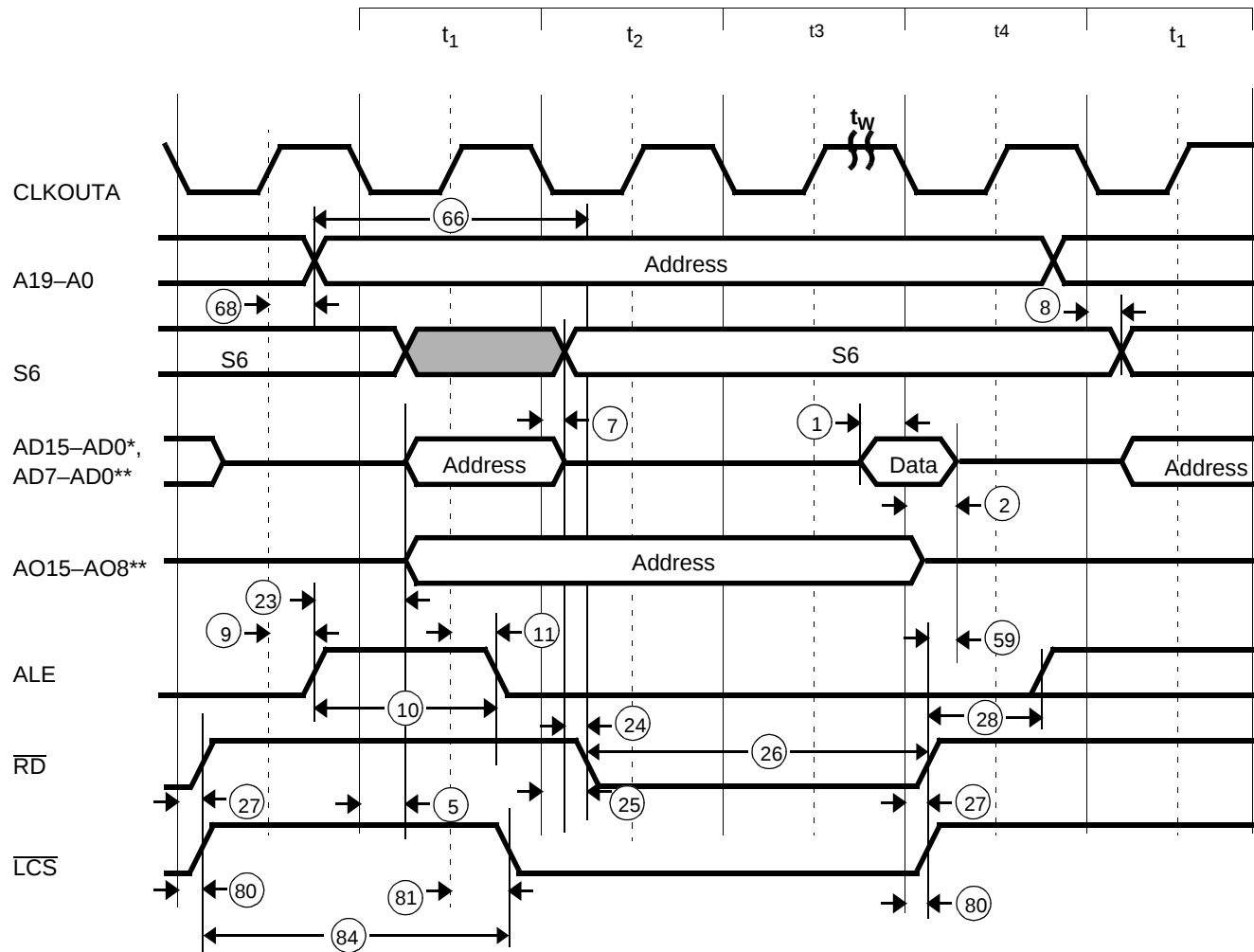
**Notes:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

## PSRAM Read Cycle Waveforms

**Notes:**

\* Am186EM microcontroller only

\*\* Am188EM microcontroller only

# SWITCHING CHARACTERISTICS over COMMERCIAL operating range

## PSRAM Write Cycle (20 MHz and 25 MHz)

| Parameter                    |                    |                                                            | Preliminary                               |     |                                           |     | Unit |
|------------------------------|--------------------|------------------------------------------------------------|-------------------------------------------|-----|-------------------------------------------|-----|------|
|                              |                    |                                                            | 20 MHz                                    |     | 25 MHz                                    |     |      |
| No.                          | Symbol             | Description                                                | Min                                       | Max | Min                                       | Max |      |
| General Timing Responses     |                    |                                                            |                                           |     |                                           |     |      |
| 5                            | t <sub>CLAV</sub>  | AD Address Valid Delay and BHE                             | 0                                         | 25  | 0                                         | 20  | ns   |
| 7                            | t <sub>CLDV</sub>  | Data Valid Delay                                           | 0                                         | 25  | 0                                         | 20  | ns   |
| 8                            | t <sub>CHDX</sub>  | Status Hold Time                                           | 0                                         |     | 0                                         |     | ns   |
| 9                            | t <sub>CHLH</sub>  | ALE Active Delay                                           |                                           | 25  |                                           | 20  | ns   |
| 10                           | t <sub>LHLL</sub>  | ALE Width                                                  | t <sub>CLCL</sub> –10=40                  |     | t <sub>CLCL</sub> –10=30                  |     | ns   |
| 11                           | t <sub>CHLL</sub>  | ALE Inactive Delay                                         |                                           | 25  |                                           | 20  | ns   |
| 23                           | t <sub>LHAV</sub>  | ALE High to Address Valid                                  | 20                                        |     | 15                                        |     | ns   |
| 20                           | t <sub>CVCTV</sub> | Control Active Delay 1 <sup>(b)</sup>                      | 0                                         | 25  | 0                                         | 20  | ns   |
| 80                           | t <sub>CLCLX</sub> | $\overline{LCS}$ Inactive Delay                            | 0                                         | 25  | 0                                         | 20  | ns   |
| 81                           | t <sub>CLCSL</sub> | $\overline{LCS}$ Active Delay                              | 0                                         | 25  | 0                                         | 20  | ns   |
| 84                           | t <sub>LRLL</sub>  | $\overline{LCS}$ Precharge Pulse Width                     | t <sub>CLCL</sub> + t <sub>CLCH</sub> – 3 |     | t <sub>CLCL</sub> + t <sub>CLCH</sub> – 3 |     |      |
| Write Cycle Timing Responses |                    |                                                            |                                           |     |                                           |     |      |
| 30                           | t <sub>CLDOX</sub> | Data Hold Time                                             | 0                                         |     | 0                                         |     | ns   |
| 31                           | t <sub>CVCTX</sub> | Control Inactive Delay <sup>(b)</sup>                      | 0                                         | 25  | 0                                         | 20  | ns   |
| 32                           | t <sub>WLWH</sub>  | $\overline{WR}$ Pulse Width                                | 2t <sub>CLCL</sub> –10 =90                |     | 2t <sub>CLCL</sub> –10 =70                |     | ns   |
| 33                           | t <sub>WHLH</sub>  | $\overline{WR}$ Inactive to ALE High <sup>(a)</sup>        | t <sub>CLCH</sub> –2                      |     | t <sub>CLCH</sub> –2                      |     | ns   |
| 34                           | t <sub>WHDX</sub>  | Data Hold after $\overline{WR}$ <sup>(a)</sup>             | t <sub>CLCL</sub> –10=40                  |     | t <sub>CLCL</sub> –10=30                  |     | ns   |
| 65                           | t <sub>AVWL</sub>  | A Address Valid to $\overline{WR}$ Low                     | t <sub>CLCL</sub> + t <sub>CHCL</sub> – 3 |     | t <sub>CLCL</sub> + t <sub>CHCL</sub> – 3 |     | ns   |
| 68                           | t <sub>CHAV</sub>  | CLKOUTA High to A Address Valid                            | 0                                         | 25  | 0                                         | 20  | ns   |
| 87                           | t <sub>AVBL</sub>  | A Address Valid to $\overline{WHB}$ , $\overline{WLB}$ Low | t <sub>CHCL</sub> –3                      | 25  | t <sub>CHCL</sub> –3                      | 20  | ns   |

**Notes:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b This parameter applies to the  $\overline{DEN}$ ,  $\overline{WR}$ ,  $\overline{WHB}$ , and  $\overline{WLB}$  signals.

# SWITCHING CHARACTERISTICS over COMMERCIAL operating range

## PSRAM Write Cycle (33 MHz and 40 MHz)

| Parameter                    |                    |                                                                          | Preliminary                              |     |                                             |     | Unit |
|------------------------------|--------------------|--------------------------------------------------------------------------|------------------------------------------|-----|---------------------------------------------|-----|------|
|                              |                    |                                                                          | 33 MHz                                   |     | 40 MHz                                      |     |      |
| No.                          | Symbol             | Description                                                              | Min                                      | Max | Min                                         | Max |      |
| General Timing Responses     |                    |                                                                          |                                          |     |                                             |     |      |
| 5                            | t <sub>CLAV</sub>  | AD Address Valid Delay and BHE                                           | 0                                        | 15  | 0                                           | 12  | ns   |
| 7                            | t <sub>CLDV</sub>  | Data Valid Delay                                                         | 0                                        | 15  | 0                                           | 12  | ns   |
| 8                            | t <sub>CHDX</sub>  | Status Hold Time                                                         | 0                                        |     | 0                                           |     | ns   |
| 9                            | t <sub>CHLH</sub>  | ALE Active Delay                                                         |                                          | 15  |                                             | 12  | ns   |
| 10                           | t <sub>LHLL</sub>  | ALE Width                                                                | t <sub>CLCL</sub> −10=20                 |     | t <sub>CLCL</sub> −5=20                     |     | ns   |
| 11                           | t <sub>CHLL</sub>  | ALE Inactive Delay                                                       |                                          | 15  |                                             | 12  | ns   |
| 20                           | t <sub>CVCTV</sub> | Control Active Delay 1 <sup>(b)</sup>                                    | 0                                        | 15  | 0                                           | 12  | ns   |
| 23                           | t <sub>LHAV</sub>  | ALE High to Address Valid                                                | 10                                       |     | 7.5                                         |     | ns   |
| 80                           | t <sub>CLCLX</sub> | $\overline{\text{LCS}}$ Inactive Delay                                   | 0                                        | 15  | 0                                           | 12  | ns   |
| 81                           | t <sub>CLCSL</sub> | $\overline{\text{LCS}}$ Active Delay                                     | 0                                        | 15  | 0                                           | 12  | ns   |
| 84                           | t <sub>LRLL</sub>  | $\overline{\text{LCS}}$ Precharge Pulse Width                            | t <sub>CLCL</sub> + t <sub>CLCH</sub> −3 |     | t <sub>CLCL</sub> + t <sub>CLCH</sub> −1.25 |     |      |
| Write Cycle Timing Responses |                    |                                                                          |                                          |     |                                             |     |      |
| 30                           | t <sub>CLDOX</sub> | Data Hold Time                                                           | 0                                        |     | 0                                           |     | ns   |
| 31                           | t <sub>CVCTX</sub> | Control Inactive Delay <sup>(b)</sup>                                    | 0                                        | 15  | 0                                           | 12  | ns   |
| 32                           | t <sub>WLWH</sub>  | $\overline{\text{WR}}$ Pulse Width                                       | 2t <sub>CLCL</sub> −10=50                |     | 2t <sub>CLCL</sub> −10=40                   |     | ns   |
| 33                           | t <sub>WHLH</sub>  | $\overline{\text{WR}}$ Inactive to ALE High <sup>(a)</sup>               | t <sub>CLCH</sub> −2                     |     | t <sub>CLCH</sub> −2                        |     | ns   |
| 34                           | t <sub>WHDX</sub>  | Data Hold after $\overline{\text{WR}}$ <sup>(a)</sup>                    | t <sub>CLCL</sub> −10=20                 |     | t <sub>CLCL</sub> −10=15                    |     | ns   |
| 65                           | t <sub>AVWL</sub>  | A Address Valid to $\overline{\text{WR}}$ Low                            | t <sub>CLCL</sub> +t <sub>CHCL</sub> −3  |     | t <sub>CLCL</sub> +t <sub>CHCL</sub> −1.25  |     | ns   |
| 68                           | t <sub>CHAV</sub>  | CLKOUTA High to A Address Valid                                          | 0                                        | 15  | 0                                           | 10  | ns   |
| 87                           | t <sub>AVBL</sub>  | A Address Valid to $\overline{\text{WHB}}$ , $\overline{\text{WLB}}$ Low | t <sub>CHCL</sub> −3                     | 15  | t <sub>CHCL</sub> −1.25                     | 12  | ns   |

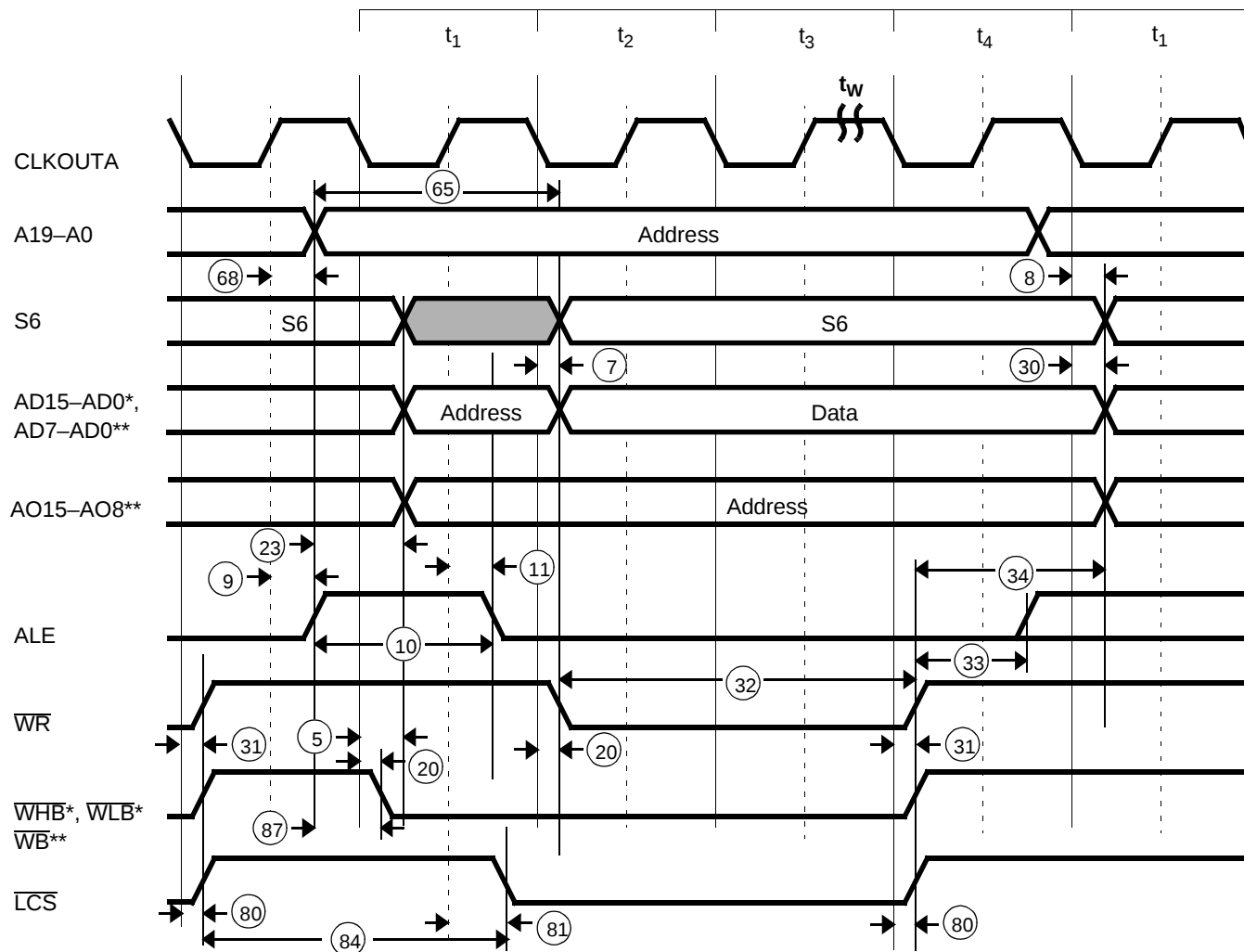
**Notes:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b This parameter applies to the  $\overline{DEN}$ ,  $\overline{WR}$ ,  $\overline{WHB}$ , and  $\overline{WLB}$  signals.

# PSRAM Write Cycle Waveforms



## Notes:

\* Am186EM microcontroller only

\*\* Am188EM microcontroller only

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

### PSRAM Refresh Cycle (20 MHz and 25 MHz)

| Parameter                         |                    |                                                             | Preliminary                   |     |                               |     | Unit |
|-----------------------------------|--------------------|-------------------------------------------------------------|-------------------------------|-----|-------------------------------|-----|------|
|                                   |                    |                                                             | 20 MHz                        |     | 25 MHz                        |     |      |
| No.                               | Symbol             | Description                                                 | Min                           | Max | Min                           | Max |      |
| General Timing Responses          |                    |                                                             |                               |     |                               |     |      |
| 9                                 | t <sub>CHLH</sub>  | ALE Active Delay                                            |                               | 25  |                               | 20  | ns   |
| 10                                | t <sub>LHLL</sub>  | ALE Width                                                   | t <sub>CLCL</sub> −10=<br>40  |     | t <sub>CLCL</sub> −10=<br>30  |     | ns   |
| 11                                | t <sub>CHLL</sub>  | ALE Inactive Delay                                          |                               | 25  |                               | 20  | ns   |
| Read/Write Cycle Timing Responses |                    |                                                             |                               |     |                               |     |      |
| 25                                | t <sub>CLRL</sub>  | $\overline{RD}$ Active Delay                                | 0                             | 25  | 0                             | 20  | ns   |
| 26                                | t <sub>RLRH</sub>  | $\overline{RD}$ Pulse Width                                 | 2t <sub>CLCL</sub> −15<br>=85 |     | 2t <sub>CLCL</sub> −15<br>=65 |     | ns   |
| 27                                | t <sub>CLRH</sub>  | $\overline{RD}$ Inactive Delay                              | 0                             | 25  | 0                             | 20  | ns   |
| 28                                | t <sub>RHLH</sub>  | $\overline{RD}$ Inactive to ALE High <sup>(a)</sup>         | t <sub>CLCH</sub> −3          |     | t <sub>CLCH</sub> −3          |     | ns   |
| 80                                | t <sub>CLCLX</sub> | $\overline{LCS}$ Inactive Delay                             | 0                             | 25  | 0                             | 20  | ns   |
| 81                                | t <sub>CLCSL</sub> | $\overline{LCS}$ Active Delay                               | 0                             | 25  | 0                             | 20  | ns   |
| Refresh Timing Cycle Parameters   |                    |                                                             |                               |     |                               |     |      |
| 79                                | t <sub>CLRFD</sub> | CLKOUTA Low to $\overline{RFSH}$ Valid                      | 0                             | 25  | 0                             | 20  | ns   |
| 82                                | t <sub>CLRF</sub>  | CLKOUTA High to $\overline{RFSH}$ Invalid                   | 0                             | 25  | 0                             | 20  | ns   |
| 85                                | t <sub>RFCY</sub>  | $\overline{RFSH}$ Cycle Time                                | 6 • t <sub>CLCL</sub>         |     | 6 • t <sub>CLCL</sub>         |     | ns   |
| 86                                | t <sub>LCRF</sub>  | $\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay | 2t <sub>CLCL</sub> −3         |     | 2t <sub>CLCL</sub> −3         |     |      |

**Note:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

### PSRAM Refresh Cycle (33 MHz and 40 MHz)

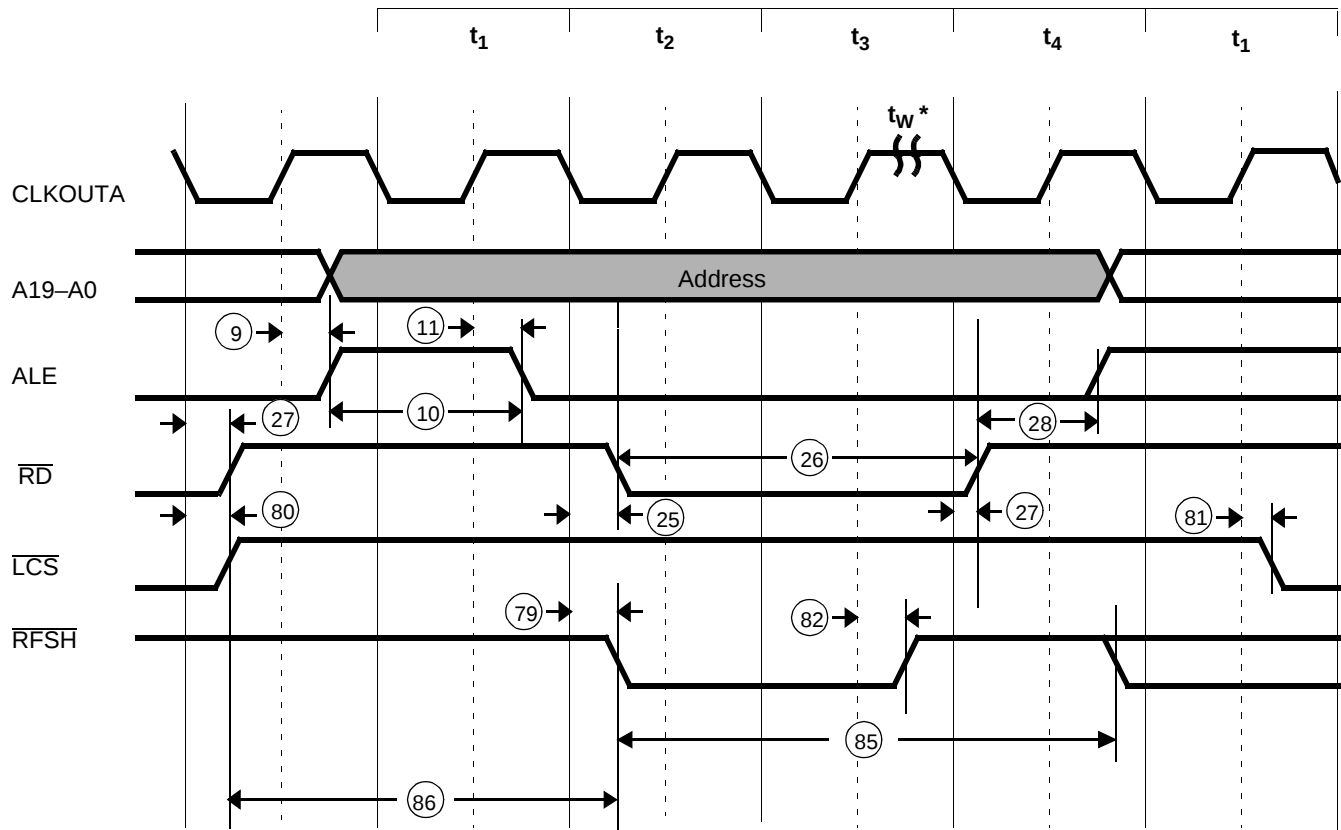
| Parameter                         |                    |                                                             | Preliminary                  |     |                              |     | Unit |
|-----------------------------------|--------------------|-------------------------------------------------------------|------------------------------|-----|------------------------------|-----|------|
|                                   |                    |                                                             | 33 MHz                       |     | 40 MHz                       |     |      |
| No.                               | Symbol             | Description                                                 | Min                          | Max | Min                          | Max |      |
| General Timing Responses          |                    |                                                             |                              |     |                              |     |      |
| 9                                 | t <sub>CHLH</sub>  | ALE Active Delay                                            |                              | 15  |                              | 12  | ns   |
| 10                                | t <sub>LHLL</sub>  | ALE Width                                                   | t <sub>CLCL</sub> − 10 = 20  |     | t <sub>CLCL</sub> − 5 = 20   |     | ns   |
| 11                                | t <sub>CHLL</sub>  | ALE Inactive Delay                                          |                              | 15  |                              | 12  | ns   |
| Read/Write Cycle Timing Responses |                    |                                                             |                              |     |                              |     |      |
| 25                                | t <sub>CLRL</sub>  | $\overline{RD}$ Active Delay                                | 0                            | 15  | 0                            | 10  | ns   |
| 26                                | t <sub>RLRH</sub>  | $\overline{RD}$ Pulse Width                                 | 2t <sub>CLCL</sub> − 15 = 45 |     | 2t <sub>CLCL</sub> − 10 = 40 |     | ns   |
| 27                                | t <sub>CLRH</sub>  | $\overline{RD}$ Inactive Delay                              | 0                            | 15  | 0                            | 12  | ns   |
| 28                                | t <sub>RHLH</sub>  | $\overline{RD}$ Inactive to ALE High <sup>(a)</sup>         | t <sub>CLCH</sub> − 3        |     | t <sub>CLCH</sub> − 2        |     | ns   |
| 80                                | t <sub>CLCLX</sub> | $\overline{LCS}$ Inactive Delay                             | 0                            | 15  | 0                            | 12  | ns   |
| 81                                | t <sub>CLCSL</sub> | $\overline{LCS}$ Active Delay                               | 0                            | 15  | 0                            | 12  | ns   |
| Refresh Timing Cycle Parameters   |                    |                                                             |                              |     |                              |     |      |
| 79                                | t <sub>CLRFD</sub> | CLKOUTA Low to $\overline{RFSH}$ Valid                      | 0                            | 15  | 0                            | 12  | ns   |
| 82                                | t <sub>CLRF</sub>  | CLKOUTA High to $\overline{RFSH}$ Invalid                   | 0                            | 15  | 0                            | 12  | ns   |
| 85                                | t <sub>RFCY</sub>  | $\overline{RFSH}$ Cycle Time                                | 6 • t <sub>CLCL</sub>        |     | 6 • t <sub>CLCL</sub>        |     | ns   |
| 86                                | t <sub>LCRF</sub>  | $\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay | 2t <sub>CLCL</sub> − 3       |     | 2t <sub>CLCL</sub> − 1.25    |     |      |

**Note:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

## PSRAM Refresh Cycle Waveforms

**Note:**

\* The period  $t_w$  is fixed at 3 wait states for PSRAM auto refresh only.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

### Interrupt Acknowledge Cycle (20 MHz and 25 MHz)

| Parameter                   |                    |                                                                    | Preliminary              |     |                          |     | Unit |
|-----------------------------|--------------------|--------------------------------------------------------------------|--------------------------|-----|--------------------------|-----|------|
|                             |                    |                                                                    | 20 MHz                   |     | 25 MHz                   |     |      |
| No.                         | Symbol             | Description                                                        | Min                      | Max | Min                      | Max |      |
| General Timing Requirements |                    |                                                                    |                          |     |                          |     |      |
| 1                           | t <sub>DVCL</sub>  | Data in Setup                                                      | 10                       |     | 10                       |     | ns   |
| 2                           | t <sub>CLDX</sub>  | Data in Hold                                                       | 3                        |     | 3                        |     | ns   |
| General Timing Responses    |                    |                                                                    |                          |     |                          |     |      |
| 3                           | t <sub>CHSV</sub>  | Status Active Delay                                                | 0                        | 25  | 0                        | 20  | ns   |
| 4                           | t <sub>CLSH</sub>  | Status Inactive Delay                                              | 0                        | 25  | 0                        | 20  | ns   |
| 7                           | t <sub>CLDV</sub>  | Data Valid Delay                                                   | 0                        | 25  | 0                        | 20  | ns   |
| 8                           | t <sub>CHDX</sub>  | Status Hold Time                                                   | 0                        |     | 0                        |     | ns   |
| 9                           | t <sub>CHLH</sub>  | ALE Active Delay                                                   |                          | 25  |                          | 20  | ns   |
| 10                          | t <sub>LHLL</sub>  | ALE Width                                                          | t <sub>CLCL</sub> −10=40 |     | t <sub>CLCL</sub> −10=30 |     | ns   |
| 11                          | t <sub>CHLL</sub>  | ALE Inactive Delay                                                 |                          | 25  |                          | 20  | ns   |
| 12                          | t <sub>AVLL</sub>  | AD Address Invalid to ALE Low <sup>(a)</sup>                       | t <sub>CLCH</sub>        |     | t <sub>CLCH</sub>        |     | ns   |
| 15                          | t <sub>CLAZ</sub>  | AD Address Float Delay                                             | t <sub>CLAX</sub> =0     | 25  | t <sub>CLAX</sub> =0     | 20  | ns   |
| 19                          | t <sub>DXDL</sub>  | $\overline{DEN}$ Inactive to DT/ $\overline{R}$ Low <sup>(a)</sup> | 0                        |     | 0                        |     | ns   |
| 20                          | t <sub>CVCTV</sub> | Control Active Delay 1 <sup>(b)</sup>                              | 0                        | 25  | 0                        | 20  | ns   |
| 21                          | t <sub>CVDEX</sub> | $\overline{DEN}$ Inactive Delay                                    | 0                        | 25  | 0                        | 20  | ns   |
| 22                          | t <sub>CHCTV</sub> | Control Active Delay 2 <sup>(c)</sup>                              | 0                        | 25  | 0                        | 20  | ns   |
| 23                          | t <sub>LHAV</sub>  | ALE High to Address Valid                                          | 20                       |     | 15                       |     | ns   |
| 31                          | t <sub>CVCTX</sub> | Control Inactive Delay <sup>(b)</sup>                              | 0                        | 25  | 0                        | 20  | ns   |
| 68                          | t <sub>CHAV</sub>  | CLKOUTA High to A Address Valid                                    | 0                        | 25  | 0                        | 20  | ns   |

#### Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b This parameter applies to the  $\overline{INTA1}$ – $\overline{INTA0}$  signals.

c This parameter applies to the  $\overline{DEN}$  and DT/ $\overline{R}$  signals.

# SWITCHING CHARACTERISTICS over COMMERCIAL operating range

## Interrupt Acknowledge Cycle (33 MHz and 40 MHz)

| Parameter                   |                    |                                                      | Preliminary              |     |                         |     | Unit |
|-----------------------------|--------------------|------------------------------------------------------|--------------------------|-----|-------------------------|-----|------|
|                             |                    |                                                      | 33 MHz                   |     | 40 MHz                  |     |      |
| No.                         | Symbol             | Description                                          | Min                      | Max | Min                     | Max |      |
| General Timing Requirements |                    |                                                      |                          |     |                         |     |      |
| 1                           | t <sub>DVCL</sub>  | Data in Setup                                        | 8                        |     | 5                       |     | ns   |
| 2                           | t <sub>CLDX</sub>  | Data in Hold                                         | 3                        |     | 2                       |     | ns   |
| General Timing Responses    |                    |                                                      |                          |     |                         |     |      |
| 3                           | t <sub>CHSV</sub>  | Status Active Delay                                  | 0                        | 15  | 0                       | 12  | ns   |
| 4                           | t <sub>CLSH</sub>  | Status Inactive Delay                                | 0                        | 15  | 0                       | 12  | ns   |
| 7                           | t <sub>CLDV</sub>  | Data Valid Delay                                     | 0                        | 15  | 0                       | 12  | ns   |
| 8                           | t <sub>CHDX</sub>  | Status Hold Time                                     | 0                        |     | 0                       |     | ns   |
| 9                           | t <sub>CHLH</sub>  | ALE Active Delay                                     |                          | 15  |                         | 12  | ns   |
| 10                          | t <sub>LHLL</sub>  | ALE Width                                            | t <sub>CLCL</sub> −10=20 |     | t <sub>CLCL</sub> −5=20 |     | ns   |
| 11                          | t <sub>CHLL</sub>  | ALE Inactive Delay                                   |                          | 15  |                         | 12  | ns   |
| 12                          | t <sub>AVLL</sub>  | AD Address Invalid to ALE Low <sup>(a)</sup>         | t <sub>CLCH</sub>        |     | t <sub>CLCH</sub>       |     | ns   |
| 15                          | t <sub>CLAZ</sub>  | AD Address Float Delay                               | t <sub>CLAX</sub> =0     | 15  | t <sub>CLAX</sub> =0    | 12  | ns   |
| 19                          | t <sub>DXDL</sub>  | $\overline{DEN}$ Inactive to DT/R Low <sup>(a)</sup> | 0                        |     | 0                       |     | ns   |
| 20                          | t <sub>CVCTV</sub> | Control Active Delay 1 <sup>(b)</sup>                | 0                        | 15  | 0                       | 12  | ns   |
| 21                          | t <sub>CVDEX</sub> | $\overline{DEN}$ Inactive Delay                      | 0                        | 15  | 0                       | 12  | ns   |
| 22                          | t <sub>CHCTV</sub> | Control Active Delay 2 <sup>(c)</sup>                | 0                        | 15  | 0                       | 12  | ns   |
| 23                          | t <sub>LHAV</sub>  | ALE High to Address Valid                            | 10                       |     | 7.5                     |     | ns   |
| 31                          | t <sub>CVCTX</sub> | Control Inactive Delay <sup>(b)</sup>                | 0                        | 15  | 0                       | 12  | ns   |
| 68                          | t <sub>CHAV</sub>  | CLKOUTA High to A Address Valid                      | 0                        | 15  | 0                       | 10  | ns   |

**Notes:**

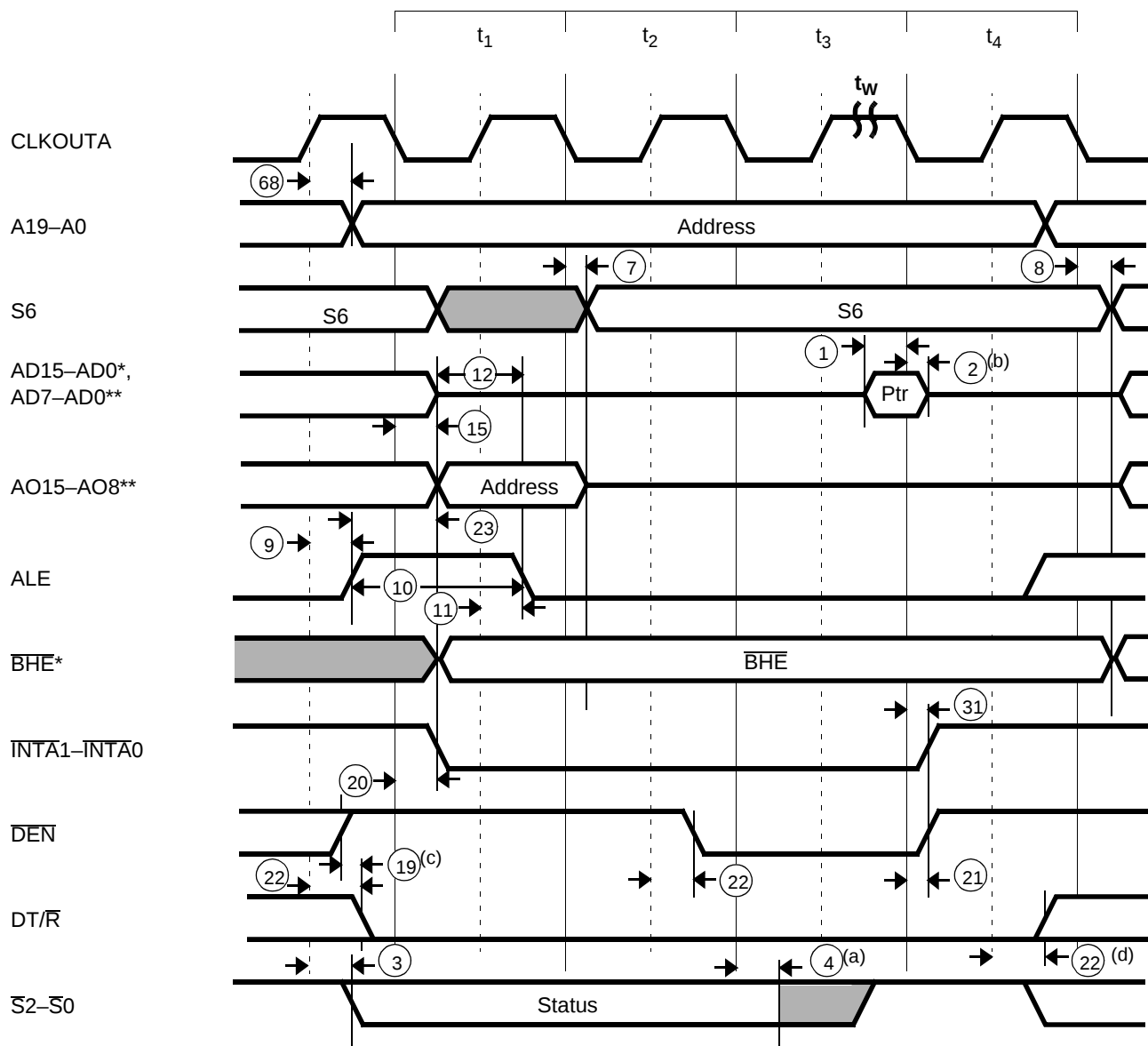
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b This parameter applies to the  $\overline{INTA1}$ – $\overline{INTA0}$  signals.

c This parameter applies to the  $\overline{DEN}$  and DT/ $\overline{R}$  signals.

# Interrupt Acknowledge Cycle Waveforms



## Notes:

\* Am186EM microcontroller only

\*\* Am188EM microcontroller only

a The status bits become inactive in the state preceding  $t_4$ .

b The data hold time lasts only until the interrupt acknowledge signal deasserts, even if the interrupt acknowledge transition occurs prior to  $t_{CLDX} (min)$ .

c This parameter applies for an interrupt acknowledge cycle that follows a write cycle.

d If followed by a write cycle, this change occurs in the state preceding that write cycle.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

### Software Halt Cycle (20 MHz and 25 MHz)

| Parameter                |                    |                                                                    | Preliminary              |     |                          |     | Unit |
|--------------------------|--------------------|--------------------------------------------------------------------|--------------------------|-----|--------------------------|-----|------|
|                          |                    |                                                                    | 20 MHz                   |     | 25 MHz                   |     |      |
| No.                      | Symbol             | Description                                                        | Min                      | Max | Min                      | Max |      |
| General Timing Responses |                    |                                                                    |                          |     |                          |     |      |
| 3                        | t <sub>CHSV</sub>  | Status Active Delay                                                | 0                        | 25  | 0                        | 20  | ns   |
| 4                        | t <sub>CLSH</sub>  | Status Inactive Delay                                              | 0                        | 25  | 0                        | 20  | ns   |
| 5                        | t <sub>CLAV</sub>  | AD Address Invalid Delay and BHE                                   | 0                        | 25  | 0                        | 20  | ns   |
| 9                        | t <sub>CHLH</sub>  | ALE Active Delay                                                   |                          | 25  |                          | 20  | ns   |
| 10                       | t <sub>LHLL</sub>  | ALE Width                                                          | t <sub>CLCL</sub> −10=40 |     | t <sub>CLCL</sub> −10=30 |     | ns   |
| 11                       | t <sub>CHLL</sub>  | ALE Inactive Delay                                                 |                          | 25  |                          | 20  | ns   |
| 19                       | t <sub>DXDL</sub>  | $\overline{DEN}$ Inactive to DT/ $\overline{R}$ Low <sup>(a)</sup> | 0                        |     | 0                        |     | ns   |
| 22                       | t <sub>CHCTV</sub> | Control Active Delay 2 <sup>(b)</sup>                              | 0                        | 25  | 0                        | 20  | ns   |
| 68                       | t <sub>CHAV</sub>  | CLKOUTA High to A Address Invalid                                  | 0                        | 25  | 0                        | 20  | ns   |

**Notes:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b This parameter applies to the  $\overline{DEN}$  signal.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

### Software Halt Cycle (33 MHz and 40 MHz)

| Parameter                |                    |                                         | Preliminary              |     |                         |     | Unit |
|--------------------------|--------------------|-----------------------------------------|--------------------------|-----|-------------------------|-----|------|
|                          |                    |                                         | 33 MHz                   |     | 40 MHz                  |     |      |
| No.                      | Symbol             | Description                             | Min                      | Max | Min                     | Max |      |
| General Timing Responses |                    |                                         |                          |     |                         |     |      |
| 3                        | t <sub>CHSV</sub>  | Status Active Delay                     | 0                        | 15  | 0                       | 12  | ns   |
| 4                        | t <sub>CLSH</sub>  | Status Inactive Delay                   | 0                        | 15  | 0                       | 12  | ns   |
| 5                        | t <sub>CLAV</sub>  | AD Address Invalid Delay and BHE        | 0                        | 15  | 0                       | 12  | ns   |
| 9                        | t <sub>CHLH</sub>  | ALE Active Delay                        |                          | 15  |                         | 12  | ns   |
| 10                       | t <sub>LHLL</sub>  | ALE Width                               | t <sub>CLCL</sub> −10=20 |     | t <sub>CLCL</sub> −5=20 |     | ns   |
| 11                       | t <sub>CHLL</sub>  | ALE Inactive Delay                      |                          | 15  |                         | 12  | ns   |
| 19                       | t <sub>DXDL</sub>  | DEN Inactive to DT/R Low <sup>(a)</sup> | 0                        |     | 0                       |     | ns   |
| 22                       | t <sub>CHCTV</sub> | Control Active Delay 2 <sup>(b)</sup>   | 0                        | 15  | 0                       | 12  | ns   |
| 68                       | t <sub>CHAV</sub>  | CLKOUTA High to A Address Invalid       | 0                        | 15  | 0                       | 10  | ns   |

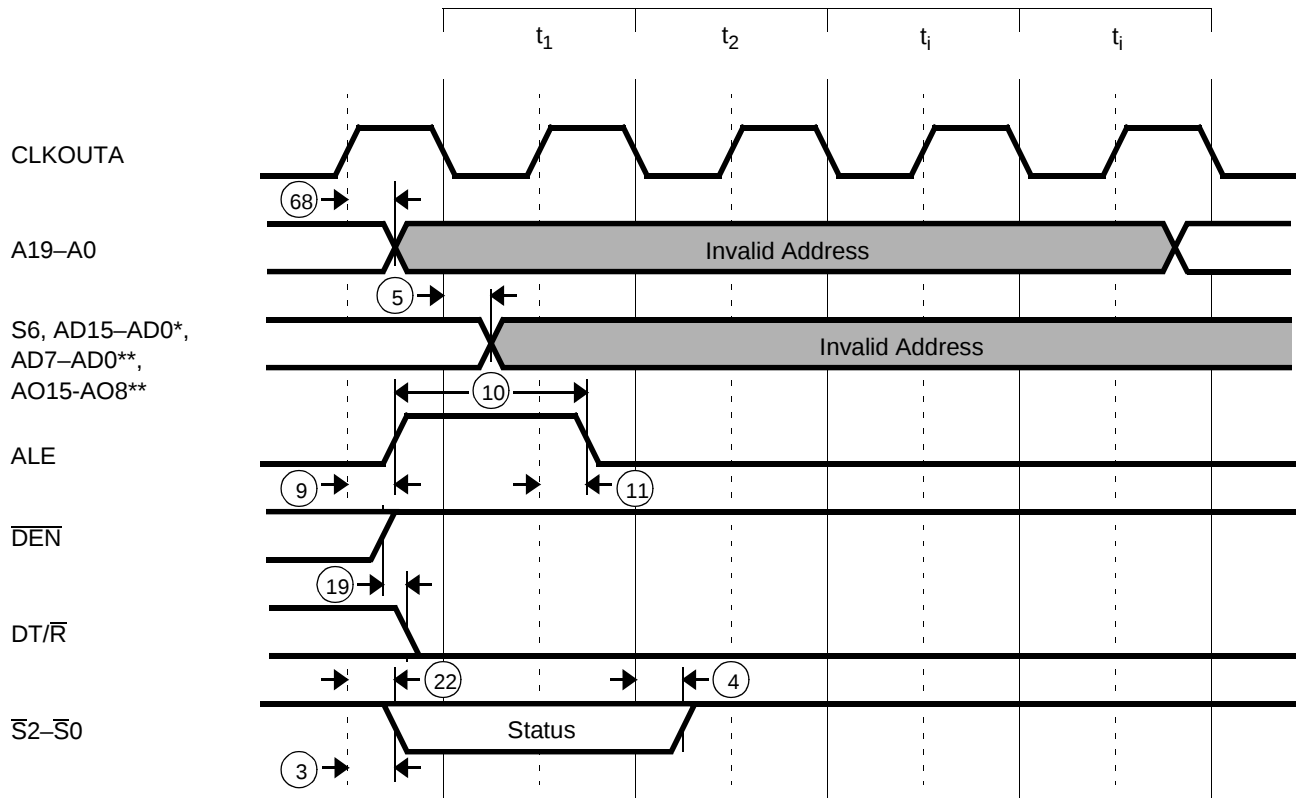
#### Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a Equal loading on referenced pins.

b This parameter applies to the  $\overline{DEN}$  signal.

## Software Halt Cycle Waveforms

**Notes:**

\* Am186EM microcontroller only

\*\* Am188EM microcontroller only

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

### Clock (20 MHz and 25 MHz)

| Parameter          |                     |                                            | Preliminary                    |     |                                |     | Unit |
|--------------------|---------------------|--------------------------------------------|--------------------------------|-----|--------------------------------|-----|------|
|                    |                     |                                            | 20 MHz                         |     | 25 MHz                         |     |      |
| No.                | Symbol              | Description                                | Min                            | Max | Min                            | Max |      |
| CLKIN Requirements |                     |                                            |                                |     |                                |     |      |
| 36                 | t <sub>CKIN</sub>   | X1 Period <sup>(a)</sup>                   | 50                             | 60  | 40                             | 60  | ns   |
| 37                 | t <sub>CLCK</sub>   | X1 Low Time (1.5 V) <sup>(a)</sup>         | 15                             |     | 15                             |     | ns   |
| 38                 | t <sub>CHCK</sub>   | X1 High Time (1.5 V) <sup>(a)</sup>        | 15                             |     | 15                             |     | ns   |
| 39                 | t <sub>CKHL</sub>   | X1 Fall Time (3.5 to 1.0 V) <sup>(a)</sup> |                                | 5   |                                | 5   | ns   |
| 40                 | t <sub>CKLH</sub>   | X1 Rise Time (1.0 to 3.5 V) <sup>(a)</sup> |                                | 5   |                                | 5   | ns   |
| CLKOUT Timing      |                     |                                            |                                |     |                                |     |      |
| 42                 | t <sub>CLCL</sub>   | CLKOUTA Period                             | 50                             |     | 40                             |     | ns   |
| 43                 | t <sub>CLCH</sub>   | CLKOUTA Low Time (C <sub>L</sub> =50 pF)   | 0.5t <sub>CLCL</sub> −2<br>=23 |     | 0.5t <sub>CLCL</sub> −2<br>=18 |     | ns   |
| 44                 | t <sub>CHCL</sub>   | CLKOUTA High Time (C <sub>L</sub> =50 pF)  | 0.5t <sub>CLCL</sub> −2<br>=23 |     | 0.5t <sub>CLCL</sub> −2<br>=18 |     | ns   |
| 45                 | t <sub>CH1CH2</sub> | CLKOUTA Rise Time (1.0 to 3.5 V)           |                                | 3   |                                | 3   | ns   |
| 46                 | t <sub>CL2CL1</sub> | CLKOUTA Fall Time (3.5 to 1.0 V)           |                                | 3   |                                | 3   | ns   |
| 61                 | t <sub>LOCK</sub>   | Maximum PLL Lock Time                      |                                | 1   |                                | 1   | ms   |
| 69                 | t <sub>CICOA</sub>  | X1 to CLKOUTA Skew                         |                                | 15  |                                | 15  | ns   |
| 70                 | t <sub>CICOB</sub>  | X1 to CLKOUTB Skew                         |                                | 21  |                                | 21  | ns   |

#### Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a The specifications for CLKIN are applicable to the normal PLL and CLKDIV2 modes.

The PLL should be used for operations from 16.667 MHz to 40 MHz. For operations below 16.667 MHz, the CLKDIV2 mode should be used.

Because the CLKDIV2 input frequency is two times the system frequency, the specifications for twice the frequency should be used for CLKDIV2 mode. For example, use the 20 MHz CLKIN specifications for 10 MHz operation.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

### Clock (33 MHz and 40 MHz)

| Parameter          |                     |                                            | Preliminary                       |     |                                     |     | Unit |
|--------------------|---------------------|--------------------------------------------|-----------------------------------|-----|-------------------------------------|-----|------|
|                    |                     |                                            | 33 MHz                            |     | 40 MHz                              |     |      |
| No.                | Symbol              | Description                                | Min                               | Max | Min                                 | Max |      |
| CLKIN Requirements |                     |                                            |                                   |     |                                     |     |      |
| 36                 | t <sub>CKIN</sub>   | X1 Period <sup>(a)</sup>                   | 30                                | 60  | 25                                  | 60  | ns   |
| 37                 | t <sub>CLCK</sub>   | X1 Low Time (1.5 V) <sup>(a)</sup>         | 10                                |     | 7.5                                 |     | ns   |
| 38                 | t <sub>CHCK</sub>   | X1 High Time (1.5 V) <sup>(a)</sup>        | 10                                |     | 7.5                                 |     | ns   |
| 39                 | t <sub>CKHL</sub>   | X1 Fall Time (3.5 to 1.0 V) <sup>(a)</sup> |                                   | 5   |                                     | 5   | ns   |
| 40                 | t <sub>CKLH</sub>   | X1 Rise Time (1.0 to 3.5 V) <sup>(a)</sup> |                                   | 5   |                                     | 5   | ns   |
| CLKOUT Timing      |                     |                                            |                                   |     |                                     |     |      |
| 42                 | t <sub>CLCL</sub>   | CLKOUTA Period                             | 30                                |     | 25                                  |     | ns   |
| 43                 | t <sub>CLCH</sub>   | CLKOUTA Low Time (C <sub>L</sub> = 50 pF)  | 0.5t <sub>CLCL</sub> – 1.5 = 13.5 |     | 0.5t <sub>CLCL</sub> – 1.25 = 11.25 |     | ns   |
| 44                 | t <sub>CHCL</sub>   | CLKOUTA High Time (C <sub>L</sub> = 50 pF) | 0.5t <sub>CLCL</sub> – 1.5 = 13.5 |     | 0.5t <sub>CLCL</sub> – 1.25 = 11.25 |     | ns   |
| 45                 | t <sub>CH1CH2</sub> | CLKOUTA Rise Time (1.0 to 3.5 V)           |                                   | 3   |                                     | 3   | ns   |
| 46                 | t <sub>CL2CL1</sub> | CLKOUTA Fall Time (3.5 to 1.0 V)           |                                   | 3   |                                     | 3   | ns   |
| 61                 | t <sub>LOCK</sub>   | Maximum PLL Lock Time                      |                                   | 1   |                                     | 1   | ms   |
| 69                 | t <sub>CICOA</sub>  | X1 to CLKOUTA Skew                         |                                   | 15  |                                     | 15  | ns   |
| 70                 | t <sub>CICOB</sub>  | X1 to CLKOUTB Skew                         |                                   | 21  |                                     | 21  | ns   |

#### Notes:

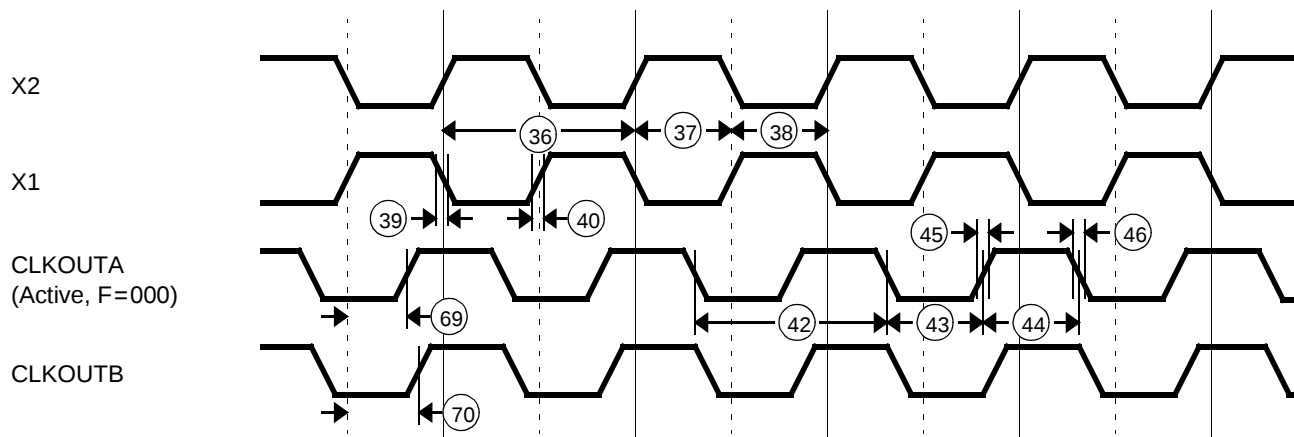
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C<sub>L</sub> = 50 pF. For switching tests, V<sub>IL</sub> = 0.45 V and V<sub>IH</sub> = 2.4 V, except at X1 where V<sub>IH</sub> = V<sub>CC</sub> - 0.5 V.

a The specifications for CLKIN are applicable to the normal PLL and CLKDIV2 modes.

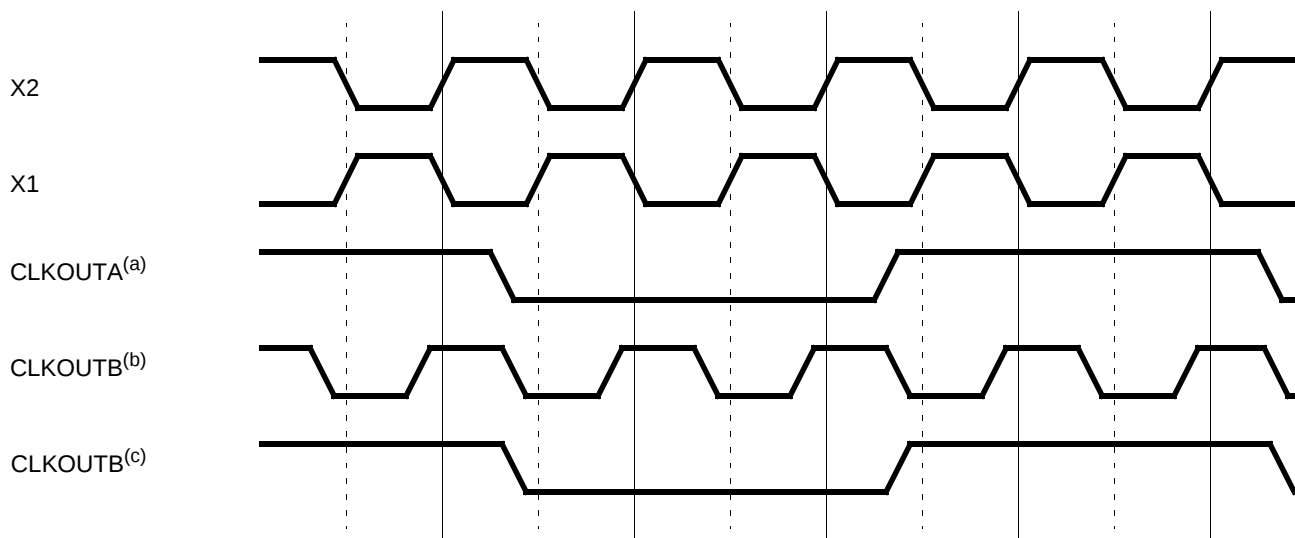
The PLL should be used for operations from 16.667 MHz to 40 MHz. For operations below 16.667 MHz, the CLKDIV2 mode should be used.

Because the CLKDIV2 input frequency is two times the system frequency, the specifications for twice the frequency should be used for CLKDIV2 mode. For example, use the 20 MHz CLKIN specifications for 10 MHz operation.

## Clock Waveforms—Active Mode



## Clock Waveforms—Power-Save Mode



### Notes:

- a The Clock Divisor Select (F2–F0) bits in the Power Save Control Register (PDCON) are set to 010 (divide by 4).
- b The CLKOUTB Output Frequency (CBF) bit in the Power Save Control Register (PDCON) is set to 1.
- c The CLKOUTB Output Frequency (CBF) bit in the Power Save Control Register (PDCON) is set to 0.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

### Ready and Peripheral Timing (20 MHz and 25 MHz)

| Parameter                                |                      |                                                      | Preliminary |     | Preliminary |     | Unit |
|------------------------------------------|----------------------|------------------------------------------------------|-------------|-----|-------------|-----|------|
|                                          |                      |                                                      | 20 MHz      |     | 25 MHz      |     |      |
| No.                                      | Symbol               | Description                                          | Min         | Max | Min         | Max |      |
| Ready and Peripheral Timing Requirements |                      |                                                      |             |     |             |     |      |
| 47                                       | t <sub>SR YCL</sub>  | SRDY Transition Setup Time <sup>(a)</sup>            | 10          |     | 10          |     | ns   |
| 48                                       | t <sub>CL SRY</sub>  | SRDY Transition Hold Time <sup>(a)</sup>             | 3           |     | 3           |     | ns   |
| 49                                       | t <sub>AR YCH</sub>  | ARDY Resolution Transition Setup Time <sup>(b)</sup> | 10          |     | 10          |     | ns   |
| 50                                       | t <sub>CL ARX</sub>  | ARDY Active Hold Time <sup>(a)</sup>                 | 4           |     | 4           |     | ns   |
| 51                                       | t <sub>AR YCHL</sub> | ARDY Inactive Holding Time                           | 6           |     | 6           |     | ns   |
| 52                                       | t <sub>AR YLCL</sub> | ARDY Setup Time <sup>(a)</sup>                       | 15          |     | 15          |     | ns   |
| 53                                       | t <sub>INVCH</sub>   | Peripheral Setup Time <sup>(b)</sup>                 | 10          |     | 10          |     | ns   |
| 54                                       | t <sub>INVCL</sub>   | DRQ Setup Time <sup>(b)</sup>                        | 10          |     | 10          |     | ns   |
| Peripheral Timing Responses              |                      |                                                      |             |     |             |     |      |
| 55                                       | t <sub>CL TMV</sub>  | Timer Output Delay                                   |             | 25  |             | 20  | ns   |

#### Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{\text{IL}} = 0.45$  V and  $V_{\text{IH}} = 2.4$  V, except at X1 where  $V_{\text{IH}} = V_{\text{CC}} - 0.5$  V.

a This timing must be met to guarantee proper operation.

b This timing must be met to guarantee recognition at the clock edge.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

### Ready and Peripheral Timing (33 MHz and 40 MHz)

| Parameter                                |                     |                                                      | Preliminary |     |        |     | Unit |
|------------------------------------------|---------------------|------------------------------------------------------|-------------|-----|--------|-----|------|
|                                          |                     |                                                      | 33 MHz      |     | 40 MHz |     |      |
| No.                                      | Symbol              | Description                                          | Min         | Max | Min    | Max |      |
| Ready and Peripheral Timing Requirements |                     |                                                      |             |     |        |     |      |
| 47                                       | t <sub>SRYCL</sub>  | SRDY Transition Setup Time <sup>(a)</sup>            | 8           |     | 5      |     | ns   |
| 48                                       | t <sub>CLSRY</sub>  | SRDY Transition Hold Time <sup>(a)</sup>             | 3           |     | 2      |     | ns   |
| 49                                       | t <sub>ARYCH</sub>  | ARDY Resolution Transition Setup Time <sup>(b)</sup> | 8           |     | 5      |     | ns   |
| 50                                       | t <sub>CLARX</sub>  | ARDY Active Hold Time <sup>(a)</sup>                 | 4           |     | 3      |     | ns   |
| 51                                       | t <sub>ARYCHL</sub> | ARDY Inactive Holding Time                           | 6           |     | 5      |     | ns   |
| 52                                       | t <sub>ARYLCL</sub> | ARDY Setup Time <sup>(a)</sup>                       | 10          |     | 5      |     | ns   |
| 53                                       | t <sub>INVCH</sub>  | Peripheral Setup Time <sup>(b)</sup>                 | 8           |     | 5      |     | ns   |
| 54                                       | t <sub>INVCL</sub>  | DRQ Setup Time <sup>(b)</sup>                        | 8           |     | 5      |     | ns   |
| Peripheral Timing Responses              |                     |                                                      |             |     |        |     |      |
| 55                                       | t <sub>CLTMV</sub>  | Timer Output Delay                                   |             | 15  |        | 12  | ns   |

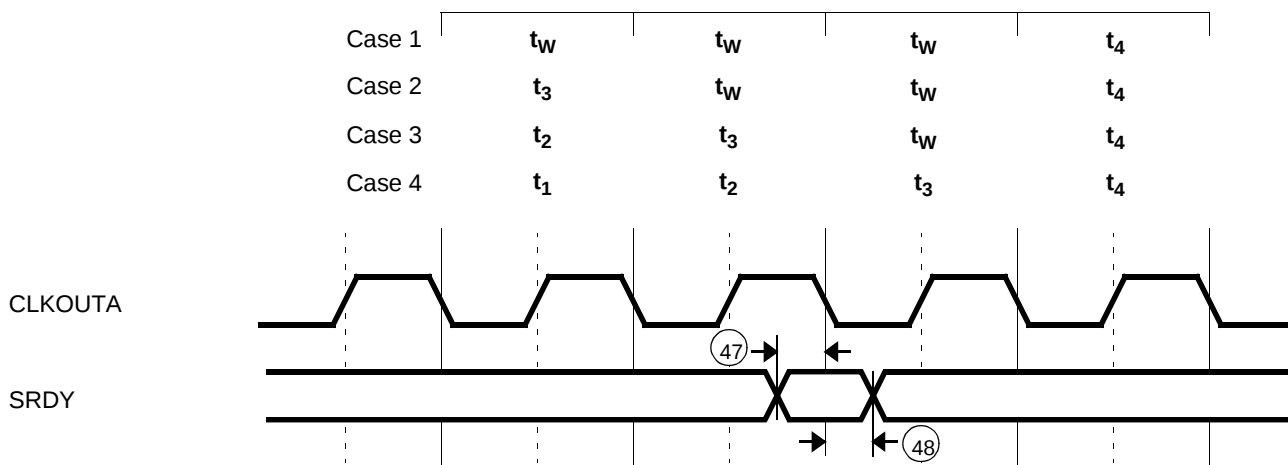
#### Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

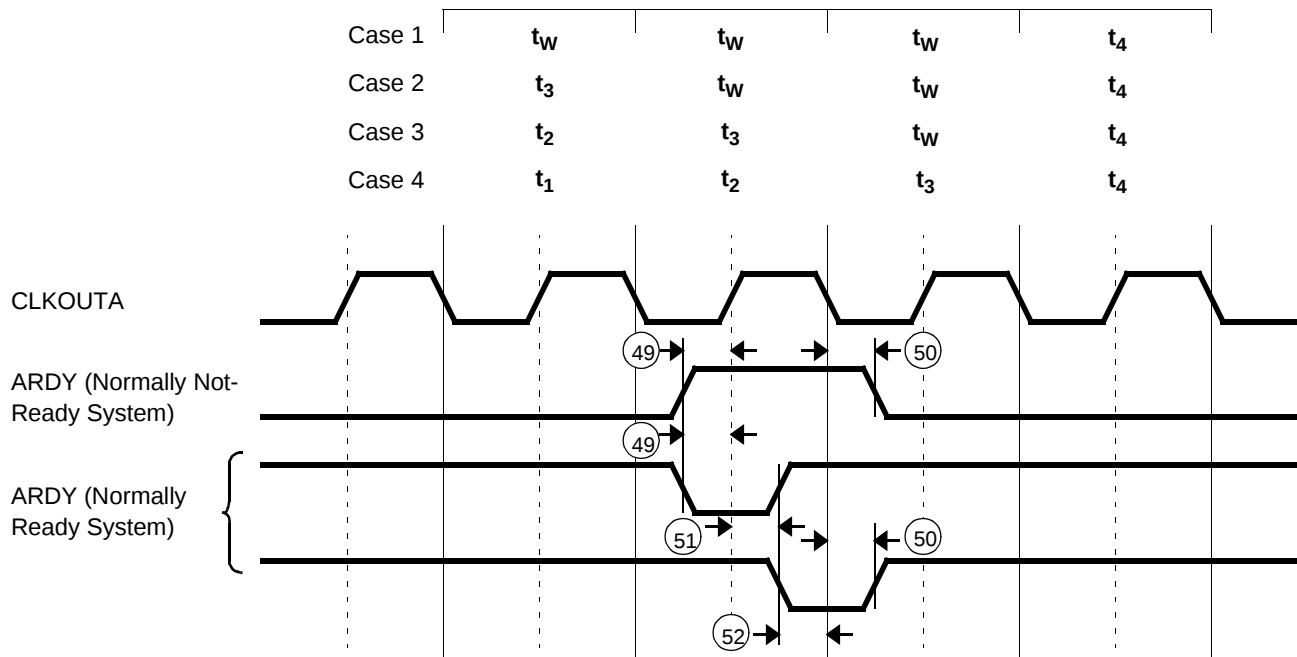
a This timing must be met to guarantee proper operation.

b This timing must be met to guarantee recognition at the clock edge.

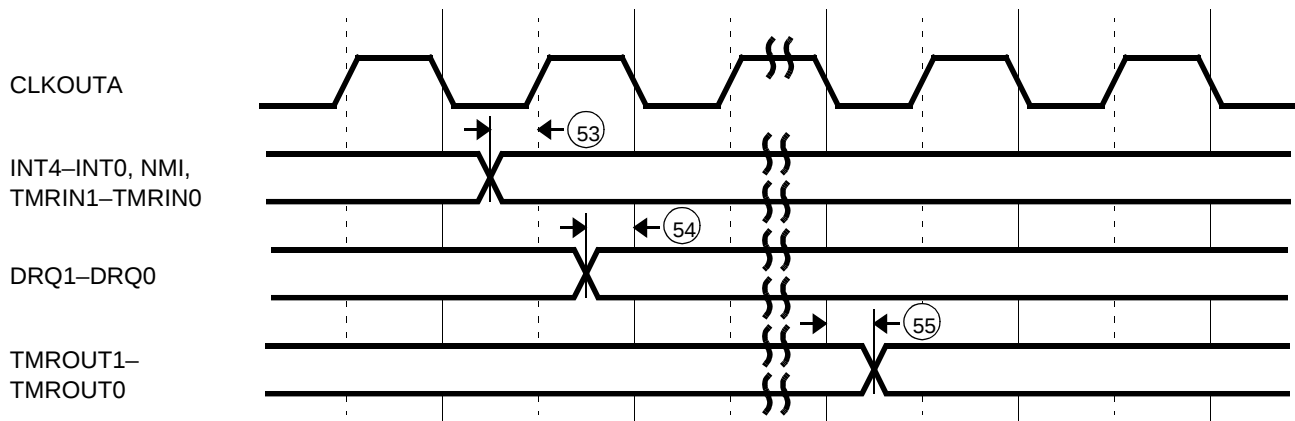
## Synchronous Ready Waveforms



## Asynchronous Ready Waveforms



## Peripheral Waveforms



## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

## Reset and Bus Hold (20 MHz and 25 MHz)

| Parameter                              |                    |                                         | Preliminary |     |        |     | Unit |
|----------------------------------------|--------------------|-----------------------------------------|-------------|-----|--------|-----|------|
|                                        |                    |                                         | 20 MHz      |     | 25 MHz |     |      |
| No.                                    | Symbol             | Description                             | Min         | Max | Min    | Max |      |
| Reset and Bus Hold Timing Requirements |                    |                                         |             |     |        |     |      |
| 5                                      | t <sub>CLAV</sub>  | AD Address Valid Delay and BHE          | 0           | 25  | 0      | 20  | ns   |
| 15                                     | t <sub>CLAZ</sub>  | AD Address Float Delay                  | 0           | 25  | 0      | 20  | ns   |
| 57                                     | t <sub>RESIN</sub> | RES Setup Time                          | 10          |     | 10     |     | ns   |
| 58                                     | t <sub>HVCL</sub>  | HOLD Setup <sup>(a)</sup>               | 10          |     | 10     |     | ns   |
| Reset and Bus Hold Timing Responses    |                    |                                         |             |     |        |     |      |
| 62                                     | t <sub>CLHAV</sub> | HLDA Valid Delay                        | 0           | 25  | 0      | 20  | ns   |
| 63                                     | t <sub>CHCZ</sub>  | Command Lines Float Delay               |             | 25  |        | 20  | ns   |
| 64                                     | t <sub>CHCV</sub>  | Command Lines Valid Delay (after Float) |             | 25  |        | 20  | ns   |

**Note:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a This timing must be met to guarantee recognition at the next clock.

## Reset and Bus Hold (33 MHz and 40 MHz)

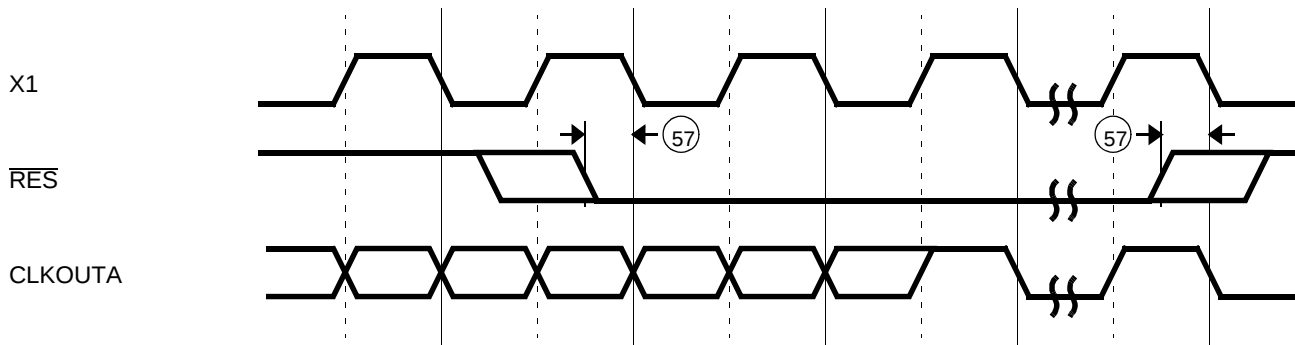
| Parameter                              |                    |                                         | Preliminary |     |        |     | Unit |
|----------------------------------------|--------------------|-----------------------------------------|-------------|-----|--------|-----|------|
|                                        |                    |                                         | 33 MHz      |     | 40 MHz |     |      |
| No.                                    | Symbol             | Description                             | Min         | Max | Min    | Max |      |
| Reset and Bus Hold Timing Requirements |                    |                                         |             |     |        |     |      |
| 5                                      | t <sub>CLAV</sub>  | AD Address Valid Delay and BHE          | 0           | 15  | 0      | 12  | ns   |
| 15                                     | t <sub>CLAZ</sub>  | AD Address Float Delay                  | 0           | 15  | 0      | 12  | ns   |
| 57                                     | t <sub>RESIN</sub> | $\overline{RES}$ Setup Time             | 8           |     | 5      |     | ns   |
| 58                                     | t <sub>HVCL</sub>  | HOLD Setup <sup>(a)</sup>               | 8           |     | 5      |     | ns   |
| Reset and Bus Hold Timing Responses    |                    |                                         |             |     |        |     |      |
| 62                                     | t <sub>CLHAV</sub> | HLDA Valid Delay                        | 0           | 15  | 0      | 12  | ns   |
| 63                                     | t <sub>CHCZ</sub>  | Command Lines Float Delay               |             | 15  |        | 12  | ns   |
| 64                                     | t <sub>CHCV</sub>  | Command Lines Valid Delay (after Float) |             | 15  |        | 12  | ns   |

**Note:**

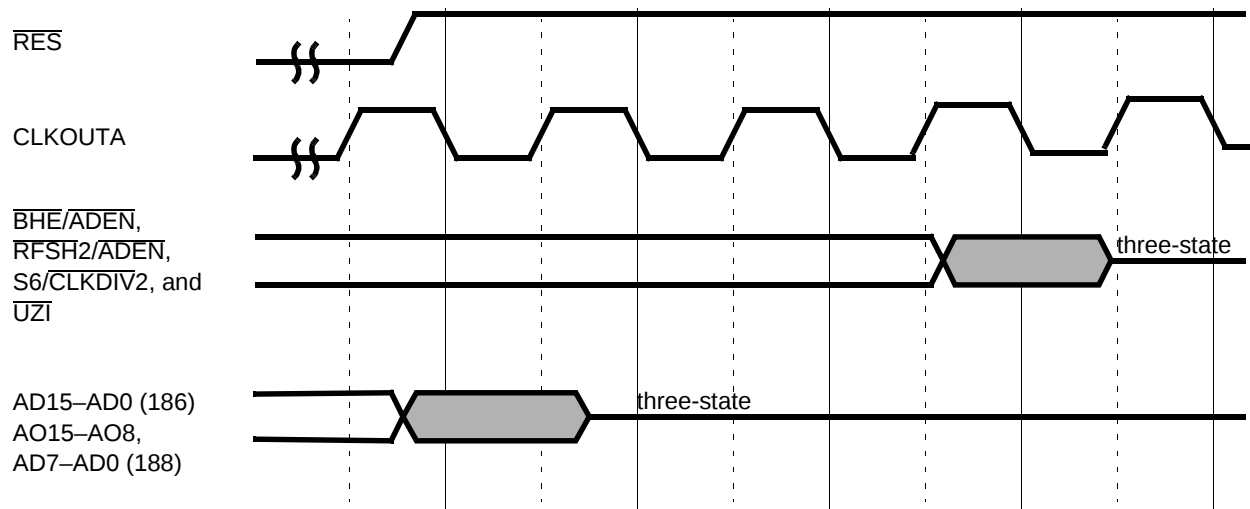
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

a This timing must be met to guarantee recognition at the next clock.

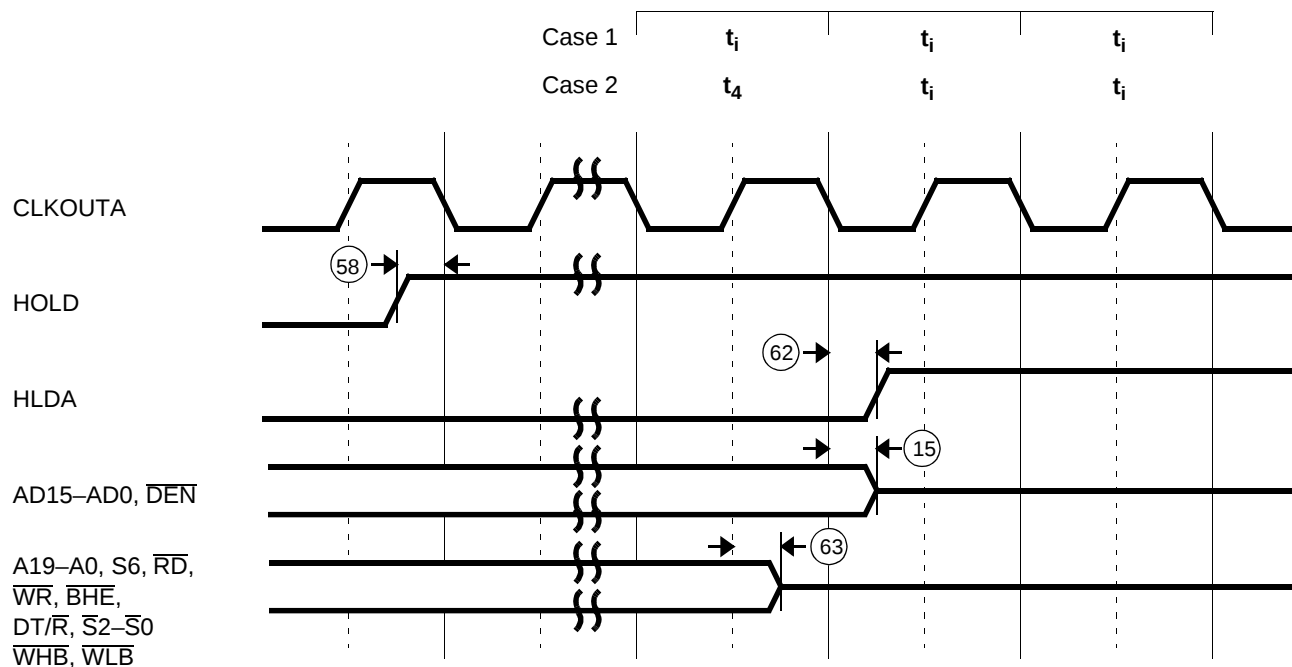
## Reset Waveforms



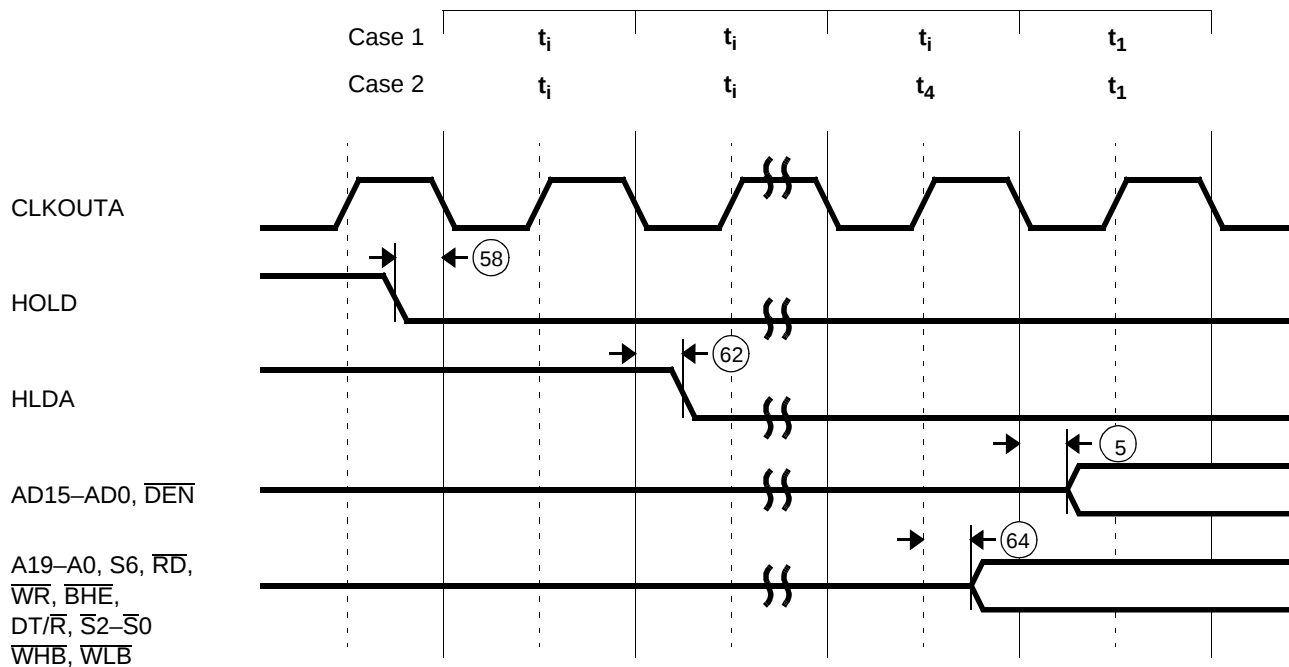
## Signals Related to Reset Waveforms



## Bus Hold Waveforms—Entering



## Bus Hold Waveforms—Leaving



## SWITCHING CHARACTERISTICS over COMMERCIAL operating range

### Synchronous Serial Interface (SSI) (20 MHz and 25 MHz)

| Parameter                                   |                   |                            | Preliminary |     |        |     | Unit |
|---------------------------------------------|-------------------|----------------------------|-------------|-----|--------|-----|------|
|                                             |                   |                            | 20 MHz      |     | 25 MHz |     |      |
| No.                                         | Symbol            | Description                | Min         | Max | Min    | Max |      |
| Synchronous Serial Port Timing Requirements |                   |                            |             |     |        |     |      |
| 75                                          | t <sub>DVSH</sub> | Data Valid to SCLK High    | 10          |     | 10     |     | ns   |
| 77                                          | t <sub>SHDX</sub> | SCLK High to SPI Data Hold | 3           |     | 3      |     | ns   |
| Synchronous Serial Port Timing Responses    |                   |                            |             |     |        |     |      |
| 71                                          | t <sub>CLEV</sub> | CLKOUTA Low to SDEN Valid  |             | 25  |        | 20  | ns   |
| 72                                          | t <sub>CLSL</sub> | CLKOUTA Low to SCLK Low    |             | 25  |        | 20  | ns   |
| 78                                          | t <sub>SLDV</sub> | SCLK Low to Data Valid     |             | 25  |        | 20  | ns   |

**Note:**

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

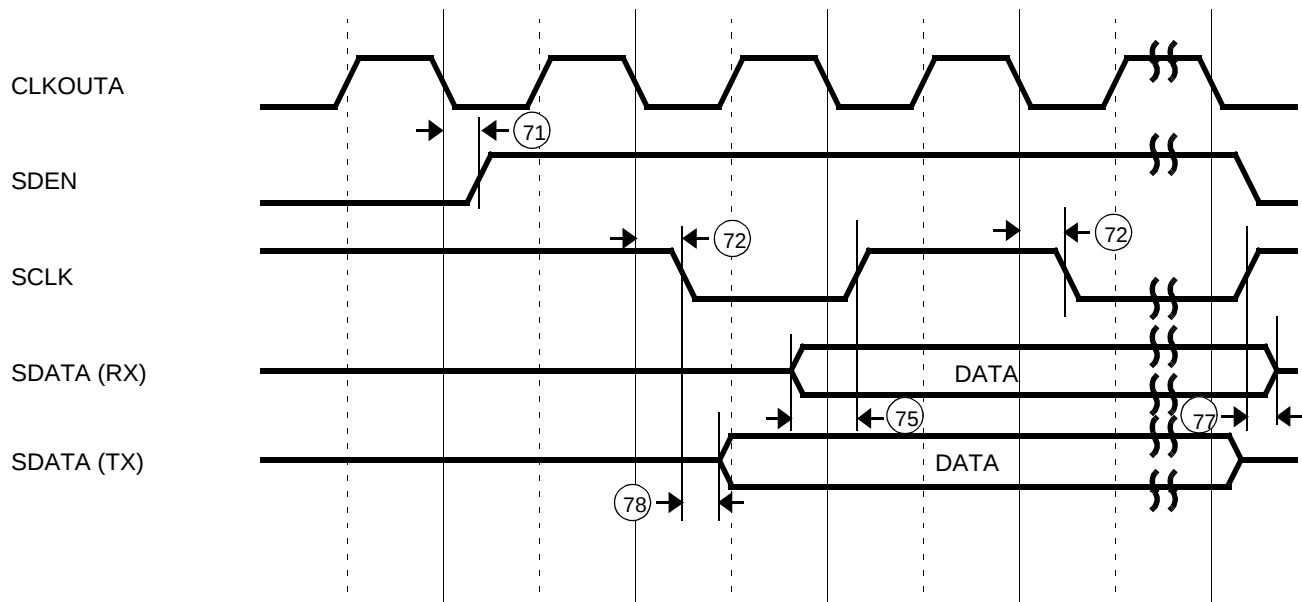
### Synchronous Serial Interface (SSI) (33 MHz and 40 MHz)

| Parameter                                   |                   |                            | Preliminary |     |        |     | Unit |
|---------------------------------------------|-------------------|----------------------------|-------------|-----|--------|-----|------|
|                                             |                   |                            | 33 MHz      |     | 40 MHz |     |      |
| No.                                         | Symbol            | Description                | Min         | Max | Min    | Max |      |
| Synchronous Serial Port Timing Requirements |                   |                            |             |     |        |     |      |
| 75                                          | t <sub>DVSH</sub> | Data Valid to SCLK High    | 8           |     | 5      |     | ns   |
| 77                                          | t <sub>SHDX</sub> | SCLK High to SPI Data Hold | 2           |     | 2      |     | ns   |
| Synchronous Serial Port Timing Responses    |                   |                            |             |     |        |     |      |
| 71                                          | t <sub>CLEV</sub> | CLKOUTA Low to SDEN Valid  | 0           | 15  | 0      | 12  | ns   |
| 72                                          | t <sub>CLSL</sub> | CLKOUTA Low to SCLK Low    | 0           | 15  | 0      | 12  | ns   |
| 78                                          | t <sub>SLDV</sub> | SCLK Low to Data Valid     | 0           | 15  | 0      | 12  | ns   |

**Note:**

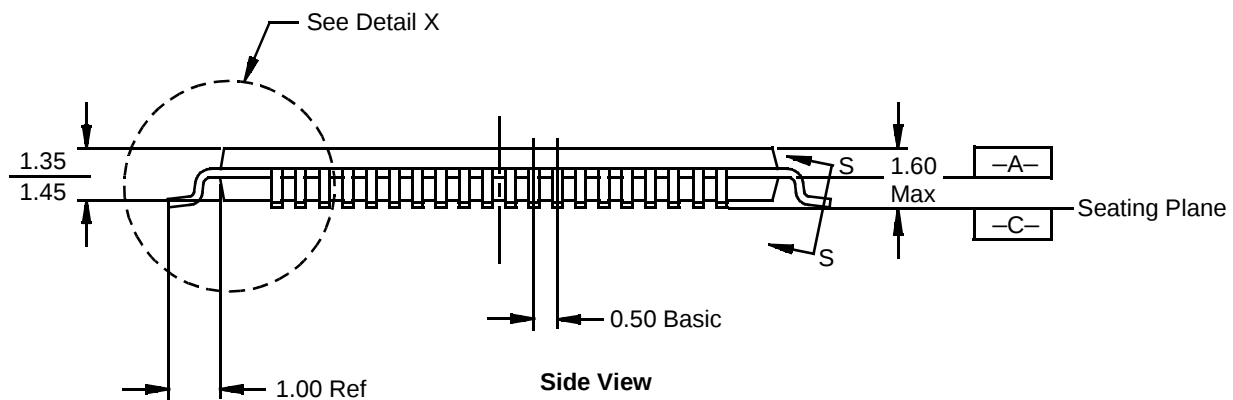
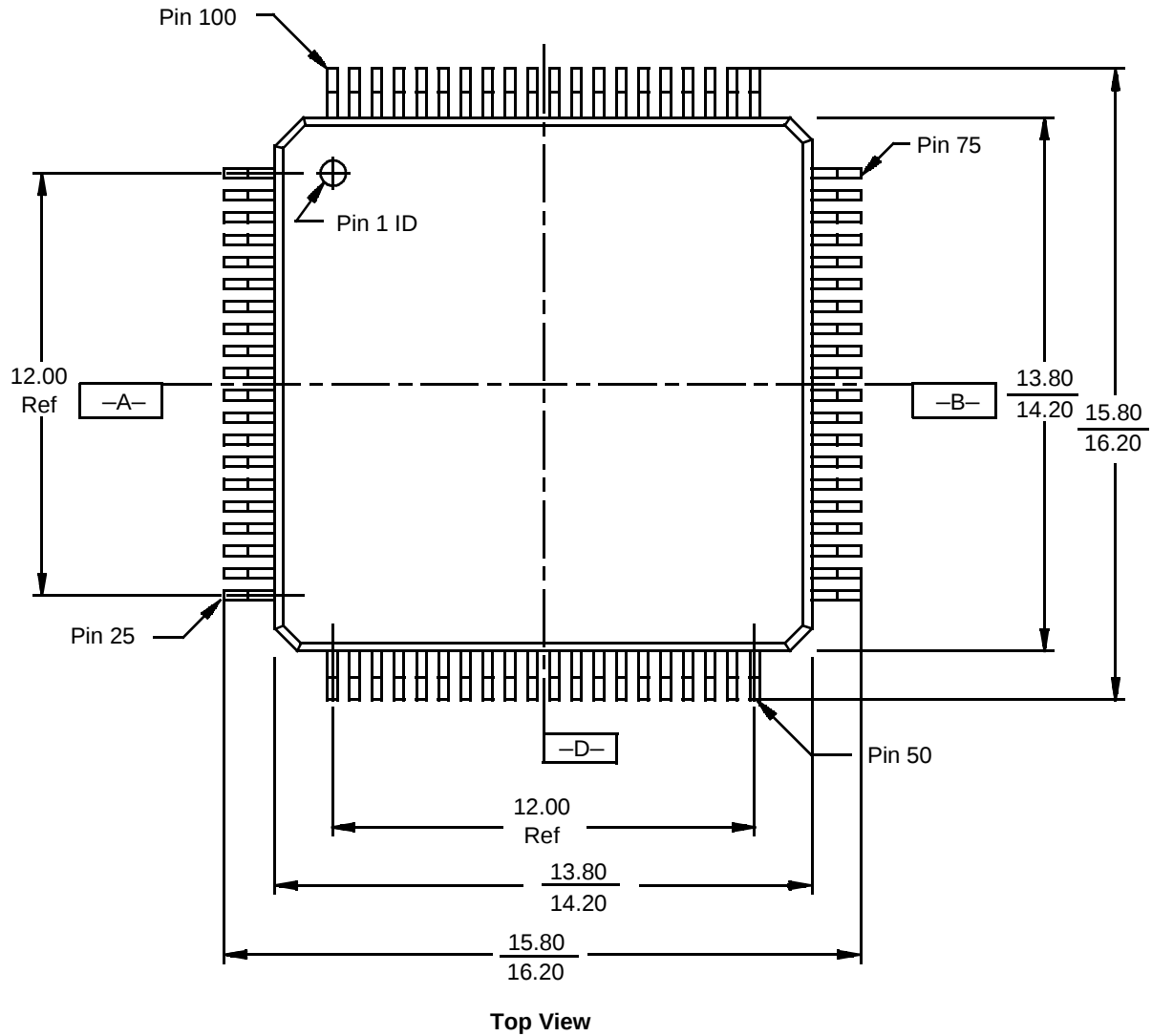
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with  $C_L = 50$  pF. For switching tests,  $V_{IL} = 0.45$  V and  $V_{IH} = 2.4$  V, except at X1 where  $V_{IH} = V_{CC} - 0.5$  V.

## Synchronous Serial Interface (SSI) Waveforms

**Note:**

SDATA is bidirectional and used for either transmit (TX) or receive (RX). Timing is shown separately for each case.

**TQFP PHYSICAL DIMENSIONS**  
**PQL 100, Trimmed and Formed**  
**Thin Quad Flat Pack**

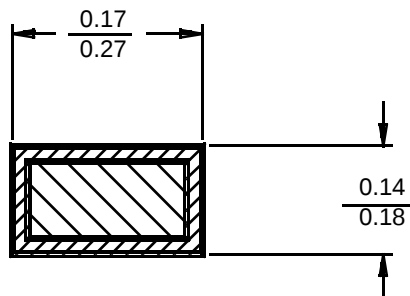
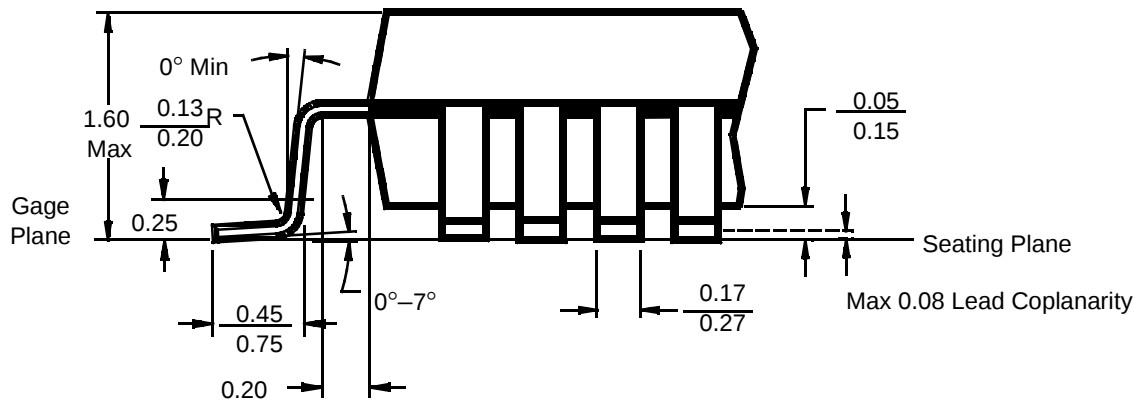


**Notes:**

1. All measurements are in millimeters unless otherwise noted.
2. Not to scale; for reference only.

pql100  
4-15-94

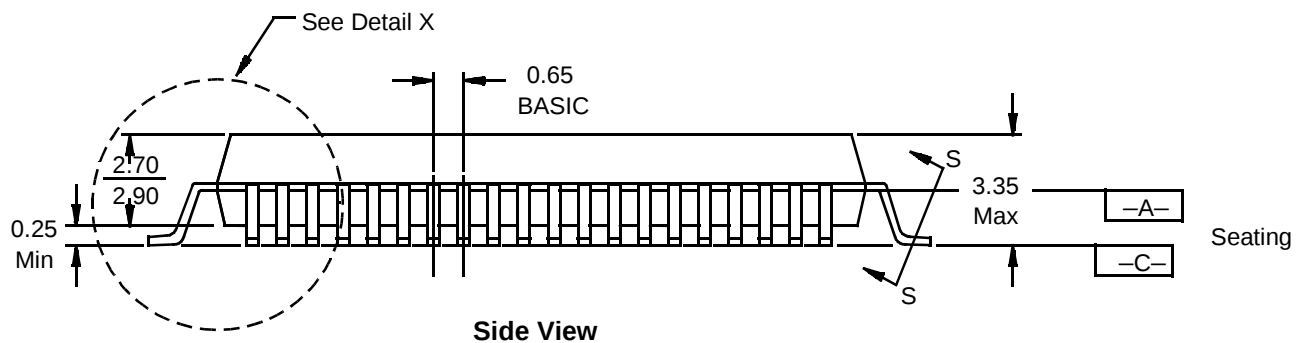
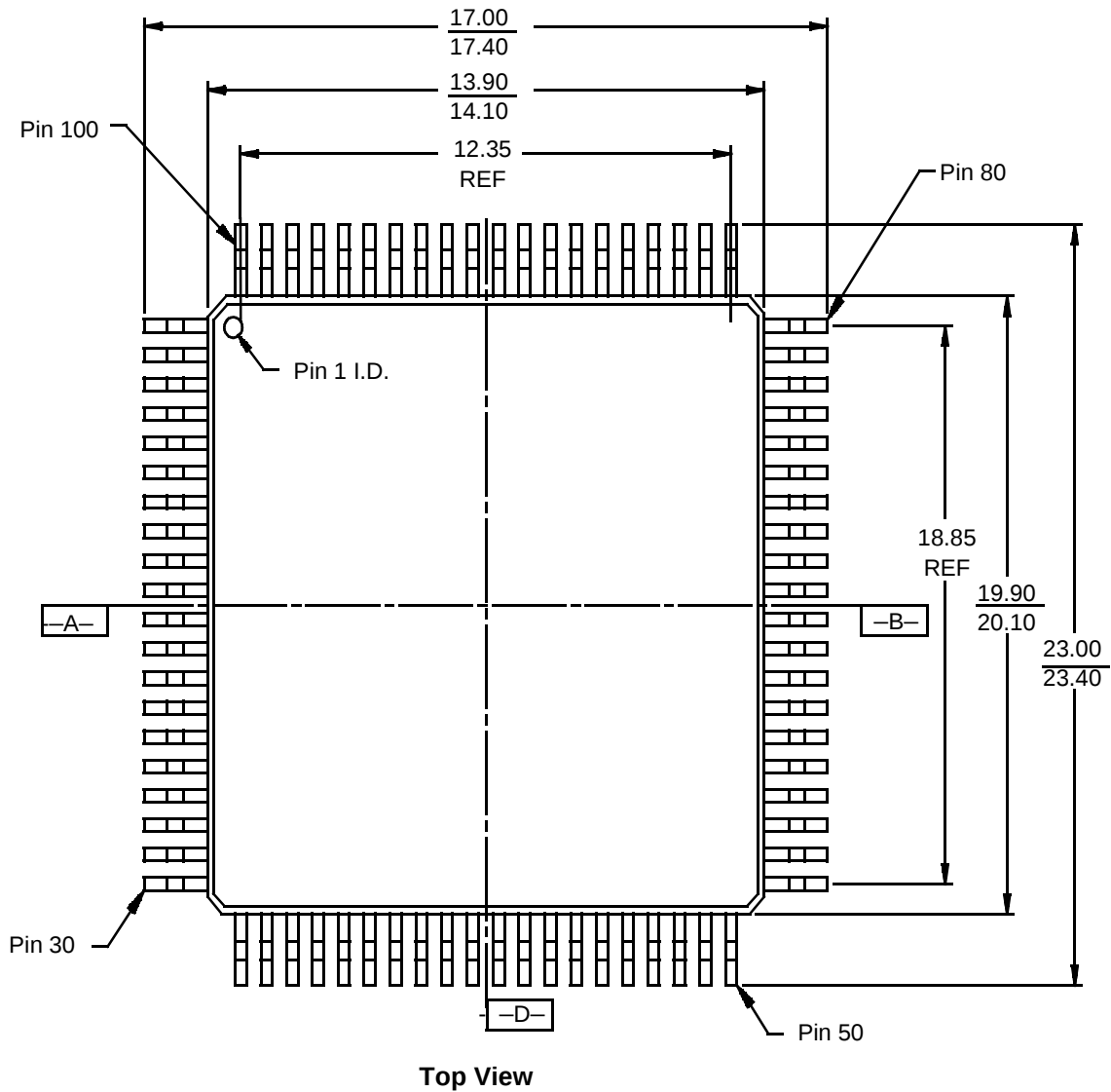
## PQL 100 (continued)

**Notes:**

1. All measurements are in millimeters unless otherwise noted.
2. Not to scale; for reference only.

pql100  
4-15-94

**PQFP PHYSICAL DIMENSIONS**  
**PQR 100, Trimmed and Formed**  
**Plastic Quad Flat Pack**

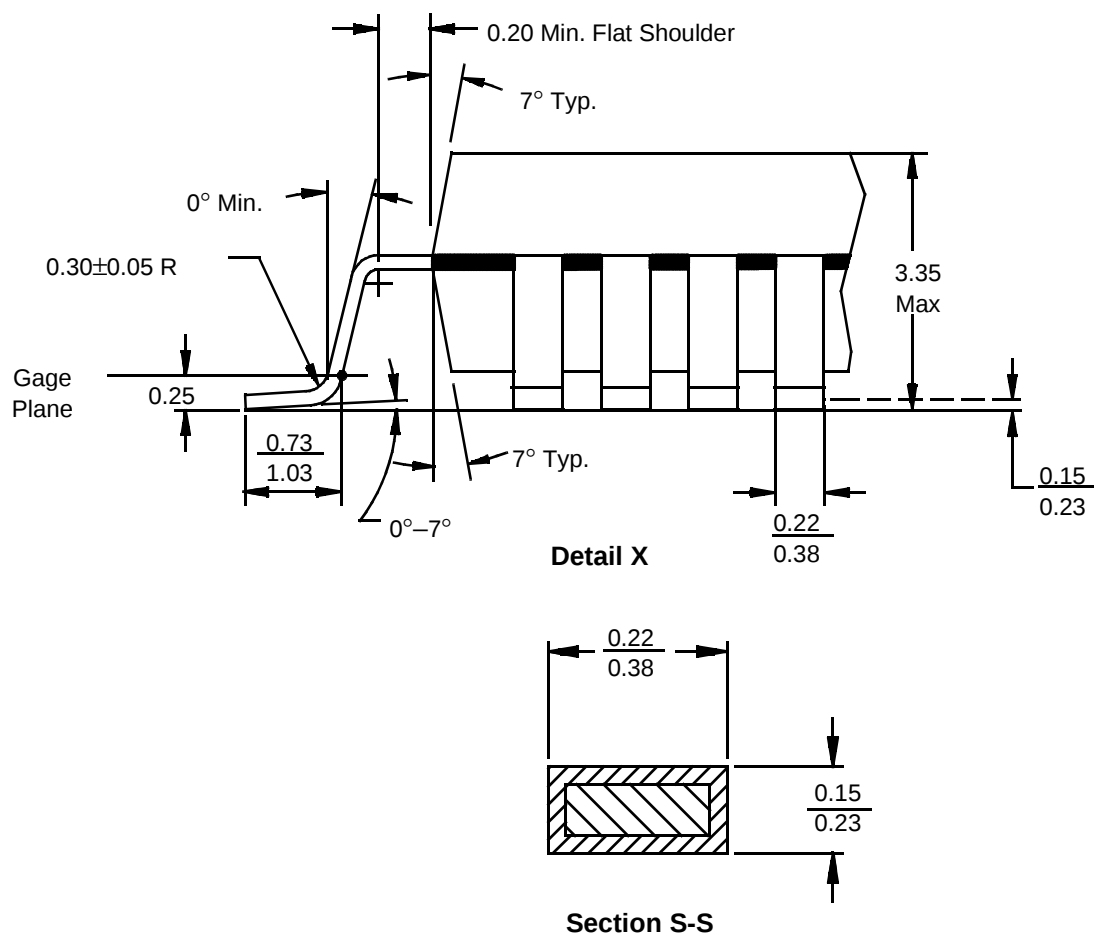


**Notes:**

1. All measurements are in millimeters unless otherwise noted.
2. Not to scale; for reference only.

pqr100  
 4-15-94

PQFP PQR 100 (continued)



**Note:**

Not to scale; for reference only.

pqr100  
4-15-94

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