TFT-LCD TV Panel Power Solution

General Description

The uP6668 is a complete power supply solution for TFT-LCD application with VIN range from 8V to 14V. The uP6668 includes a boost converter with p-channel MOSFET for timing sequence, a buck converter, a VGL regulator, a VGH regulator, an OP Amplifier for VCOM, stable voltage reference for Gamma R-string or IC, power good function, and gate shading function.

The uP6668 integrates a power MOSFET and program soft start for boost converter. The p-channel MOSFET for timing sequence is turned on by EN pin. The boost converter provides the source drivers with supply voltage. The buck converter provides the logic system with supply voltage. VGL regulator supplies charge pump for TFT-LCD gate-off voltage. VGH regulator supplies charge pump for TFT-LCD gate-on voltage. The operation amplifier is used for VCOM. The uP6668 provides the Gamma reference with a stable voltage source. Power good function provides a signal for timing controller when power on. The uP6668 integrates high-voltage switches for gate shading function to modulate the voltage applied to gate IC.

For the boost and buck converters, switching frequency can be selected by external circuit connection. The uP6668 provides over temperature protection, over-voltage protection, under-voltage protection and current limit to achieve complete protection. The uP6668 is available in the WQFN7x7-48L package.

Ordering Information

Order Number	Package Type	Remark
uP6668PQDK	WQFN7x7-48L	

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

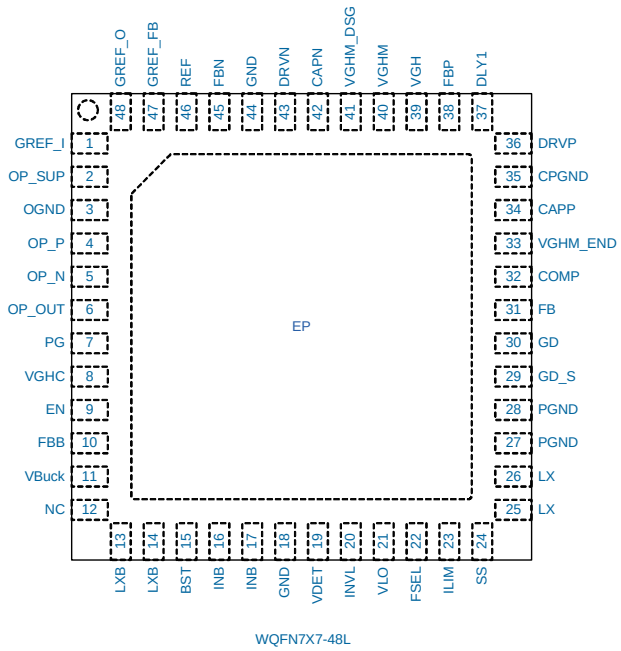
Applications

- **TFT-LCD TV Panel**

Features

- **8V to 14V Input Voltage Range**
- **20V Boost Converter with 4.2A Power MOSFET**
- **500kHz/750kHz Selectable Switching Frequency**
- **External P-Channel MOSFET for Boost Output**
- **Buck Converter with 2.5A Power MOSFET**
- **Power Good Function**
- **Regulated VGL**
- **Regulated VGH**
- **High-Voltage Switches for Gate Shading Function**
- **OP Amplifier for VCOM**
- **Under-Voltage Lockout**
- **Over-Voltage Protection**
- **Over-Current Protection**
- **Over Temperature Protection**
- **Short Circuit Protection**
- **WQFN7x7-48L Package**
- **RoHS Compliant and Halogen Free**

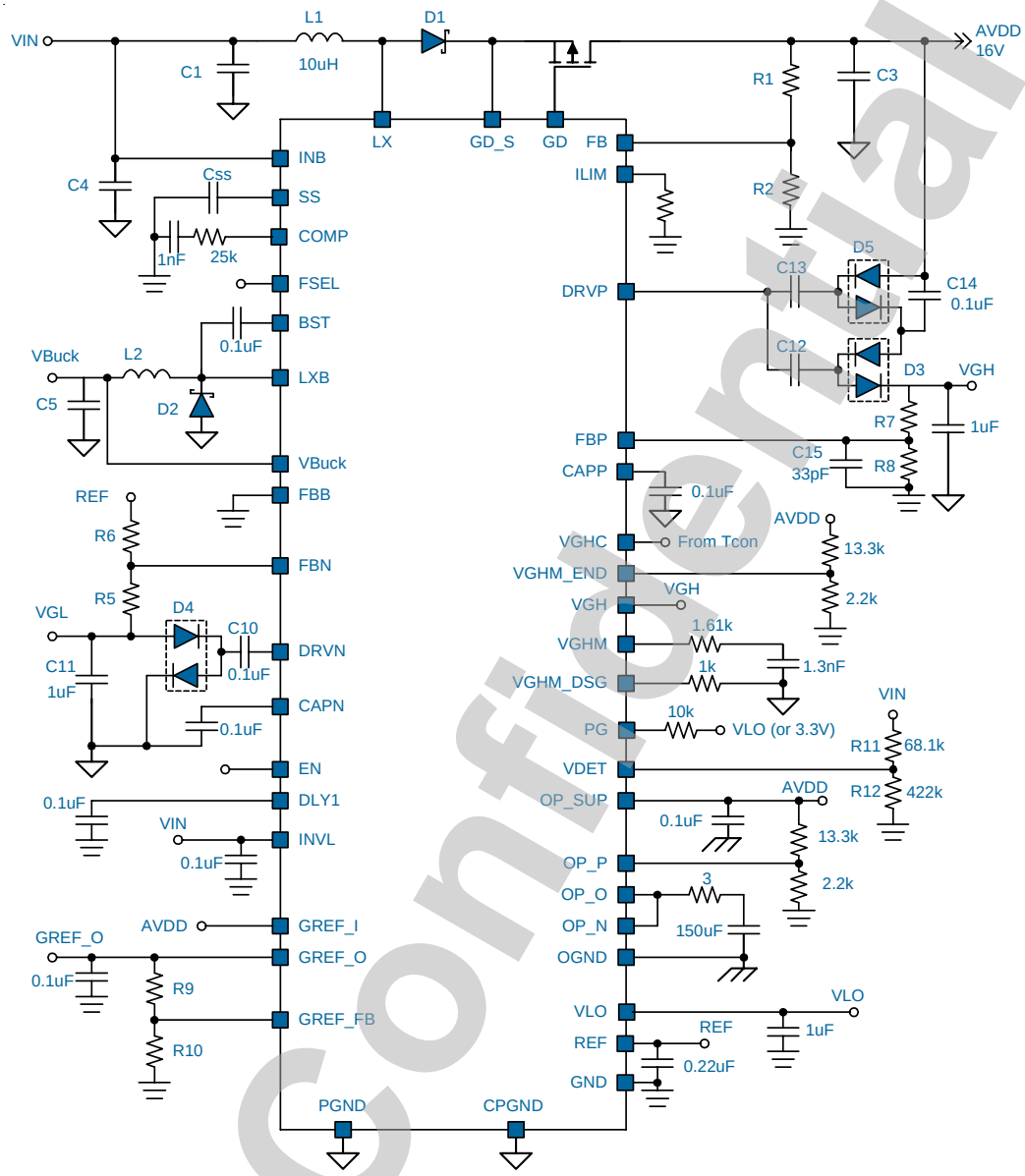
Pin Configuration



WQFN7X7-48L

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Typical Application Circuit



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Functional Pin Description

No.	Pin Name	Pin Function
1	GREF_I	**Gamma Reference Input.**
2	OP_SUP	**OP. Amplifier Power Supply.**
3	OGND	**OP. Amplifier Power Ground.**
4	OP_P	**OP. Amplifier Non-inverting Input.**
5	OP_N	**OP. Amplifier Inverting Input.**
6	OP_OUT	**OP. Amplifier Output.**
7	PG	**Power Good.** Open-drain output pulled high to VLO or buck output with external 10kΩ resistor.
8	VGHC	**Gate Shading Function Logic Control Input.**
9	EN	**Enable Pin. Active high.** When EN is high, uP6668 turns on boost converter and positive charge pump.
10	FBB	**Buck Converter Feedback Pin.** Set buck converter output to fixed 3.3V by connecting FBB to GND. For other buck converter output voltages, connect FBB to the center of resistive voltage-divider between buck converter output and GND. Place the resistive voltage-divider close to this pin.
11	VBuck	**Buck Converter Output Voltage Sense Pin.** Connect this pin to buck converter output.
12	NC	**Not Connected.**
13	LXB	**Switching Node of Buck Converter.**
14		
15	BST	**Buck Converter Bootstrap Capacitor Connection Pin.** Connect a 0.1uF ceramic capacitor between LXB and BST.
16	INB	**Buck Converter Power Input.**
17		
18	GND	**Analog Ground.**
19	VDET	**Voltage Detector Input.** Connect VDET to the center of a resistor voltage-divider between input voltage and GND.
20	INVL	**Input of Internal 5V Linear Regulator.** Bypass INVL to GMD with a 0.22uF ceramic capacitor.
21	VLO	**5V Internal Linear Regulator Output.** Connect a 1uF ceramic capacitor between VLO to GND. Provides power for the internal MOSFET driving circuit, the PWM controllers, charge-pump regulators, logic, and reference and other analog circuitry. Provides 25mA load current when all switching regulators are enabled. VLO is active whenever input voltage is high enough.
22	FSEL	**Frequency Select Pin.** Connect FSEL to VLO, INVL or floating for 750kHz operation. Connect to GND for 500kHz.
23	ILIM	**Boost Current-Limit Setting.** Connect a resistor between ILIM and GND to set current limit for Boost converter.

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Functional Pin Description

No.	Pin Name	Pin Function
24	SS	**Soft-Start Pin.** Connect a capacitor between SS and GND to set the soft-start time for boost converter. When GD is done, the capacitor on SS will be charged by 5uA current. SS is internal pulled to GND through 1kΩ resistance when EN is low or when VLO is below its UVLO threshold.
25	LX	**Switching Node of Boost Converter.**
26		
27	PGND	**Power Ground.** PGND is the source of power MOSFET of boost converter.
28		
29	GD_S	**External P-Channel MOSFET Source.** Connect to the Schottky diode cathode of boost converter.
30	GD	**External P-Channel MOSFET Gate.** A 10uA current source pulls down the gate of the external p-channel MOSFET.
31	FB	**Boost Voltage Feedback Pin.** FB regulates to 1.25V nominal. Connect FB to the center of a resistive voltage-divider between AVDD and the analog ground (AGND) the boost regulator output voltage. Place the resistive voltage-divider close to this pin.
32	COMP	**Boost Converter Compensation Pin.** Connect a compensation network to ground.
33	VGHM_END	**VGHM Low Level Setting Pin.** Connect VGHM_END to the center of a resistive voltage-divider between AVDD and GMD to set the VGHM falling level. The level is 10 times of VGHM_END.
34	CAPP	**Positive Charge-Pump Driver Power Supply.** Bypasses to CPGND with a 0.1uF capacitor. CAPP is internally connected to GD_S.
35	CPGND	**Charge-Pump and Buck Power Ground**
36	DRVP	**Positive Charge-Pump Driver Output.** Connects DRVP to the positive charge-pump flying capacitor(s).
37	DLY1	**High-Voltage Switches Delay.** Bypasses to GND with a capacitor to set the delay time for high-voltage switches ready after finishing the positive charge-pump soft-start. A 10uA current source charges the capacitor connected to DLY1. DLY1 is internal pulled to GND through 50Ω resistance when EN is low or when VLO is below its UVLO threshold.
38	FBP	**Positive Charge-Pump Feedback.** Connects FBP to the center of a resistive voltage-divider between the positive charge-pump output and GND to set the positive charge-pump output voltage. Place the resistive voltage-divider close to this pin.
39	VGH	**High-Voltage Switches Input.**
40	VGHM	**VGH Modulation.**
41	VGHM_DSG	**VGH Modulation Discharge Path.** Bypass a resistor to GND.
42	CAPN	**Negative Charge-Pump Driver Power Supply.** Bypasses to CPGND with a 0.1uF capacitor. CAPN is internally connected to INB.
43	DRVN	**Negative Charge-Pump Driver Output.** Connects DRVN to the negative charge-pump flying capacitor(s).
44	GND	**Analog Ground.**

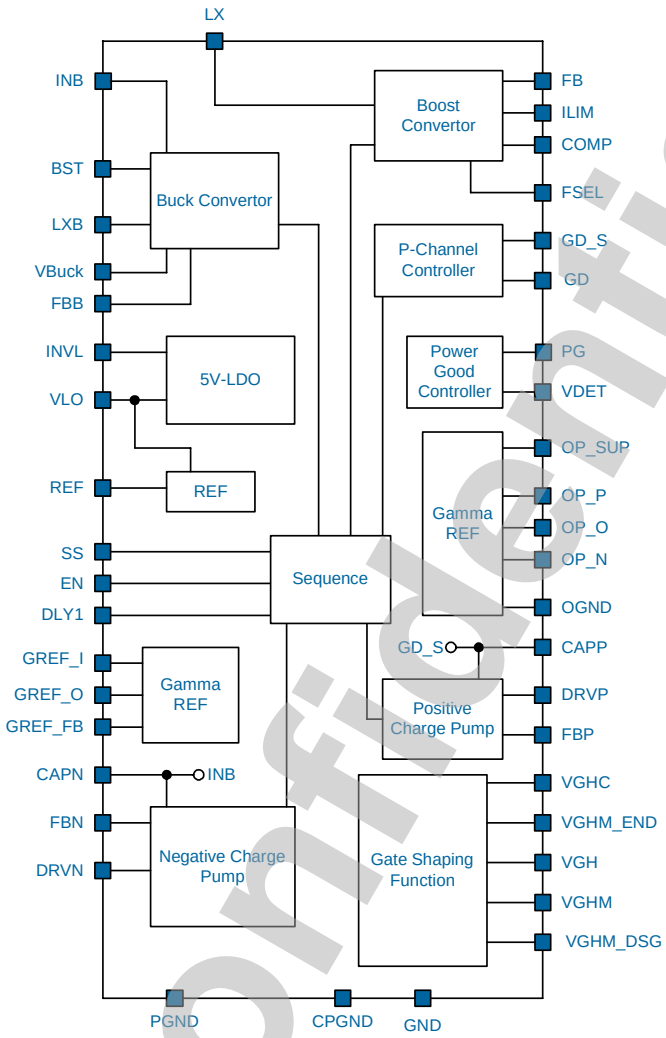
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Functional Pin Description

No.	Pin Name	Pin Function
45	FBN	**Negative Charge-Pump Feedback.** Connects FBN to the center of a resistive voltage-divider between the negative charge-pump output and REF to set the negative charge-pump output voltage. Place the resistive voltage-divider close to this pin.
46	REF	**Reference Voltage Output.** Connects a 0.22uF capacitor from REF to GND. All power outputs are disabled until REF exceeds its UVLO threshold.
47	GREF_FB	**Gamma Reference Feedback.** Connects GREF_FB to the center of a resistive voltage-divider between GREF_O and GND to set the gamma reference output voltage. Place the resistive voltage-divider close to this pin.
48	GREF_O	**Gamma Reference Output.**

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Functional Block Diagram



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Functional Description

The uP6668 is a complete power supply solution for TFTLCD TV application. The uP6668 includes a boost converter, a buck converter, a VGL regulator, a VGH regulator, VGH modulation function, a power good function, a OP amplifier for Vcom, and a high accuracy LDO for Gamma reference.

Buck Regulator

- Buck Output Setting

uP6668 supports two modes to set buck output. The first mode is fixed mode. The buck output will be 3.3V by connecting FBB to GND. The second mode is for adjustable buck output by external feedback series of resistors.

Buck output voltage setting equation:

$$VBuck = REF \times (1 + \frac{R3}{R3 + R4})$$

where REF = 1.25V, R3 and R4 are shown in Typical Application Circuit.

It is recommended that the on-time of buck in CCM is larger than 200ns.

- Selectable Switching Frequency

The buck switching frequency can be selected by FSEL pin as below table:

FSEL	Frequency
L	500kHz
H	750kHz

- Soft Start (Buck)

The uP6668 provides soft-start function for buck converter to minimize the inrush current. Buck ramps up to the setting voltage in 128 steps in 3ms (typ.) after REF rises higher than REF's UVLO. The buck fault protection is disabled during its soft-start.

- Over Current Protection (Buck OCP)

The buck converter has the function for over-current protection to limit peak inductor current. It prevents large current from damaging the inductor and diode. During the ON time, once the inductor current exceeds the current limit, the internal power MOSFET turns off immediately and shortens the duty cycle. Therefore, the output voltage drops if the over-current condition occurs. The buck current limit is typically 2.5A.

Boost Regulator

- Boost Output Setting

Step-up: Output voltage is adjusted by external feedback series of resistors.

Boost output voltage setting equation (unit in V):

$$AVDD = REF \times (1 + \frac{R1}{R2})$$

where REF = 1.25V, R1 and R2 are shown in Typical Application Circuit.

- Selectable Switching Frequency

The boost switching frequency can be selected by FSEL pin as below table:

FSEL	Frequency
L	500kHz
H	750kHz

- Gate Driver Isolate Function

The GD pin can be used to control external isolation switch. The GD supports PMOS device isolate input voltage and power inductor. When EN is low, GD is internally pulled to GD_S through a 25Ω resistor and then the external p-channel MOSFET is off. When V_{IN} > UVLO and EN = High, the GD pin is pulled low by 10uA current source. When GD falls lower than threshold voltage of p-channel MOSFET from GD_S, external p-channel MOSFET is on. When GD falls deeper than GD_S - 6V (GD done), the boost regulator is enable and the soft-start begins.

When the p-channel MOSFET is not used, let GD be floating and GD_S to boost output.

- Soft Start (Boost)

The uP6668 provides soft-start function for boost converter to minimize the inrush current. There are two soft-start features for boost converter. The first one is that boost ramps up to set voltage in 128 steps in 16ms after GD done if the capacitance on SS pin is smaller than 200pF. The second one is that a 5uA current source will charge the capacitor on SS pin and boost ramps up to setting voltage between GD done and SS > 1.25V if the capacitance on SS pin is larger than 200pF. The capacitance at SS pin should be smaller than 100nF. The boost under voltage protection and short circuit protection are disabled before its soft-start completed.

- Over Current Protection (Boost OCP)

The boost converter has the function for over-current protection to limit peak inductor current. It prevents large current from damaging the inductor and diode. During the ON time, once the inductor current exceeds the current limit, the internal power MOSFET turns off immediately and shortens the duty cycle. Therefore, the output voltage drops if the over-current condition occurs. Actual current limit is always larger than the nominal value because of the internal circuit delay. Current limit is also affected by the input voltage, duty cycle, and inductor value.

The boost current limit can be adjusted by the resistor on ILIM pin.

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Functional Description

The setting equation is as follows (unit in A):

$$I_{LIM} = 4.2 - (\frac{68k}{R_{LIM}})$$

- Over Voltage Protection (Boost OVP)

The boost converter contains over voltage protection. The function limits output voltage when FB short to ground or floating. OP_SUP pin or GD_S pin is used to detect boost output. The function will turn off boost converter switch when OVP happens. It remains turned off until below the OVP hysteresis voltage, and then the boost converter switch starts switching again.

Gate-Low Regulator

- Gate-Low Voltage Setting

The gate-low regulator provides the TFT-LCD gate off voltage. The charge pump can provide a programmable output voltage. To regulate the output voltage must set the resistive voltage-divider sensing at FBN pin as shown in Typical Application Circuit. The error amplifier varies the difference voltage by sensing FBN pin to regulate the output voltage as the following equation (unit in V):

$$V_{GL} = 0.25 - (\frac{R5}{R6})$$

- Soft Start (Negative Charge Pump)

The uP6668 provides soft-start function for negative charge-pump to minimize the inrush current. The negative charge-pump ramps down to the setting voltage in 128 steps in 1.8ms (typ.) after buck soft-start is finished. The negative charge-pump under voltage protection and short circuit protection are disabled before its soft-start completed.

Gate-High Regulator

- Gate-High Voltage Setting

The gate-high regulator provides the TFT-LCD gate on voltage. The charge pump can provide a programmable output voltage. To regulate the output voltage must set the resistive voltage-divider sensing at FBP pin as shown in Typical Application Circuit. The error amplifier varies the difference voltage by sensing FBP pin to regulate the output voltage as the following equation (unit in V):

$$V_{GH} = 1.25 \times (1 + \frac{R7}{R8})$$

- Soft Start (Positive Charge Pump)

The uP6668 provides soft-start function for positive charge-pump to minimize the inrush current. The positive charge-pump ramps up to the setting voltage in 128 steps in 2ms (typ.) after boost soft-start is finished. The positive charge-pump under voltage protection and short circuit protection are disabled during its soft-start.

Operational Amplifier

The OP amplifier in uP6668 is used for Vcom. It features 100mA sink or source short-circuit current, 45V/us slew rate, and 20MHz for 3dB bandwidth.

Linear Regulator (VLO)

The uP6668 includes a linear regulator for IC internal used. The output is 5V fixed. The total external load ability is 25mA . Bypass VLO to GND with a minimum 1uF ceramic capacitor.

Reference Voltage (REF)

The reference output is 1.25V (typ.) and sourcing ability is 50uA at least. Bypass REF with a 0.22uF capacitor to GND.

High Accuracy LDO for Gamma Reference

The LDO is used for Gamma correction R-string or Gamma IC reference. This LDO features high output accuracy (±0.5%) and lo-dropout voltage (0.25V typ.) and can supply at least 60mA. To regulate the output voltage must set the resistive voltage-divider sensing at GREF_FB pin as shown in Typical Application Circuit. The error amplifier varies the difference voltage by sensing GREF_FB pin to regulate the output voltage as the following equation (unit in V):

$$GREF_O = 1.25 \times (1 + \frac{R9}{R10})$$

Select R10 in the 10kΩ to 50kΩ range.

Power Good Function

PG is an open-drain output with external resistor to VLO or VBuck. PG is active after VLO rises above UVLO threshold. The voltage detector monitors the VDET voltage and PG is pulled to GND while VDET is lower than the detecting level. The detecting level is decided by an external resistor divider as shown in *Typical Application Circuit*. The detect voltage follows the equation below (unit in V):

$$V_{IN_PG} = 1.25 \times (1 + \frac{R11}{R12})$$

where V_{IN_PG} is the desired power good threshold.

Gate Shaping Function

When gate shaping function is disabled, Q1 and Q2 are turned off and VGHM is discharged via the 1kΩ resistor over Q3. The gate shaping function is enabled after VGH soft start is completed. Then, the capacitor at DLY1 is charged with a 10uA current source. After DLY1 voltage is over 1.25V, Q3 is turned off and Q1 and Q2 is controlled by VGHC. With VGHC =high, Q1 is turned on and Q2 is turned off. VGHM will be VGH through Q1. When VGHC = low, Q1 is turned off and Q2 is turned on. VGHM is discharged by the resistor connected to the VGHM_DSG pin. Once VGHM

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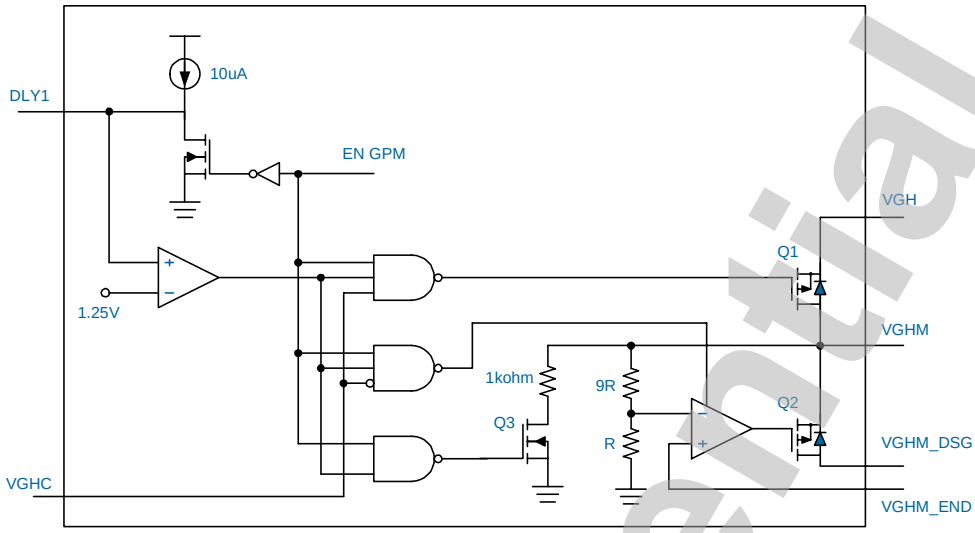


Figure 1. Gate Shaping Function Block Diagram

is discharged to ten times VGHM_END, Q2 is turned off and VGHM is high impedance. When the junction temperature exceeds 160oC, a thermal sensor immediately activates the fault protection that shuts down all the outputs. Cycle the input voltage to clear the fault latch and restart the uP6668. This function is functional only if VDET is high, or VGHM will be VGH all the time.

It is recommended that the gate shaping end volate level is lower than 20V (VHGM_END < 2V) and the voltage difference between VGH and gate shaping end voltage level is larger than 20V.

Protection Function

- Under Voltage Protection (UVP)

During operation, if any output of the four regulators (boost, buck, positive charge-pump, and negative charge-pump) goes lower than its respective under voltage protection threshold, the uP6668 activates an internal fault timer. If any condition or the combination of conditions from AVDD, VGH, or VGL indicates a continuous fault for the fault timer duration (50ms typ.), the uP6668 latches off all its outputs except for Buck. Only if the Buck UVP happens, the uP6668 latches off all its outputs. Recycle VIN to recover normal operation.

- Short-Circuit Protection (SCP)

If a short happened to any of the three regulator outputs (AVDD, VGH, and VGL), no fault timer is applied; the uP6668 latches off immediately except for Buck. Only if the Buck SCP happens, the uP6668 latches off all its outputs. Recycle VIN to recover normal operation.

- Over Temperature Protection

The uP6668 has thermal protection function to prevent the excessive power dissipation from overheating. When the junction temperature exceeds 160°C, a thermal sensor immediately activcates the fault protection that shuts down all the outputs. Cycle the input voltage to clear the fault latch and restart the uP6668. For continuous operation, do not operate over the maximum junction temperature rating around 150°C.

Power On Sequence

The internal reference voltage (REF) starts up when VLO is above its UVLO threshold. The buck converter starts up in 3ms when REF is above its UVLO threshold. After the buck converter soft-start is done, UVP and SCP of the buck converter activate and the negative charge-pump soft-start begins within 1.8ms. After the negative charge-pump soft-start is done, UVP and SCP of the buck converter activate.

When EN goes to high, a 10uA current source starts to pull down GD pin, and the external p-channel MOSFET is turned on as V_{GD} is lower than the threshold voltage of the p-channel MOSFET. When V_{GD} is lower than the GD-done threshold (V_{GD_S} - 6V), the boost converter soft-start begins. Gamma reference is enabled at the same time.

After the boost soft-start completed, the UVP and SCP of boost converter activate and the positive charge-pump soft-start begins within 2ms. After the positive charge-pump soft-start completed, the UVP and SCP of the positive charge-pump activate. The delay block for high-voltage switches activates at the same time. A 10uA current source charges the capacitor on DLY1 pin. When V_{DLY1} reaches REF, the high-voltage switches block is enabled.

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Power Off Sequence

The boost converter, buck converter, positive charge-pump, negative charge-pump, and high-voltage switching block all start to shut down when INVL drops below its UVLO threshold. VLO stays flat until INVL does not have enough headroom. REF starts to fall after VLO drops below its UVLO threshold.

Gamma reference GREF_O stays flat until AVDD does not have enough headroom. The external p-channel MOSFET still turns on after VLO drops below its UVLO threshold to guarantee GREF_O does not go over AVDD.

PG is pulled low after its input voltage (VBuck in this case) drops below the designated threshold. After VLO drops below its UVLO threshold, PG is not controlled and is resistively pulled up to its input voltage (VLO in this case.)

VGH and VGHM will be discharged by uP6668 as VIN is lower than its UVLO threshold.

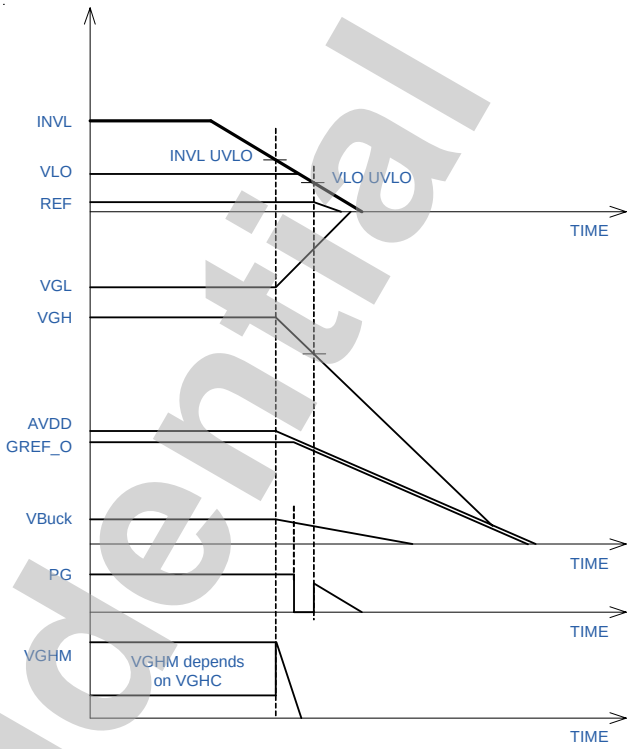


Figure 3. Power Off Sequence

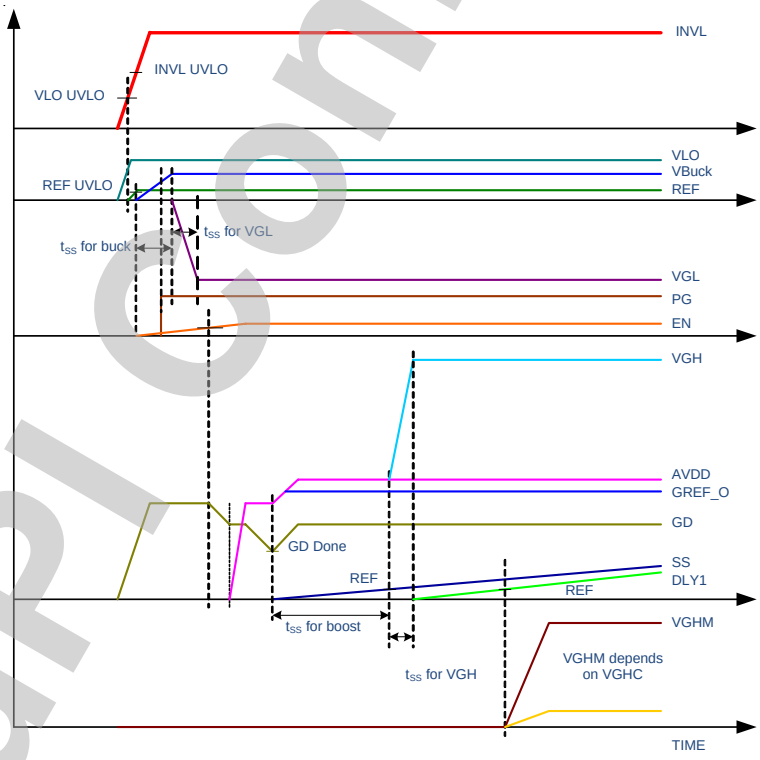


Figure 2. Power On Sequence

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Absolute Maximum Rating

(Note 1)

INVL, INB, OP_SUP, EN, FSEL, GD, GD_S, GREF_I to GND ---------- -0.3V to +24V

PGND, OGND, CPGND, to GND ---------- -0.3V to +0.3V

DLY1, VGHC, VGHM_END, VLO to GND ---------- -0.3V to +7.5V

REF, FBP, FBN, FB, FBB, COMP, SS, ILIM, PG, VDET, GREF_FB, VBuck to GND ---------- -0.3V to (VLO +0.3V)

LX to PGND ---------- -0.3V to +24V

OP_P, OP_N, OP_OUT to OGND ---------- -0.3V to (OP_SUP +0.3V)

DRVP to CPGND ---------- -0.3V to (CAPP +0.3V)

LXB to PGND ---------- -0.3V to (CAPN +0.3V)

CAPP to GND ---------- -0.7V to (INB +0.3V)

BST to VLO ---------- -0.3V to (GD_S +0.3V)

VGH to GND ---------- -0.3V to (INB +0.3V)

VGHM, VGHM_DSG to GND ---------- -0.3V to +30V

VGHM to VGHM_DSG ---------- -0.3V to +40V

GREF_O to GND ---------- -0.3V to (GREF +0.3V)

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

HBM (Human Body Mode) ---------- 2kV

MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

WQFN7x7-48L θ_{JA} ---------- 31°C/W

WQFN7x7-48L θ_{JC} ---------- 2°C/W

Power Dissipation, P_D @ T_A = 25°C

WQFN7x7-48L ---------- 3.23W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to *absolute maximum rating* conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

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Electrical Characteristics

(VIN= V_{INVL}= V_{INB} =12V, V_{OP_SUP} = V_{GREF_I} =15V, T_A= 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{INVL} , V_{INB} Supply Input Range			8	--	14	V
INVL + INB Quiescent Current		Only LXB switching (V_{FB} = V_{FBP} = 1.5V, V_{FBN} = 0V) EN = VLO, FSEL = high	--	8.5	20	mA
INVL + INB Standby Current		LXB not switching (V_{FB} = V_{FBB} = V_{FBP} = 1.5V, V_{FBN} = 0V) EN = VLO, FSEL = high	--	5	--	mA
Operation Frequency	FRE	FSEL = INVL or high impedance	630	750	870	kHz
		FSEL = GND	420	500	580	
FSEL Input Low Voltage		500kHz	--	--	0.6	V
FSEL Input High Voltage		750kHz	1.6	--	--	V
FSEL Pull-up Resistance			--	1	--	MΩ
INVL Undervoltage- Lockout	$INVL_{UVLO}$	INVL rising, 150mV typical hysteresis	6.0	7.0	8.0	V
Under Voltage Timer			--	50	--	ms
VL Regulator						
VL Output Voltage	VLO	I_{VLO} = 25mA, V_{FB} = V_{FBB} = V_{FBP} =1.1V, V_{FBN} = 0.4V (all regulators switching)	4.85	5	5.15	V
VL Undervoltage-Lockout Threshold	VLO_{UVLO}	VLO rising, 50mV typical hysteresis	3.5	3.9	4.3	V
Reference Voltage						
REF Output Voltage	REF	No external load	1.2375	1.250	1.2625	V
REF Load Regulation		0A < I_{LOAD} < 50uA	--	--	5	mV
REF Sink Current		In Regulation	10	--	--	uA
REF Undervoltage-Lockout Threshold	REF_{UVLO}	REF rising, 250mV typical hysteresis	--	1.0	1.2	V
Buck Regulator						
Output Voltage in Fixed Mode	VBuck	FBB = GND, no load	3.234	3.3	3.366	V
FBB Voltage in Adjustable Mode	FBB	VBuck = 2.5V, no load	1.2375	1.25	1.2625	V
FBB Adjustable Mode Threshold Voltage			0.1	0.15	0.2	V
Output Voltage Adjustable Range	VBuck		1.5	--	5	V
FBB UVP Level	V_{BU_UVP}	Falling edge	0.96	1.0	1.04	V
FBB Input Leakage Current	I_{BU_LEAK}	FBB = 1.25V	50	125	200	nA
DC Load Regulation		0A < I_{LOAD} < 2A	--	0.5	--	%
DC Line Regulation		No load, 10.8V < INB <13.2V	--	0.1	--	%/V

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Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LXB-to-INB nMOS Switch On-Resistance	$R_{BU_DS(ON)}$		--	100	200	mΩ
LXB-to-GND nMOS Switch On-Resistance			6	10	23	Ω
BST-to-VLO pMOS Switch On-Resistance			30	40	110	Ω
LXB Positive Current Limit	I_{BU_LIM}		2	2.5	3	A
Soft-Start Ramp Time	t_{BU_SS}	Zero to full limit	--	3	--	ms
Maximum Duty Factor	D_{BU}		70	78	85	%
Boost Converter						
Output Voltage Range	V_{AVDD}		V_{INVL}	--	20	V
Oscillator Maximum Duty Cycle	D_{BO}		70	78	85	%
FB Regulation Voltage	V_{FB}	FB = COMP, C_{COMP} = 1nF	1.2375	1.25	1.2625	V
FB UVP Level	V_{BO_UVP}	Falling edge	0.96	1.0	1.04	V
FB Load Regulation		I_{AVDD} = 0.1A to full	--	0.5	--	%
FB Line Regulation		V_{IN}=10.8V to 13.2V, I_{AVDD} =100mA	--	0.08	--	%/V
FB Input Bias Current	I_{FB}	V_{FB} = 1.25V	30	125	200	nA
FB Transconductance		ΔI = +2.5uA at COMP, FB = COMP	300	560	700	uS
FB Voltage Gain		FB to COMP	--	1400	--	V/V
LX Leakage Current	I_{BO_LEAK}	FB = 1.5V, VLX = 20V	--	10	40	uA
LX Current Limit	I_{BO_LIM}	FB = 1.1V, R_{ILIM} = unconnected	3.6	4.2	4.8	A
		FB = 1.1V, with R_{ILIM} at ILIM pin	-20%	4.2-(68-k/RILIM)	+20%	
ILIM Voltage		R_{ILIM} =60.5kΩ	0.56	0.625	0.69	V
Current-Sense Transresistance			0.19	0.21	0.25	V/A
LX On-Resistance	$R_{BO_DS(ON)}$		--	0.1	0.185	Ω
Soft-Start Period	t_{BO_SS}	C_{SS} < 200pF	--	16	--	ms
Soft-Start Current	I_{SS}	V_{SS} = 1.2V	4	5.5	7	uA
Gate Driver Isolation Switch Control						
GD to GD_S Pull-up Resistance		EN = 0V	--	25	50	Ω
GD Output Sink Current		EN = VLO	5	10	15	uA
GD Done Threshold		$V_{GD_S - VGD}$ at EN = VLO	5	6	7	V

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Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VGH Charge Pump Regulator						
GD_S Input Supply Range			8.0	--	20	V
GD_S Input Supply Current		FBP = 1.5V (no switching)	--	0.15	0.3	mA
GD_S Overvoltage Threshold	V_{BO_OVP}	GD_S rising, 250mV typical hysteresis	20.1	21	22	V
FBP Regulation Voltage	V_{FBP}		1.2375	1.25	1.2625	V
FBP Line Regulation Error		V_{GD_S} = 11V to 16V, not in dropout	--	--	0.2	%/V
FBP Input Bias Current	I_{FBP}	V_{FB} = 1.5V	-50	--	50	nA
DRVP p-Channel MOSFET On-Resistance			--	1.5	3	Ω
DRVP n-Channel MOSFET On-Resistance			--	1	2	Ω
FBN OVP Level	V_{NC_UVP}	Rising edge	720	800	880	mV
Negative Charge-Pump Soft-Start Period	t_{NC_SS}	FSEL = INVL or high impedance	--	2	--	ms
		FSEL = GND	--	3	--	
VGL Charge Pump Regulator						
FBN Regulation Voltage		V_{REF} - V_{FBN}	0.99	1.0	1.01	V
FBP Input Bias Current	I_{FBN}	V_{FBN} = 0V	-50	--	50	nA
FBP Line Regulation Error		V_{INB} = 11V to 16V, not in dropout	--	--	0.2	%/V
DRVN p-Channel MOSFET On-Resistance			--	1.5	3	Ω
DRVN n-Channel MOSFET On-Resistance			--	1	2	Ω
FBN OVP Level	V_{NC_UVP}	Rising edge	720	800	880	mV
Negative Charge-Pump Soft-Start Period	t_{NC_SS}	FSEL = INVL or high impedance	--	2	--	ms
		FSEL = GND	--	3	--	
Operational Amplifier						
OP Supply Range	V_{OP_SUP}		8	--	20	V
OP_SUP Overvoltage Threshold	V_{BO_OVP}	V_{OP_SUP} rising, hysteresis = 200mV	20.1	21	22	V
OP_SUP Supply Current		Buffer configuration, V_{OP_P} = V_{OP_N} = V_{OP_SUP}/2, no load	--	2	4	mA
Input Offset Voltage		2V < (V_{OP_P}, V_{OP_N}) < (V_{OP_SUP} - 2V)	-20	0	20	mV
Input Bias Current		2V < (V_{OP_P}, V_{OP_N}) < (V_{OP_SUP} - 2V)	-1	--	+1	uA
Input Common-Mode Voltage Range			0	--	V_{OP_SUP}	V

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Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Common-Mode Rejection Ratio		2V < (V_{OP_P}, V_{OP_N}) < (V_{OP_SUP} - 2V)	--	80	--	dB
Output Voltage Swing High		I_{OP_O} = 25mA	V_{OP_SUP} -320	V_{OP_SUP} -150	--	mV
Output Voltage Swing Low		I_{OP_O} = -25mA	--	150	300	mV
Large Signal Voltage Gain		2V < (V_{OP_P}, V_{OP_N}) < (V_{OP_SUP} - 2V)	--	80	--	dB
Slew Rate		2V < (V_{OP_P}, V_{OP_N}) < (V_{OP_SUP} - 2V)	--	45	--	V/us
-3dB Bandwidth	F_{3dB}	2V < (V_{OP_P}, V_{OP_N}) < (V_{OP_SUP} - 2V)	--	20	--	MHz
Short-Circuit Current	I_{OP_SC}	V_{OP_O} = V_{OP_SUP}/2, short OP_O to GND	100	--	--	mA
		V_{OP_O} = V_{OP_SUP}/2, short OP_O to V_{OP_SUP}	100	--	--	
High Voltage Switch Array						
VGH Supply Range	VGH		--	--	35	V
VGH Supply Current	IGH		--	150	300	uA
VGHM-to-VGH Switch On-Resistance		V_{DLY1}= 2V, VGHC = VLO	--	5	10	Ω
VGHM-to-VGH Switch Saturation Current		VGH - VGHM > 5V	150	390	--	mA
VGHM-to-VGHM_DSG Switch On-Resistance		V_{DLY1} = 2V, VGHC = GND	--	20	50	Ω
VGHM-to-VGHM_DSG Switch Saturation Current		VGHM - VGHM_DSG > 5V	75	200	--	mA
VGHM-to-GND Switch On-Resistance		DLY1 = GND	1	2.5	4	kΩ
VGHC Input Low Voltage	V_{IL}		--	--	0.6	V
VGHC Input High Voltage	V_{IH}		1.6	--	--	V
VGHC Input Current		VGHC = 0V or VLO	-1	--	+1	uA
VGHC-to-VGHM Rising Propagation Delay		1kΩ from VGHM_DSG to CPGND, VGHC = 0V to VLO step, no load on VGHM, measured from VGHC = 2V to VGHM = 20%	--	100	--	ns
VGHC-to-VGHM Falling Propagation Delay		1kΩ from VGHM_DSG to CPGND, VGHC = VLO to 0V step, no load on VGHM_DSG and VGHM, measured from VGHC = 0.6V to VGHM = 80%	--	200	--	ns
VGHM_END-to-VGHM Voltage Gain			9.4	10	10.6	V/V

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Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Sequence Control						
EN Pull-down Resistance		V_{DET} falling	--	1	--	mΩ
DLY1 Charge Current		V_{DLY1} = 1V, if DLY1 cap is not used, there is no delay.	6	8	10	uA
EN, DLY1 Turn-on Threshold			1.19	1.25	1.31	V
DLY1 Discharge Switch On-Resistance		EN = GND, SCP, or UVP.	--	10	--	Ω
FBN Discharge Switch On-Resistance		(EN = GND and INVL < UVLO), SCP, or UVP.	--	3	--	kΩ
Gamma Reference						
GREF_I Input Voltage Range	V_{GREF_I}		10	--	18	V
GREF_I Undervoltage Lockout		GREF_I rising	--	--	5.2	V
GREF_I Input Bias Current		No Load	--	125	250	uA
GREF_O Dropout Voltage		I_{GREF_O} = 60mA	--	0.25	0.5	V
GREF_FB Regulation Voltage		V_{GREF_I} = 13.5V, 1mA ≤ I_{GREF_O} ≤ 30mA, V_{GREF_O} = 9.5V	1.2375	--	1.2625	V
		V_{GREF_I} from 10V to 18V, I_{GREF_O} = 20mA, V_{GREF_O} = 9.5V	--	--	0.9	mV/V
GREF_O Maximum Output Current			60	--	--	mA
PG Function						
VDET Threshold		VDET rising, hysteresis = 50mV	1.26	1.3	1.34	V
VDET Input Bias Current			50	175	300	nA
PG Output Voltage		VDET = AGND, I_{PG} = 1mA	--	--	0.4	V
Short Circuit Protection						
Boost Short-Circuit Protection		FB falling edge	0.36 x V_{REF}	0.4 x V_{REF}	0.44 x V_{REF}	V
Buck Short-Circuit Protection		Adjustable mode: FBB falling	0.18 x V_{REF}	0.2 x V_{REF}	0.22 x V_{REF}	V
		Fixed mode: VBuck falling, internal feedback divider voltage	0.18 x V_{REF}	0.2x V_{REF}	0.22 x V_{REF}	
Positive Charge-Pump Short-Circuit Protection		FBP falling edge	0.36 x V_{REF}	0.4 x V_{REF}	0.44 x V_{REF}	V
Negative Charge-Pump Short-Circuit Protection		V_{REF} - V_{FBN}	0.4	0.45	0.5	V
Over Temperature Protection						
Over Temperature Threshold	T_{OTP}		--	150	--	°C
Over Temperature Hysteresis	T_{OTP_HYS}		--	20	--	°C

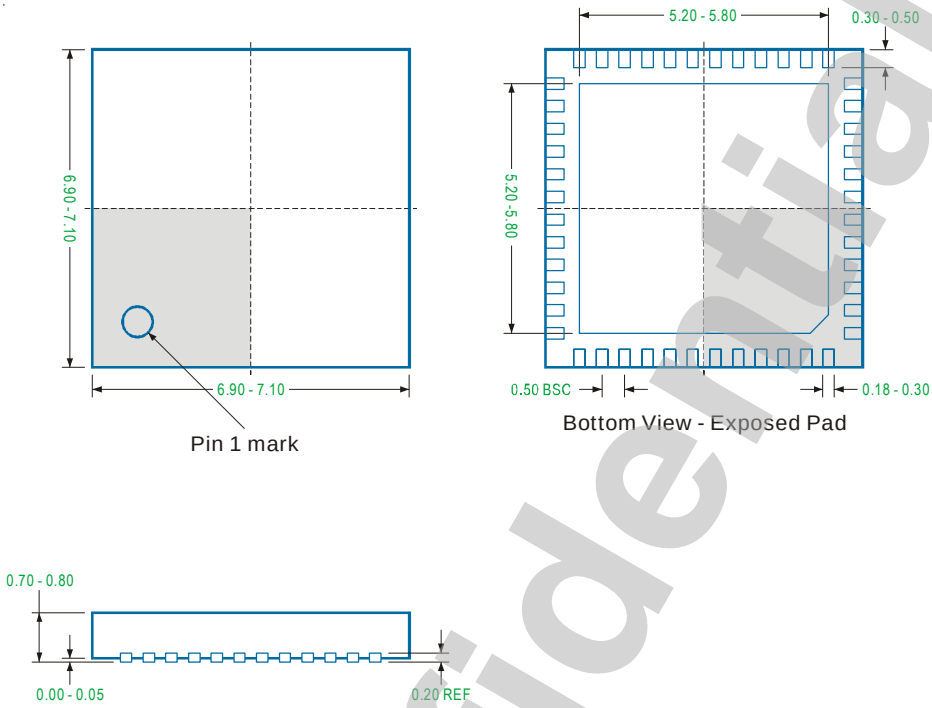
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Package Information

WQFN7x7-48L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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