

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4043B

MSI

Quadruple R/S latch with 3-state outputs

Product specification
File under Integrated Circuits, IC04

January 1995

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DESCRIPTION

The HEF4043B is a quadruple R/S latch with 3-state outputs with a common output enable input (EO). Each latch has an active HIGH set input (S_0 to S_3), an active HIGH reset input (R_0 to R_3) and an active HIGH 3-state output (O_0 to O_3).

When EO is HIGH, the state of the latch output (O_n) can be determined from the function table below. When EO is LOW, the latch outputs are in the high impedance OFF-state. EO does not affect the state of the latch.

The high impedance off-state feature allows common busing of the outputs.

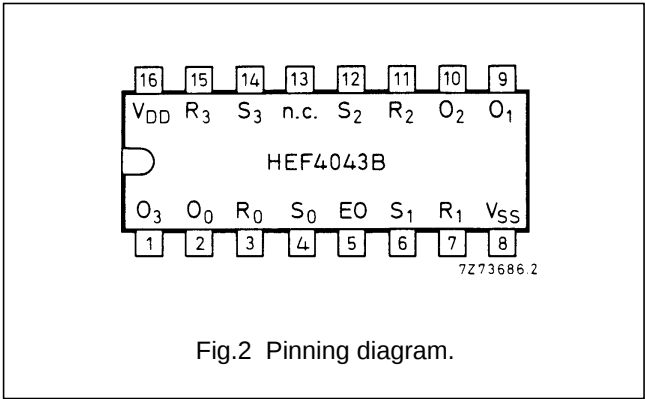


Fig.2 Pinning diagram.

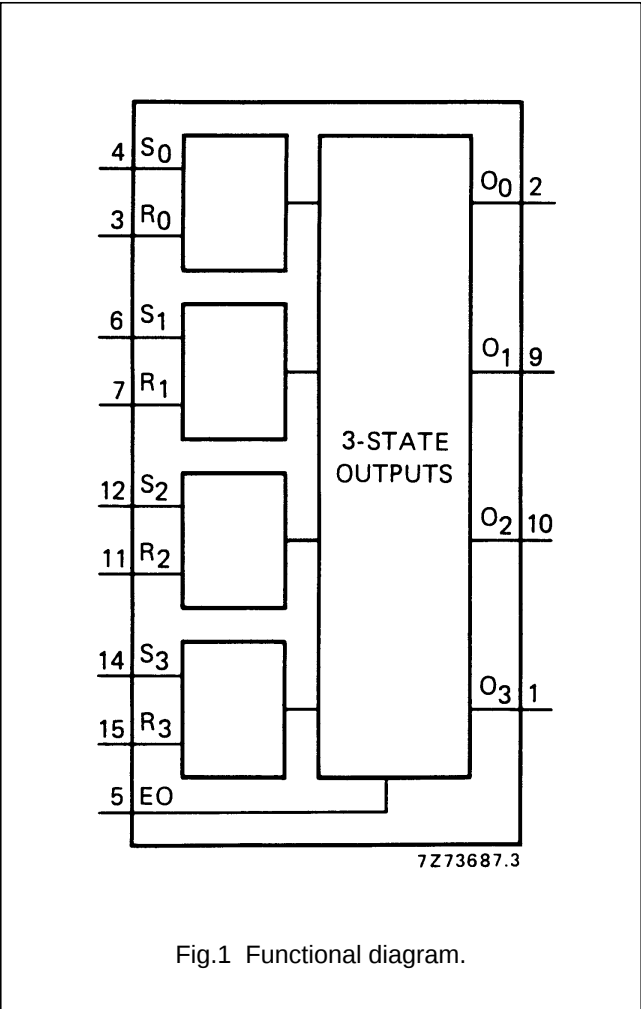


Fig.1 Functional diagram.

HEF4043BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4043BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4043BT(D): 16-lead SO; plastic (SOT109-1)
(): Package Designator North America

PINNING

EO common output enable input
 S_0 to S_3 set inputs (active HIGH)
 R_0 to R_3 reset inputs (active HIGH)
 O_0 to O_3 3-state buffered latch outputs

FUNCTION TABLE

INPUTS			OUTPUT O_n
EO	S_n	R_n	
L	X	X	Z
H	L	H	L
H	H	X	H
H	L	L	latched

Notes

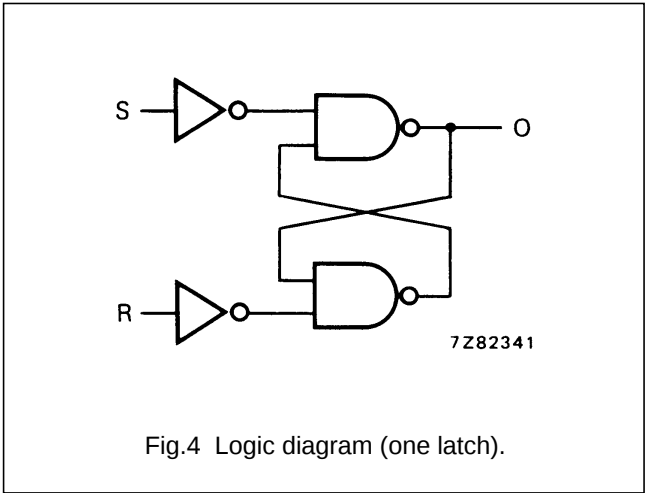
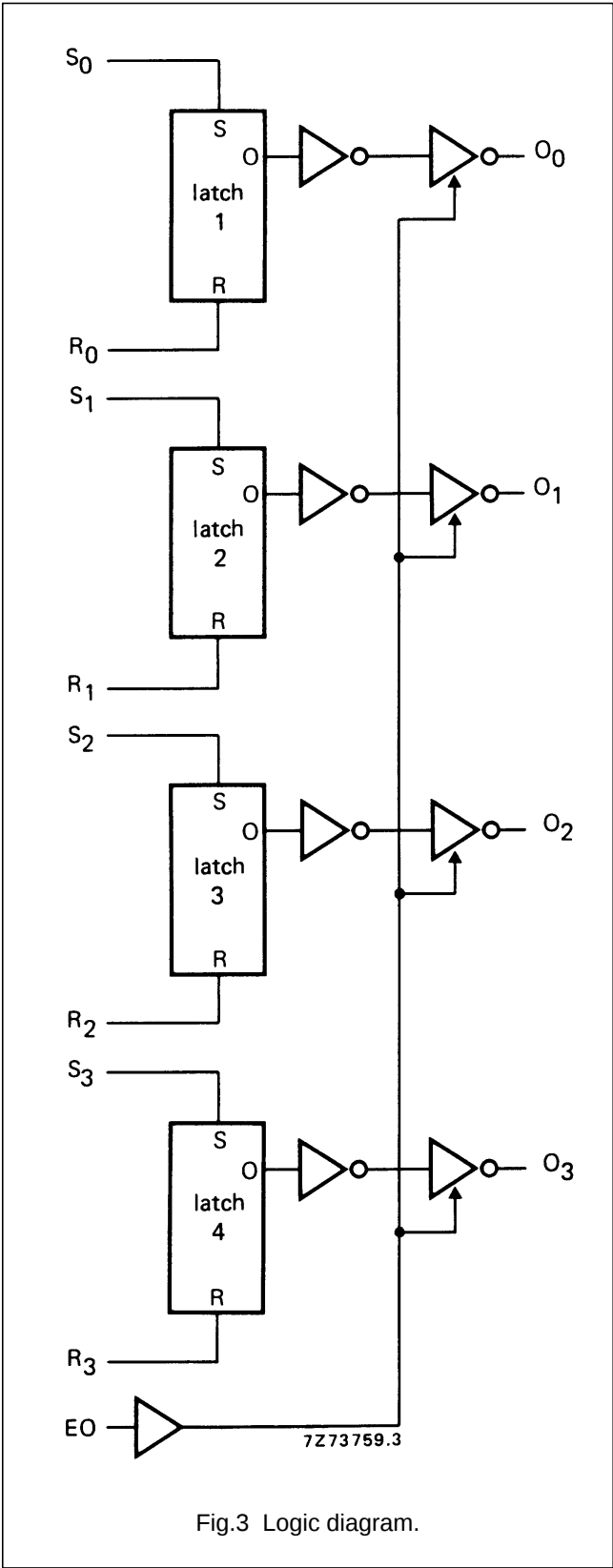
- H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state immaterial
Z = high impedance state

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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AC CHARACTERISTICS

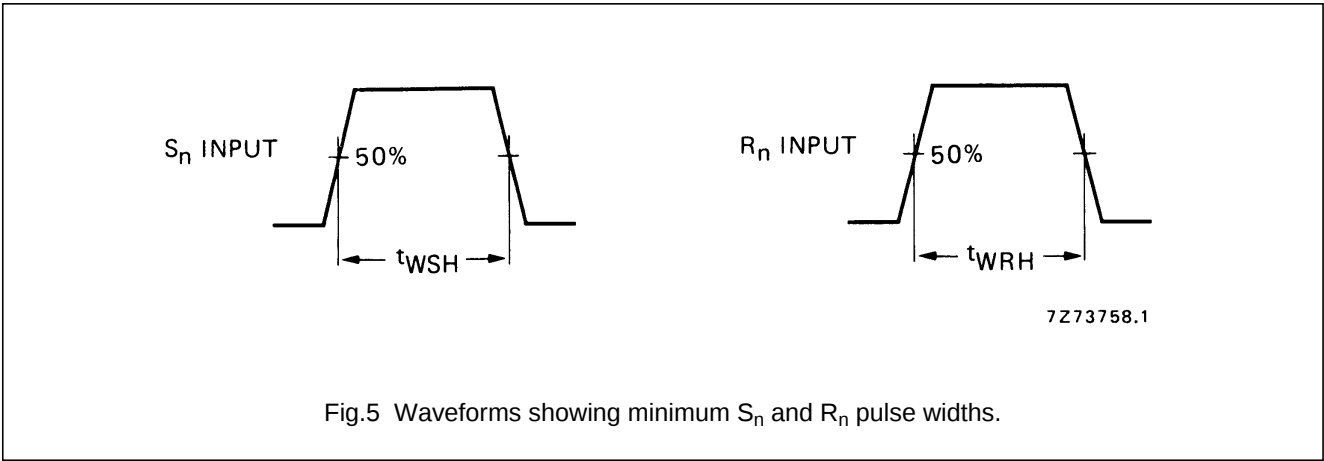
 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$R_n \rightarrow O_n$	5			90	180 ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70 ns	24 ns + (0,23 ns/pF) C_L
	15			25	50 ns	17 ns + (0,16 ns/pF) C_L
$S_n \rightarrow O_n$	5			65	135 ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		25	50 ns	14 ns + (0,23 ns/pF) C_L
	15			15	35 ns	7 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
	10	t_{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
3-state propagation delays						
Output disable times						
$EO \rightarrow O_n$	5			45	90 ns	
HIGH	10	t_{PHZ}		20	35 ns	
	15			10	25 ns	
LOW	5			50	100 ns	
	10	t_{PLZ}		20	40 ns	
	15			10	25 ns	
Output enable times						
$EO \rightarrow O_n$	5			25	50 ns	
HIGH	10	t_{PZH}		15	30 ns	
	15			10	25 ns	
LOW	5			40	80 ns	
	10	t_{PZL}		20	45 ns	
	15			15	35 ns	
Minimum S_n	5		30	15	ns	see also waveforms Fig.5
pulse width; HIGH	10	t_{WSH}	20	10	ns	
	15		16	8	ns	
Minimum R_n	5		30	15	ns	
pulse width; HIGH	10	t_{WRH}	20	10	ns	
	15		16	8	ns	

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	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	1100 f _i + Σ(f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	4400 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	11 400 f _i + Σ(f _o C _L) × V _{DD} ²	



APPLICATION INFORMATION

An example of application for the HEF4043B is:

- Four-bit storage with output enable