



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Revised V_{TERM} to V_{T1} and V_{T2} Revised Test Condition of $I_{\text{SB1}}/I_{\text{DR}}$ Added LL Spec.	Feb.2.2009
Rev. 1.2	Revised Test Condition of $I_{\text{CC}}/I_{\text{SB}}$ Revised <u>FEATURES & ORDERING INFORMATION</u> <u>Lead free and green package available</u> to <u>Green package available</u> Deleted T_{SOLDER} in <u>ABSOLUTE MAXIMUN RATINGS</u> Added packing type in <u>ORDERING INFORMATION</u>	Apr.17.2009

FEATURES

- Fast access time : 10/12/15ns
- Low power consumption:
Operating current : 60/50/40mA (TYP.)
Standby current : 0.5mA (TYP.)
1μA (TYP.) LL-version
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 28-pin 300 mil SOJ
28-pin 8mm x 13.4mm STSOP

GENERAL DESCRIPTION

The LY61L256 is a 262,144-bit high speed CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

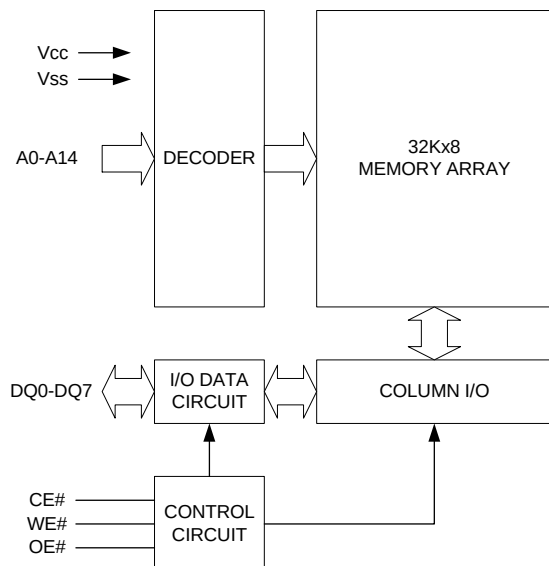
The LY61L256 is well designed for high speed system application. Easy expansion is provided by using an active LOW Chip Enable(CE#). The active LOW Write Enable(WE#) controls both writing and reading of the memory.

The LY61L256 operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{CC} ,TYP.)
LY61L256	0 ~ 70°C	3.15 ~ 3.6V	10ns	0.5mA	60mA
LY61L256	0 ~ 70°C	3.0 ~ 3.6V	12/15ns	0.5mA	50/40mA
LY61L256(E)	-20 ~ 80°C	3.15 ~ 3.6V	10ns	0.5mA	60mA
LY61L256(E)	-20 ~ 80°C	3.0 ~ 3.6V	12/15ns	0.5mA	50/40mA
LY61L256(I)	-40 ~ 85°C	3.15 ~ 3.6V	10ns	0.5mA	60mA
LY61L256(I)	-40 ~ 85°C	3.0 ~ 3.6V	12/15ns	0.5mA	50/40mA
LY61L256(LL)	0 ~ 70°C	3.15 ~ 3.6V	10ns	1μA(LL)	60mA
LY61L256(LL)	0 ~ 70°C	3.0 ~ 3.6V	12/15ns	1μA(LL)	50/40mA
LY61L256(LLE)	-20 ~ 80°C	3.15 ~ 3.6V	10ns	1μA(LL)	60mA
LY61L256(LLE)	-20 ~ 80°C	3.0 ~ 3.6V	12/15ns	1μA(LL)	50/40mA
LY61L256(LLI)	-40 ~ 85°C	3.15 ~ 3.6V	10ns	1μA(LL)	60mA
LY61L256(LLI)	-40 ~ 85°C	3.0 ~ 3.6V	12/15ns	1μA(LL)	50/40mA

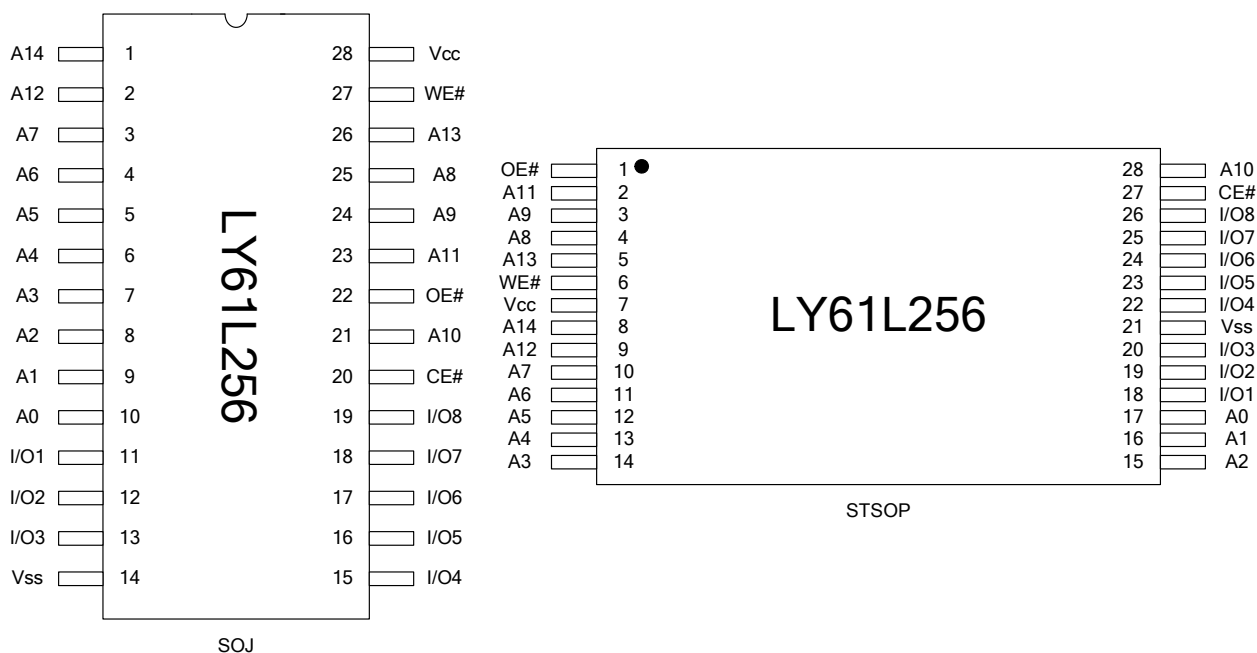
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ^{*4}	MAX.	UNIT
Supply Voltage	V _{CC}	-10	3.15	3.3	3.6	V
		-12/-15	3.0	3.3	3.6	V
Input High Voltage	V _{IH} ^{*1}		2.0	-	V _{CC} +0.5	V
Input Low Voltage	V _{IL} ^{*2}		-0.5	-	0.6	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	3.0	-	V
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA Others at V _{IL} or V _{IH}	-10	60	75	mA
			-12	50	60	mA
			-15	40	50	mA
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V	-	1	5	mA
Standby Power Supply Current	I _{SB}	CE# = V _{IH} , others at V _{IL} or V _{IH}	-	10	15	mA
	I _{SB1}	CE# ≥ V _{CC} - 0.2V	Normal	0.5	3	mA
		CE# ≥ V _{CC} - 0.2V Others at 0.2V or V _{CC} -0.2V	LL	1	20	μA

Notes:

1. $V_{IH(max)} = V_{CC} + 3.0V$ for pulse width less than 10ns.
2. $V_{IL(min)} = V_{SS} - 3.0V$ for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at $V_{CC} = V_{CC(TYP.)}$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C$, $f = 1.0MHz$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL$, $I_{OH}/I_{OL} = -4mA/8mA$

AC ELECTRICAL CHARACTERISTICS
(1) READ CYCLE

PARAMETER	SYM.	LY61L256-10		LY61L256-12		LY61L256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	ns
Chip Enable Access Time	t_{ACE}	-	10	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	5	-	6	-	7	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	2	-	3	-	4	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	5	-	6	-	7	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	5	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	1	-	3	-	3	-	ns

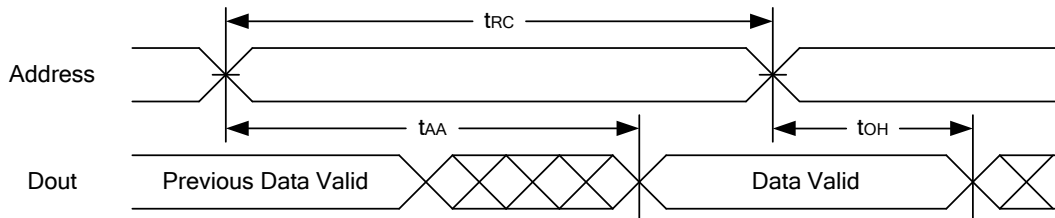
(2) WRITE CYCLE

PARAMETER	SYM.	LY61L256-10		LY61L256-12		LY61L256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	12	-	ns
Chip Enable to End of Write	t_{CW}	8	-	10	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	8	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	2	-	3	-	4	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	6	-	7	-	8	ns

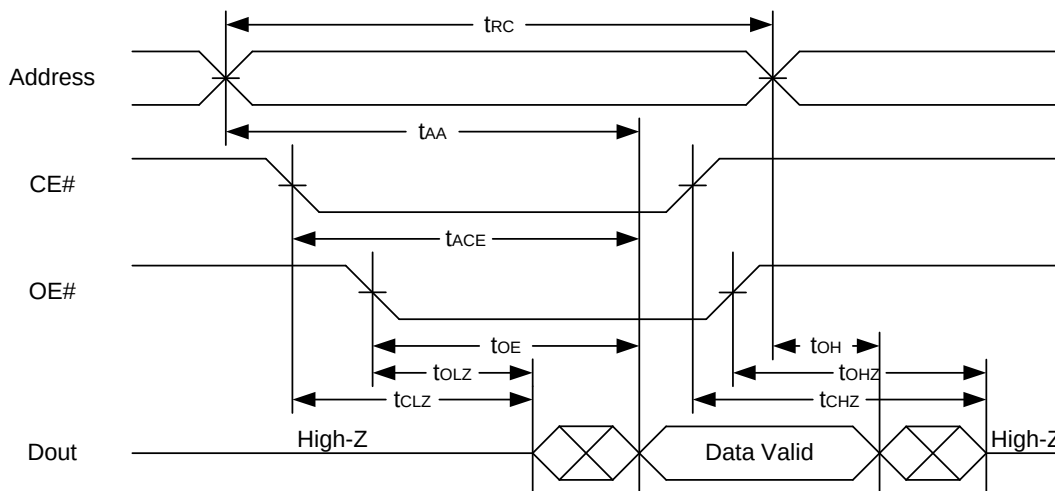
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



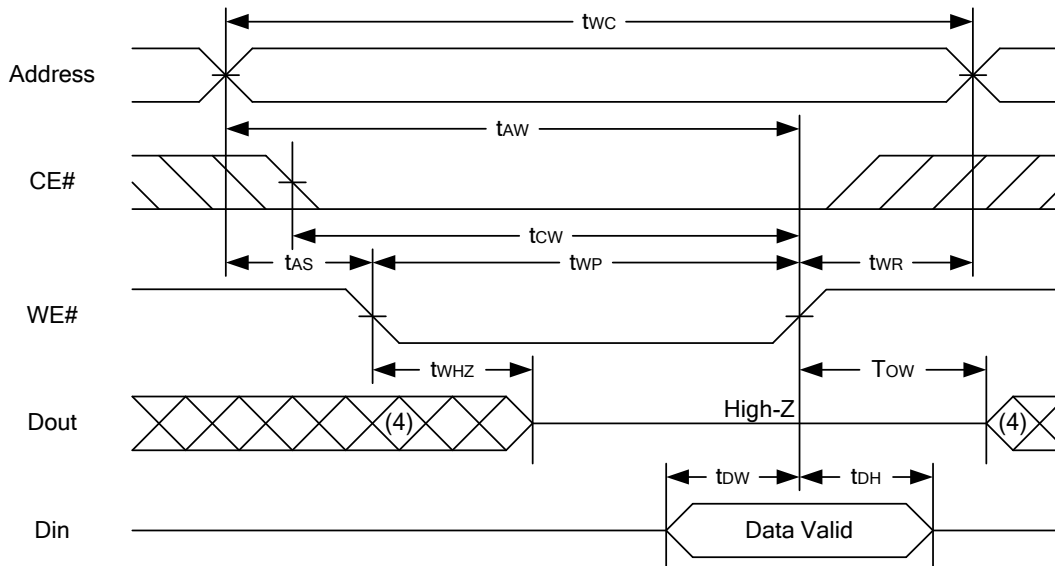
READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



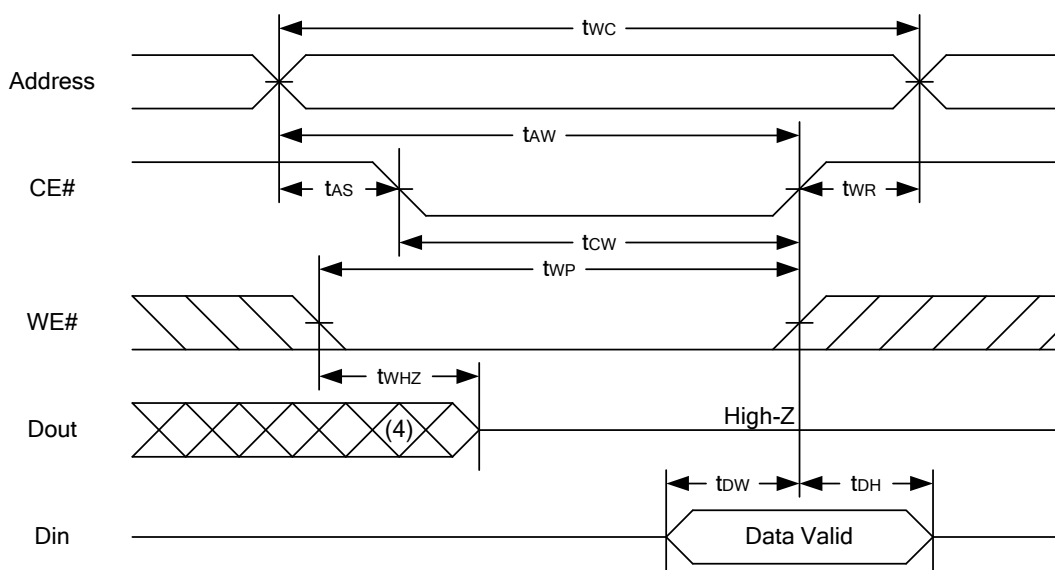
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



Notes :

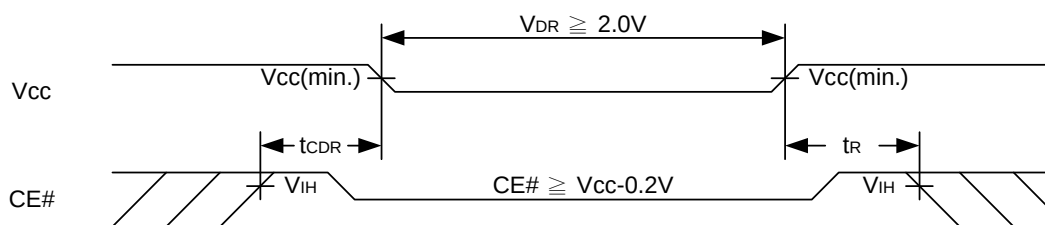
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, t_{wp} must be greater than $t_{wh} + t_{dw}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{ow} and t_{wh} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

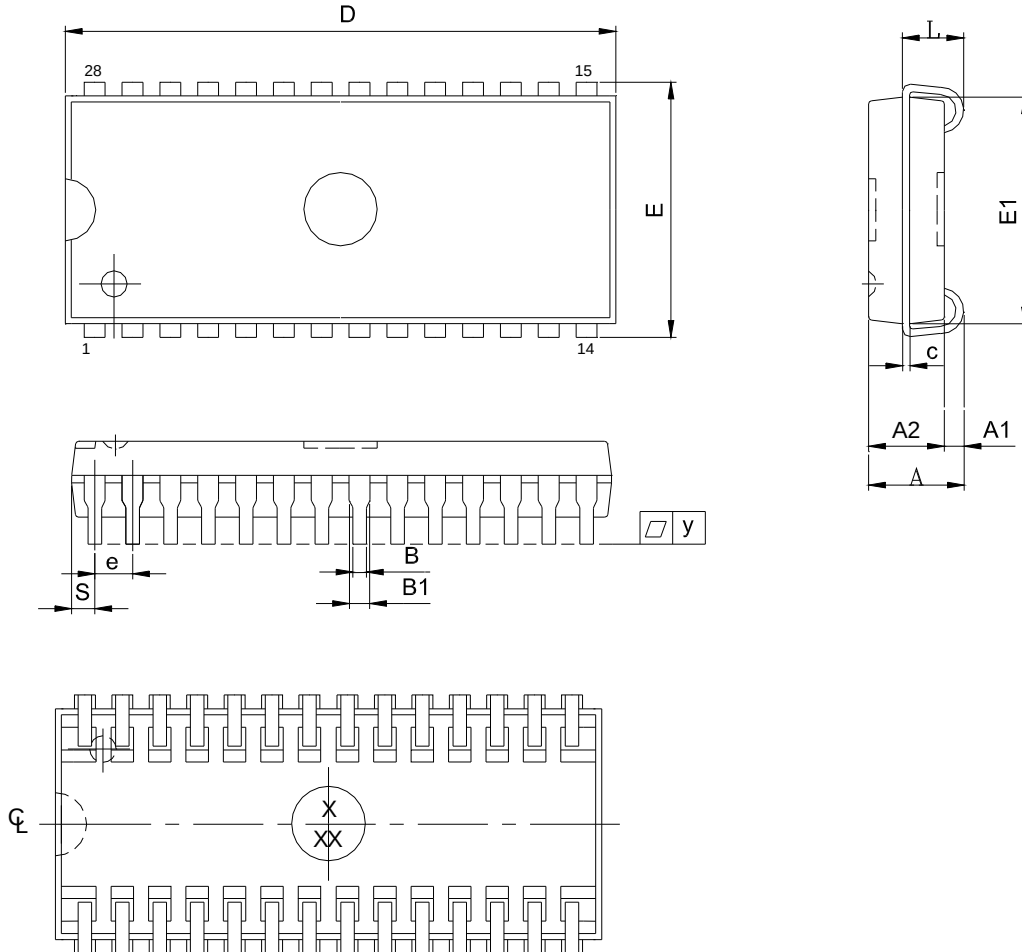
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V	2.0	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V CE# $\geq$ V _{CC} - 0.2V	-	0.3	2	mA
		V _{CC} = 2.0V CE# $\geq$ V _{CC} - 0.2V Others at 0.2V or V _{CC} -0.2V	-	0.5	20	μ A
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

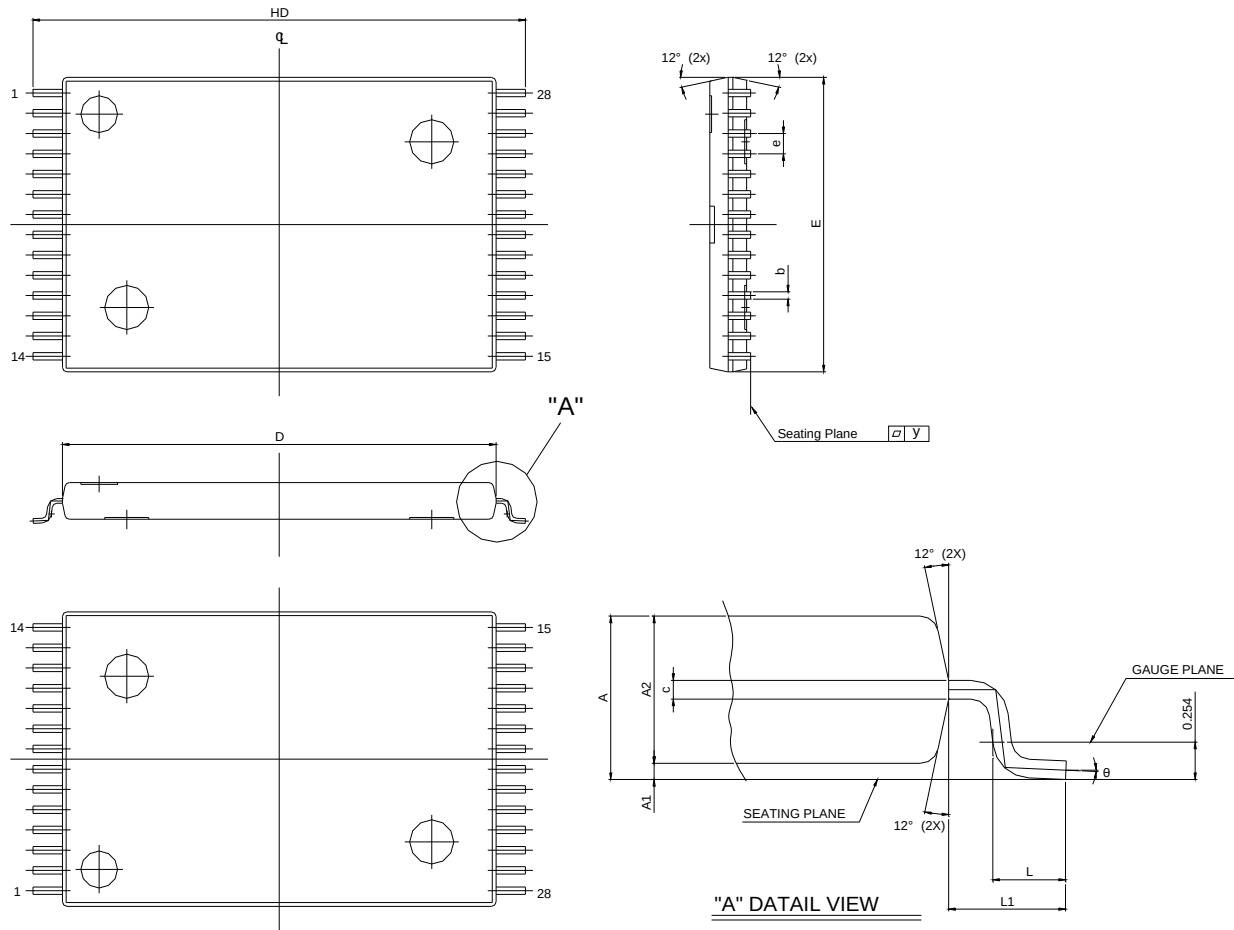


PACKAGE OUTLINE DIMENSION
28-pin 300 mil SOJ Package Outline Dimension


SYM. \ UNIT	INCH(REF)	MM(BASE)
A	0.140 (MAX)	3.556 (MAX)
A1	0.026 (MIN)	0.660 (MIN)
A2	0.100±0.005	2.540±0.127
B	0.018±0.003	0.457±0.076
B1	0.028 ±0.003	0.711±0.076
c	0.010±0.003	0.254±0.076
D	0.710±0.010	18.03±0.254
E	0.337±0.010	8.560±0.254
E1	0.300±0.005	7.620±0.127
e	0.050±0.003	1.270±0.076
L	0.087±0.010	2.210±0.254
S	0.030±0.004	0.762±0.102
Y	0.003 (MAX)	0.076 (MAX)

Note : 1.S/E/D dimension is not including mold flash.

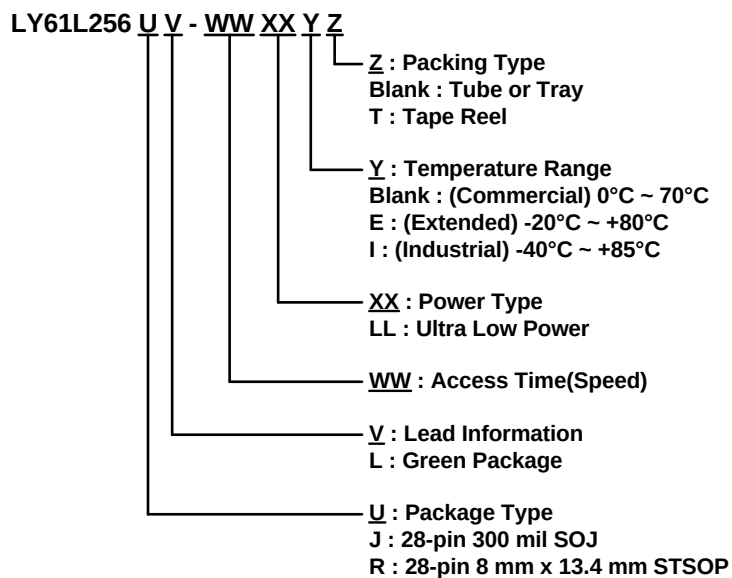
2.The end flash in package lengthwise is not more than 10 mils each side.

28 pin 8x13.4mm STSOP Package Outline Dimension


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	0.15	0.20	0.004	0.006	0.008
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
θ	0°	3°	5°	0°	3°	5°



ORDERING INFORMATION





Lyontek Inc.

LY61L256

Rev. 1.2

32K X 8 BIT HIGH SPEED CMOS SRAM

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