MX25U1635E

DATASHEET

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16M-BIT [x 1/x 2/x 4] 1.8V CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 16,777,216 x 1 bit structure or 8,388,608 x 2 bits (two I/O read mode) structure or 4,194,304 x 4 bits (four I/O read mode) structure
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - 1.65 to 2.0 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.0V to 1.4V

PERFORMANCE

- High Performance
  - Fast read for SPI mode
    - 1 I/O: 104MHz with 8 dummy cycles
    - 2 I/O: 84MHz with 4 dummy cycles, equivalent to 168MHz
    - 4 I/O: 104MHz with 6 dummy cycles, equivalent to 416MHz
  - Fast read for QPI mode
    - 4 I/O: 84MHz with 4 dummy cycles, equivalent to 336MHz
    - 4 I/O: 104MHz with 6 dummy cycles, equivalent to 416MHz
  - Fast program time: 1.2ms(typ.) and 3ms(max.)/page (256-byte per page)
  - Byte program time: 10us (typical)
  - 8/16/32/64 byte Wrap-Around Burst Read Mode
  - Fast erase time: 45ms (typ.)/sector (4K-byte per sector); 250ms(typ.) /block (32K-byte per block); 500ms(typ.) / block (64K-byte per block); 9s(typ.) /chip
- Low Power Consumption
  - Low active read current: 20mA(max.) at 104MHz, 15mA(max.) at 84MHz
  - Low active erase/programming current: 20mA (typ.)
  - Standby current: 25uA (typ.)
- Deep Power Down: 2uA(typ.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection

  The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
  - Additional 4k-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector or block

- Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Command Reset
- Program/Erase Suspend
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- NC/SIO3
  - NC pin or Serial input & Output for 4 x I/O read mode
- PACKAGE
  - 8-pin SOP (150mil)
  - 8-pin SOP (200mil)
  - 8-land WSON (6x5mm)
  - 8-land USON (4x4mm)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

The MX25U1635E are 16,777,216 bit serial Flash memory, which is configured as 2,097,152 x 8 internally. When it is in two or four I/O read mode, the structure becomes 8,388,608 bits x 2 or 4,194,304 bits x 4. MX25U1635E feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin and WP# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25U1635E MXSMIO® (Serial Multi I/O) provides sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for erase command is executed on sector (4K-byte), block (32K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode and typically draws 30uA DC current.

The MX25U1635E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

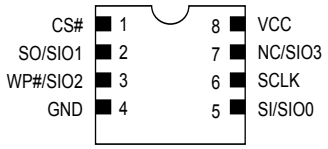
Table 1. Additional Feature Comparison

Additional Features / Part Name	Protection and Security		Read Performance					
			SPI				QPI	
	Flexible Block Protection (BP0-BP3)	4K-bit security OTP	1 I/O (104 MHz)	2 I/O (84 MHz)	4 I/O (84 MHz)	4 I/O (104 MHz)	4 I/O (84 MHz)	4 I/O (104 MHz)
MX25U1635E	V	V	V	V	V	V	V	V

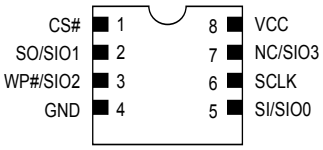
Additional Features / Part Name	Identifier			
	RES (command: AB hex)	REMS (command: 90 hex)	RDID (command: 9F hex)	QPIID (Command: AF hex)
MX25U1635E	35 (hex)	C2 35 (hex) (if ADD=0)	C2 25 35	C2 25 35

3. PIN CONFIGURATIONS

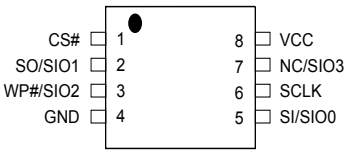
8-LAND USON (4x4mm)



8-LAND WSON (6x5mm)



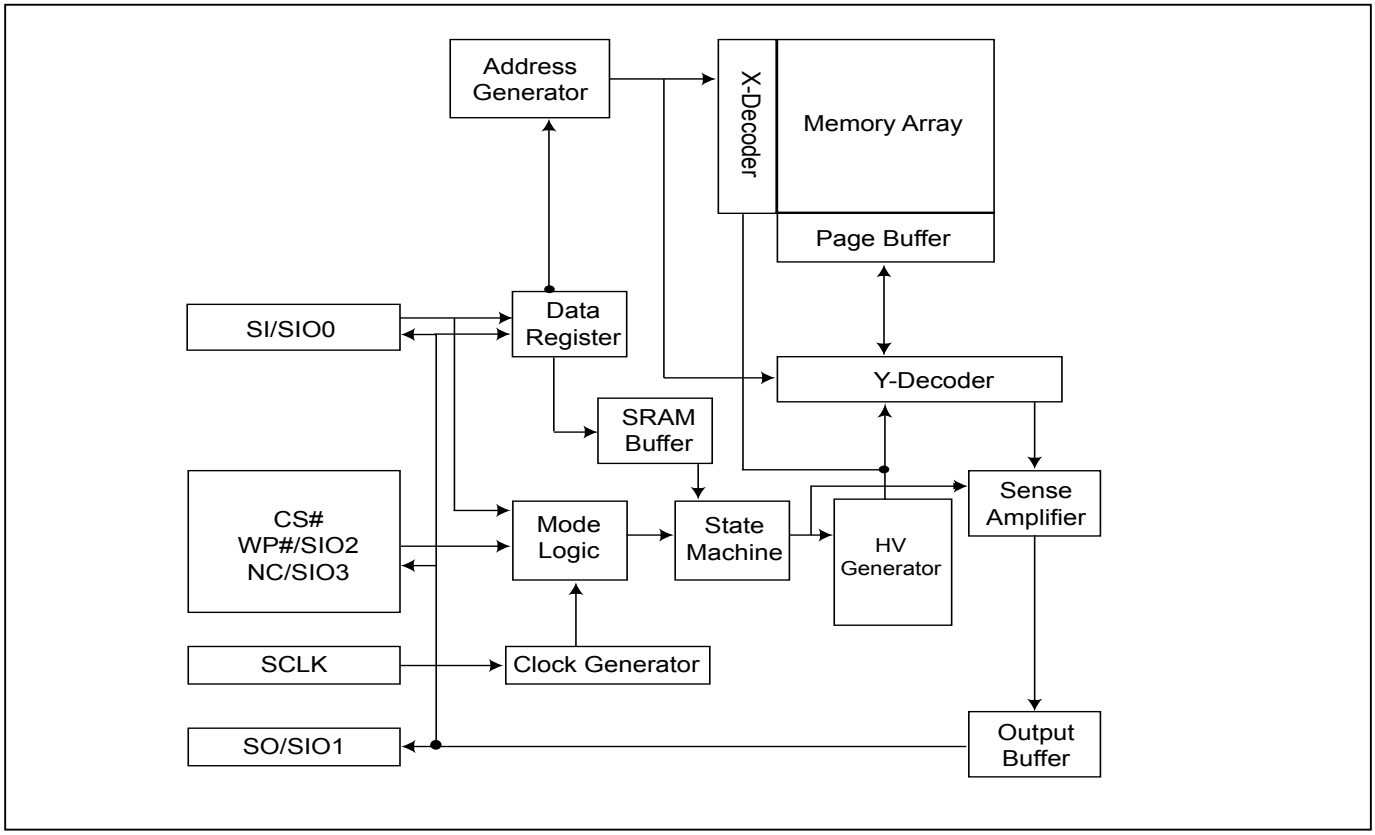
8-PIN SOP (150mil) / 8-PIN SOP (200mil)



4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (for 4xI/O read mode)
NC/SIO3	NC pin (Not connected) or Serial Data Input & Output (for 4xI/O read mode)
VCC	+ 1.8V Power Supply
GND	Ground

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Power-on reset and tPUW: to avoid sudden power switch by system power supply transition, the power-on reset and tPUW (internal timer) may protect the Flash.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issung other commands to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP) command completion
  - Quad I/O Page Program (4PP) command completion
  - Sector Erase (SE) command completion
  - Block Erase 32KB (BE32K) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion
  - Program/Erase Suspend
  - Softreset command completion
  - Write Security Register (WRSCUR) command completion
  - Write Protection Selection (WPSEL) command completion

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES) and softreset command.

- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

  I. Block lock protection

  - The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
  - The Hardware Proteced Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
  - In four I/O and QPI mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Status bit				Protect Level
BP3	BP2	BP1	BP0	
0	0	0	0	0 (none)
0	0	0	1	1 (1block, protected block 31st)
0	0	1	0	2 (2blocks, protected block 30th~31st)
0	0	1	1	3 (4blocks, protected block 28th~31st)
0	1	0	0	4 (8blocks, protected block 24th~31st)
0	1	0	1	5 (16blocks, protected block 16th~31st)
0	1	1	0	6 (32blocks, protected all)
0	1	1	1	7 (32blocks, protected all)
1	0	0	0	8 (32blocks, protected all)
1	0	0	1	9 (32blocks, protected all)
1	0	1	0	10 (16blocks, protected block 0th~15th)
1	0	1	1	11 (24blocks, protected block 0th~23rd)
1	1	0	0	12 (28blocks, protected block 0th~27th)
1	1	0	1	13 (30blocks, protected block 0th~29th)
1	1	1	0	14 (31blocks, protected block 0th~30th)
1	1	1	1	15 (32blocks, protected all)

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer. Please refer to *"Table 3. 4K-bit Secured OTP Definition"*.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with Enter Security OTP (ENSO) command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing Exit Security OTP (EXSO) command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 10. Security Register Definition"* for security register bit definition and *"Table 3. 4K-bit Secured OTP Definition"* for address range definition.

- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	

7. Memory Organization

Table 4. Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
31	63	511	1FF000h	1FFFFFh
	|	:	:	:
	62	496	1F0000h	1F0FFFh
30	61	495	1EF000h	1EFFFFh
	|	:	:	:
	60	480	1E0000h	1E0FFFh
29	59	479	1DF000h	1DFFFFh
	|	:	:	:
	58	464	1D0000h	1D0FFFh
28	57	463	1CF000h	1CFFFFh
	|	:	:	:
	56	448	1C0000h	1C0FFFh
27	55	447	1BF000h	1BFFFFh
	|	:	:	:
	54	432	1B0000h	1B0FFFh
26	53	431	1AF000h	1AFFFFh
	|	:	:	:
	52	416	1A0000h	1A0FFFh
25	51	415	19F000h	19FFFFh
	|	:	:	:
	50	400	190000h	190FFFh
24	49	399	18F000h	18FFFFh
	|	:	:	:
	48	384	180000h	180FFFh
23	47	383	17F000h	17FFFFh
	|	:	:	:
	46	368	170000h	170FFFh
22	45	367	16F000h	16FFFFh
	|	:	:	:
	44	352	160000h	160FFFh
21	43	351	15F000h	15FFFFh
	|	:	:	:
	42	336	150000h	150FFFh
20	41	335	14F000h	14FFFFh
	|	:	:	:
	40	320	140000h	140FFFh
19	39	319	13F000h	13FFFFh
	|	:	:	:
	38	304	130000h	130FFFh
18	37	303	12F000h	12FFFFh
	|	:	:	:
	36	288	120000h	120FFFh
17	35	287	11F000h	11FFFFh
	|	:	:	:
	34	272	110000h	110FFFh
16	33	271	10F000h	10FFFFh
	|	:	:	:
	32	256	100000h	100FFFh

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
15	31	255	0FF000h	0FFFFFh
	|	:	:	:
	30	240	0F0000h	0F0FFFh
14	29	239	0EF000h	0EFFFFh
	|	:	:	:
	28	224	0E0000h	0E0FFFh
13	27	223	0DF000h	0DFFFFh
	|	:	:	:
	26	208	0D0000h	0D0FFFh
12	25	207	0CF000h	0CFFFFh
	|	:	:	:
	24	192	0C0000h	0C0FFFh
11	23	191	0BF000h	0BFFFFh
	|	:	:	:
	22	176	0B0000h	0B0FFFh
10	21	175	0AF000h	0AFFFFh
	|	:	:	:
	20	160	0A0000h	0A0FFFh
9	19	159	09F000h	09FFFFh
	|	:	:	:
	18	144	090000h	090FFFh
8	17	143	08F000h	08FFFFh
	|	:	:	:
	16	128	080000h	080FFFh
7	15	127	07F000h	07FFFFh
	|	:	:	:
	14	112	070000h	070FFFh
6	13	111	06F000h	06FFFFh
	|	:	:	:
	12	96	060000h	060FFFh
5	11	95	05F000h	05FFFFh
	|	:	:	:
	10	80	050000h	050FFFh
4	9	79	04F000h	04FFFFh
	|	:	:	:
	8	64	040000h	040FFFh
3	7	63	03F000h	03FFFFh
	|	:	:	:
	6	48	030000h	030FFFh
2	5	47	02F000h	02FFFFh
	|	:	:	:
	4	32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
	|	:	:	:
	2	16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
	|	:	:	:
	0	2	002000h	002FFFh
		1	001000h	001FFFh
		0	000000h	000FFFh

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.

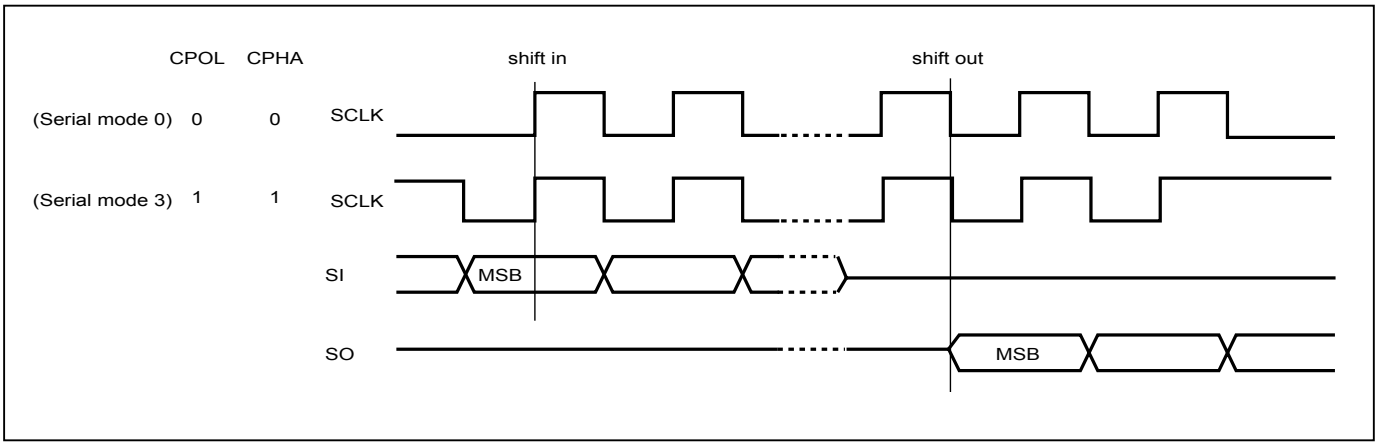
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, 2READ, 4READ, RES, REMS, SQIID, RDBLOCK, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, WPSEL, SBLK, SBULK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

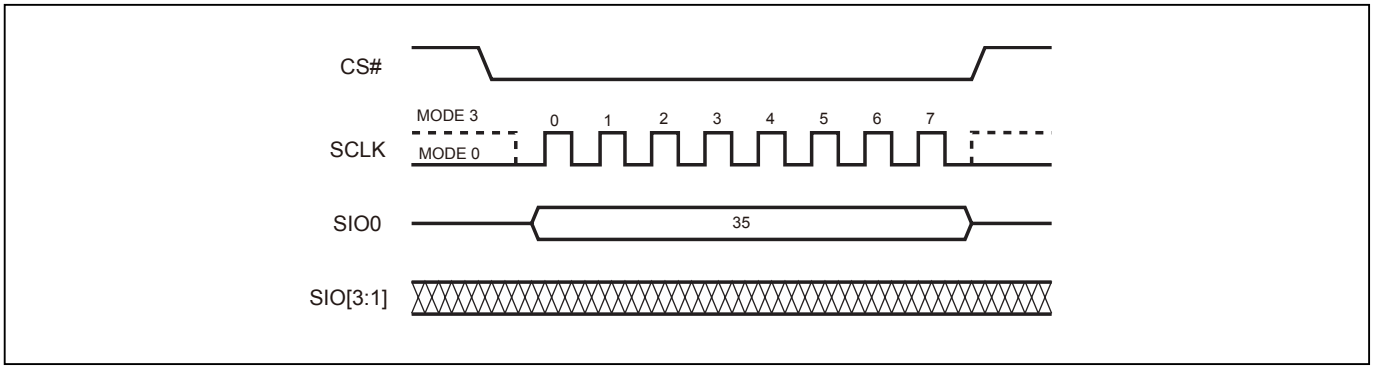
8-1. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing 35H command, the QPI mode is enabled.

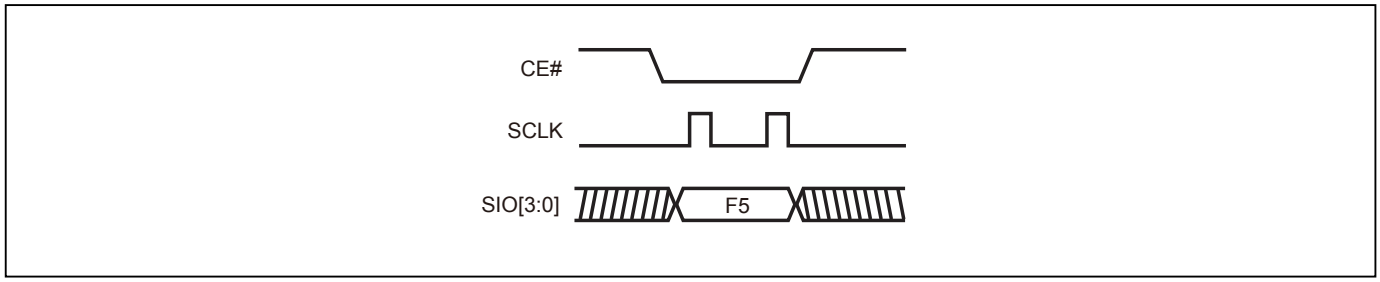
Figure 2. Enable QPI Sequence (Command 35H)



Reset QPI mode

By issuing F5H command, the device is reset to 1-I/O SPI mode.

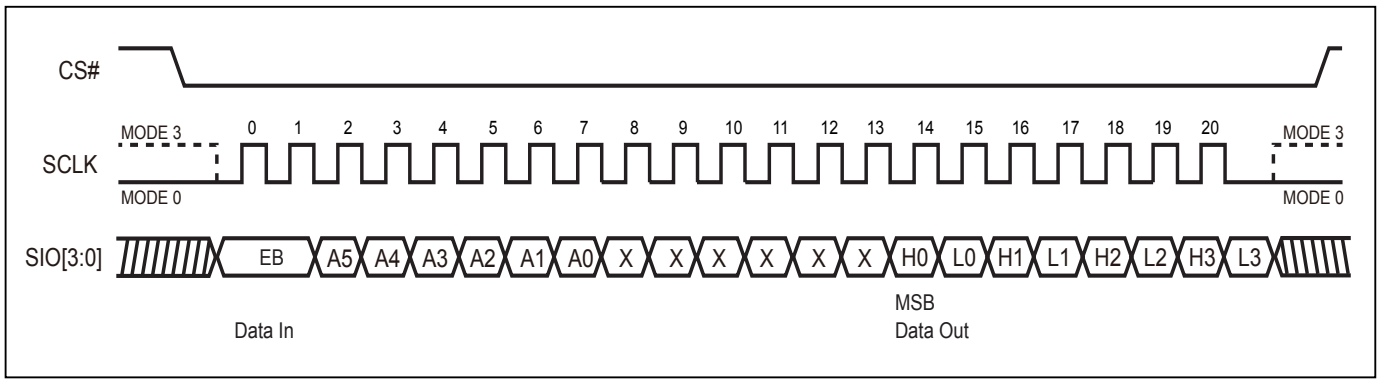
Figure 3. Reset QPI Mode (Command F5H)



Fast QPI Read mode (FASTRDQ)

To increase the code transmission speed, the device provides a "Fast QPI Read Mode" (FASTRDQ). By issuing command code EBH, the FASTRDQ mode is enabled. The number of dummy cycle increase from 4 to 6 cycles. The read cycle frequency will increase from 84MHz to 104MHz.

Figure 4. Fast QPI Read Mode (FASTRDQ) (Command EBH)



9. COMMAND DESCRIPTION

Table 5. Command Set

Read Commands

I/O	1	1	1	2	4	4	4	4
Read Mode	SPI	SPI	SPI	SPI	SPI	SPI	QPI	QPI
Command (byte)	READ (normal read)	FAST READ * (fast read data)	RDSFDP (Read SFDP)	2READ (2 x I/O read command) Note1	W4READ	4READ * (4 x I/O read command) Note1	FAST READ * (fast read data)	4READ * (4 x I/O read command) Note1
Clock rate (MHz)	33	104	104	84	84	104	84	104
1st byte	03 (hex)	0B (hex)	5A (hex)	BB (hex)	E7 (hex)	EB (hex)	0B (hex)	EB (hex)
2nd byte	AD1(8)	AD1(8)	AD1(8)	AD1(4)	AD1(2)	AD1(2)	AD1(2)	AD1(2)
3rd byte	AD2(8)	AD2(8)	AD2(8)	AD2(4)	AD2(2)	AD2(2)	AD2(2)	AD2(2)
4th byte	AD3(8)	AD3(8)	AD3(8)	AD3(4)	AD3(2)	AD3(2)	AD3(2)	AD3(2)
5th byte		Dummy(8)	Dummy(8)	Dummy(4)	Dummy(4)	Dummy(6)	Dummy(4)	Dummy(6)
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	Read SFDP mode	n bytes read out by 2 x I/O until CS# goes high	Quad I/O read with 4 dummy cycles in 84MHz	Quad I/O read with 6 dummy cycles in 104MHz	n bytes read out until CS# goes high	Quad I/O read with 6 dummy cycles in 104MHz

Program/Erase Commands

Command (byte)	WREN* (write enable)	WRDI * (write disable)	RDSR * (read status register)	WRSR * (write status register)	4PP (quad page program)	SE * (sector erase)	BE 32K * (block erase 32KB)
1st byte	06 (hex)	04 (hex)	05 (hex)	01 (hex)	38 (hex)	20 (hex)	52 (hex)
2nd byte				Values	AD1	AD1	AD1
3rd byte					AD2	AD2	AD2
4th byte					AD3	AD3	AD3
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to write new values of the status register	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block

Command (byte)	BE * (block erase 64KB)	CE * (chip erase)	PP * (page program)	DP * (Deep power down)	RDP * (Release from deep power down)	PGM/ERS Suspend * (Suspends Program/ Erase)	PGM/ERS Resume * (Resumes Program/ Erase)
1st byte	D8 (hex)	60 or C7 (hex)	02 (hex)	B9 (hex)	AB (hex)	B0 (hex)	30 (hex)
2nd byte	AD1		AD1				
3rd byte	AD2		AD2				
4th byte	AD3		AD3				
Action	to erase the selected block	to erase whole chip	to program the selected page	enters deep power down mode	release from deep power down mode		

Security/ID/Mode Setting/Reset Commands

Command (byte)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	ENSO * (enter secured OTP)	EXSO * (exit secured OTP)	RDSCUR * (read security register)	WRSCUR * (write security register)
1st byte	9F (hex)	AB (hex)	90 (hex)	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)
2nd byte		x	x				
3rd byte		x	x				
4th byte		x	ADD (Note 2)				
5th byte							
Action	outputs JEDEC ID: 1-byte Manufact-urer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	to enter the 4K-bit secured OTP mode	to exit the 4K-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)

COMMAND (byte)	SBLK * (single block lock	SBULK * (single block unlock)	RDBLOCK * (block protect read)	GBLK * (gang block lock)	GBULK * (gang block unlock)	NOP * (No Operation)	RSTEN * (Reset Enable)
1st byte	36 (hex)	39 (hex)	3C (hex)	7E (hex)	98 (hex)	00 (hex)	66 (hex)
2nd byte	AD1	AD1	AD1				
3rd byte	AD2	AD2	AD2				
4th byte	AD3	AD3	AD3				
Action	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect	read individual block or sector write protect status	whole chip write protect	whole chip unprotect		

COMMAND (byte)	RST * (Reset Memory)	EQIO (Enable Quad I/O)	RSTQIO (Reset Quad I/O)	QPIID (QPI ID Read)	SBL * (Set Burst Length)	WPSEL * (Write Protect Selection)
1st byte	99 (hex)	35 (hex)	F5 (hex)	AF (hex)	C0 (hex)	68 (hex)
2nd byte					Value	
3rd byte						
4th byte						
Action		Entering the QPI mode	Exiting the QPI mode	ID in QPI interface	to set Burst length	to enter and enable individal block protect mode

Note 1: Command set highlighted with (*) are supported both in SPI and QPI mode.
Note 2: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SI/SIO1 which is different from 1 x I/O condition.
Note 3: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
Note 4: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
Note 5: *Before executing RST command, RSTEN command must be executed. If there is any other command to interfere, the reset operation will be disabled.*

9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode. (Please refer to *"Figure 23. Write Enable (WREN) Sequence (Command 06) (SPI Mode)"* and *"Figure 24. Write Enable (WREN) Sequence (Command 06) (QPI Mode)"*)

9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode. (Please refer to *"Figure 26. Write Disable (WRDI) Sequence (Command 04) (QPI Mode)"* and *"Figure 25. Write Disable (WRDI) Sequence (Command 04) (SPI Mode)"*)

The WEL bit is reset by following situations:
- Power-up
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad Page Program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Pgm/Ers Suspend

9-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *"Table 9. ID Definitions"* ID Definitions.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

9-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode. (Please refer to *"Figure 28. Read Status Register (RDSR) Sequence (Command 05) (SPI Mode)"* and *"Figure 29. Read Status Register (RDSR) Sequence (Command 05) (QPI Mode)"*)

For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 5. Program/ Erase flow with read array data

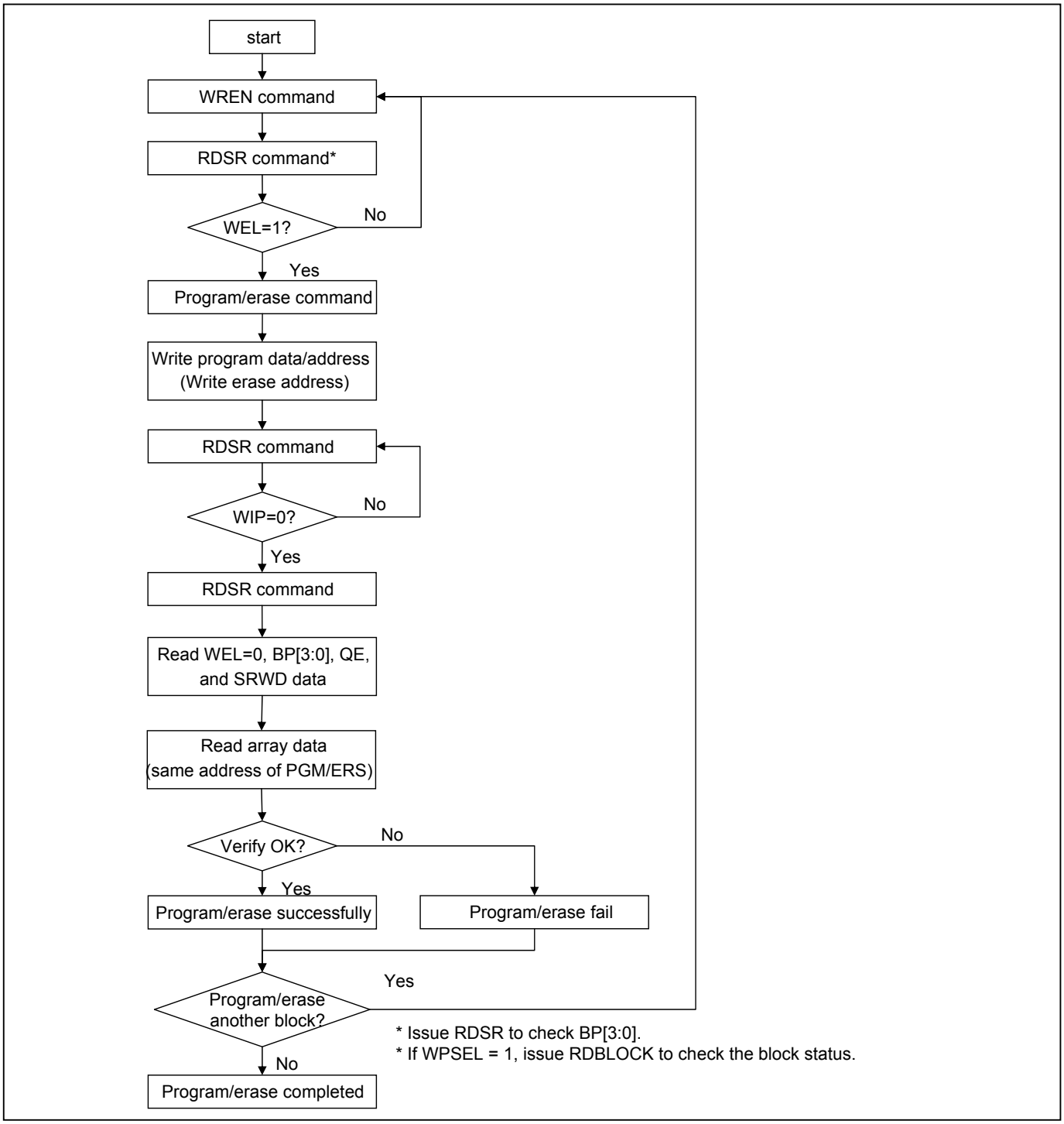


Figure 6. Program/ Erase flow without read array data (read P_FAIL/E_FAIL flag)

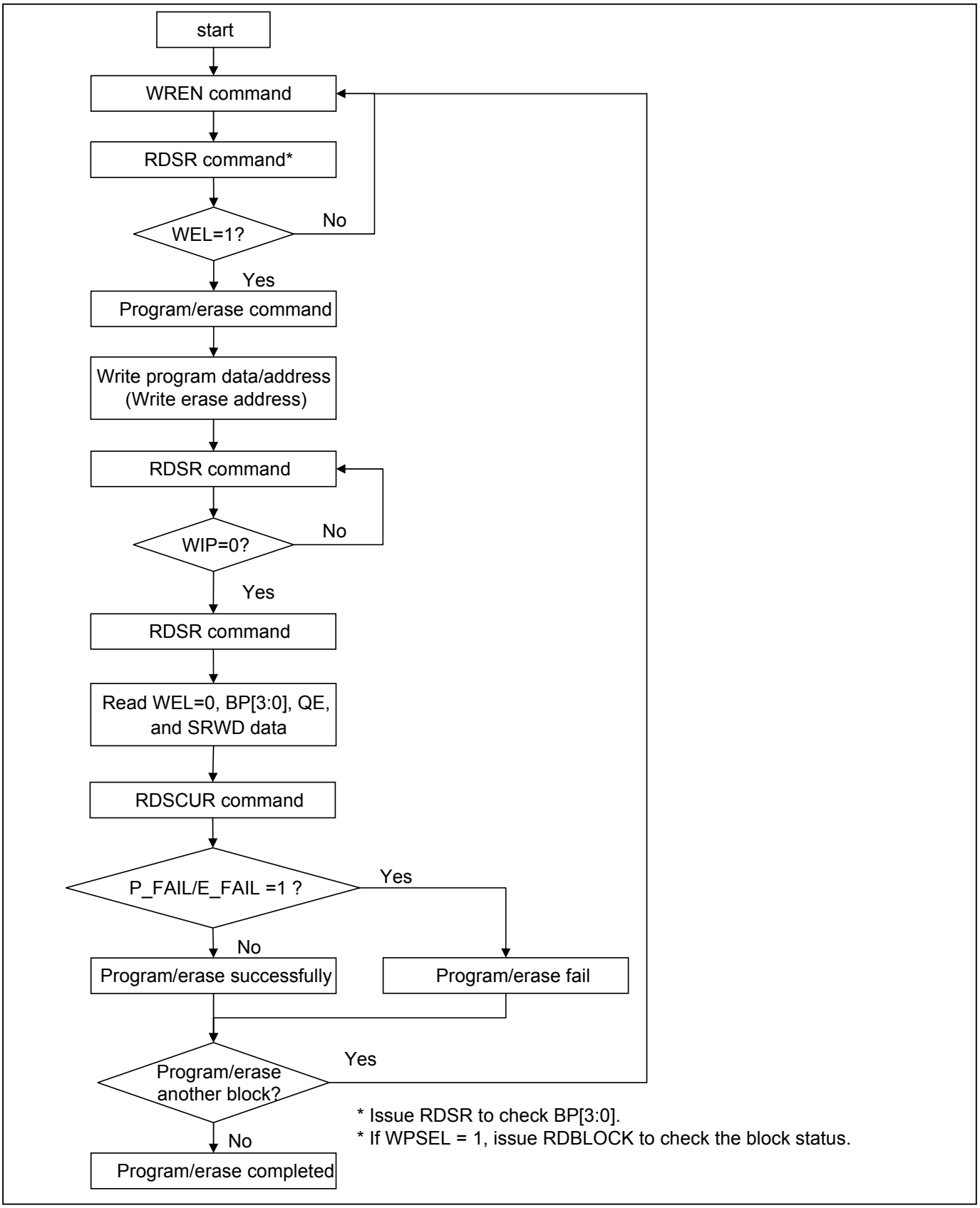
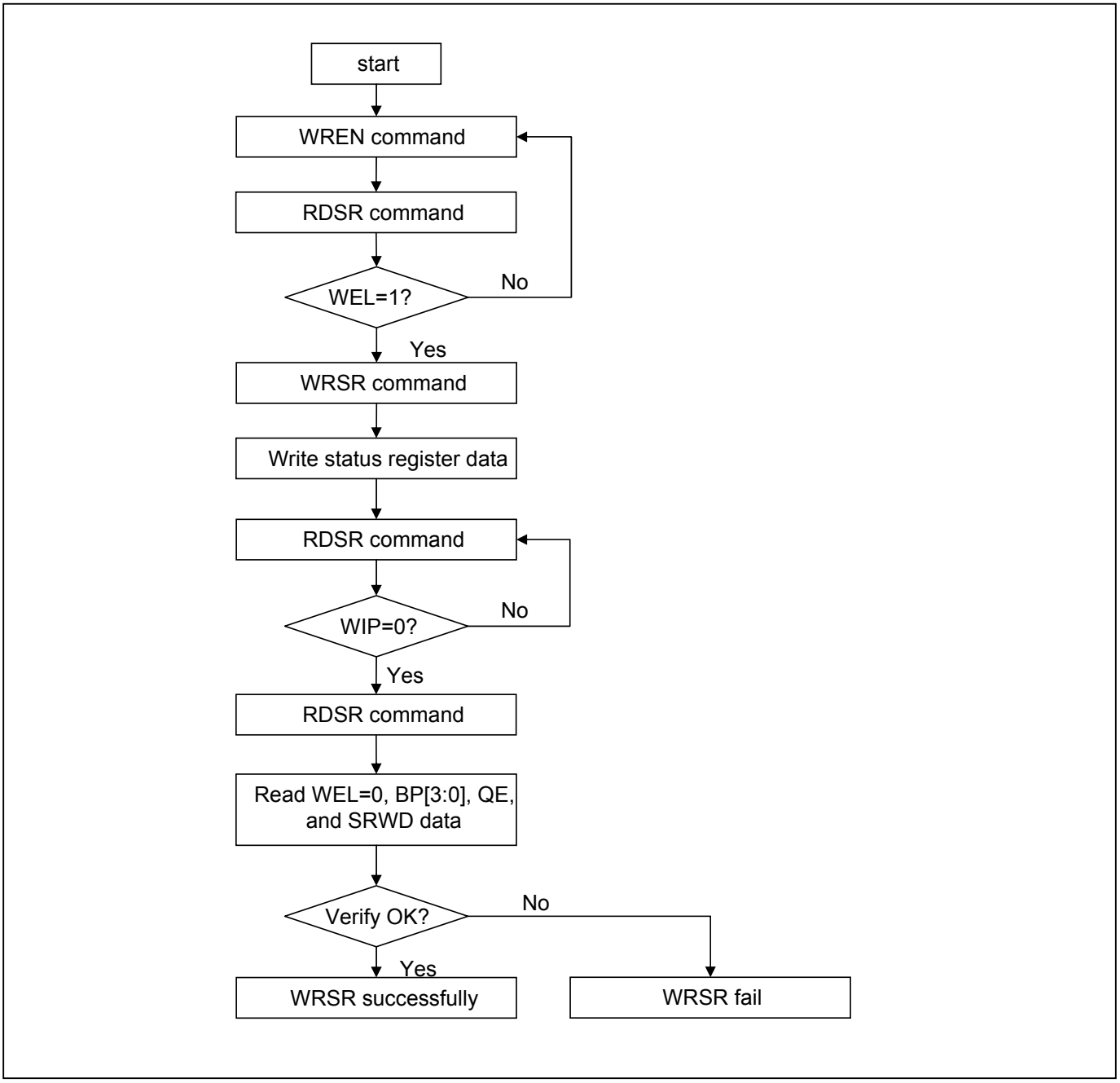


Figure 7. WRSR flow



The definitions of the status register bits are as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 2. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit, non-volatile bit, performs SPI Quad modes when it is reset to "0" (factory default) to enable WP# or is set to "1" to enable Quad SIO2 and SIO3. QE bit is only valid for SPI mode. When operate in SPI mode, and quad IO read is desired (for command EBh/E7h, or quad IO program, 38h). WRSR command has to be set the through Status Register bit 6, the QE bit. Then the SPI Quad I/O commands (EBh/E7h/38h) will be accepted by flash. If QE bit is not set, SPI Quad I/O commands (EBh/E7h/38h) will be invalid commands, the device will not respond to them. Once QE bit is set, all SPI commands are valid. 1I/O commands and 2 I/O commands can be issued no matter QE bit is "0" or "1". When in QPI mode, QE bit will not affect the operation of QPI mode at all. Therefore either "0" or "1" value of QE bit does not affect the QPI mode operation.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Table 6. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: See the *"Table 2. Protected Area Sizes"*.

9-5. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 2. Protected Area Sizes"*). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high. (Please refer to *"Figure 30. Write Status Register (WRSR) Sequence (Command 01) (SPI Mode)"* and *"Figure 31. Write Status Register (WRSR) Sequence (Command 01) (QPI Mode)"*)

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 7. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:
1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *"Table 2. Protected Area Sizes"*.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):
- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Note:
If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):
- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

Note:
To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered.
If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.
If the system enter QPI or set QE=1, the feature of HPM will be disabled.

9-6. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 32. Read Data Bytes (READ) Sequence (Command 03) (SPI Mode only) (33MHz)"*)

9-7. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

Read on SPI Mode The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 33. Read at Higher Speed (FAST_READ) Sequence (Command 0B) (SPI Mode) (104MHz)"*)

Read on QPI Mode The sequence of issuing FAST_READ instruction in QPI mode is: CS# goes low→ sending FAST_READ instruction, 2 cycles→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QPI FAST_READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 34. Read at Higher Speed (FAST_READ) Sequence (Command 0B) (QPI Mode) (84MHz)"*)

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h,5Ah,F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

9-8. 2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4 dummy cycles on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out (Please refer to *"Figure 35. 2 x I/O Read Mode Sequence (Command BB) (SPI Mode only) (84MHz)"*).

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

9-9. 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

4 x I/O Read on SPI Mode (4READ) The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

W4READ instruction (E7) is also available is SPI mode for 4 I/O read. The sequence is similar to 4READ, but with only 4 dummy cycles. The clock rate runs at 84MHz.

4 x I/O Read on QPI Mode (4READ) The 4READ instruction also support on QPI command mode. The sequence of issuing 4READ instruction QPI mode is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out (Please refer to *"Figure 36. 4 x I/O Read Mode Sequence (Command EB) (SPI Mode) (104MHz)"*).

Another sequence of issuing 4 READ instruction especially useful in random access is : CS# goes low→sending 4 READ instruction→3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles →data out still CS# goes high → CS# goes low (reduce 4 Read instruction) →24-bit random access address (Please refer to *"Figure 37. 4 x I/O Read enhance performance Mode Sequence (Command EB) (SPI Mode) (104MHz)"* and *"Figure 38. 4 x I/O Read enhance performance Mode Sequence (Command EB) (QPI Mode) (104MHz)"*).

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

9-10. Burst Read

This device supports Burst Read in both SPI and QPI mode.
To set the Burst length, following command operation is required
Issuing command: “C0h” in the first Byte (8-clocks), following 4 clocks defining wrap around enable with “0h” and disable with“1h”.

Next 4 clocks are to define wrap around depth. Definition as following table:

Table 8. Wrap Around Definition Table

Data	Wrap Around	Wrap Depth	Data	Wrap Around	Wrap Depth
1xh	No	X	00h	Yes	8-byte
1xh	No	X	01h	Yes	16-byte
1xh	No	X	02h	Yes	32-byte
1xh	No	X	03h	Yes	64-byte

The wrap around unit is defined within the 256Byte page, with random initial address. It’s defined as “wrap-around mode disable” for the default state of the device. To exit wrap around, it is required to issue another “C0” command in which data=‘1xh”. Otherwise, wrap around status will be retained until power down or reset command. To change wrap around depth, it is requried to issue another “C0” command in which data=“0xh”. QPI “0Bh” “EBh” and SPI “EBh” “E7h” support wrap around feature after wrap around enable. Burst read is supported in both SPI and QPI mode. (The device ID default without Burst Read)

Figure 8. SPI Mode

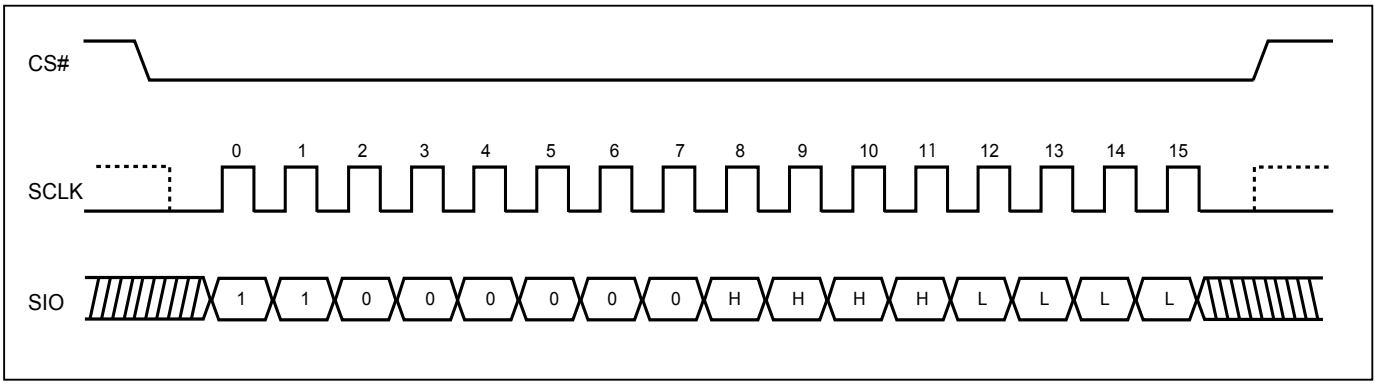
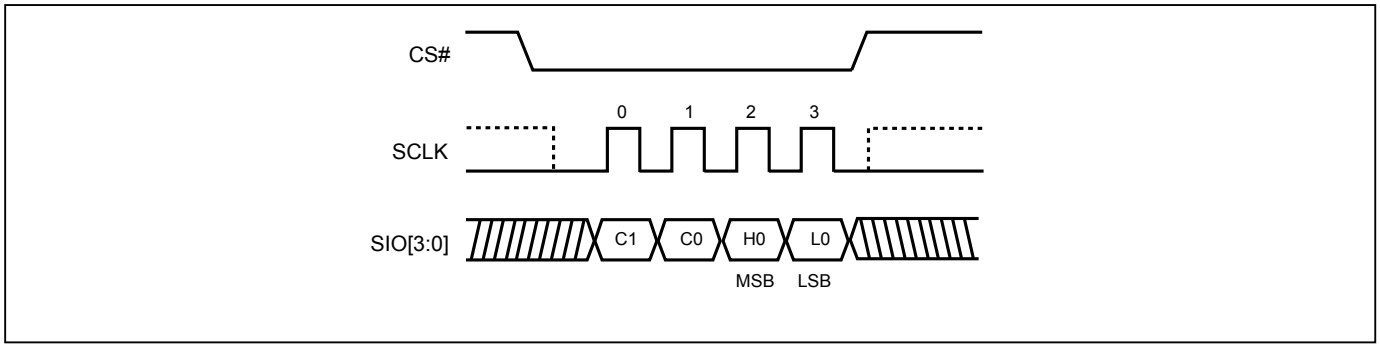


Figure 9. QPI Mode



Note: MSB=Most Significant Bit
LSB=Least Significant Bit

9-11. Performance Enhance Mode

The device could waive the command cycle bits if the two cycle bits after address cycle toggles. (Please refer to *"Figure 37. 4 x I/O Read enhance performance Mode Sequence (Command EB) (SPI Mode) (104MHz)"* and *"Figure 38. 4 x I/O Read enhance performance Mode Sequence (Command EB) (QPI Mode) (104MHz)"*).

Performance enhance mode is supported in both SPI and QPI mode.
In QPI mode, “EBh” “0Bh” and SPI “EBh” “E7h” commands support enhance mode. The performance enhance mode is not supported in dual I/O mode.

After entering enhance mode, following CSB go high, the device will stay in the read mode and treat CSB go low of the first clock as address instead of command cycle.

To exit enhance mode, a new fast read command whose first two dummy cycles is not toggle then exit. Or issue ”FFh” command to exit enhance mode.

9-12. Performance Enhance Mode Reset (FFh)

To conduct the Performance Enhance Mode Reset operation in SPI mode, FFh command code, 8 clocks, should be issued in 1I/O sequence. In QPI Mode, FFFFFFFFh command code, 8 clocks, in 4I/O should be issued. (Please refer to *"Figure 61. Performance Enhance Mode Reset for Fast Read Quad I/O (SPI Mode)", "Figure 62. Performance Enhance Mode Reset for Fast Read Quad I/O (QPI Mode)"*)

If the system controller is being Reset during operation, the flash device will return to the standard SPI operation.

Upon Reset of main chip, SPI instruction would be issued from the system. Instructions like Read ID (9Fh) or Fast Read (0Bh) would be issued.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

9-13. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see *"Table 4. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→ sending SE instruction code→ 3-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode. (Please refer to *"Figure 42. Sector Erase (SE) Sequence (Command 20) (SPI Mode)"*, *"Figure 43. Sector Erase (SE) Sequence (Command 20) (QPI Mode)"*)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the sector is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

9-14. Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (see *"Table 4. Memory Organization"*) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low→ sending BE32K instruction code→ 3-byte address on SI→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode. (Please refer to *"Figure 44. Block Erase 32KB (BE32K) Sequence (Command 52) (SPI Mode)"*and *"Figure 45. Block Erase 32KB (BE32K) Sequence (Command 52) (QPI Mode)"*)

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE32K) instruction will not be executed on the block.

9-15. Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to *"Table 4. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ sending BE instruction code→ 3-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode. (Please refer to *"Figure 46. Block Erase (BE) Sequence (Command D8) (SPI Mode)"* and *"Figure 47. Block Erase (BE) Sequence (Command D8) (QPI Mode)"*)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

9-16. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→sending CE instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode. (Please refer to *"Figure 48. Chip Erase (CE) Sequence (Command 60 or C7) (SPI Mode)", "Figure 49. Chip Erase (CE) Sequence (Command 60 or C7) (QPI Mode)"*)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the chip is protected by BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP2, BP1, BP0 all set to "0".

9-17. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high. (Please refer to *"Figure 39. Page Program (PP) Sequence (Command 02) (SPI Mode)"* and *"Figure 40. Page Program (PP) Sequence (Command 02) (QPI Mode)"*)

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary(the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

9-18. 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application of lower clock less than 33MHz. For system with faster clock, the Quad page program cannot provide more performance, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 33MHz below. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high.

9-19. Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device to minimum power consumption (the current is reduced from standby to deep power-down). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored.

The sequence of issuing DP instruction is: CS# goes low→sending DP instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode. (Please refer to *"Figure 50. Deep Power-down (DP) Sequence (Command B9) (SPI Mode)"* and *"Figure 51. Deep Power-down (DP) Sequence (Command B9) (QPI Mode)"*)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction and softreset command. (those instructions allow the ID being reading out). When Power-down, or software reset command the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For DP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode.

9-20. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in *"Table 15. AC Characteristics"*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 9. ID Definitions"* on next page. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

The sequence is shown as *"Figure 52. RDP and Read Electronic Signature (RES) Sequence (Command AB) (SPI Mode)", "Figure 53. Release from Deep Power-down (RDP) Sequence (Command AB) (SPI Mode)" and "Figure 54. Release from Deep Power-down (RDP) Sequence (Command AB) (QPI Mode)"*. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

SPI (8 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

9-21. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for Macronix (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in *"Figure 55. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90) (SPI Mode only)"*. The Device ID values are listed in *"Table 9. ID Definitions"*. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

9-22. QPI ID Read (QPIID)

User can execute this QPIID Read instruction to identify the Device ID and Manufacturer ID. The sequence of issue QPIID instruction is CS# goes low→sending QPI ID instruction→→Data out on SO→CS# goes high. Most significant bit (MSB) first.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and device ID data byte will be output continuously, until the CS# goes high.

Table 9. ID Definitions

Command Type	MX25U1635E		
RDID (JEDEC ID)	manufacturer ID	memory type	memory density
	C2	25	35
RES	electronic ID		
	35		
REMS	manufacturer ID	device ID	
	C2	35	

9-23. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit secured OTP mode. While the device is in 4K-bit secured OTP mode, main array access is not available. The additional 4K-bit secured OTP is independent from main array, and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

9-24. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

9-25. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→sending RDSCUR instruction→Security Register data out on SO→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode. Please see *"Figure 56. Read Security Register (RDSCUR) Sequence (Command 2B) (SPI Mode)"* & *"Figure 57. Read Security Register (RDSCUR) Sequence (Command 2B) (QPI Mode)"*.

The definition of the Security Register bits is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more.

Table 10. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Reserved	ESB (Erase Suspend bit)	PSB (Program Suspend bit)	LDSO (indicate if lock-down)	Secured OTP indicator bit
0=normal WP mode 1=individual mode (default=0)	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	-	0=Erase is not suspended 1= Erase suspended (default=0)	0=Program is not suspended 1= Program suspended (default=0)	0 = not lock-down 1 = lock-down (cannot program/ erase OTP)	0 = non-factory lock 1 = factory lock
Non-volatile bit (OTP)	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non-volatile bit (OTP)	Non-volatile bit (OTP)

9-26. Write Security Register (WRSCUR)

The WRSCUR instruction is for setting the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more. The LDSO bit is an OTP bit. Once the LDSO bit is set, the value of LDSO bit can not be altered any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode. Please see *"Figure 58. Write Security Register (WRSCUR) Sequence (Command 2F) (SPI Mode)"* & *"Figure 59. Write Security Register (WRSCUR) Sequence (Command 2F) (QPI Mode)"*.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

9-27. Write Protection Selection (WPSEL)

There are two write protection methods, (1) BP protection mode (2) individual block protection mode. If WPSEL=0, flash is under BP protection mode . If WPSEL=1, flash is under individual block protection mode. The default value of WPSEL is "0". WPSEL command can be used to set WPSEL=1. **Please note that WPSEL is an OTP bit. Once WPSEL is set to 1, there is no chance to recovery WPSEL back to "0".** If the flash is put on BP mode, the individual block protection mode is disabled. Contrarily, if flash is on the individual block protection mode, the BP mode is disabled.

Every time after the system is powered-on, the Security Register bit 7 is checked. If WPSEL=1, all the blocks and sectors will be write protected by default. User may only unlock the blocks or sectors via SBULK and GBULK instructions. Program or erase functions can only be operated after the Unlock instruction is executed.

BP protection mode, WPSEL=0:
ARRAY is protected by BP3~BP0 and BP3~BP0 bits are protected by "SRWD=1 and WP#=0", where SRWD is bit 7 of status register that can be set by WRSR command.

Individual block protection mode, WPSEL=1:
Blocks are individually protected by their own SRAM lock bits which are set to "1" after power up. SBULK and SBLK command can set SRAM lock bit to "0" and "1". When the system accepts and executes WPSEL instruction, bit 7 in the security register will be set. It will activate SBLK, SBULK, RDBLOCK, GBLK, GBULK etc instructions to conduct block lock protection and replace the original Software Protect Mode (SPM) use (BP3~BP0) indicated block methods. Under the individual block protection mode (WPSEL=1), hardware protection is performed by driving WP#=0. Once WP#=0 all array blocks/sectors are protected regardless of the contents of SRAM lock bits.

The sequence of issuing WPSEL instruction is: CS# goes low → sending WPSEL instruction to enter the individual block protect mode → CS# goes high.

WPSEL instruction function flow is as follows:

Figure 10. BP and SRWD if WPSEL=0

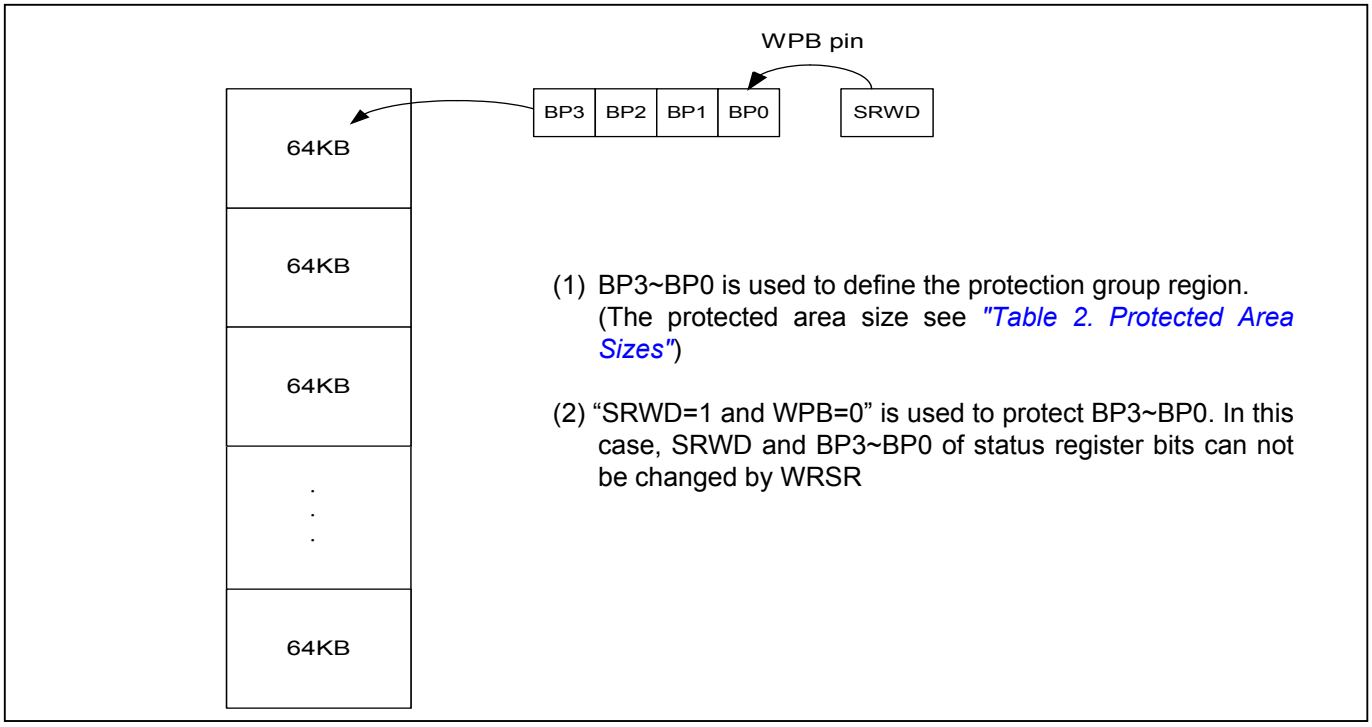
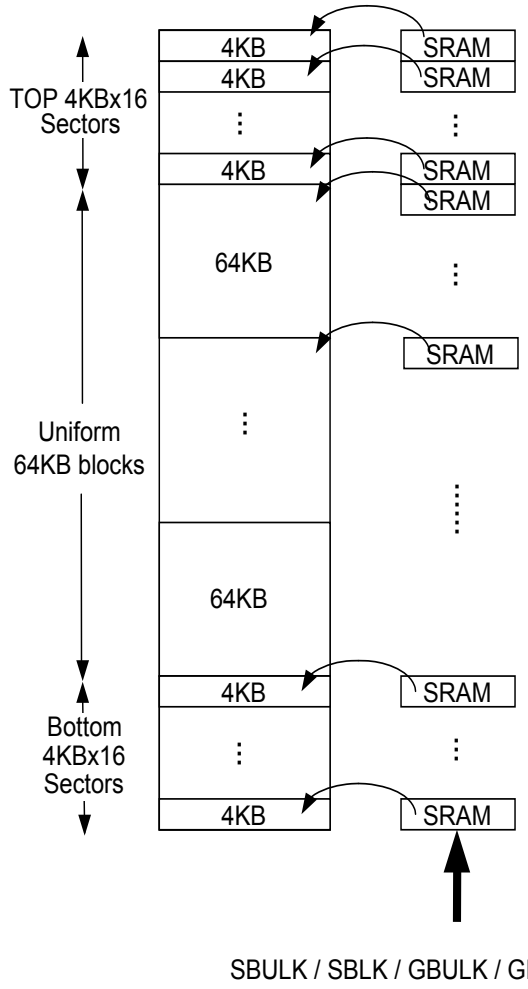
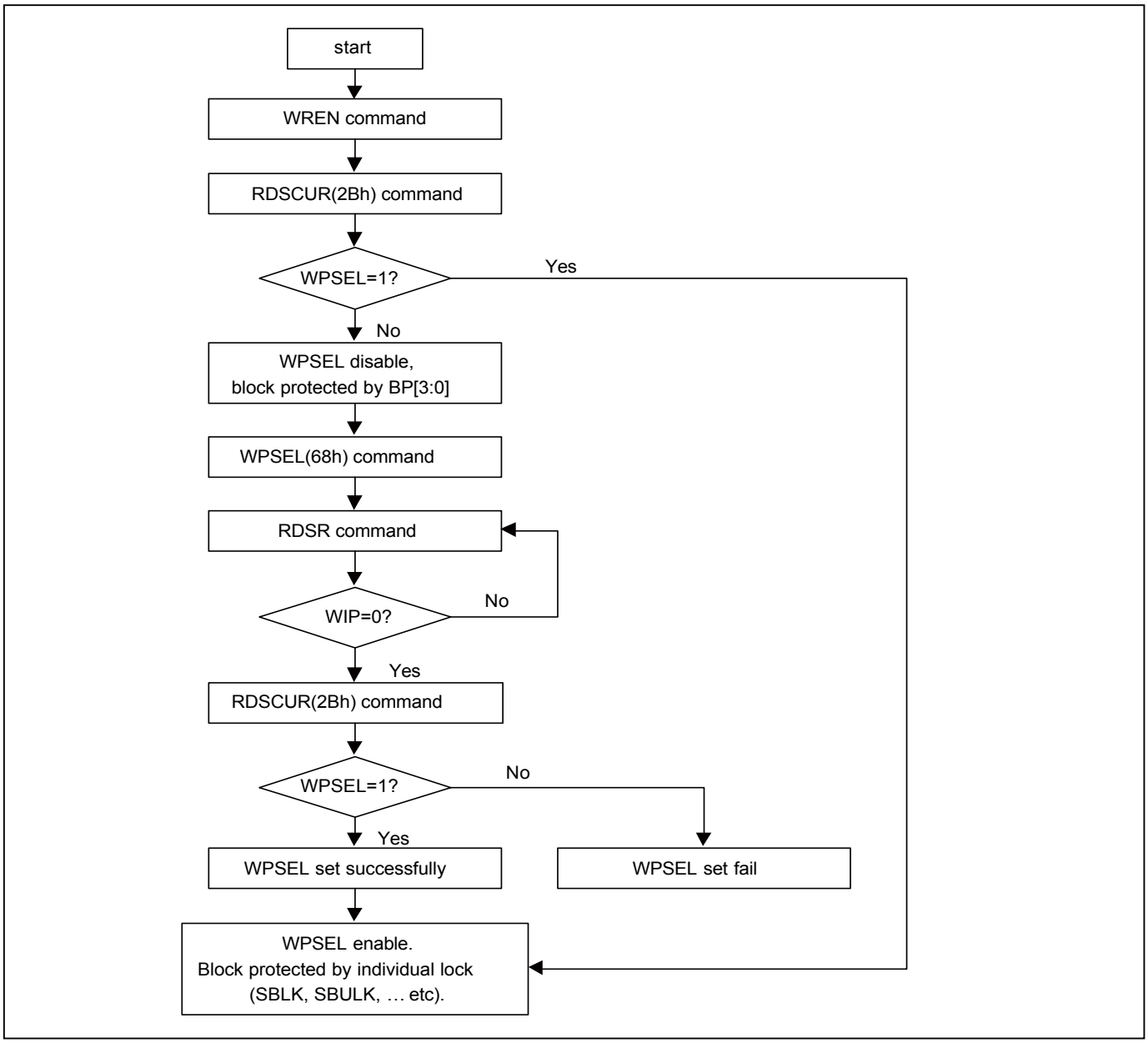


Figure 11. The individual block lock mode is effective after setting WPSEL=1



- Power-Up: All SRAM bits=1 (all blocks are default protected). All array cannot be programmed/erased
- SBLK/SBULK(36h/39h):
  - SBLK(36h): Set SRAM bit=1 (protect) : array can not be programmed/erased
  - SBULK(39h): Set SRAM bit=0 (unprotect): array can be programmed/erased
  - All top 4KBx16 sectors and bottom 4KBx16 sectors and other 64KB uniform blocks can be protected and unprotected SRAM bits individually by SBLK/SBULK command set.
- GBLK/GBULK(7Eh/98h):
  - GBLK(7Eh): Set all SRAM bits=1,whole chip are protected and cannot be programmed/erased.
  - GBULK(98h): Set all SRAM bits=0,whole chip are unprotected and can be programmed/erased.
  - All sectors and blocks SRAM bits of whole chip can be protected and unprotected at one time by GBLK/GBULK command set.
- RDBLOCK(3Ch):
  - use RDBLOCK mode to check the SRAM bits status after SBULK /SBLK/GBULK/GBLK command set.

Figure 12. WPSEL Flow



9-28. Single Block Lock/Unlock Protection (SBLK/SBULK)

These instructions are only effective after WPSEL was executed. The SBLK instruction is for write protection a specified block (or sector) of memory, using A_{MAX}-A16 or (A_{MAX}-A12) address bits to assign a 64Kbyte block (or 4K bytes sector) to be protected as read only. The SBULK instruction will cancel the block (or sector) write protection state. This feature allows user to stop protecting the entire block (or sector) through the chip unprotect command (GBULK).

The WREN (Write Enable) instruction is required before issuing SBLK/SBULK instruction.
The sequence of issuing SBLK/SBULK instruction is: CS# goes low → send SBLK/SBULK (36h/39h) instruction→send 3 address bytes assign one block (or sector) to be protected on SI pin → CS# goes high. The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

SBLK/SBULK instruction function flow is as follows:

Figure 13. Block Lock Flow

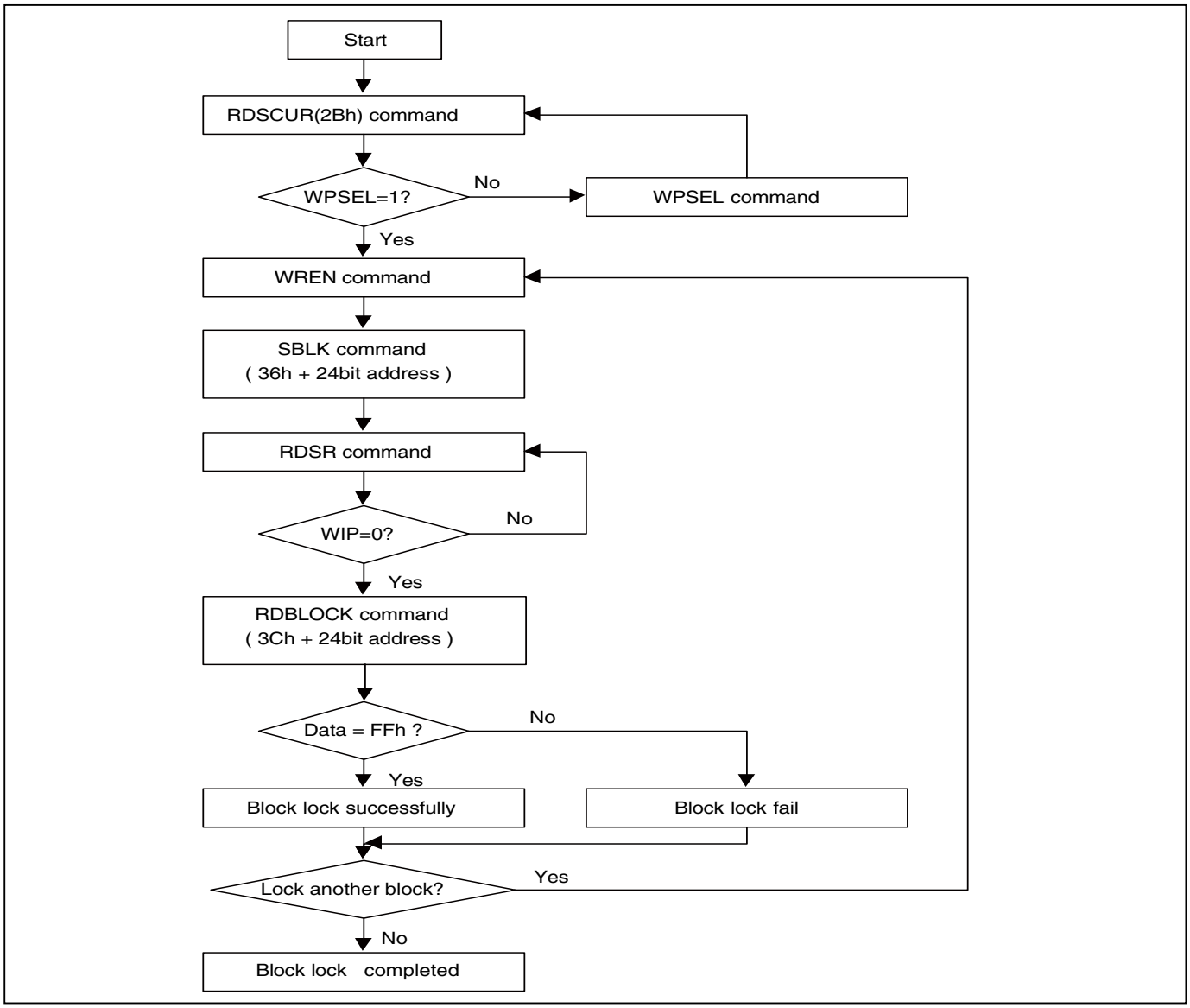
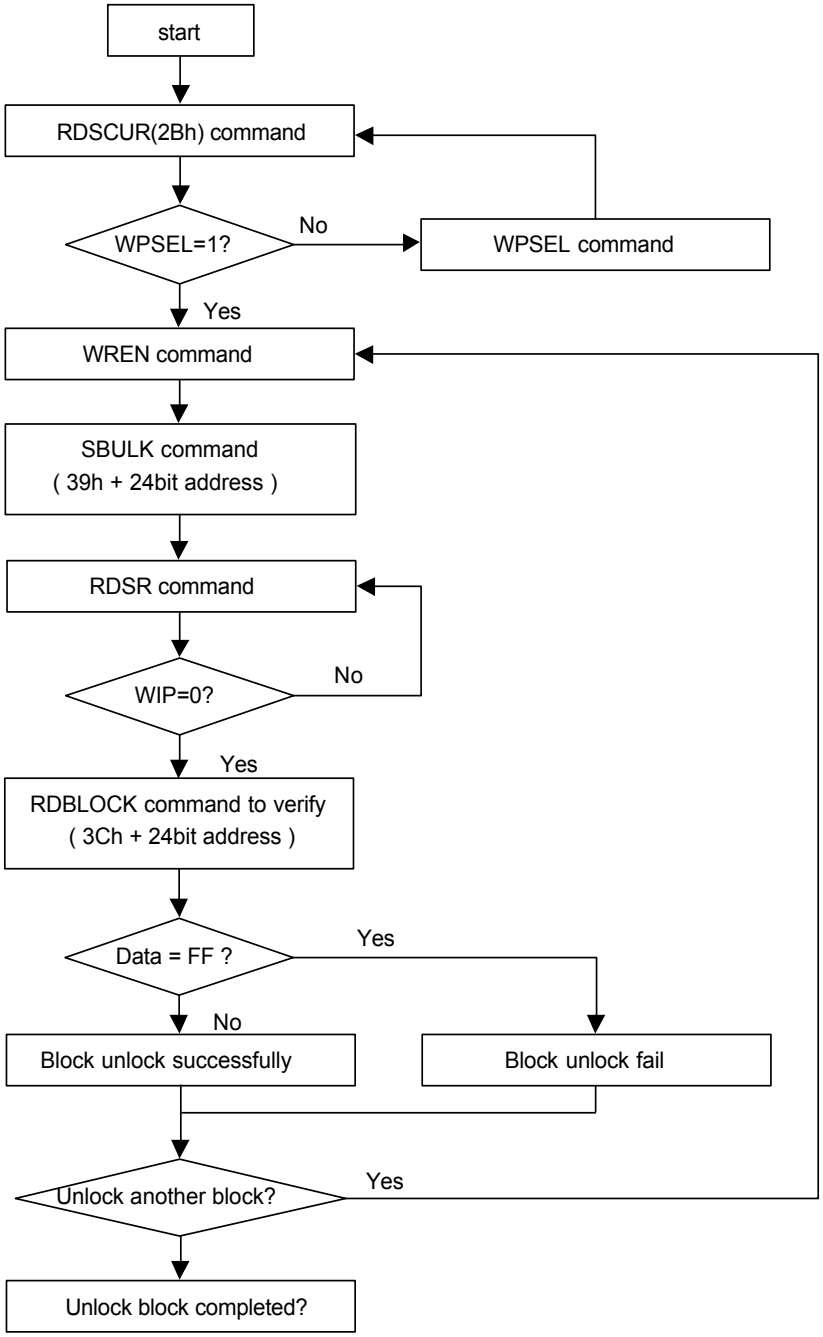


Figure 14. Block Unlock Flow



9-29. Read Block Lock Status (RDBLOCK)

This instruction is only effective after WPSEL was executed. The RDBLOCK instruction is for reading the status of protection lock of a specified block (or sector), using A_{MAX}-A16 (or A_{MAX}-A12) address bits to assign a 64K bytes block (4K bytes sector) and read protection lock status bit which the first byte of Read-out cycle. The status bit is "1" to indicate that this block has be protected, that user can read only but cannot write/program /erase this block. The status bit is "0" to indicate that this block hasn't be protected, and user can read and write this block.

The sequence of issuing RDBLOCK instruction is: CS# goes low → send RDBLOCK (3Ch) instruction → send 3 address bytes to assign one block on SI pin → read block's protection lock status bit on SO pin → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

9-30. Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is for enable/disable the lock protection block of the whole chip.

The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.
The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction →CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

9-31. Program/Erase Suspend/Resume

The device allow the interruption of Sector-Erase, Block-Erase or Page-Program operations and conduct other operations. Details as follows.

To enter the suspend/resume mode: issuing B0h for suspend; 30h for resume (SPI/QPI all acceptable)
Read security register bit2 (PSB) and bit3 (ESB) (please refer to *"Table 10. Security Register Definition"*) to check suspend ready information.

For "Suspend to Read", "Resume to Read", "Resume to Suspend" timing specification please note *"Figure 66. Suspend to Read Latency"*, *"Figure 67. Resume to Read Latency"* and *"Figure 68. Resume to Suspend Latency"*.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

9-32. Erase Suspend

Erase suspend allow the interruption of all erase operations.

After erase suspend, WEL bit will be clear, only read related, resume and reset command can be accepted unconditionally. (including: 03h, 0Bh, BBh, EBh, E7h, 9Fh, AFh, 90h, 05h, 2Bh, B1h, C1h, 5Ah, 3Ch, 30h, 66h, 99h, C0h, 35h, F5h, 00h, ABh)

For erase suspend to program operation, the programming command (38, 02) can be accepted under conditions as follows:
The bank is divided into 16 banks in this device, each bank's density is 4Mb. While conducting erase suspend in one bank, the programming operation that follows can only be conducted in one of the other banks and cannot be conducted in the bank executing the suspend operation. The boundaries of the banks are illustrated as below table.

MX25U1635E	
BANK (4M bit)	**Address Range**
3	180000h-1FFFFFh
2	100000h-17FFFFh
1	080000h-0FFFFFh
0	000000h-07FFFFh

After erase suspend command has been issued, latency time 18us is needed before issue another command. For "Suspend to Read", "Resume to Read", "Resume to Suspend" timing specification please note *"Figure 66. Suspend to Read Latency", "Figure 67. Resume to Read Latency"* and *"Figure 68. Resume to Suspend Latency"*.

Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

When ESB bit is issued, the Write Enable Latch (WEL) bit will be reset.
See *"Figure 66. Suspend to Read Latency"* for Suspend to Read latency.

9-33. Program Suspend

Program suspend allows the interruption of all program operations.

After program suspend, WEL bit will be cleared, only read related, resume and reset command can be accepted. (including: 03h, 0Bh, BBh, EBh, E7h, 9Fh, AFh, 90h, 05h, 2Bh, B1h, C1h, 5Ah, 3Ch, 30h, 66h, 99h, C0h, 35h, F5h, 00h, ABh)

After program suspend command has been issued, latency time 18us is needed before issue another command.
For "Suspend to Read", "Resume to Read", "Resume to Suspend" timing specification please note *"Figure 66. Suspend to Read Latency", "Figure 67. Resume to Read Latency"* and *"Figure 68. Resume to Suspend Latency"*.

Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

9-34. Write-Resume

The Write operation is being resumed when Write-Resume instruction issued. ESB or PSB (suspend status bit) in Status register will be changed back to “0”

The operation of Write-Resume is as follows: CS# drives low → send write resume command cycle (30H) → drive CS# high. By polling Busy Bit in status register, the internal write operation status could be checked to be completed or not. The user may also wait the time lag of TSE, TBE, TPP for Sector-erase, Block-erase or Page-programming. WREN (command "06" is not required to issue before resume. Resume to another suspend operation requires latency time. Please refer to *"Figure 68. Resume to Suspend Latency".*

Please note that, if "performance enhance mode" is executed during suspend operation, the device can not be resume. To restart the write command, disable the "performance enhance mode" is required. After the "performance enhance mode" is disable, the write-resume command is effective.

9-35. No Operation (NOP)

The "No Operation" command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

9-36. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode. Please refer to *"Figure 63. Reset Sequence (SPI mode)"* and *"Figure 64. Reset Sequence (QPI mode)".*

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. Longer latency time is required to recover from a program operation than from other operations.

9-37. Reset Quad I/O (RSTQIO)

To reset the QPI mode, the RSTQIO (F5H) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

Note:
For EQIO and RSTQIO commands, CS# high width has to follow "write spec" tSHSL for next instruction.

9-38. Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216.

Figure 15. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence

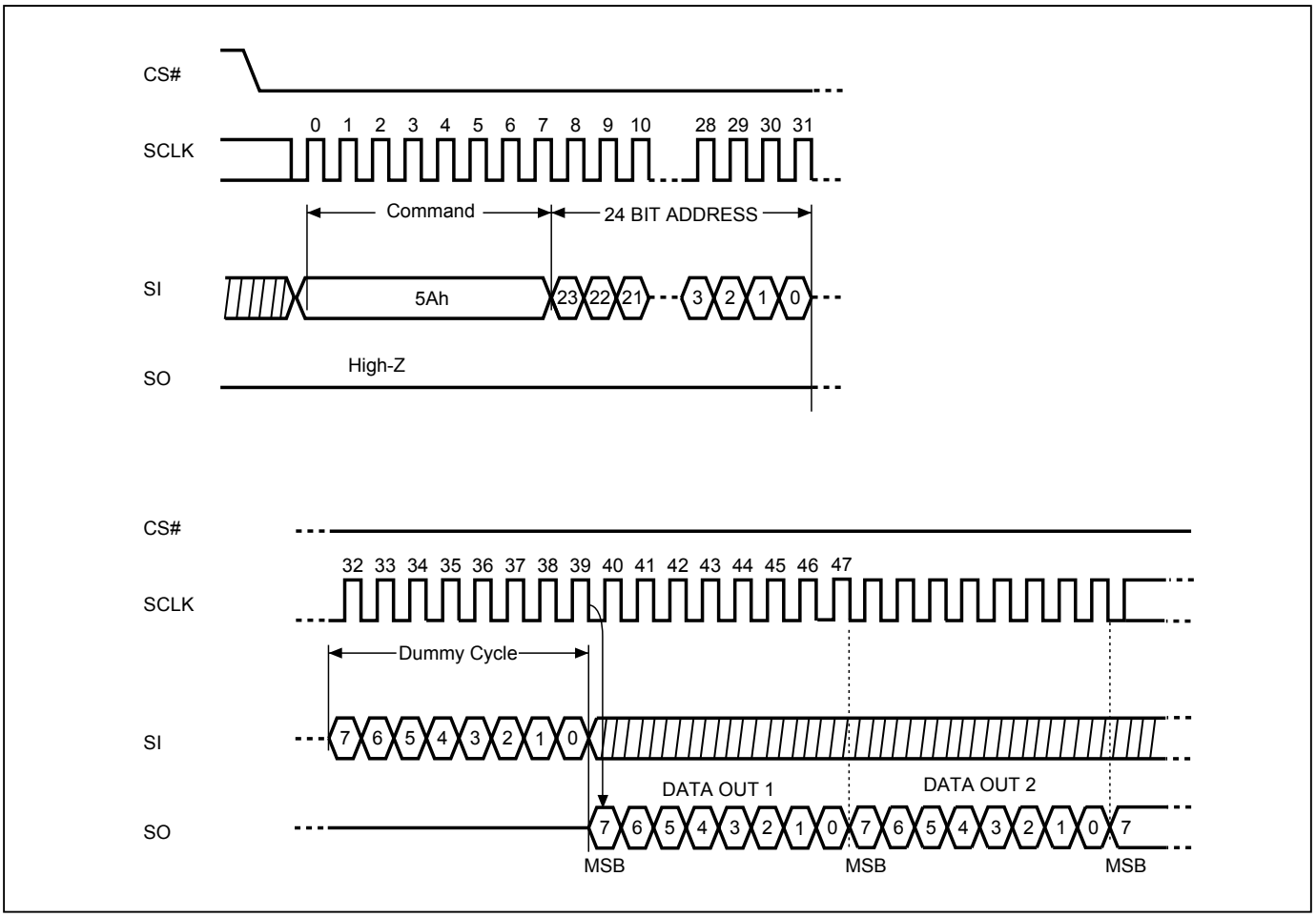


Table 11. Signature and Parameter Identification Data Values

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
SFDP Signature	Fixed: 50444653h	00h	07:00	53h	53h
		01h	15:08	46h	46h
		02h	23:16	44h	44h
		03h	31:24	50h	50h
SFDP Minor Revision Number	Start from 00h	04h	07:00	00h	00h
SFDP Major Revision Number	Start from 01h	05h	15:08	01h	01h
Number of Parameter Headers	This number is 0-based. Therefore, 0 indicates 1 parameter header.	06h	23:16	01h	01h
Unused		07h	31:24	FFh	FFh
ID number (JEDEC)	00h: it indicates a JEDEC specified header.	08h	07:00	00h	00h
Parameter Table Minor Revision Number	Start from 00h	09h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	0Ah	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0Bh	31:24	09h	09h
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0Ch	07:00	30h	30h
		0Dh	15:08	00h	00h
		0Eh	23:16	00h	00h
Unused		0Fh	31:24	FFh	FFh
ID number (Macronix manufacturer ID)	it indicates Macronix manufacturer ID	10h	07:00	C2h	C2h
Parameter Table Minor Revision Number	Start from 00h	11h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	12h	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13h	31:24	04h	04h
Parameter Table Pointer (PTP)	First address of Macronix Flash Parameter table	14h	07:00	60h	60h
		15h	15:08	00h	00h
		16h	23:16	00h	00h
Unused		17h	31:24	FFh	FFh

Table 12. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Block/Sector Erase sizes	00: Reserved, 01: 4KB erase, 10: Reserved, 11: not support 4KB erase	30h	01:00	01b	E5h
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Required for Writing to Volatile Status Registers	0: not required 1: required 00h to be written to the status register		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: use 50h opcode, 1: use 06h opcode Note: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31h	15:08	20h	20h
(1-1-2) Fast Read (Note2)	0=not support 1=support	32h	16	0b	B0h
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) Clocking	0=not support 1=support		19	0b	
(1-2-2) Fast Read	0=not support 1=support		20	1b	
(1-4-4) Fast Read	0=not support 1=support		21	1b	
(1-1-4) Fast Read	0=not support 1=support		22	0b	
Unused			23	1b	
Unused		33h	31:24	FFh	FFh
Flash Memory Density		37h:34h	31:00	00FF FFFFh	
(1-4-4) Fast Read Number of Wait states (Note3)	0 0000b: Wait states (Dummy Clocks) not support	38h	04:00	0 0100b	44h
(1-4-4) Fast Read Number of Mode Bits (Note4)	000b: Mode Bits not support		07:05	010b	
(1-4-4) Fast Read Opcode		39h	15:08	EBh	EBh
(1-1-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Ah	20:16	0 0000b	00h
(1-1-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3Bh	31:24	FFh	FFh

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Ch	04:00	0 0000b	00h
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcode		3Dh	15:08	FFh	FFh
(1-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Eh	20:16	0 0100b	04h
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(1-2-2) Fast Read Opcode		3Fh	31:24	BBh	BBh
(2-2-2) Fast Read	0=not support 1=support	40h	00	0b	FEh
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	1b	
Unused			07:05	111b	
Unused		43h:41h	31:08	FFh	FFh
Unused		45h:44h	15:00	FFh	FFh
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46h	20:16	0 0000b	00h
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47h	31:24	FFh	FFh
Unused		49h:48h	15:00	FFh	FFh
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4Ah	20:16	0 0100b	44h
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	010b	
(4-4-4) Fast Read Opcode		4Bh	31:24	EBh	EBh
Sector Type 1 Size	Sector/block size = 2^N bytes (Note5) 0x00b: this sector type doesn't exist	4Ch	07:00	0Ch	0Ch
Sector Type 1 erase Opcode		4Dh	15:08	20h	20h
Sector Type 2 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	4Eh	23:16	0Fh	0Fh
Sector Type 2 erase Opcode		4Fh	31:24	52h	52h
Sector Type 3 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	50h	07:00	10h	10h
Sector Type 3 erase Opcode		51h	15:08	D8h	D8h
Sector Type 4 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	52h	23:16	00h	00h
Sector Type 4 erase Opcode		53h	31:24	FFh	FFh

Table 13. Parameter Table (1): Macronix Flash Parameter Tables

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Vcc Supply Maximum Voltage	2000h=2.000V 2700h=2.700V 3600h=3.600V	61h:60h	07:00 15:08	00h 20h	00h 20h
Vcc Supply Minimum Voltage	1650h=1.650V 2250h=2.250V 2350h=2.350V 2700h=2.700V	63h:62h	23:16 31:24	50h 16h	50h 16h
H/W Reset# pin	0=not support 1=support	65h:64h	00	0b	F99Ch
H/W Hold# pin	0=not support 1=support		01	0b	
Deep Power Down Mode	0=not support 1=support		02	1b	
S/W Reset	0=not support 1=support		03	1b	
S/W Reset Opcode	Reset Enable (66h) should be issued before Reset Opcode		11:04	1001 1001b (99h)	
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	1b	
Wrap-Around Read mode Opcode		66h	23:16	C0h	C0h
Wrap-Around Read data length	08h:support 8B wrap-around read 16h:8B&16B 32h:8B&16B&32B 64h:8B&16B&32B&64B	67h	31:24	64h	64h
Individual block lock	0=not support 1=support	6Bh:68h	00	1b	C8D9h
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	0011 0110b (36h)	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	0b	
Unused			15:14	11b	
Unused			31:16	FFh	FFh
Unused		6Fh:6Ch	31:00	FFh	FFh

Note 1: h/b is hexadecimal or binary.

Note 2: **(x-y-z)** means I/O mode nomenclature used to indicate the number of active pins used for the opcode (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4)

Note 3: **Wait States** is required dummy clock cycles after the address bits or optional mode bits.

Note 4: **Mode Bits** is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg,read performance enhance toggling bits)

Note 5: 4KB=2^0Ch,32KB=2^0Fh,64KB=2^10h

Note 6: All unused and undefined area data is blank FFh.

10. POWER-ON STATE

The device is at the following states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage until the VCC reaches the following levels:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, after VCC reaching the VWI level, a tPUW time delay is required before the device is fully accessible for commands like write enable (WREN), page program (PP), quad page program (4PP), sector erase (SE), block erase 32KB (BE32K), block erase (BE), chip erase (CE), WRSCUR and write status register (WRSR). If the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- tPUW after VCC reached VWI level
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL, even time of tPUW has not passed.
Please refer to the figure of *"Figure 70. Power-up Timing"*.

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during this stage if a write, program, erase cycle is in progress.

11. ELECTRICAL SPECIFICATIONS

11-1. Absolute Maximum Ratings

Rating		Value
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to +2.5V

NOTICE:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

Figure 16. Maximum Negative Overshoot Waveform

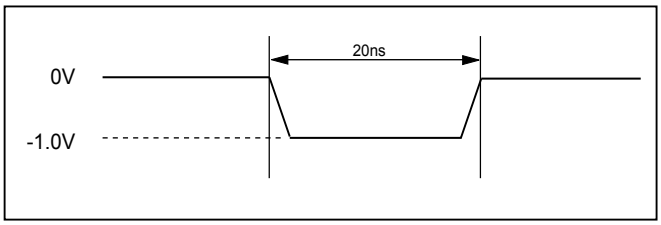
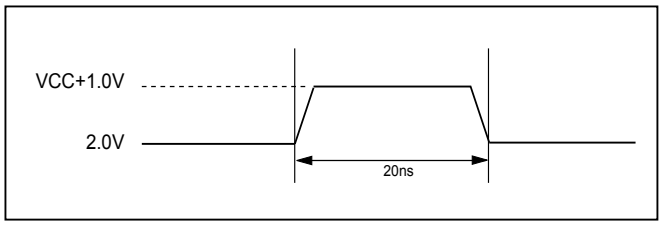


Figure 17. Maximum Positive Overshoot Waveform

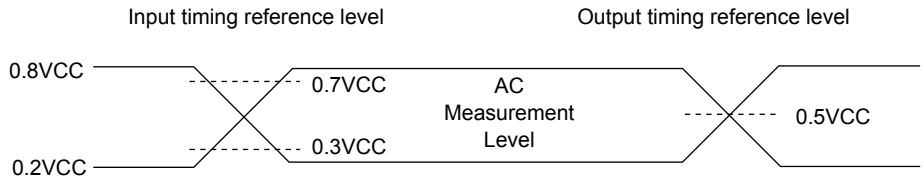


11-2. Capacitance

TA = 25°C, f = 1.0 MHz

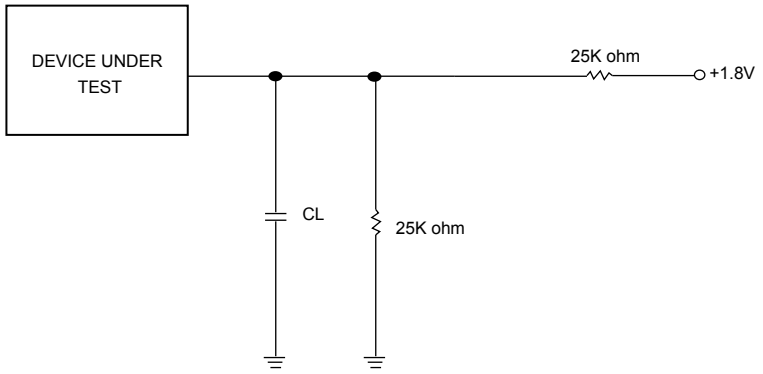
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			10	pF	VIN = 0V
COUT	Output Capacitance			25	pF	VOUT = 0V

Figure 18. Input Test Waveforms and Measurement Level



Note: Input pulse rise and fall time are <5ns

Figure 19. Output Loading



CL=30pF Including jig capacitance

Table 14. DC Characteristics

Temperature = -40°C to 85°C, VCC = 1.65V ~ 2.0V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			±2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			±2	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		25	80	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			2	15	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1			20	mA	f=104MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
					15	mA	f=84MHz, SCLK=0.1VCC/0.9VCC, SO=Open
				7	10	mA	f=33MHz, SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		20	25	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			10	15	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector/Block (32K, 64K) Erase Current (SE/BE/BE32K)	1		20	25	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		20	25	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5		0.2VCC	V	
VIH	Input High Voltage		0.8VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL = 100uA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :
1. Typical values at VCC = 1.8V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 15. AC Characteristics

Temperature = -40°C to 85°C, VCC = 1.65V ~ 2.0V

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, RDSFDP, PP, 4PP, SE, BE, CE, DP, RES, RDP, WREN, WRDI, RDID, RDSR, WRSR		D.C.		104	MHz
fRSCLK	fR	Clock Frequency for READ instructions				33	MHz
fTSCLK	fT	Clock Frequency for 2READ instructions				84	MHz
	fQ	Clock Frequency for 4READ instructions (5)				84/104	MHz
tCH(1)(2)	tCLH	Clock High Time	Others (fSCLK)	4.5			ns
			Normal Read (fRSCLK)	13			ns
tCL(1)(2)	tCLL	Clock Low Time	Others (fSCLK)	4.5			ns
			Normal Read (fRSCLK)	13			ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)		0.1			V/ns
tCHCL(2)		Clock Fall Time (3) (peak to peak)		0.1			V/ns
tSLCH(2)	tCSS	CS# Active Setup Time (relative to SCLK)		4			ns
tCHSL(2)		CS# Not Active Hold Time (relative to SCLK)		4			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX(2)	tDH	Data In Hold Time		3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)		5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		7			ns
tSHSL(3)	tCSH	CS# Deselect Time	Read	12			ns
			Write/Erase/Program	30			ns
tSHQZ(2)	tDIS	Output Disable Time				8	ns
tCLQV	tV	Clock Low to Output Valid Loading: 30pF/15pF	Loading: 30pF			8	ns
			Loading: 15pF			6	ns
tCLQX	tHO	Output Hold Time		1			ns
tWHSL		Write Protect Setup Time		20			ns
tSHWL		Write Protect Hold Time		100			ns
tDP(2)		CS# High to Deep Power-down Mode				10	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read				10	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read				10	us
tRCR		Recovery Time from Read				20	us
tRCP		Recovery Time from Program				20	us
tRCE		Recovery Time from Erase				12	ms
tW		Write Status Register Cycle Time				40	ms
tBP		Byte-Program			10	30	us
tPP		Page Program Cycle Time			1.2	3	ms
tSE		Sector Erase Cycle Time			45	200	ms
tBE32		Block Erase (32KB) Cycle Time			250	1000	ms
tBE		Block Erase (64KB) Cycle Time			500	2000	ms
tCE		Chip Erase Cycle Time			9	20	s

Notes:
1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. Test condition is shown as *"Figure 18. Input Test Waveforms and Measurement Level"* and *"Figure 19. Output Loading"*
5. When dummy cycle=4 (In both QPI & SPI mode), clock rate=84MHz; when dummy cycle=6 (In both QPI & SPI mode), clock rate=104MHz.

12. Timing Analysis

Figure 20. Serial Input Timing

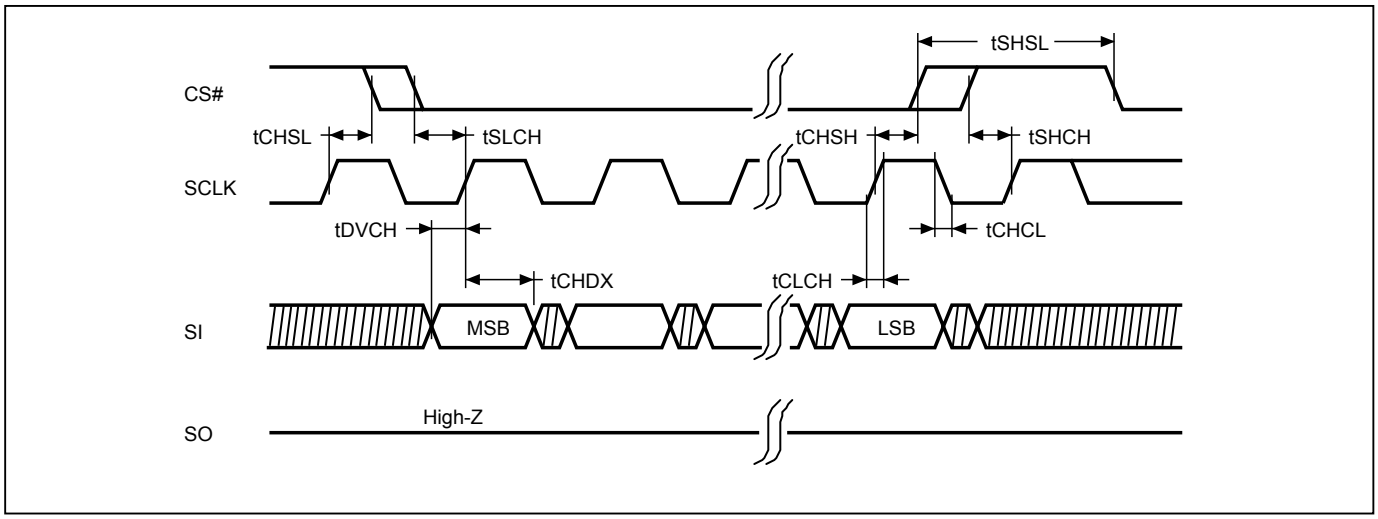


Figure 21. Output Timing

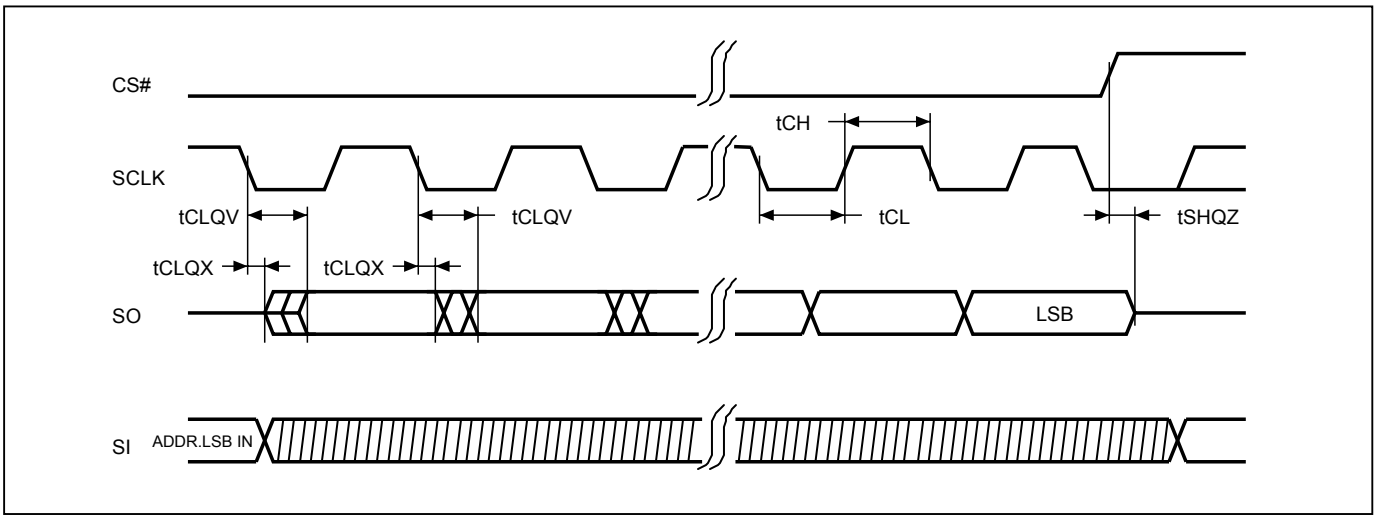


Figure 22. WP# Setup Timing and Hold Timing during WRSR when SRWD=1

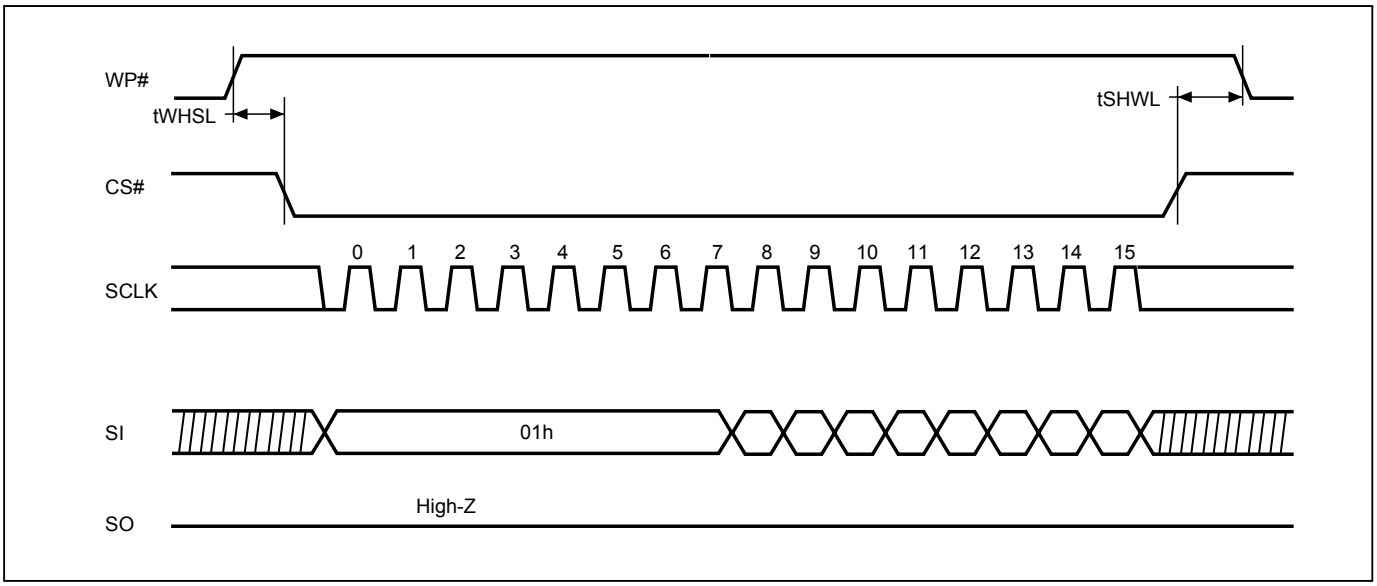


Figure 23. Write Enable (WREN) Sequence (Command 06) (SPI Mode)

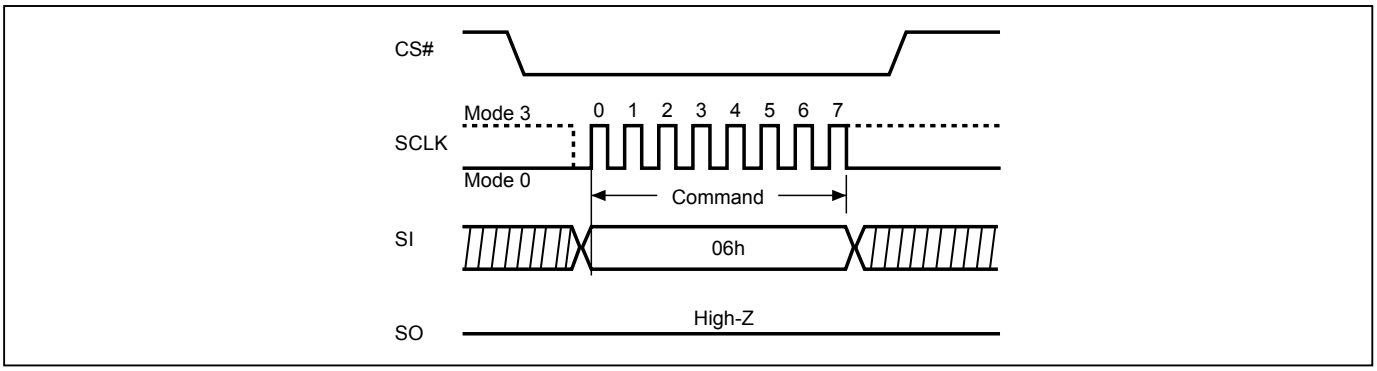


Figure 24. Write Enable (WREN) Sequence (Command 06) (QPI Mode)

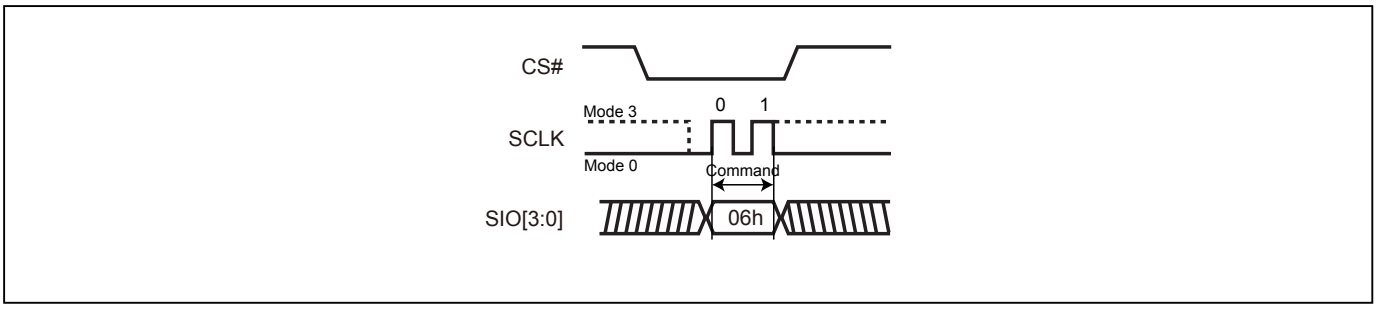


Figure 25. Write Disable (WRDI) Sequence (Command 04) (SPI Mode)

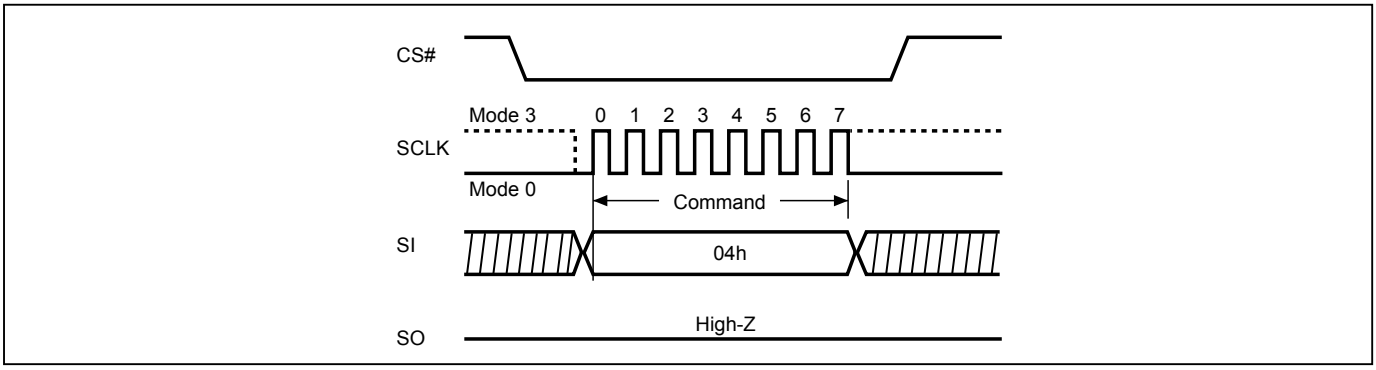


Figure 26. Write Disable (WRDI) Sequence (Command 04) (QPI Mode)

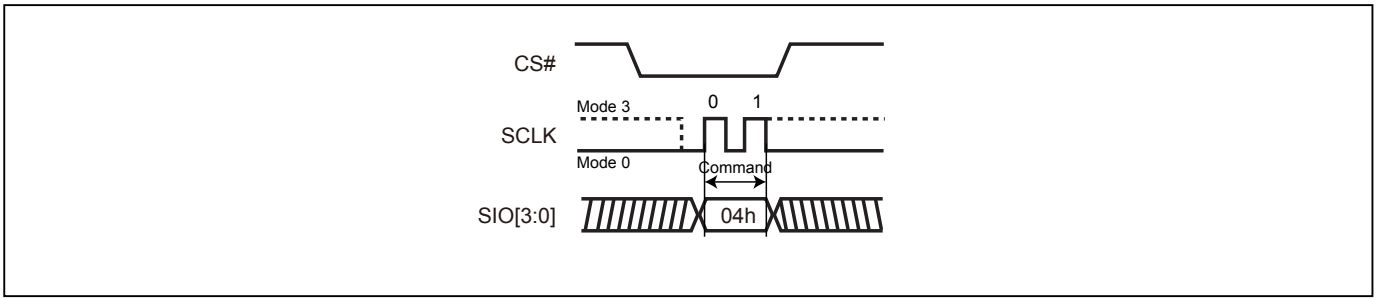


Figure 27. Read Identification (RDID) Sequence (Command 9F) (SPI mode only)

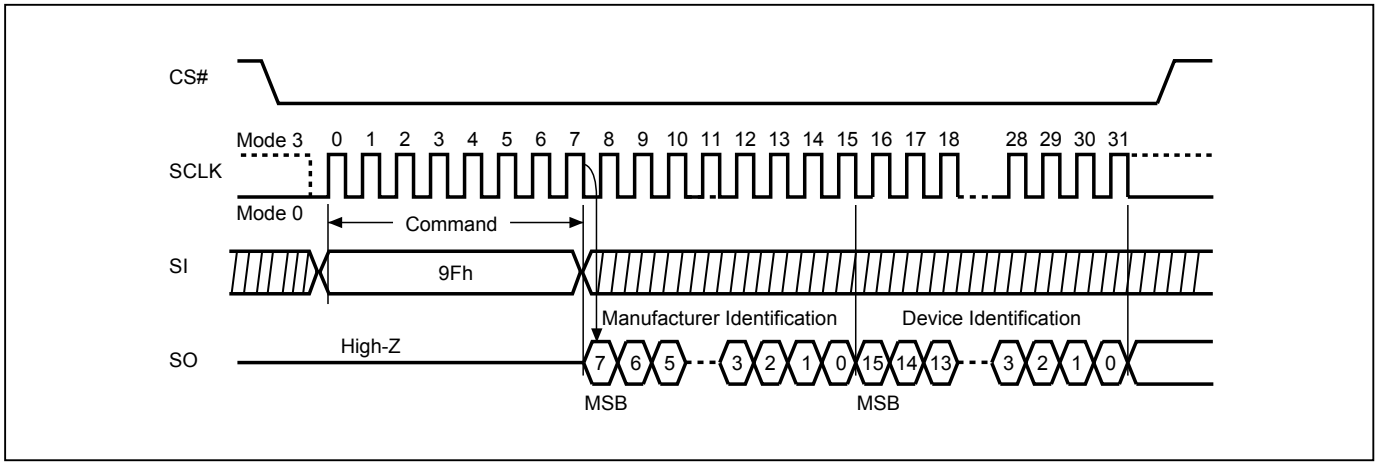


Figure 28. Read Status Register (RDSR) Sequence (Command 05) (SPI Mode)

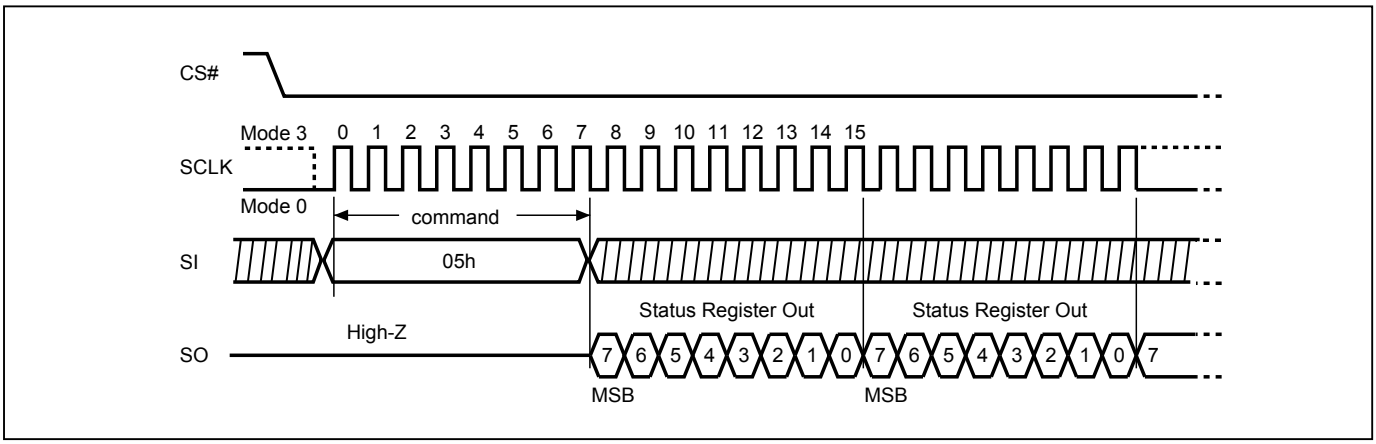


Figure 29. Read Status Register (RDSR) Sequence (Command 05) (QPI Mode)

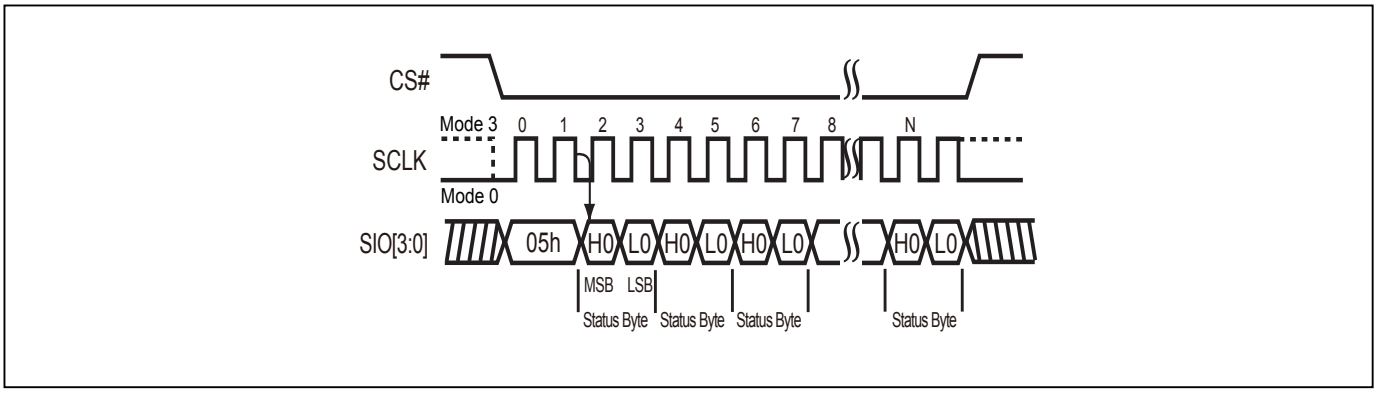
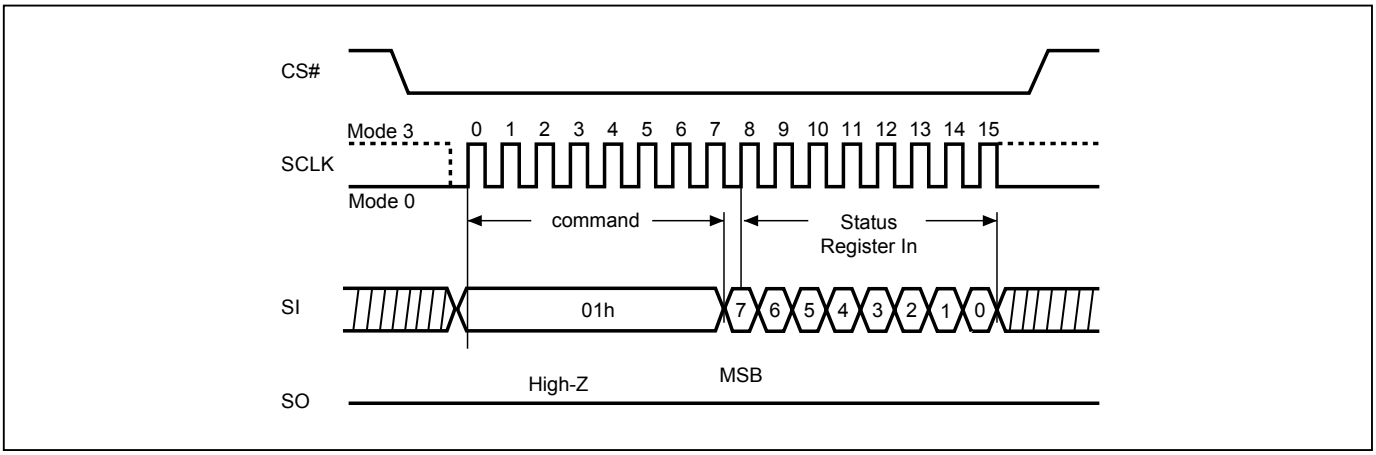


Figure 30. Write Status Register (WRSR) Sequence (Command 01) (SPI Mode)



Note : Also supported in QPI mode with command and subsequent input/output in Quad I/O mode.

Figure 31. Write Status Register (WRSR) Sequence (Command 01) (QPI Mode)

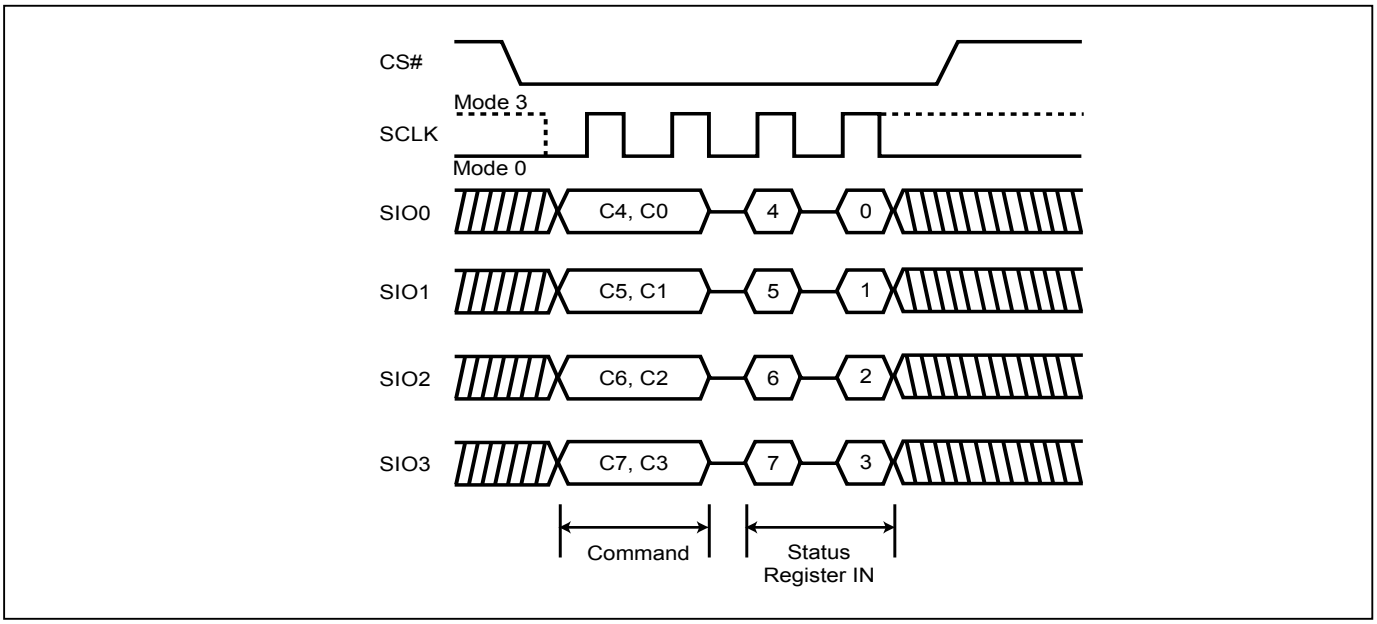


Figure 32. Read Data Bytes (READ) Sequence (Command 03) (SPI Mode only) (33MHz)

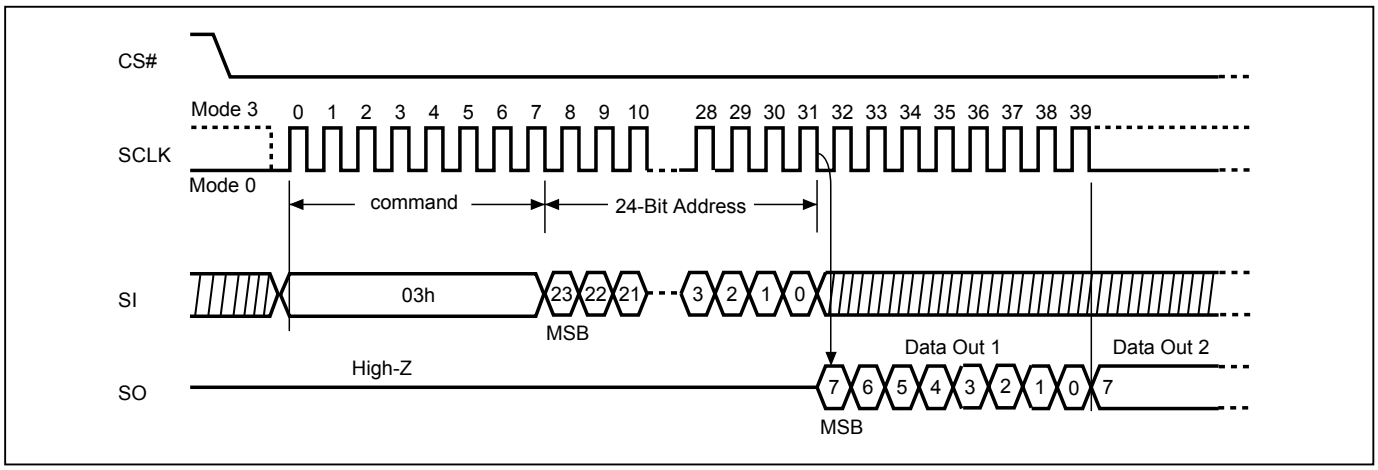


Figure 33. Read at Higher Speed (FAST_READ) Sequence (Command 0B) (SPI Mode) (104MHz)

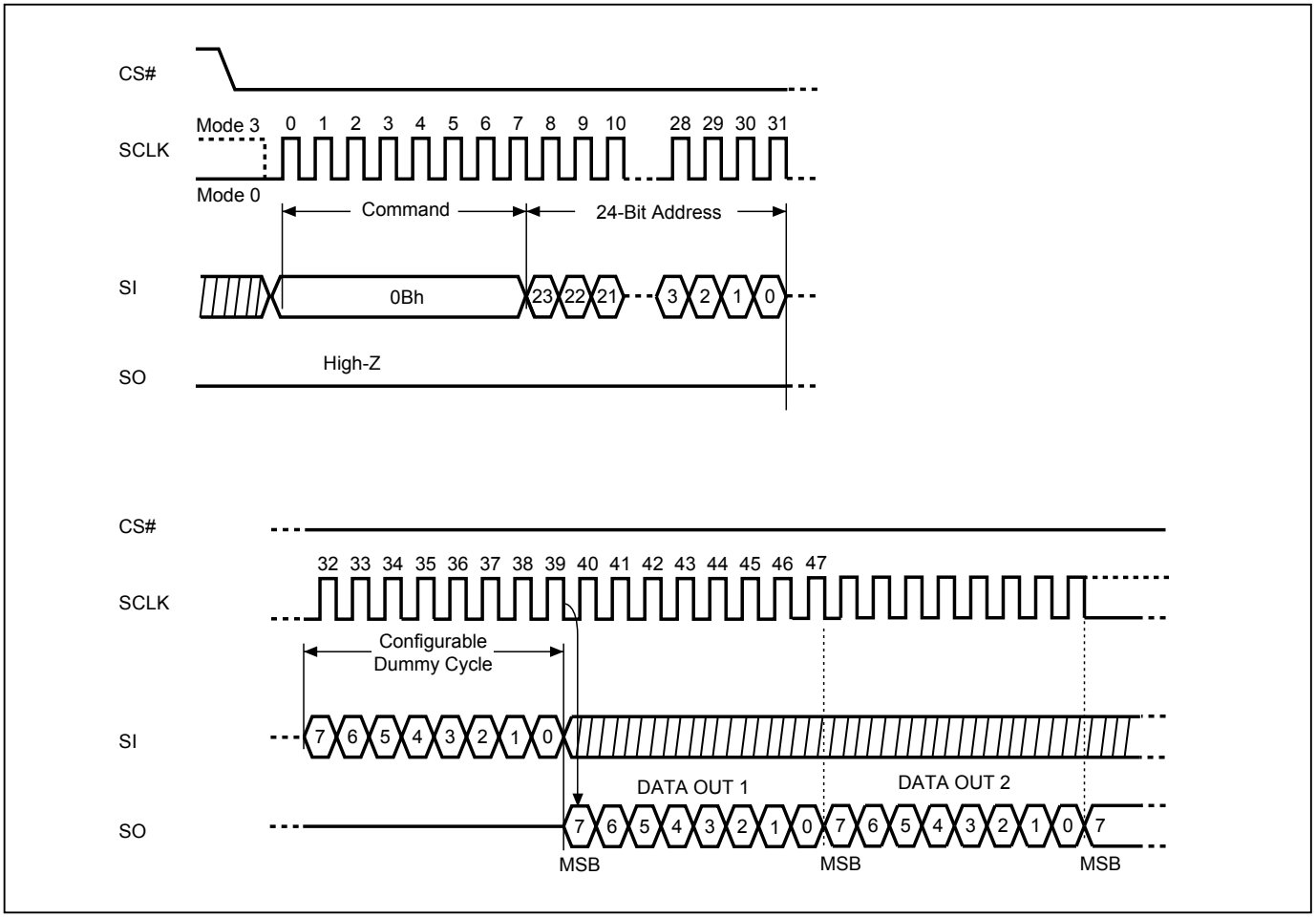


Figure 34. Read at Higher Speed (FAST_READ) Sequence (Command 0B) (QPI Mode) (84MHz)

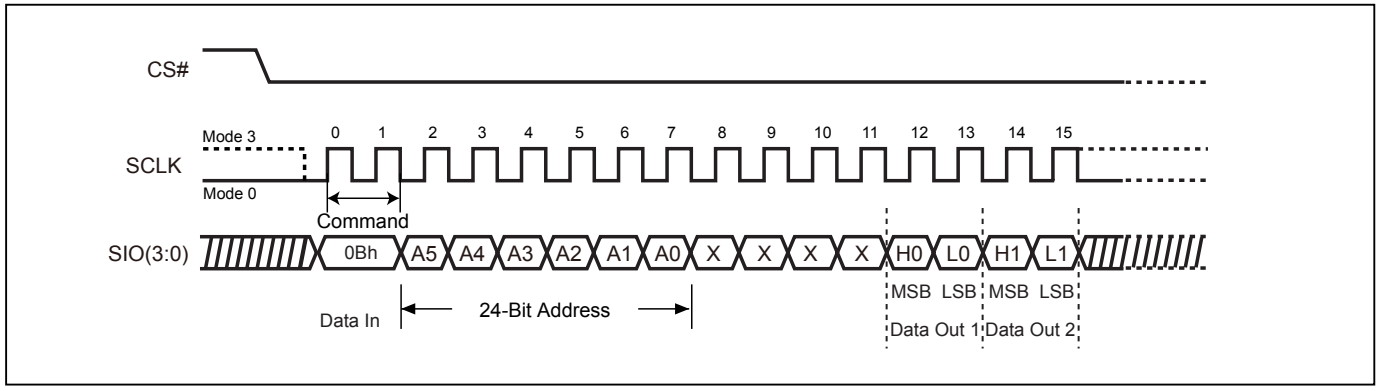


Figure 35. 2 x I/O Read Mode Sequence (Command BB) (SPI Mode only) (84MHz)

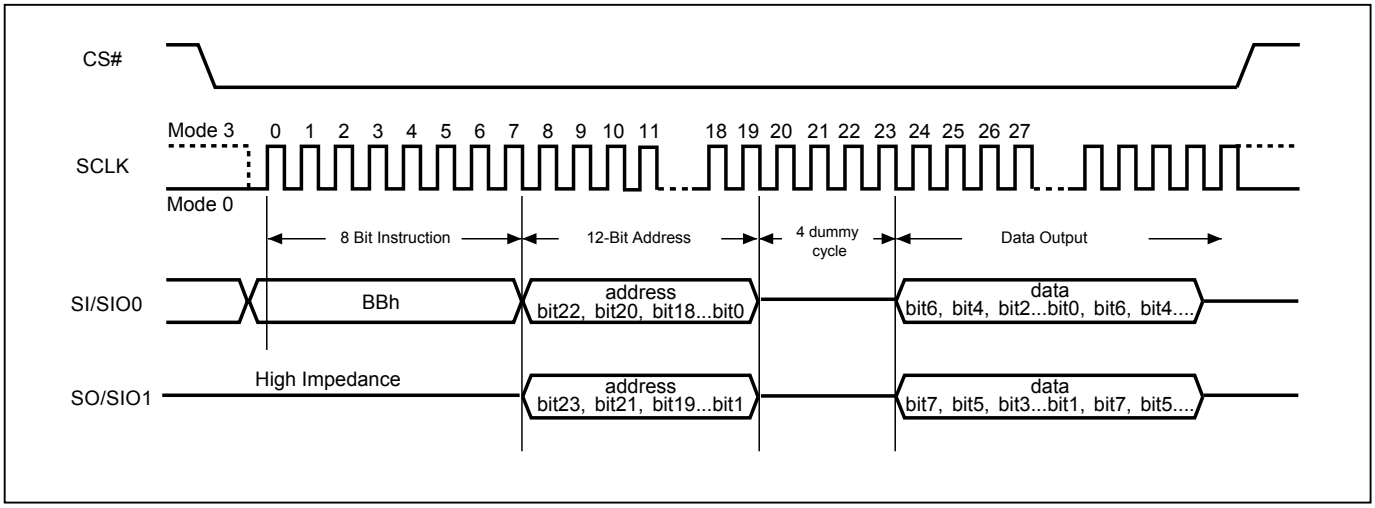
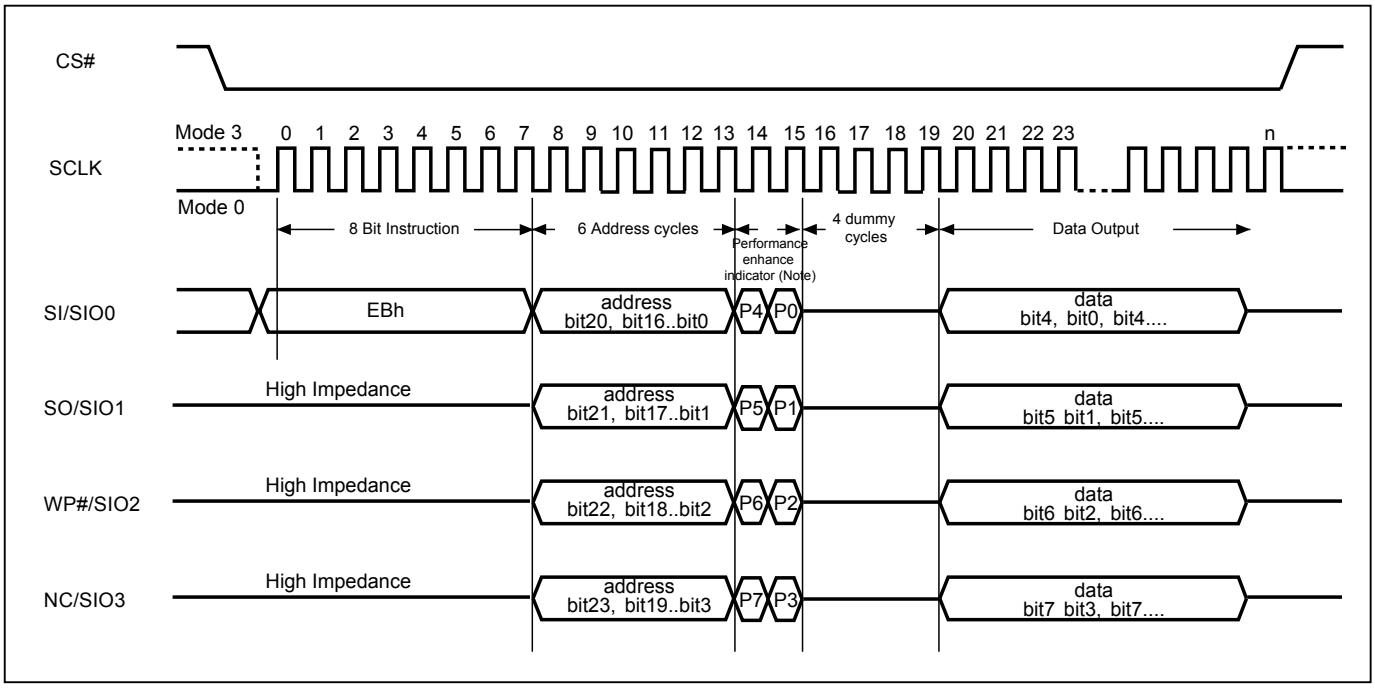
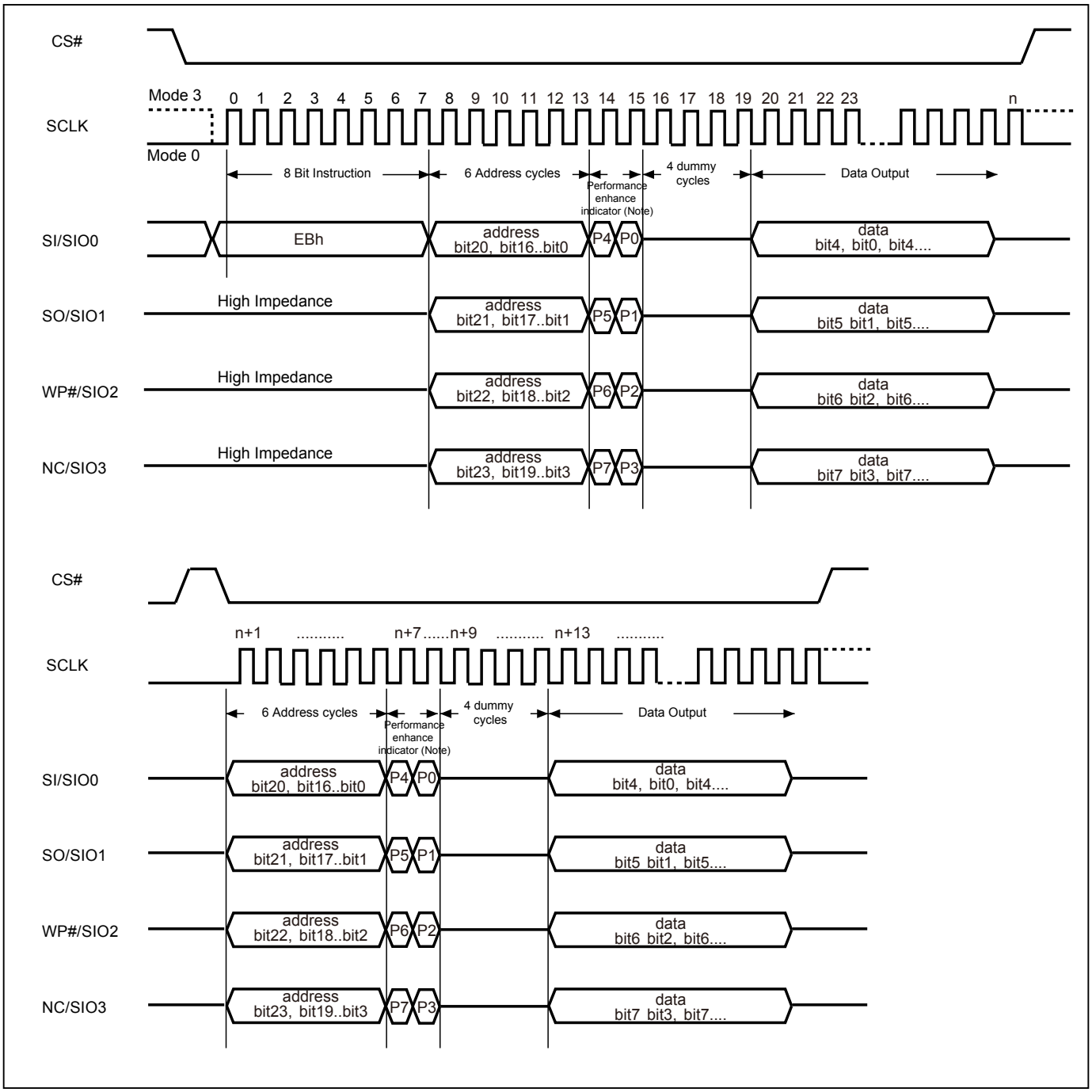


Figure 36. 4 x I/O Read Mode Sequence (Command EB) (SPI Mode) (104MHz)



Note:
1. Also supported in QPI mode with command and subsequent input/output in Quad I/O mode and runs at 104MHz.
2. Hi-impedance is inhibited for the two clock cycles.
3. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.

Figure 37. 4 x I/O Read enhance performance Mode Sequence (Command EB) (SPI Mode) (104MHz)



Note: Performance enhance mode, if P7≠P3 & P6≠P2 & P5≠P1 & P4≠P0 (Toggling), ex: A5, 5A, 0F, if not using performance enhance recommend to keep 1 or 0 in performance enhance indicator.
Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF

Figure 38. 4 x I/O Read enhance performance Mode Sequence (Command EB) (QPI Mode) (104MHz)

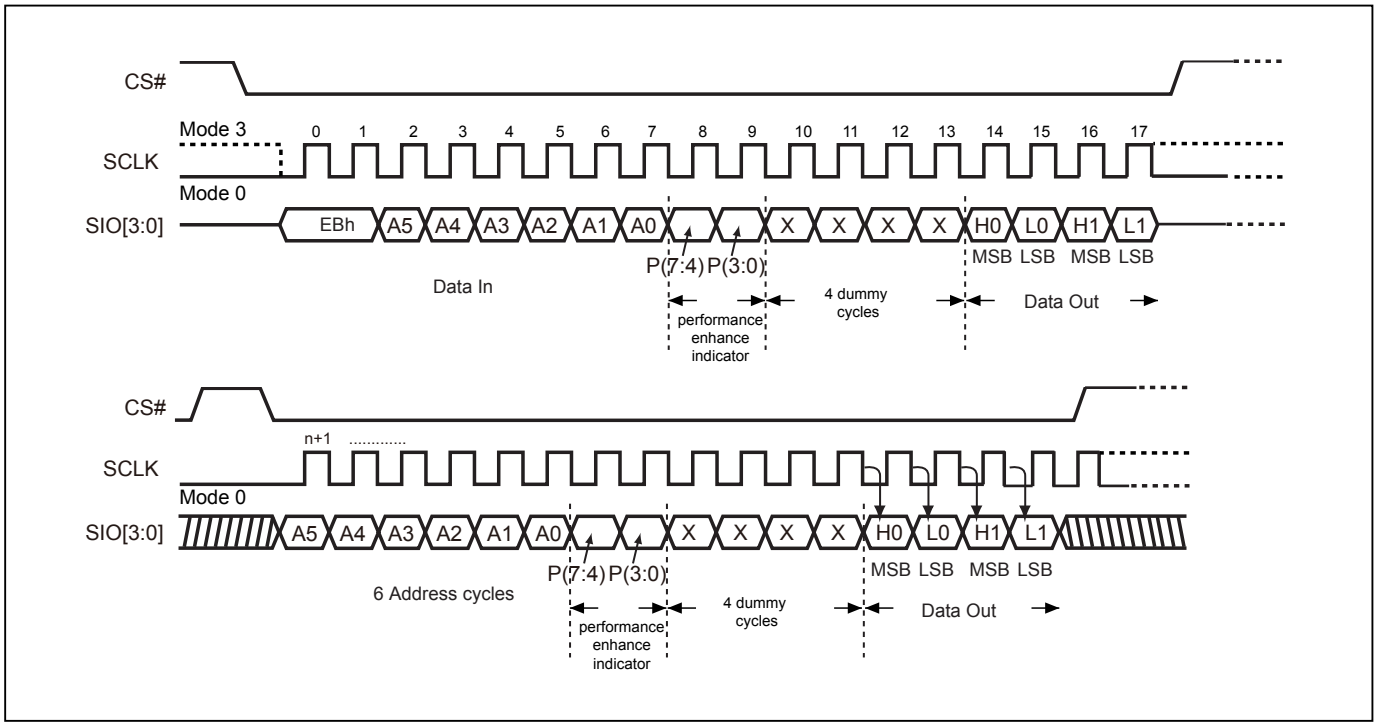


Figure 39. Page Program (PP) Sequence (Command 02) (SPI Mode)

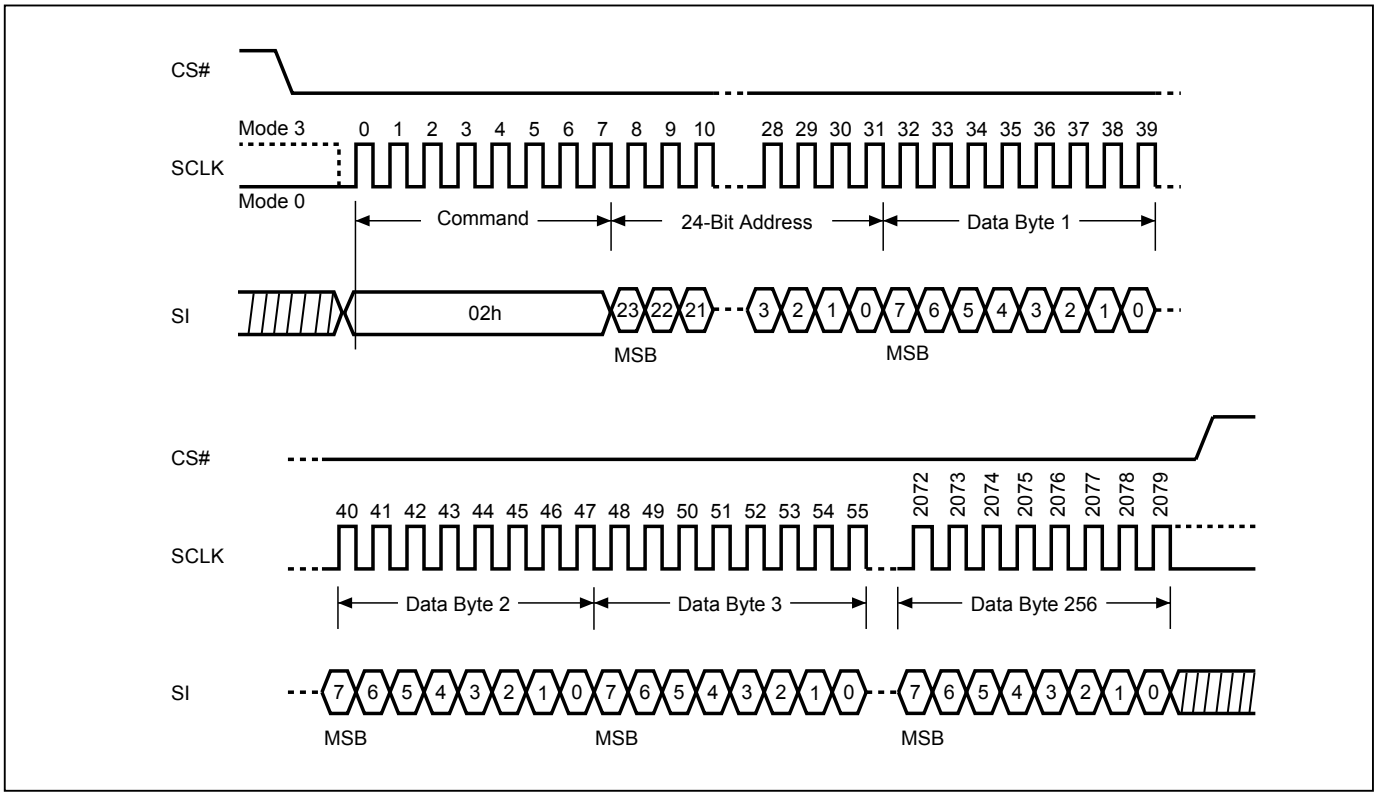


Figure 40. Page Program (PP) Sequence (Command 02) (QPI Mode)

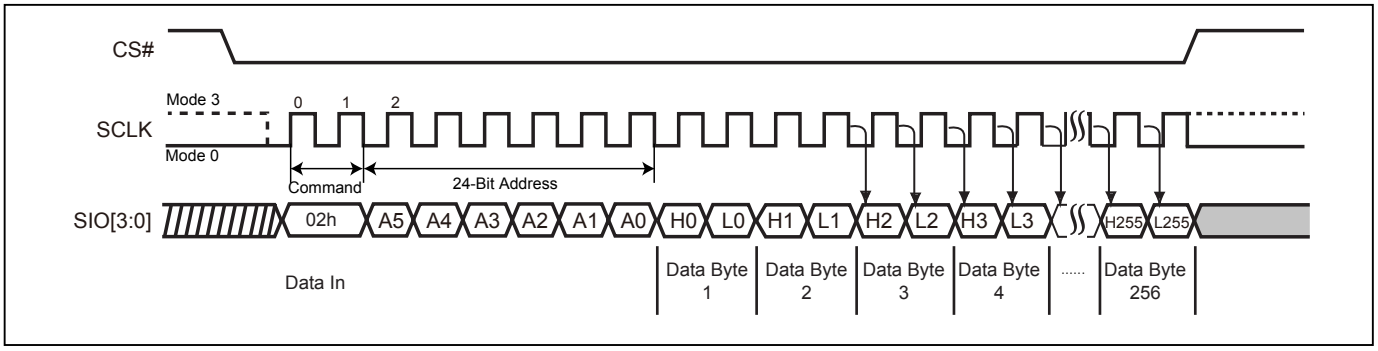


Figure 41. 4 x I/O Page Program (4PP) Sequence (Command 38) (SPI Mode only)

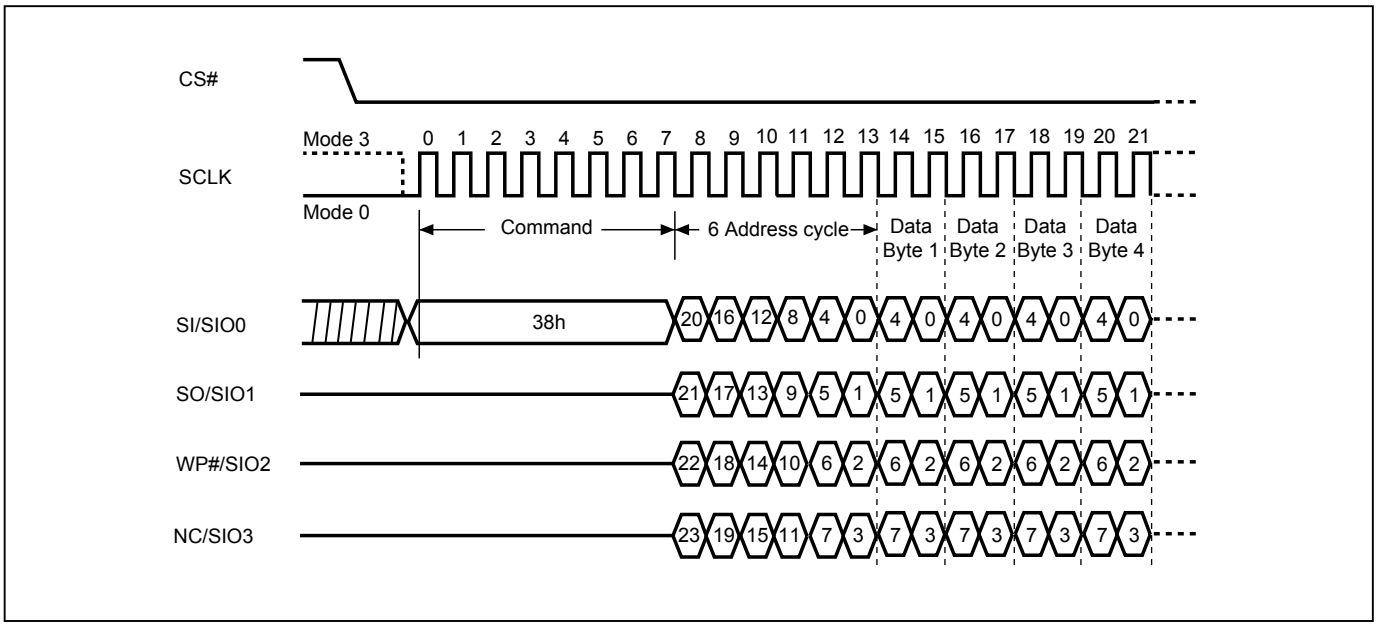


Figure 42. Sector Erase (SE) Sequence (Command 20) (SPI Mode)

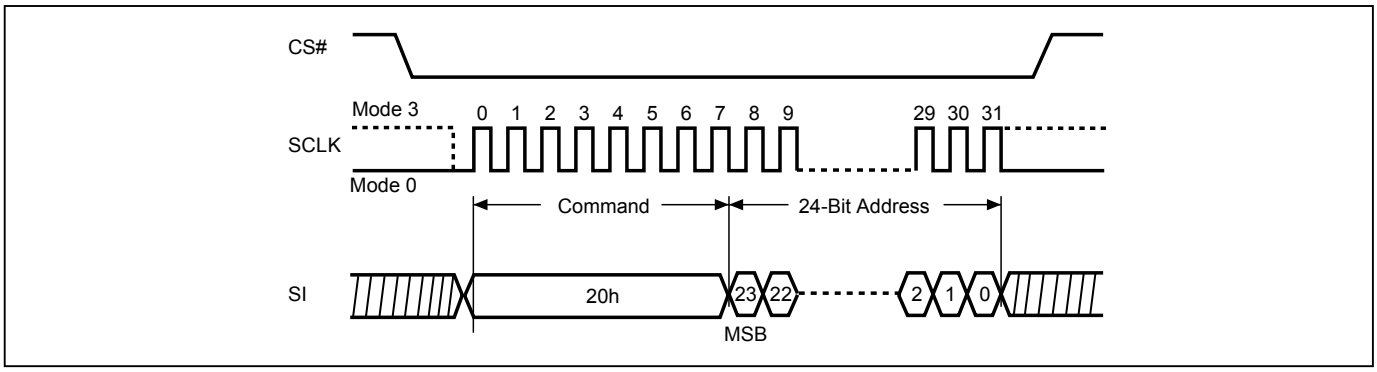


Figure 43. Sector Erase (SE) Sequence (Command 20) (QPI Mode)

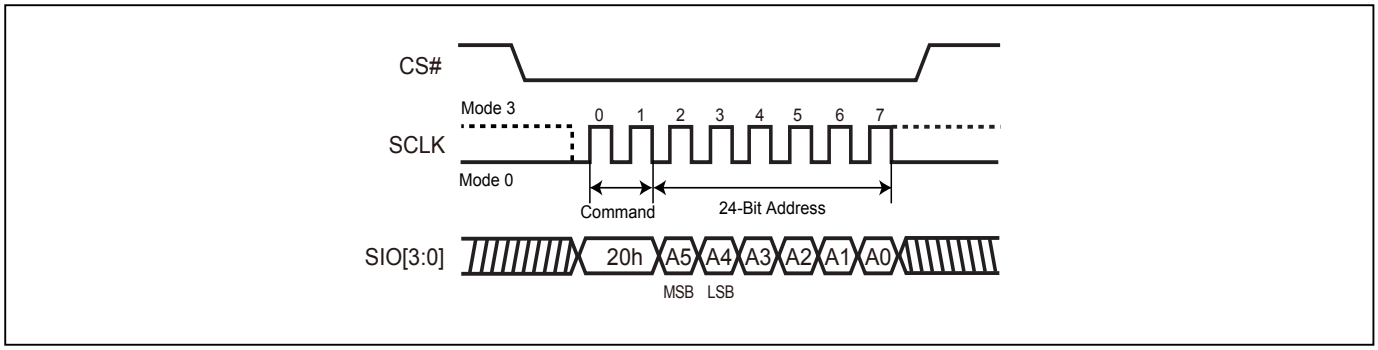


Figure 44. Block Erase 32KB (BE32K) Sequence (Command 52) (SPI Mode)

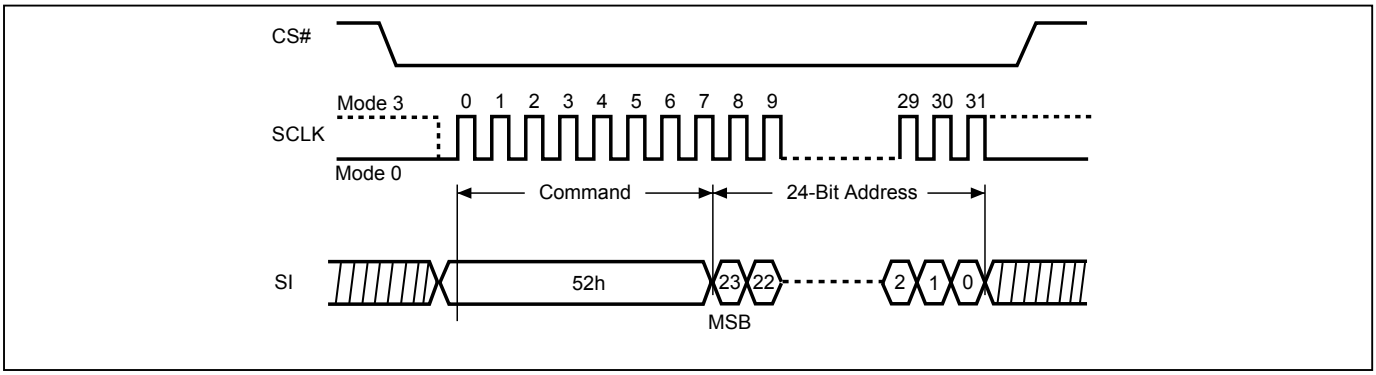


Figure 45. Block Erase 32KB (BE32K) Sequence (Command 52) (QPI Mode)

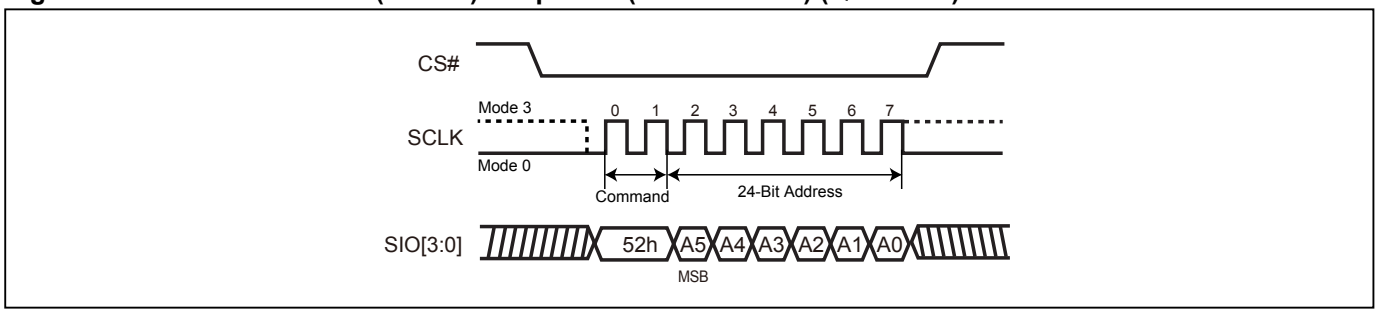


Figure 46. Block Erase (BE) Sequence (Command D8) (SPI Mode)

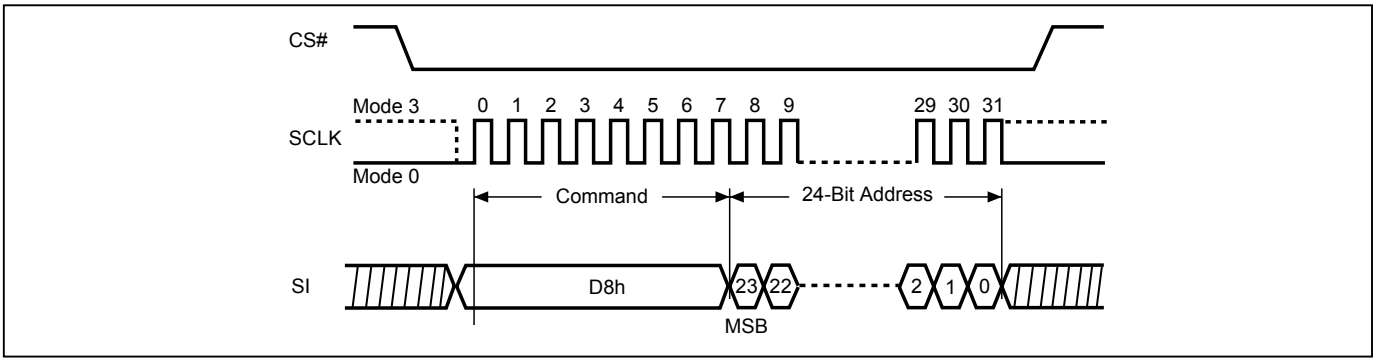


Figure 47. Block Erase (BE) Sequence (Command D8) (QPI Mode)

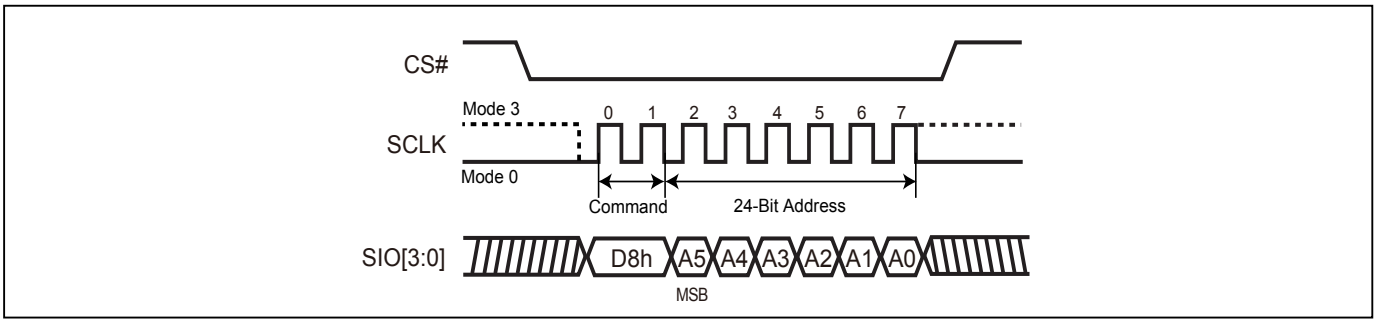


Figure 48. Chip Erase (CE) Sequence (Command 60 or C7) (SPI Mode)

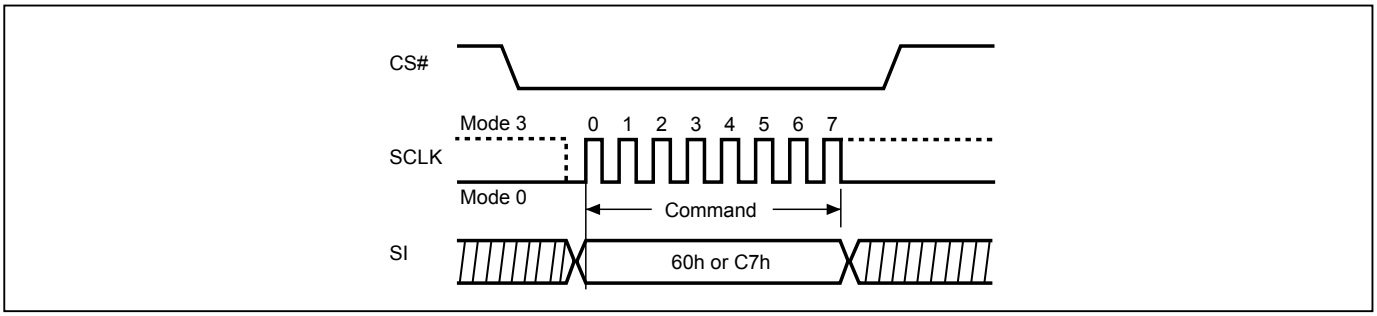


Figure 49. Chip Erase (CE) Sequence (Command 60 or C7) (QPI Mode)

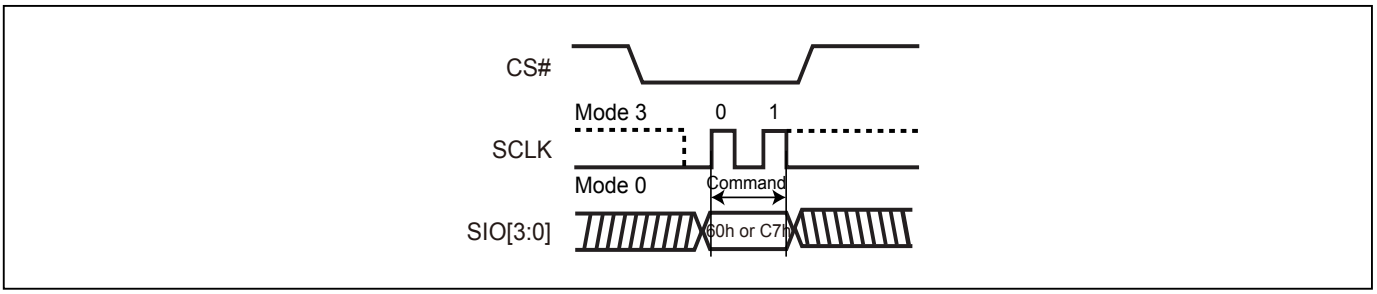


Figure 50. Deep Power-down (DP) Sequence (Command B9) (SPI Mode)

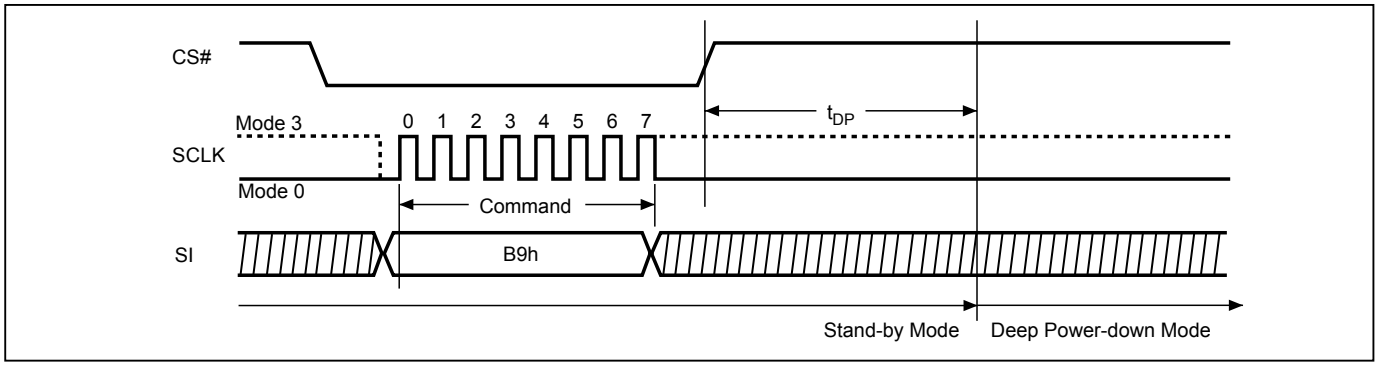


Figure 51. Deep Power-down (DP) Sequence (Command B9) (QPI Mode)

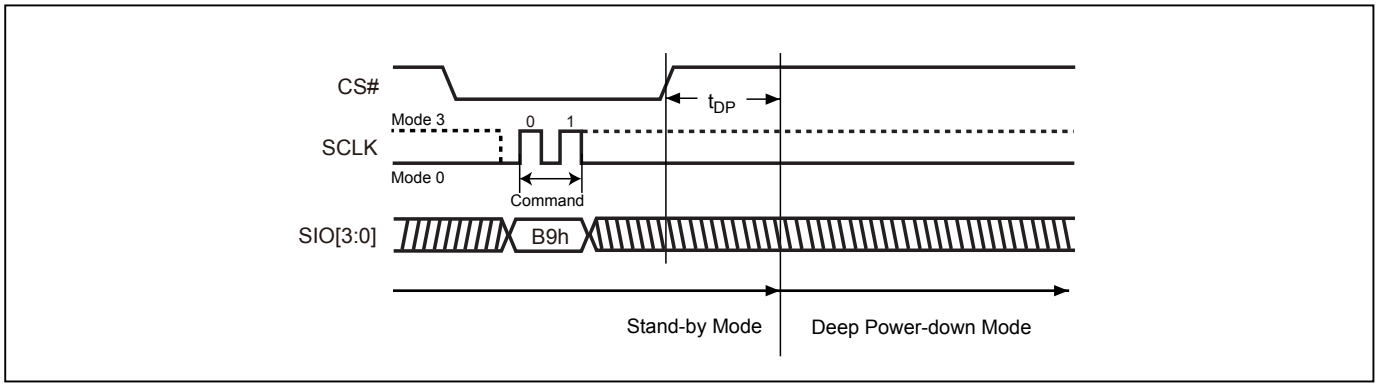


Figure 52. RDP and Read Electronic Signature (RES) Sequence (Command AB) (SPI Mode)

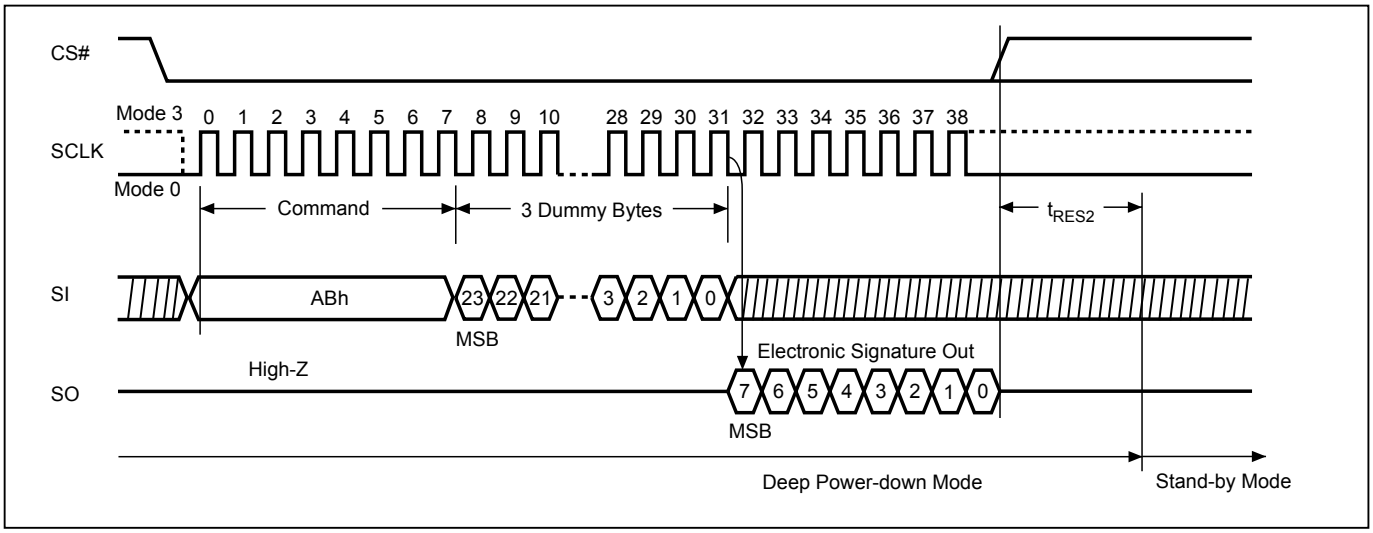


Figure 53. Release from Deep Power-down (RDP) Sequence (Command AB) (SPI Mode)

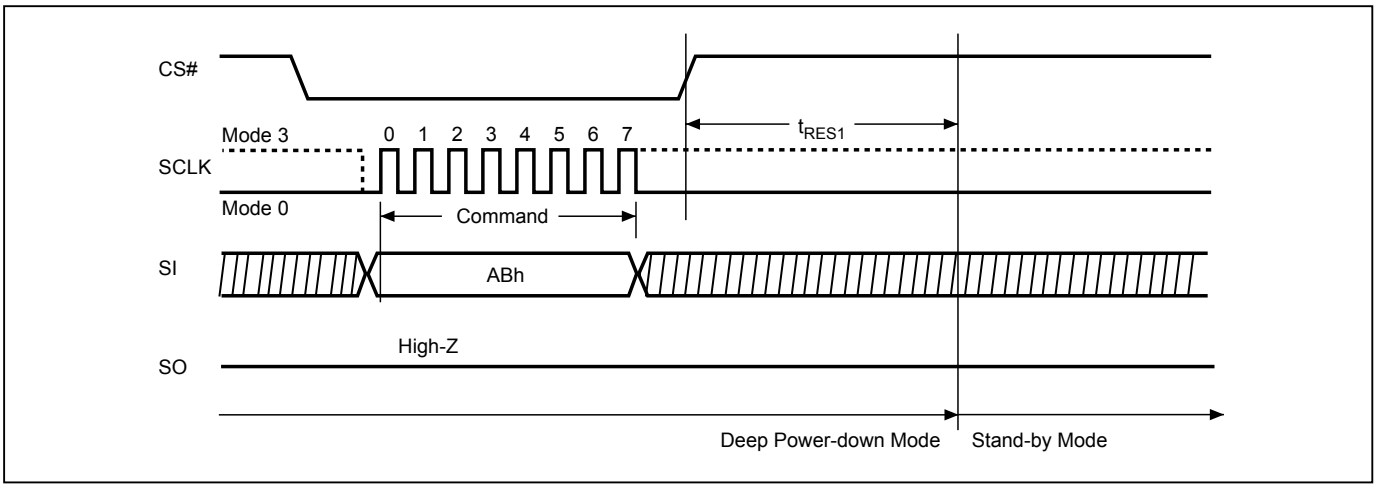


Figure 54. Release from Deep Power-down (RDP) Sequence (Command AB) (QPI Mode)

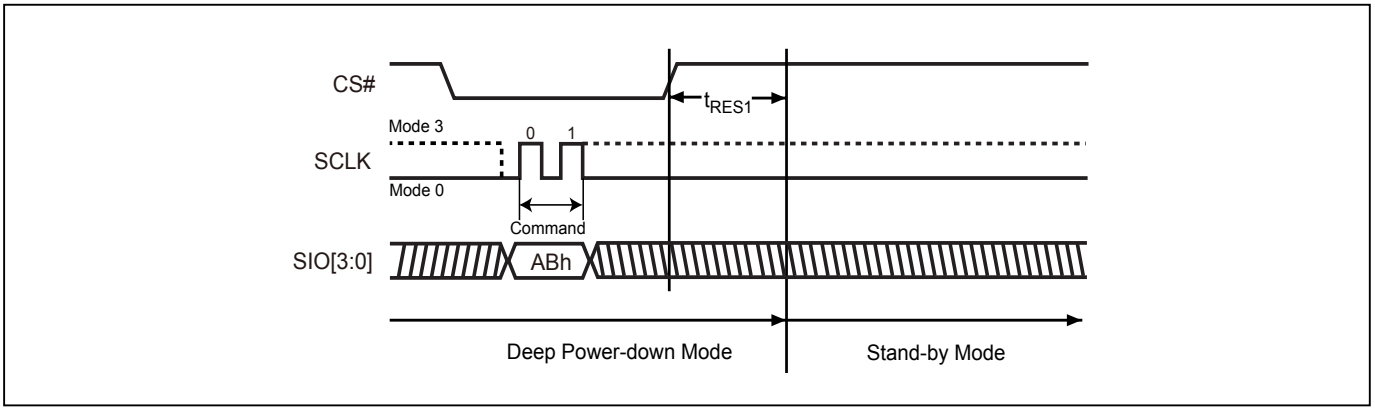
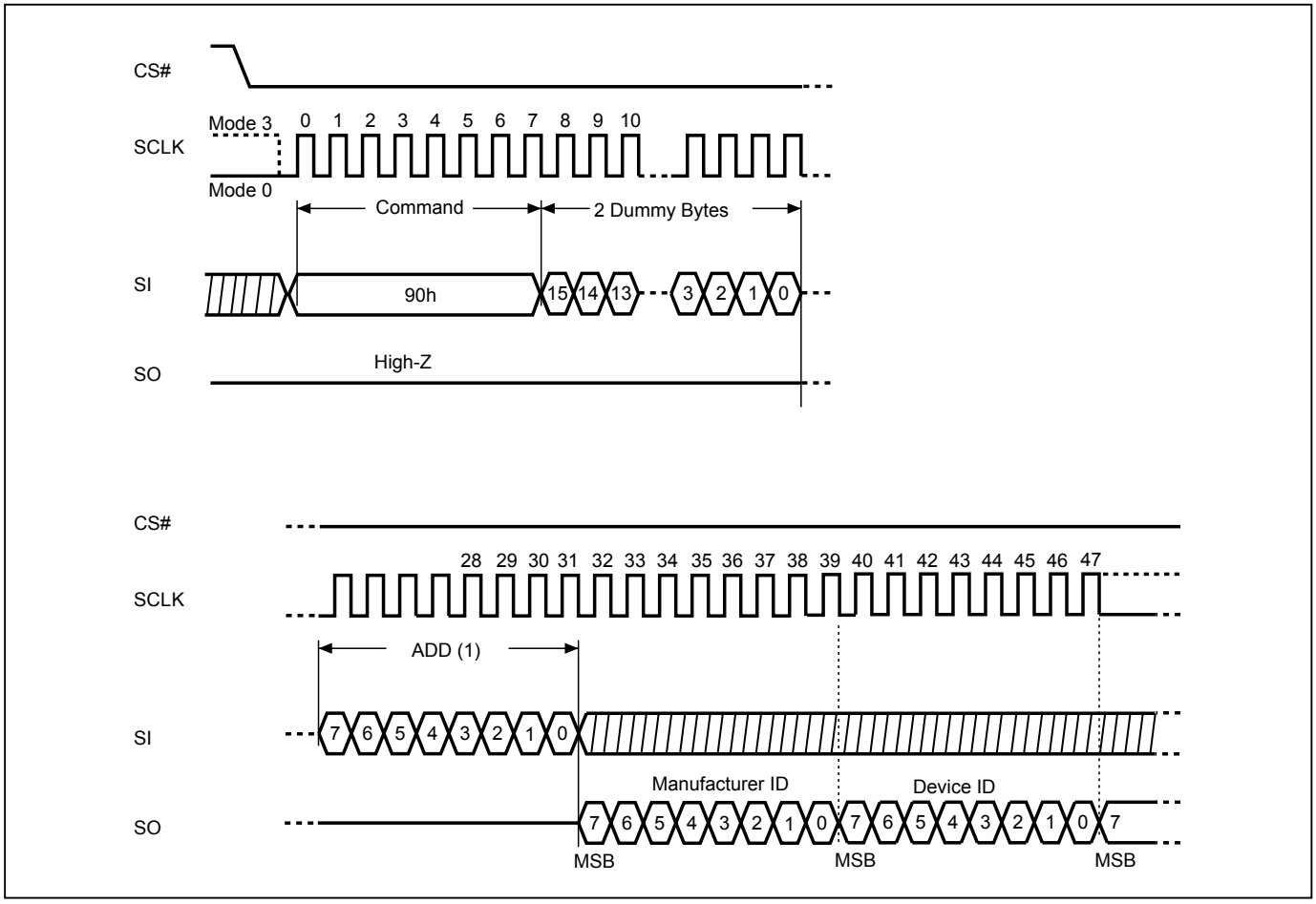


Figure 55. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90) (SPI Mode only)



Notes:
(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.
(2) Instruction is either 90(hex).

Figure 56. Read Security Register (RDSCUR) Sequence (Command 2B) (SPI Mode)

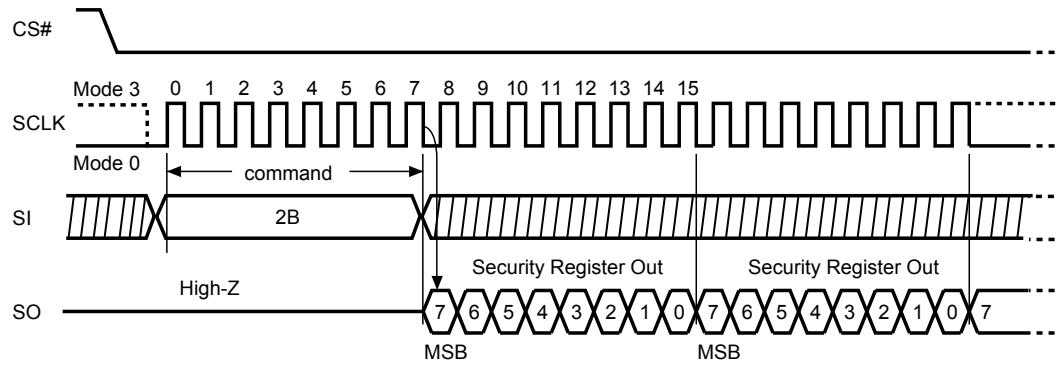


Figure 57. Read Security Register (RDSCUR) Sequence (Command 2B) (QPI Mode)

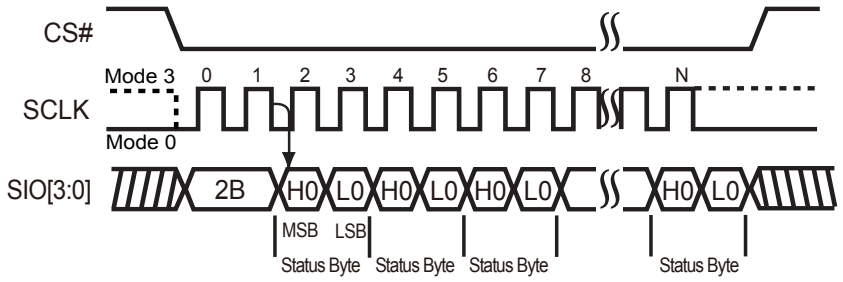


Figure 58. Write Security Register (WRSCUR) Sequence (Command 2F) (SPI Mode)

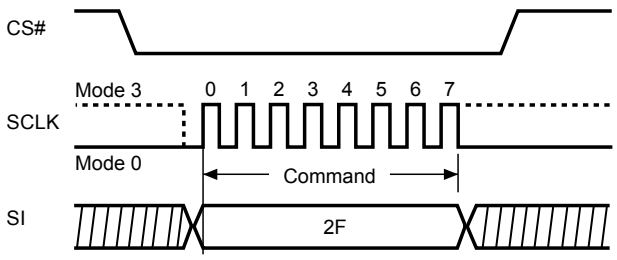


Figure 59. Write Security Register (WRSCUR) Sequence (Command 2F) (QPI Mode)

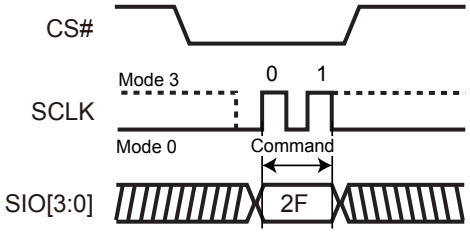


Figure 60. Word Read Quad I/O (W4READ) Sequence (Command E7) (SPI Mode only, 84MHz)

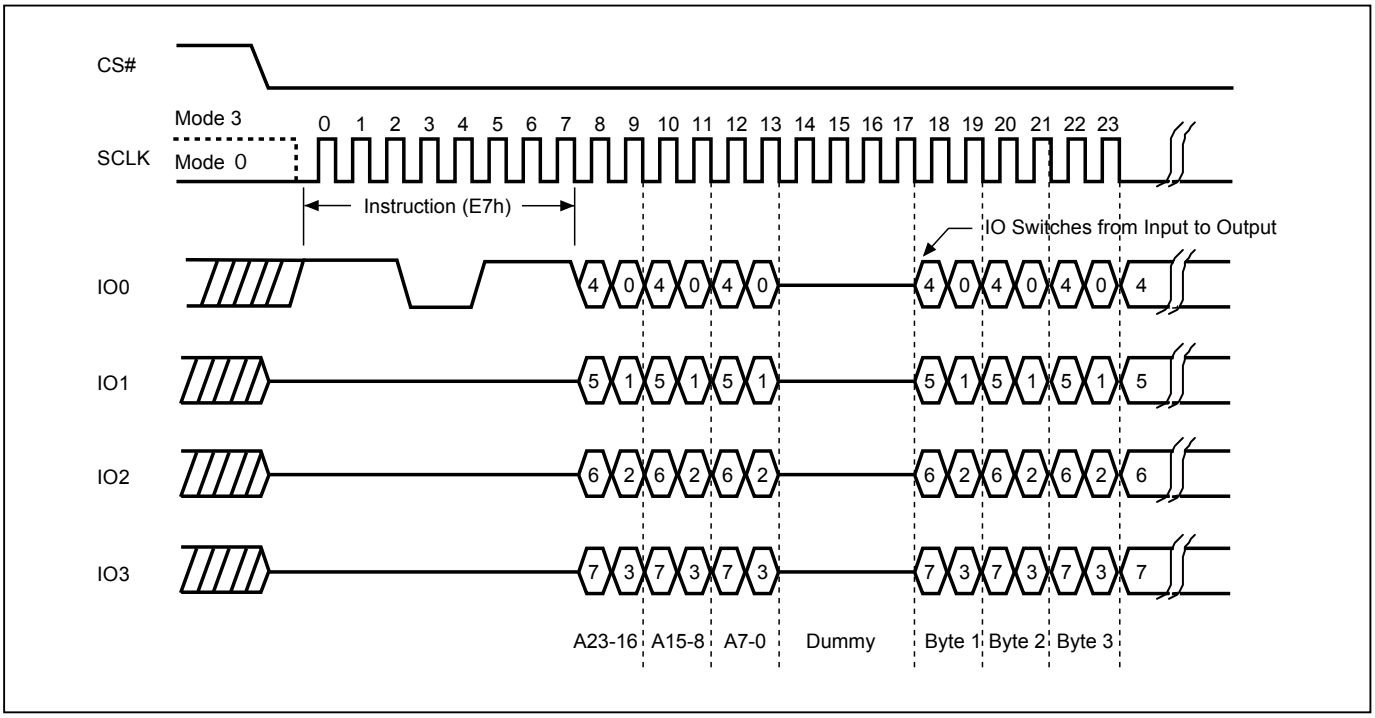


Figure 61. Performance Enhance Mode Reset for Fast Read Quad I/O (SPI Mode)

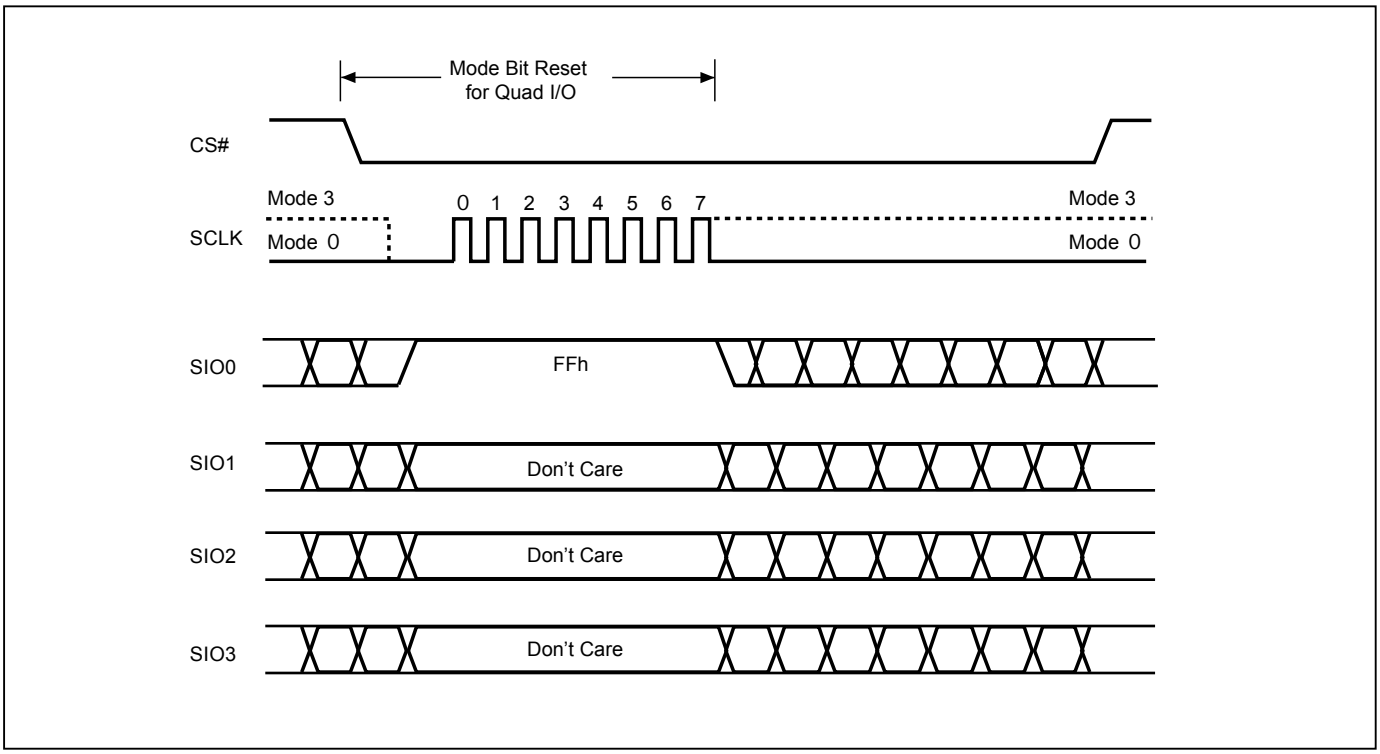


Figure 62. Performance Enhance Mode Reset for Fast Read Quad I/O (QPI Mode)

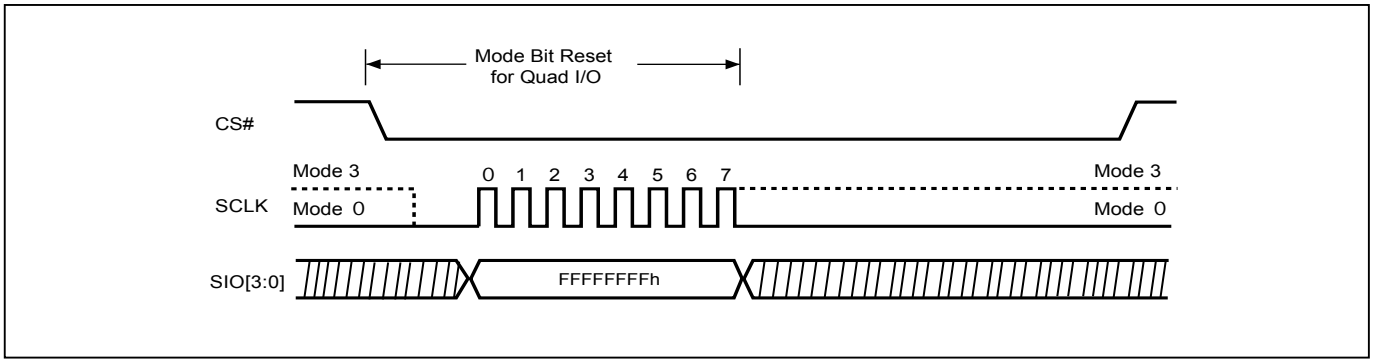


Figure 63. Reset Sequence (SPI mode)

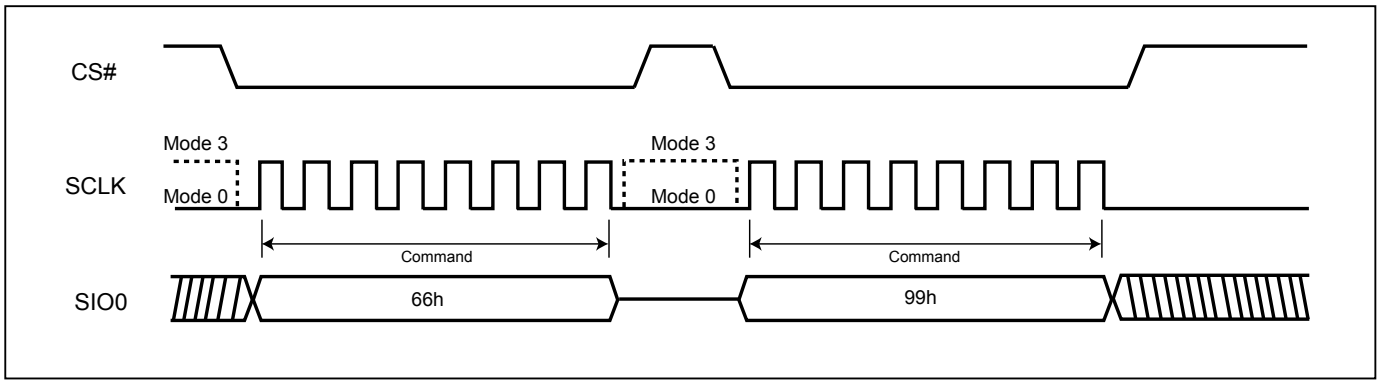


Figure 64. Reset Sequence (QPI mode)

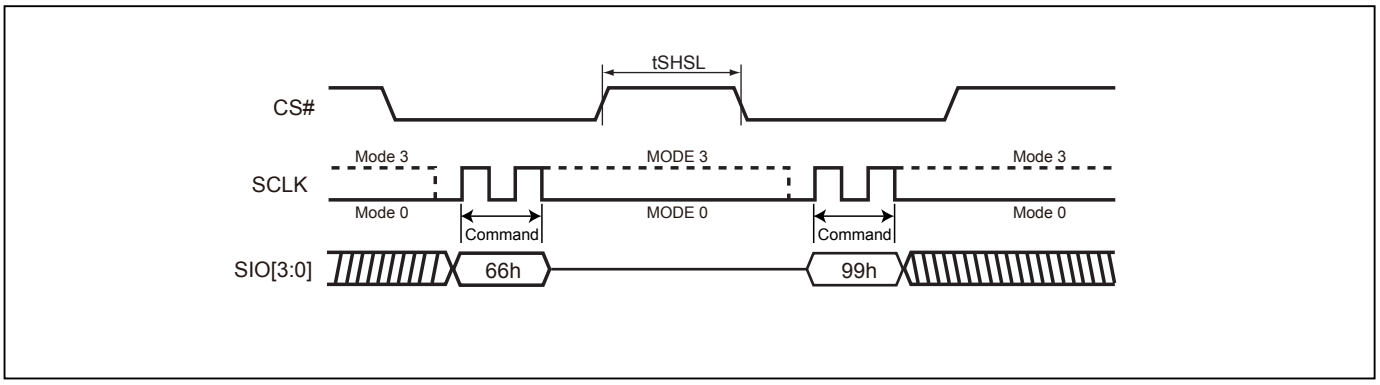


Figure 65. Enable Quad I/O Sequence

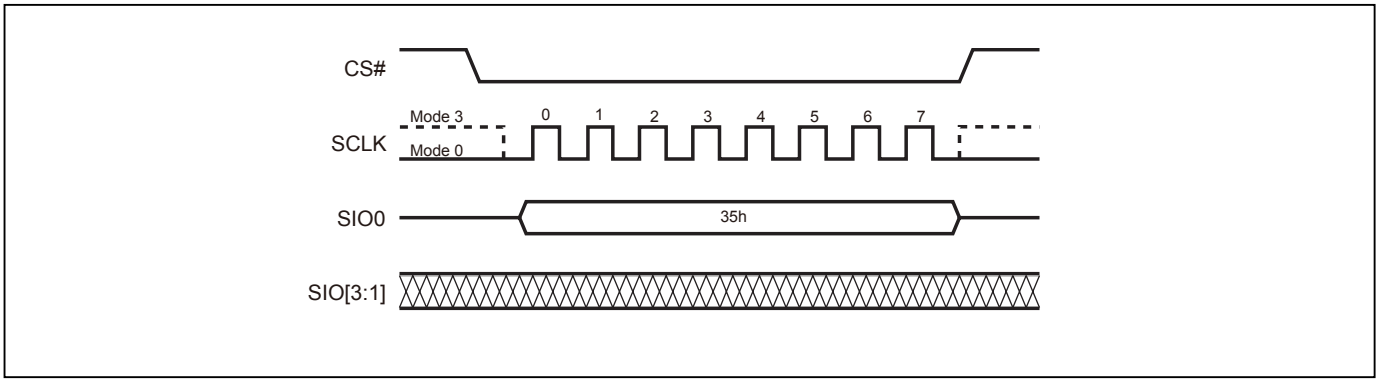


Figure 66. Suspend to Read Latency

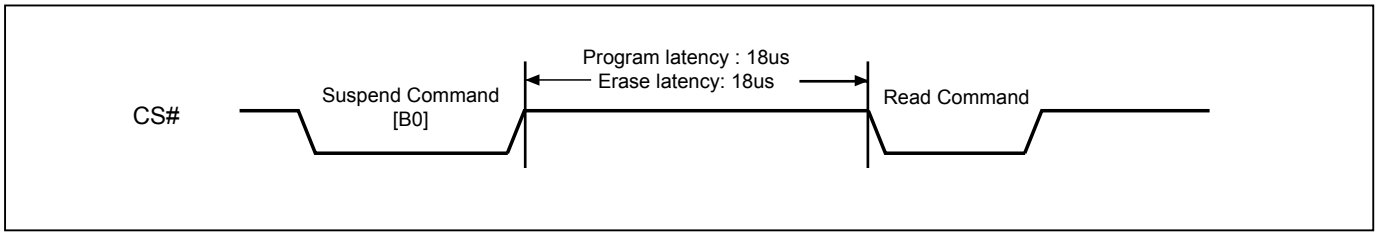


Figure 67. Resume to Read Latency

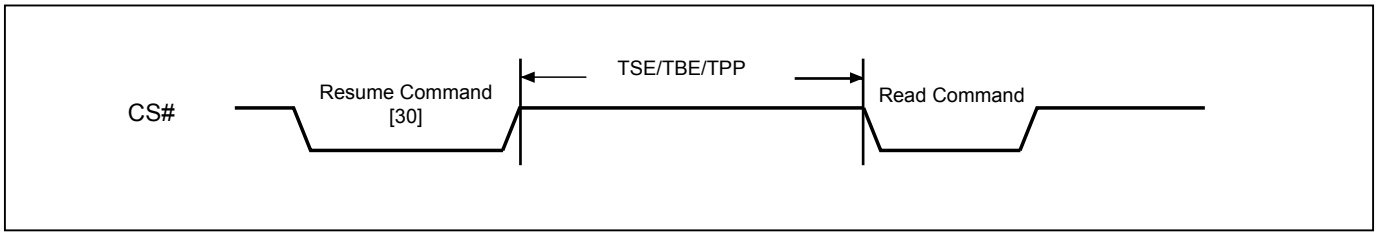


Figure 68. Resume to Suspend Latency

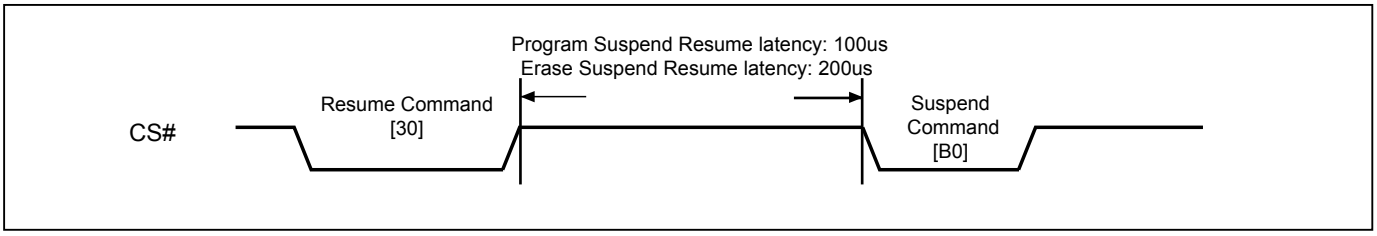


Figure 69. Software Reset Recovery

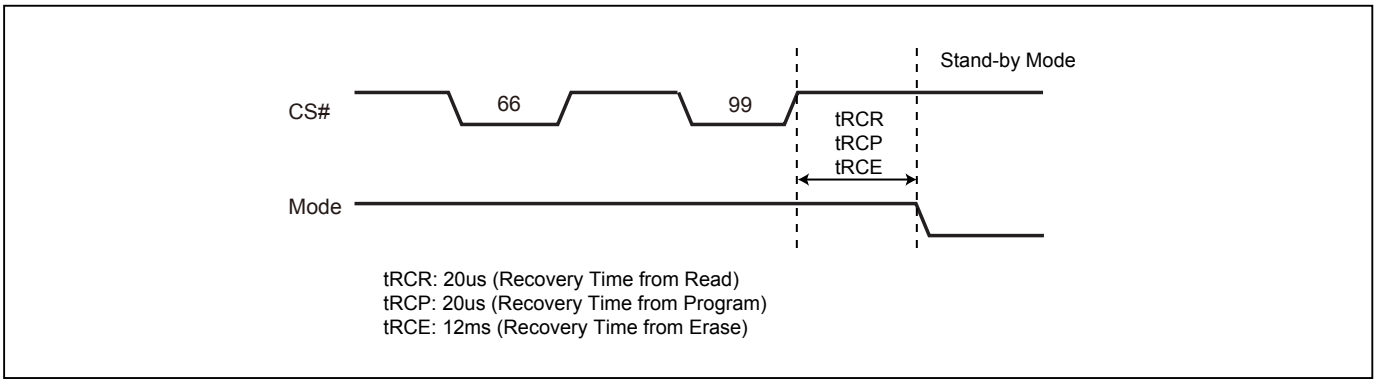
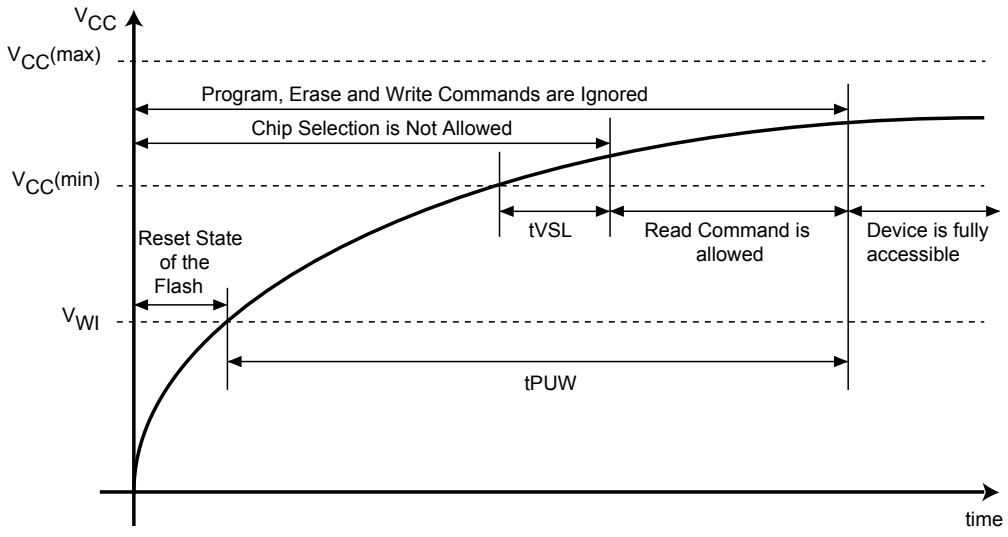


Figure 70. Power-up Timing



Note: VCC (max.) is 2.0V and VCC (min.) is 1.65V.

Table 16. Power-Up Timing and VWI Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL(1)	VCC(min) to CS# low (VCC Rise Time)	300		us
tPUW(1)	Time delay to Write instruction	1	10	ms
VWI(1)	Command Inhibit Voltage	1.0	1.4	V

Note: 1. These parameters are characterized only.

12-1. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

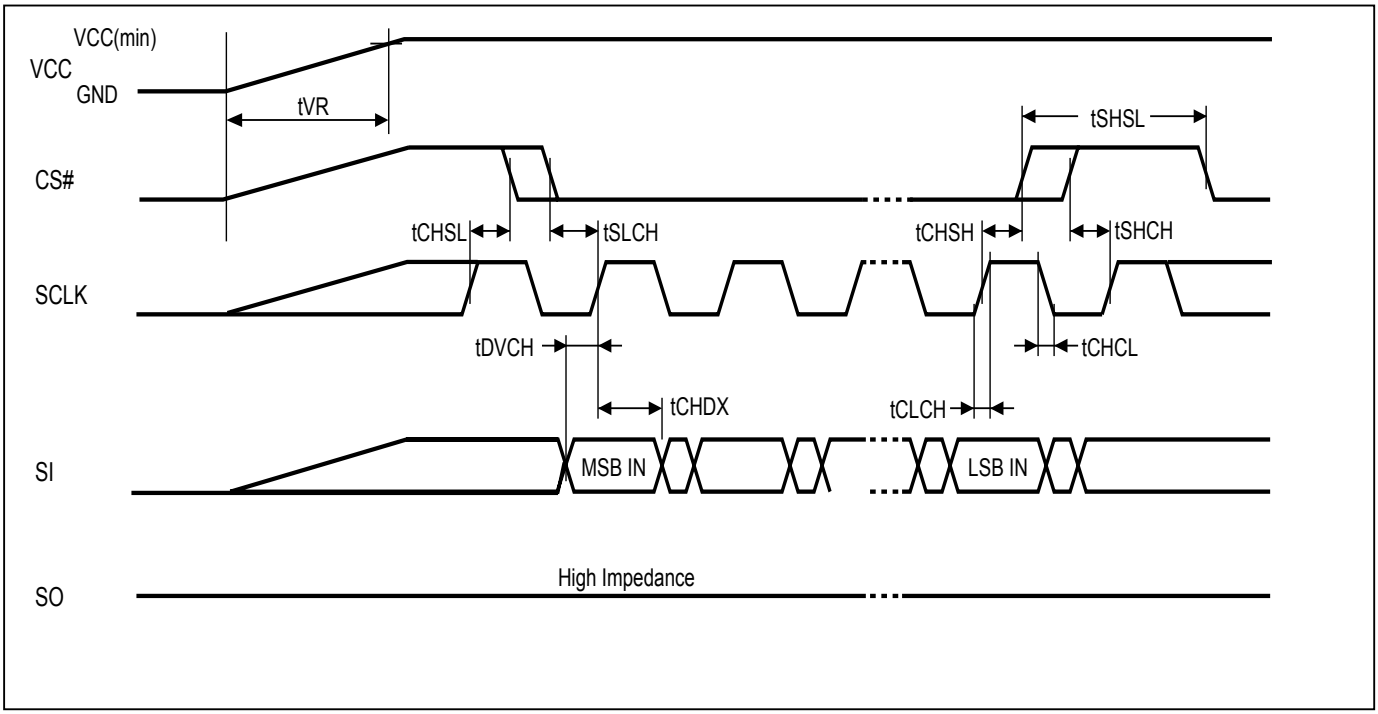
13. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *"Figure 71. AC Timing at Device Power-Up"* and *"Figure 72. Power-Down Sequence"* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 71. AC Timing at Device Power-Up

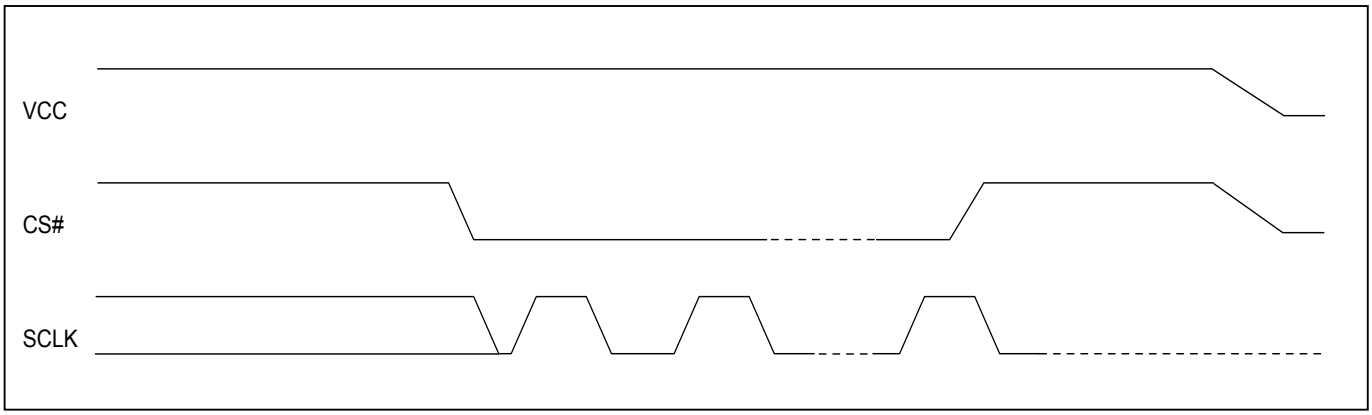


Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *"Table 15. AC Characteristics"*.

Figure 72. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.



14. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Min.	Typ. (1)	Max. (2)	Unit
Write Status Register Cycle Time			40	ms
Sector Erase Cycle Time (4KB)		45	200	ms
Block Erase Cycle Time (32KB)		250	1000	ms
Block Erase Cycle Time (64KB)		500	2000	ms
Chip Erase Cycle Time		9	20	s
Byte Program Time (via page program command)		10	30	us
Page Program Time		1.2	3	ms
Erase/Program Cycle		100,000		cycles

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 1.8V, and checkerboard pattern.
2. Under worst conditions of 85°C and 1.65V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. The maximum chip programming time is evaluated under the worst conditions of 0C, VCC=1.8V, and 100K cycle with 90% confidence level.

15. DATA RETENTION

PARAMETER	Condition	Min.	Max.	UNIT
Data retention	55˚C	20		years

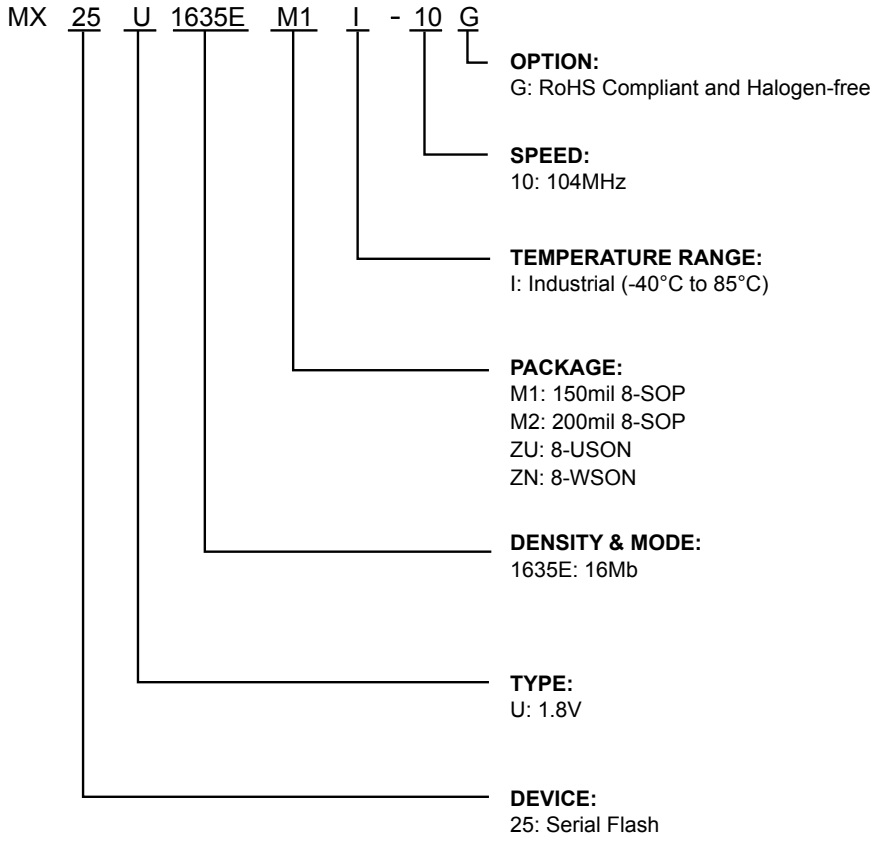
16. LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 1.8V, one pin at a time.		

17. ORDERING INFORMATION

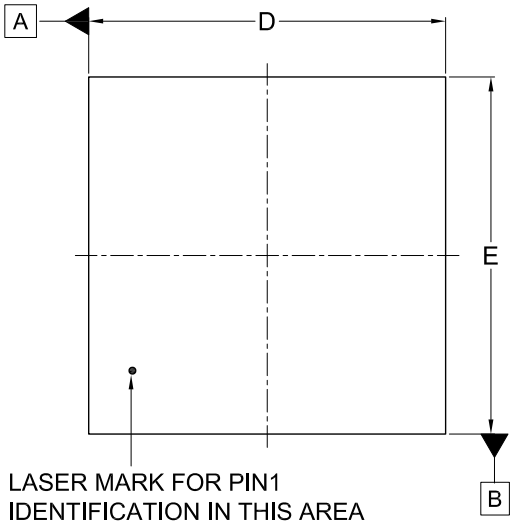
Part No.	Clock (MHz)	Temperature	Package	Remark
MX25U1635EM1I-10G	104	-40°C~85°C	8-SOP (150mil)	
MX25U1635EM2I-10G	104	-40°C~85°C	8-SOP (200mil)	
MX25U1635EZUI-10G	104	-40°C~85°C	8-USON (4x4mm)	
MX25U1635EZNI-10G	104	-40°C~85°C	8-WSON (6x5mm)	

18. PART NAME DESCRIPTION

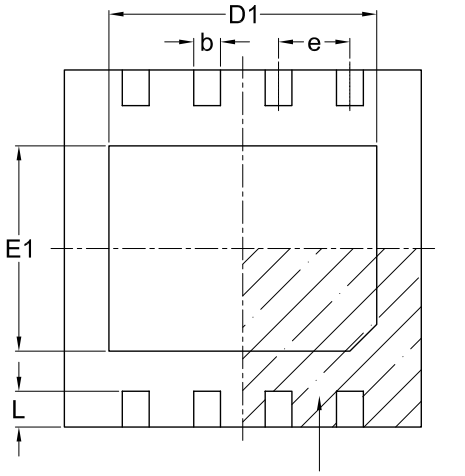


19. PACKAGE INFORMATION

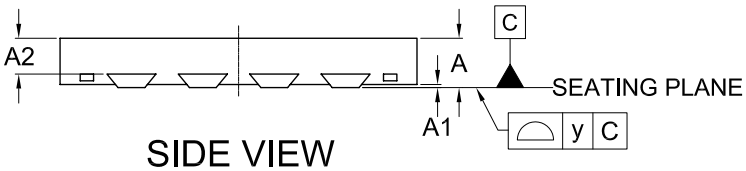
Doc. Title: Package Outline for USON 8L (4x4x0.6MM, LEAD PITCH 0.8MM)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Note:

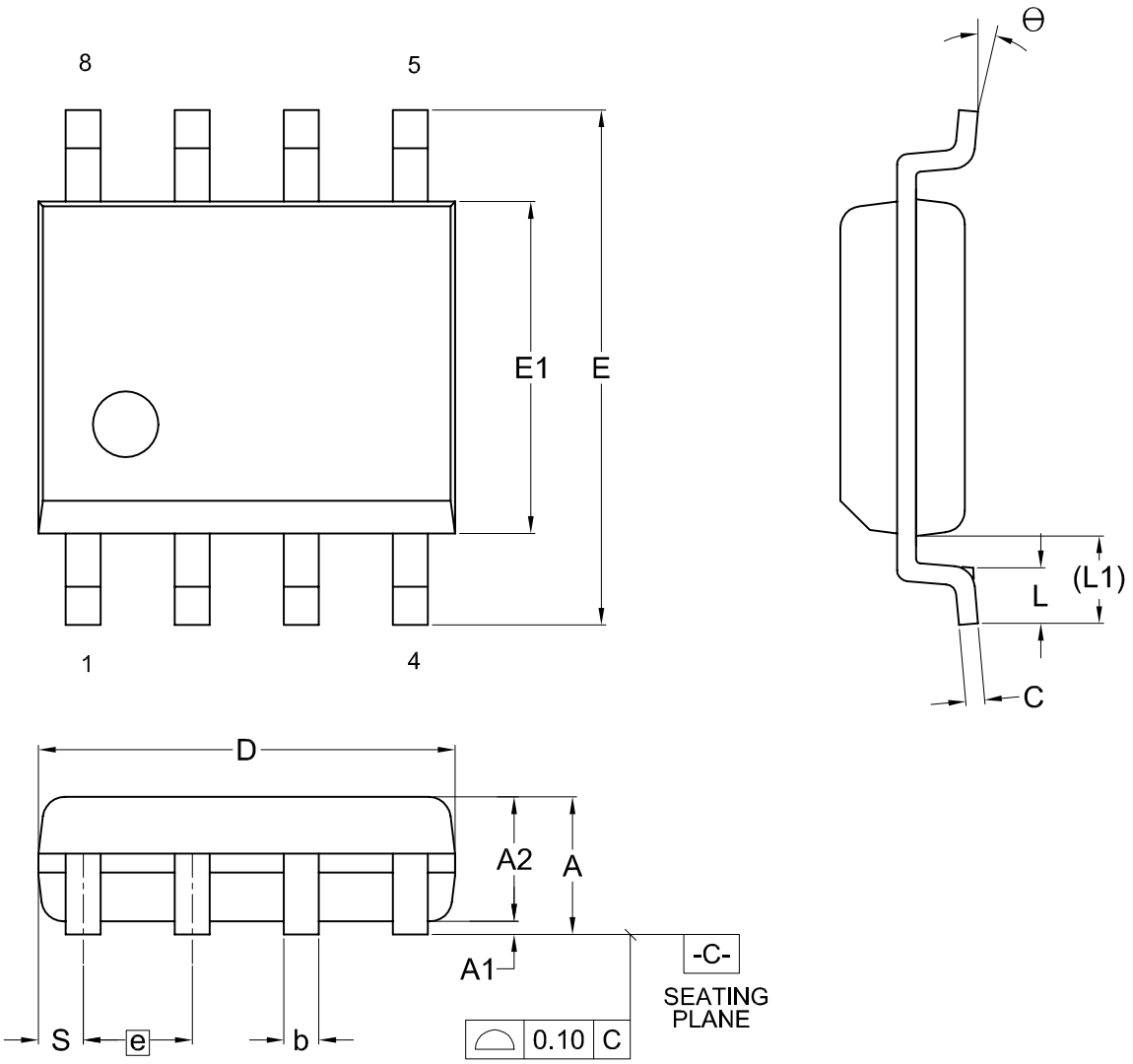
This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.50	---	---	0.25	3.90	2.90	3.90	2.20	0.35	---	0.00
	Nom.	0.55	0.04	0.40	0.30	4.00	3.00	4.00	2.30	0.40	0.80	---
	Max.	0.60	0.05	0.43	0.35	4.10	3.10	4.10	2.40	0.45	---	0.08
Inch	Min.	0.020	---	---	0.010	0.154	0.114	0.154	0.087	0.014	---	0.00
	Nom.	0.022	0.002	0.016	0.011	0.157	0.118	0.157	0.091	0.016	0.031	---
	Max.	0.024	0.002	0.017	0.014	0.161	0.122	0.161	0.094	0.018	---	0.003

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-3601	5	MO-252			

Doe. Title: Package Outline for SOP 8L (150MIL)

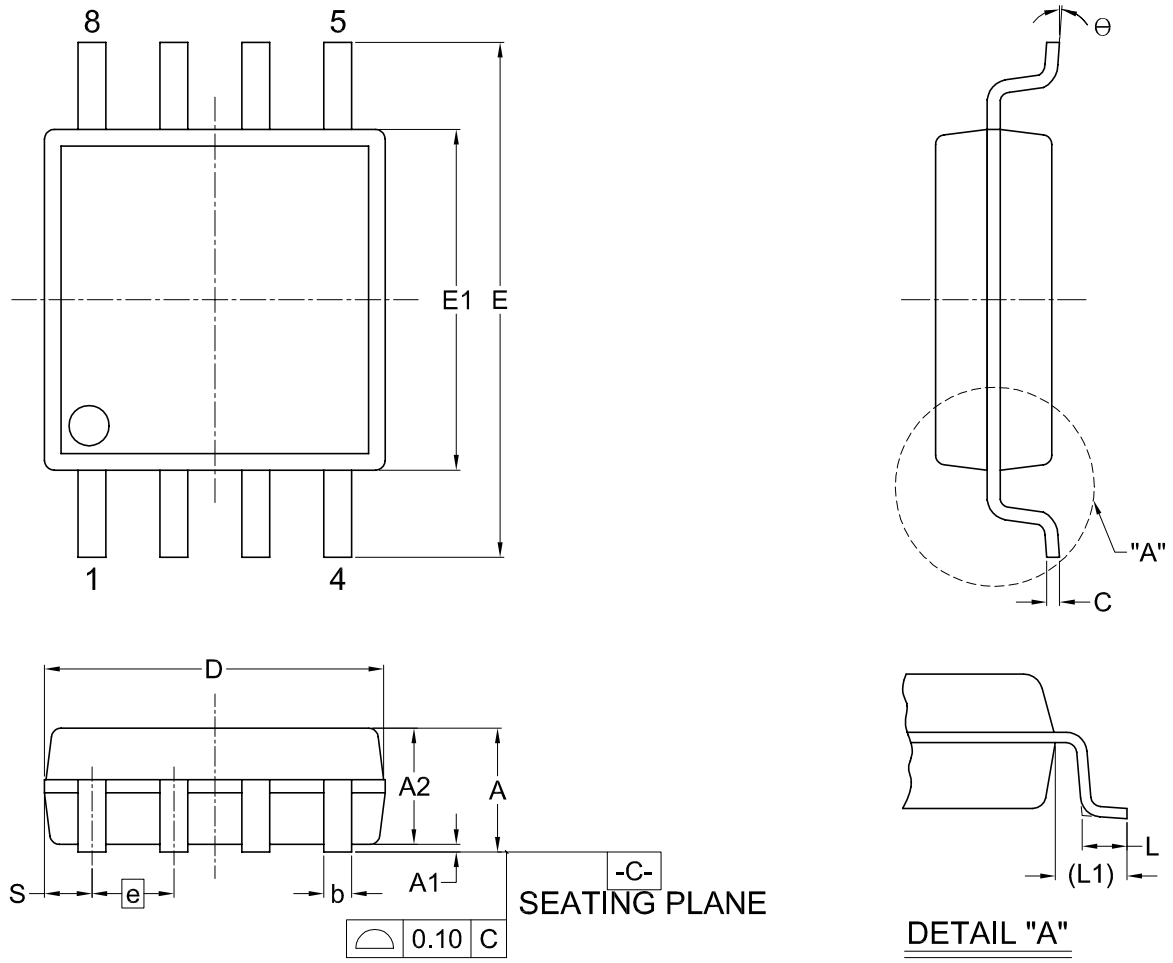


Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
mm	Min.	---	0.10	1.35	0.36	0.15	4.77	5.80	3.80		0.46	0.85	0.41	0
	Nom.	---	0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5
	Max.	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00		0.86	1.25	0.67	8
Inch	Min.	---	0.004	0.053	0.014	0.006	0.188	0.228	0.150		0.018	0.033	0.016	0
	Nom.	---	0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.050	0.026	0.041	0.021	5
	Max.	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158		0.034	0.049	0.026	8

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1401	7	MS-012			

Doc. Title: Package Outline for SOP 8L 200MIL (official name - 209MIL)

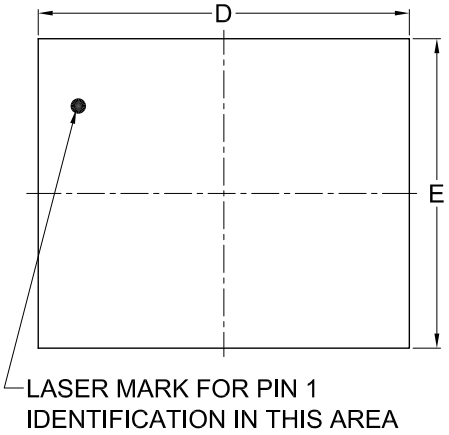


Dimensions (inch dimensions are derived from the original mm dimensions)

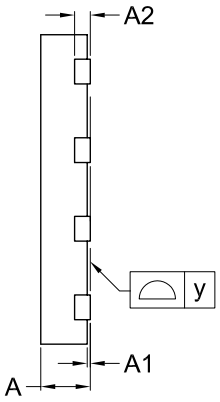
UNIT \ SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.05	1.70	0.36	0.19	5.13	7.70	5.18	---	0.50	1.21	0.62	0
	Nom.	---	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	---	0.80	1.41	0.88	8
Inch	Min.	---	0.002	0.067	0.014	0.007	0.202	0.303	0.204	---	0.020	0.048	0.024	0
	Nom.	---	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	---	0.031	0.056	0.035	8

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1406	3				

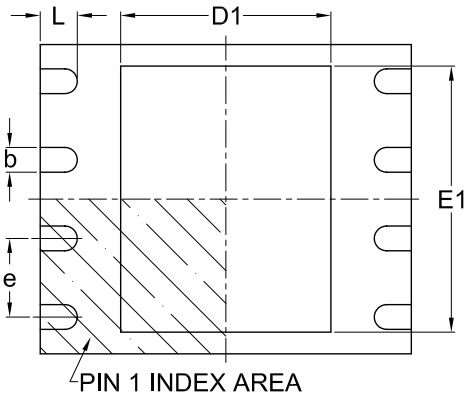
Doc. Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	5.90	3.30	4.90	3.90	0.50	---	0.00
	Nom.	---	---	0.20	0.40	6.00	3.40	5.00	4.00	0.60	1.27	---
	Max.	0.80	0.05	---	0.48	6.10	3.50	5.10	4.10	0.75	---	0.08
Inch	Min.	0.028	---	---	0.014	0.232	0.129	0.193	0.154	0.020	---	0.00
	Nom.	---	---	0.008	0.016	0.236	0.134	0.197	0.157	0.024	0.05	---
	Max.	0.032	0.002	---	0.019	0.240	0.138	0.201	0.161	0.030	---	0.003

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-3401	6	MO-220			

20. REVISION HISTORY

Revision No.	Description	Page	Date
0.01	1. Added MXSMIO™ logo and 4 I/O 104MHz specifications	P6	JUL/24/2009
	2. Take out 8WSON and 200mil 8-SOP package outline	P9	
	3. Added software reset	P11	
	4. Corrected supporting instructions	P16	
	5. Modified dummy cycle numbers (from 2 to 4)	P17	
	6. Added QPI, Write suspend/resume commands	P19	
	7. Added QPI operations in the command descriptions	ALL	
	8. AC/DC modifications; Write suspend features modify	P6,38,39,45	
	9. Updated SPI & QPI commands & descriptions	ALL	
	10. Remove loading relevance to clock rate	P6	
	11. Modify 32Mb WSON package as USON package	P7	
	12. Add WIP, WEL polling sequence description	P22	
	13. Add description about performance enhance mode not supported in 2-I/O mode	P27	
	14. Add 104MHz note in fTSCLK	P45	
	15. Added 8-SOP 200mil package for 16Mb; modified 32Mb from USON to WSON	P7	
	16. Added 8WSON package information	P9	
	17. Added RDSR flow charts	P22~24	
	18. Change CFIRD command from A5 to 5A	P19,40,41	
	19. Modified EPN for package information correction and speed grade (from -12G to -10G)	P70,71	
	20. Modified Erase/Program time spec	P6,48,69	
	21. Added program/erase flow description	P22,23	
	22. Modified performance enhance mode toggling description	P56	
	23. Revised fast program time and byte program time	P6	
	24. Added WRSCUR and WPSEL in WEL reset situation	P11	
	25. Modified Recovery Time from Read	P48,66	DEC/24/2009
0.02	1. Modified "QE bit" description	P25	
	2. Modified four I/O and QPI mode description	P11,20	
	3. Modifed Release read Enable description	P19,28	
	4. Changed title from "Advanced Information" to "Preliminary"	P6	
	5. Added MX25U8035E and MX25U8035E function	All	
0.03	1. Revised tCE	P50,71	JAN/27/2009
	2. Deleted tREHZ	P50	
1.0	1. Removed "Preliminary"	P6	APR/01/2010
	2. Low Power Consumption: modified current description	P6,49	
	3. Table 10. AC CHARACTERISTICS: modified Min. tSLCH/tCHSH	P50	
	4. Modified Figure 40	P70	
	5. Added Figure 41	P71	
	6. Modified General Description	P8	
	7. Modified Fast Erase Time	P6	
	8. Modified Page Program Cycle Time from 0.9ms to 1.2ms	P6,50	
	9. Modified "Read DMC mode (RDDMC)" description	P42	
	10. Changed the naming "CFI mode" as "DMC mode"	P18,22,42	
	11. Added dummy description	P22	
	12. Modified figure 38	P68	

Revision No.	Description	Page	Date
1.1	1. Removed DMC sequence description & content table	P18,22,42	JUL/06/2010
1.2	1. Remove "Advanced Information" in the package information and part number section	P7,74	SEP/16/2010
	2. Added NC/SIO3 description	P7,10	
	3. Added RDSCUR & WRSCUR waveforms	P65,66	
	4. Modified WRSCUR description	P38	
1.3	1. Removed MX25U8035E		NOV/26/2010
1.4	1. Removed the QPI support in RES command	P21,34,63	SEP/29/2011
	2. Modified tCH/tCL(4PP and Normal Read) from 15ns to 4.5ns	P50	
	3. Modified Write Protection Selection (WPSEL) description	P38,39	
	4. Modified tSLCH, tCHSL & tCHDX	P50	
	5. Modified CIN/COUT (max.) from 6pF/8pF to 10pF/25pF	P47	
	6. Revised Ordering Information table	P75	
1.5	1. Added Read SFDP (RDSFDP) Mode	P7,17,20, P46~55,60	FEB/10/2012
1.6	1. Modified Program/Erase Suspend/Resume latency	P43~44,80	NOV/07/2012
	2. Modified content and descriptions	P18,23~25,33 P43~44,64,76	
1.7	1. Modified tCLQX value in AC Characteristics Table	P60	DEC/12/2012
1.8	1. Modified Data Retention value	P6,78	MAY/03/2013
	2. Modified tCH, tCL and its value in AC Characteristics Table	P54	
	3. Modified Features Page to sync with AC Characteristics Table	P6	
	4. Correct Symbol in Reset Sequence (QPI mode) Figure	P73	
	5. Removed MX25U3235E	All	
1.9	1. Updated parameters for DC/AC Characteristics	P6,53,54	NOV/08/2013
	2. Updated Erase and Programming Performance	P6,78	
	3. Modified VCC to Ground Potential	P51	

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