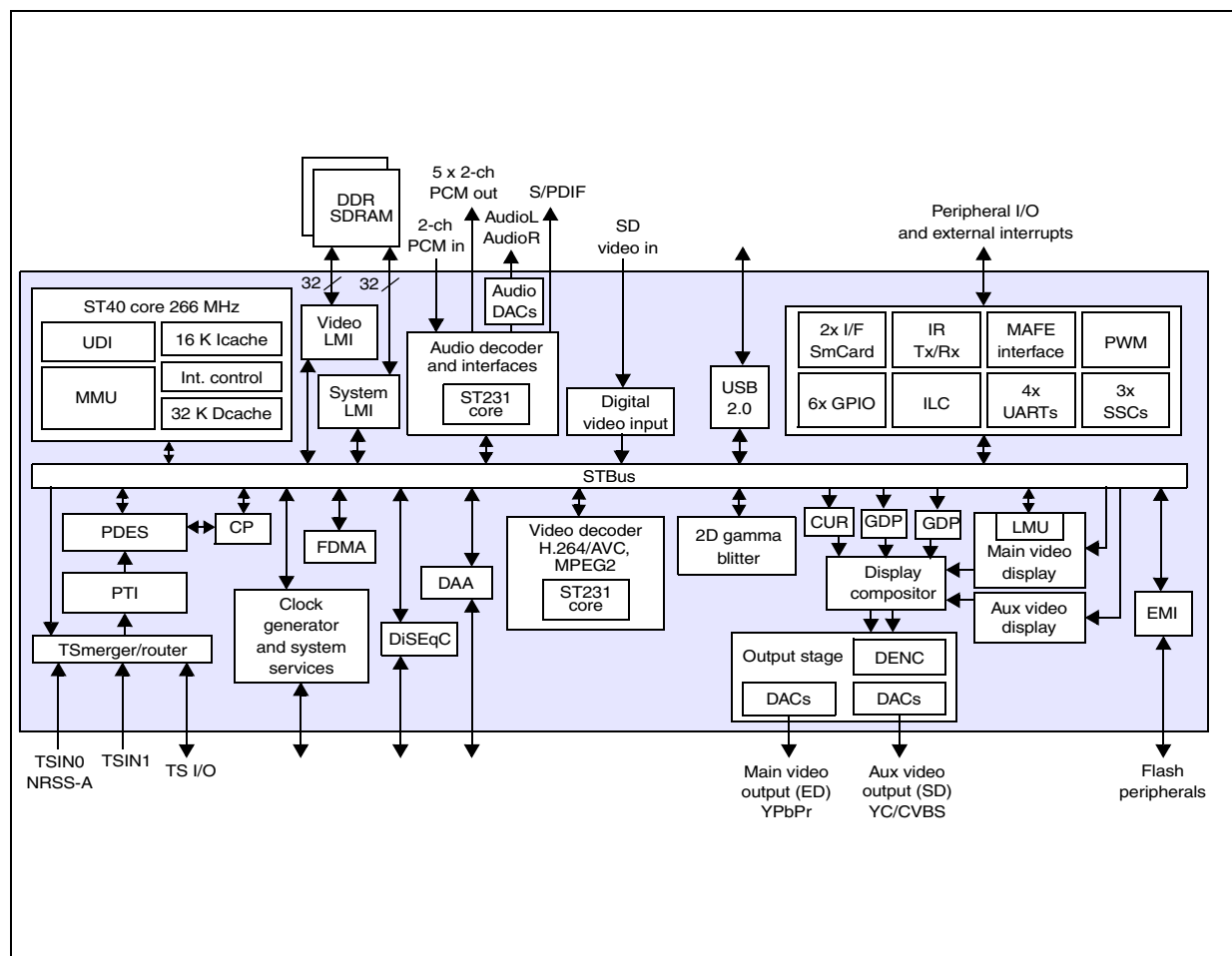


Low-cost SDTV set-top box decoder for H.264/AVC and MPEG-2

Data Brief

Features

- The STi5200 is a single-chip, standard-definition STB decoder including:
 - ST40 CPU core, 266 MHz
 - dual ST231 CPU cores for audio and video decoding, both 400 MHz
 - transport filtering and descrambling
 - video decoder: H.264/AVC and MPEG-2
- graphics engine and dual display: enhanced definition ED (480p/576p) and standard definition SD (480i/576i)
- audio decoder
- The STi5200 also features the following embedded interfaces:
 - USB 2.0
 - digital audio and video auxiliary input
 - modem



1 Description

The STi5200 is a new generation, standard-definition set-top box decoder chip, which provides very high performance for low-cost systems. With enhanced performance over the STi7710, it includes an H.264/AVC decoder for new low-bitrate applications, and dual-decode MPEG-2 capability.

Based on the Omega2 (STBus) architecture, this system on chip is a full back-end processing solution for digital terrestrial, satellite and cable standard-definition set-top boxes compliant with ATSC, DVB, DIRECTV, DCII, OpenCable and ARIB BS4 specifications.

The STi5200 demultiplexes, decrypts and decodes SD video streams with associated multichannel audio. Video is output to two independently formatted displays: a full resolution display intended for a TV monitor, and a downsampled display intended for a VCR. Connection to a TV or display panel is through an analog component interface. Composite outputs are provided for connection to the VCR with Macrovision protection. Audio is output with optional PCM mixing to an S/PDIF interface, PCM interface or through integrated stereo audio DACs.

Digitized analog programs can also be input to the STi5200 for reformatting and display.

The STi5200 can render and display graphics, and has a 2D graphics accelerator, two graphics planes and a cursor plane. A dual display compositor provides mixing of graphics and video with independent composition for each of the TV and VCR outputs.

The STi5200 includes a stream merger to allow five different transport streams from different sources to be merged and processed concurrently. Applications include DVR time shifted viewing of a terrestrial program while acquiring an EPG/data stream from a satellite or cable front end.

The flexible descrambling engine is compatible with required standards including DVB, DES, AES and Multi2.

2 Applications

The STi5200 has an embedded 266 MHz ST40 CPU for applications and device control. DDR1 SDRAM memory is used for higher performance, to allow the video decoder the required memory bandwidth for H.264 decoding and sufficient bandwidth for the CPU and the rest of the system. A second memory bus is provided for flash memory storing resident software and for connecting peripherals.

A hard-disk drive (HDD) can be connected as an expansion drive using the USB 2.0 port. The USB port can also be used to connect to a DOCSIS 2.0 CM gateway for interactive cable applications.

The STi5200 is supported by STMicroelectronics' STAPI software.

Figure 1. Low-cost satellite SD set-top box

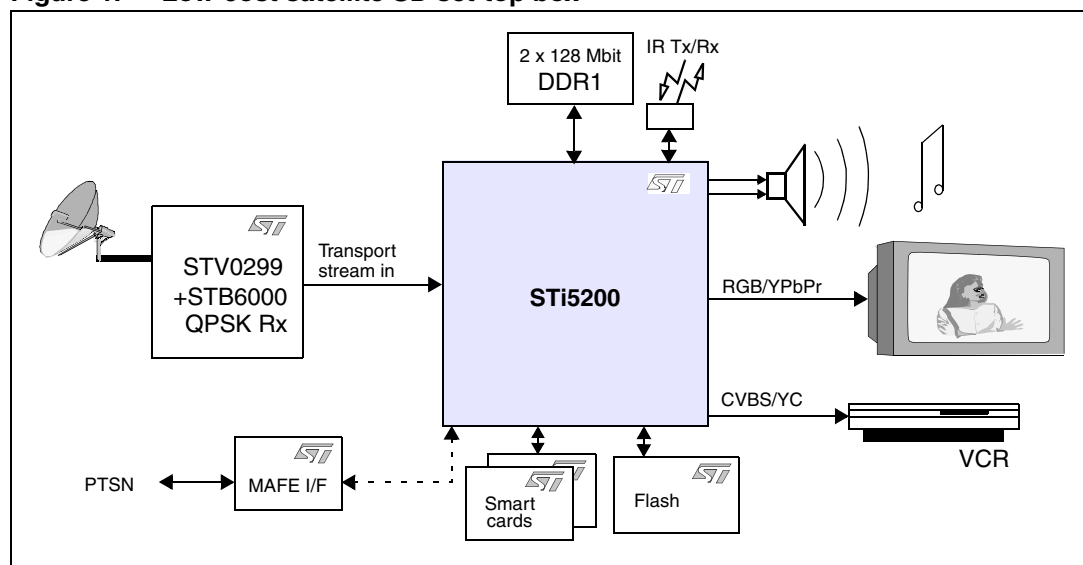


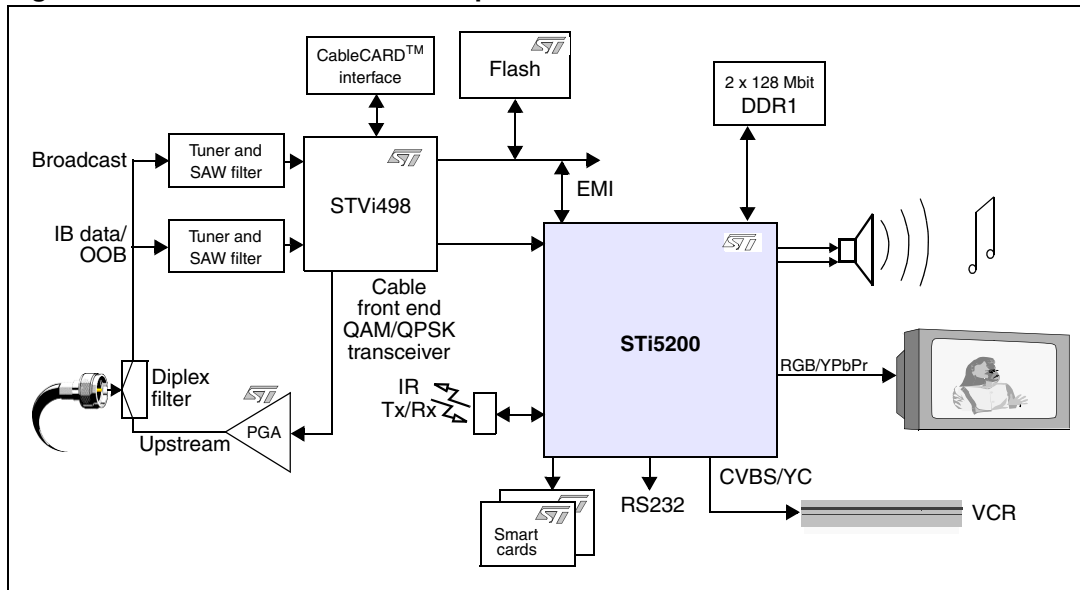
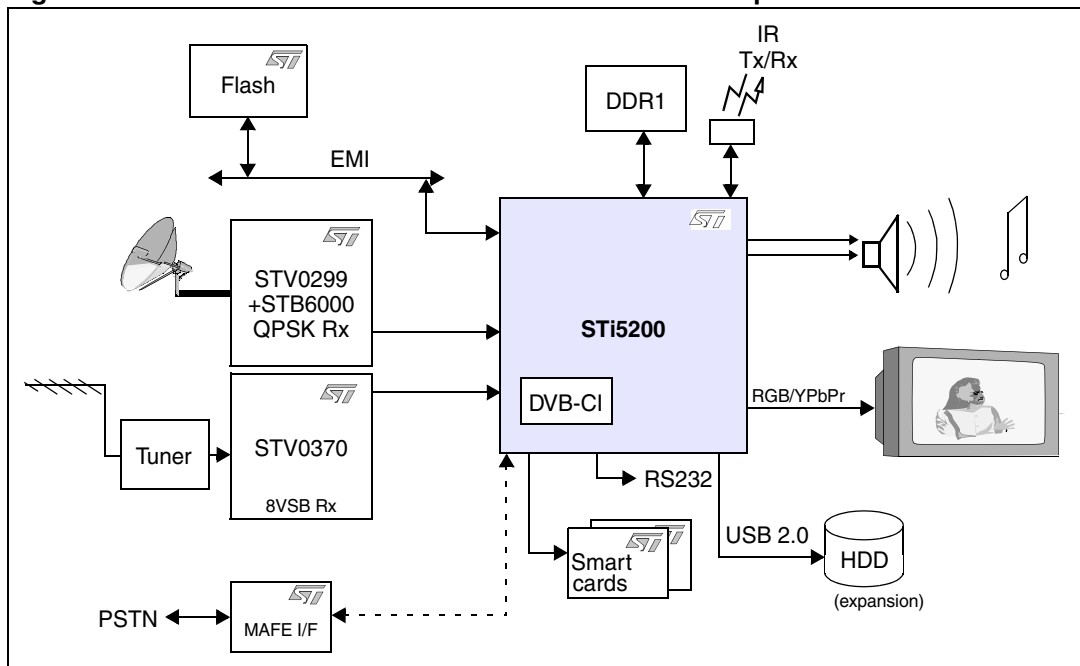
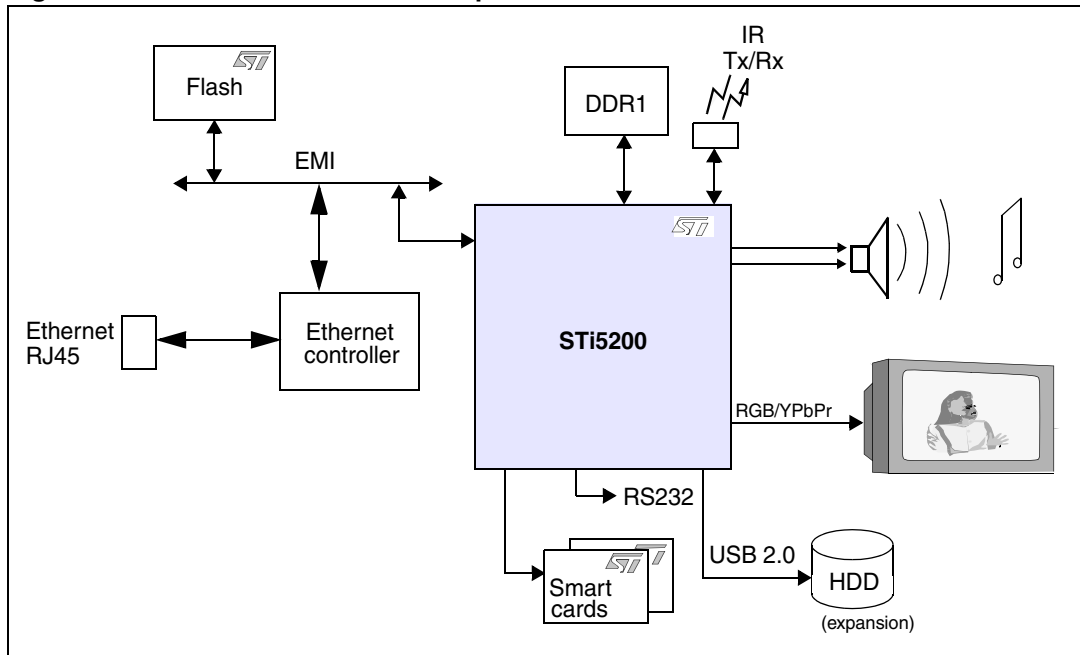
Figure 2. Low-cost cable SD set-top box with return channel**Figure 3. Low-cost dual satellite and terrestrial SD set-top box with HDD**

Figure 4. Low-cost SD IP-TV set-top box with HDD

3 Revision history

Table 1. Document revision history

Date	Revision	Changes
16-Feb-2007	1	Initial release.

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