Ordering number: EN 3889B

CMOS LSI

SANYO

No. 3889B

LC7152, 7152M, 7152NM, 7152KM

Universal Dual-PLL Frequency Synthesizers

Overview

The LC7152, 7152M, 7152NM, 7152KM are universal dual-PLL frequency synthesizers for use in cordless telephone applications in the USA, South Korea and Japan, and broadcast satellite (BS) tuners in the USA and Europe.

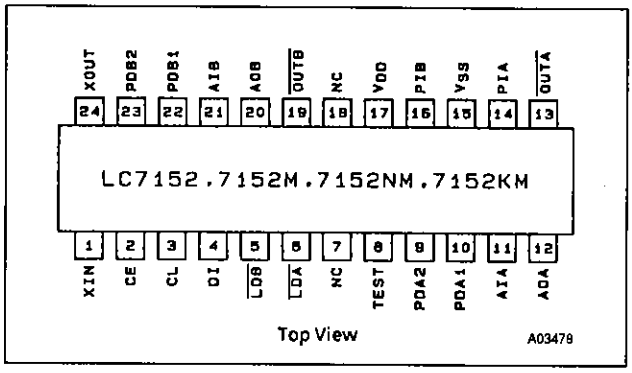
Features

- Dual charge pump for fast channel switching
- Digital lock detector for PLL lock status check with crystal oscillator precision
- Programmable reference frequency divider ideal for various applications
- LC7152NM with built-in power-on reset circuit version of the LC7152M
- LC7152KM with enhanced frequency characteristics version of the LC7152M

Functions

- 2-system PLL built-in (dual PLL)
- 16-bit programmable local-oscillator divider 1.5 to 55MHz (V_{DD} = 2.0 to 3.3V), LC7152KM: 55 to 80MHz (V_{DD} = 2.7 to 3.3V)
- 14-bit programmable reference-frequency divider
- 320Hz to 640kHz reference frequency using a 10.24MHz crystal
- Digital lock detector
- Dual charge pump
- Amplifier built-in for an active LPF
- Serial transmission data input (CCB format)
- LC7152NM with power-on reset circuit (outputs $\overline{\text{OUTA}}$ and $\overline{\text{OUTB}}$ become open at power-on)
- 2.0 to 3.3V supply
- DIP24S and MFP24S packages

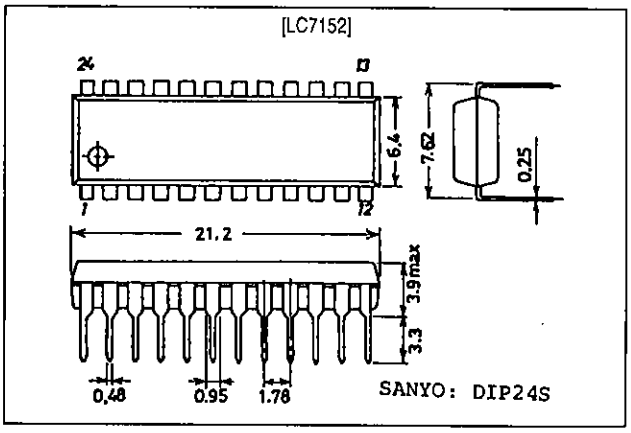
Pin Assignment



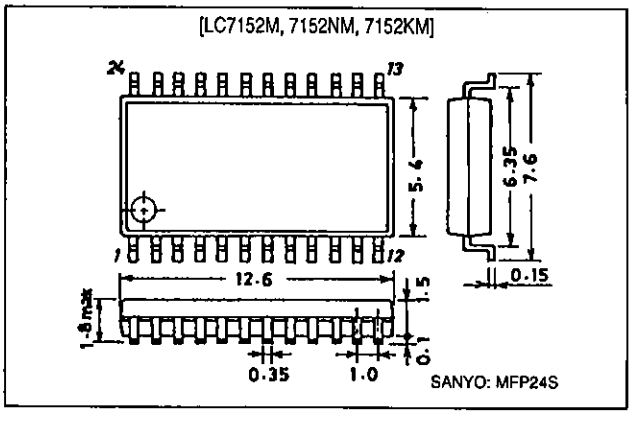
Package Dimensions

Unit: mm

3067-DIP24S

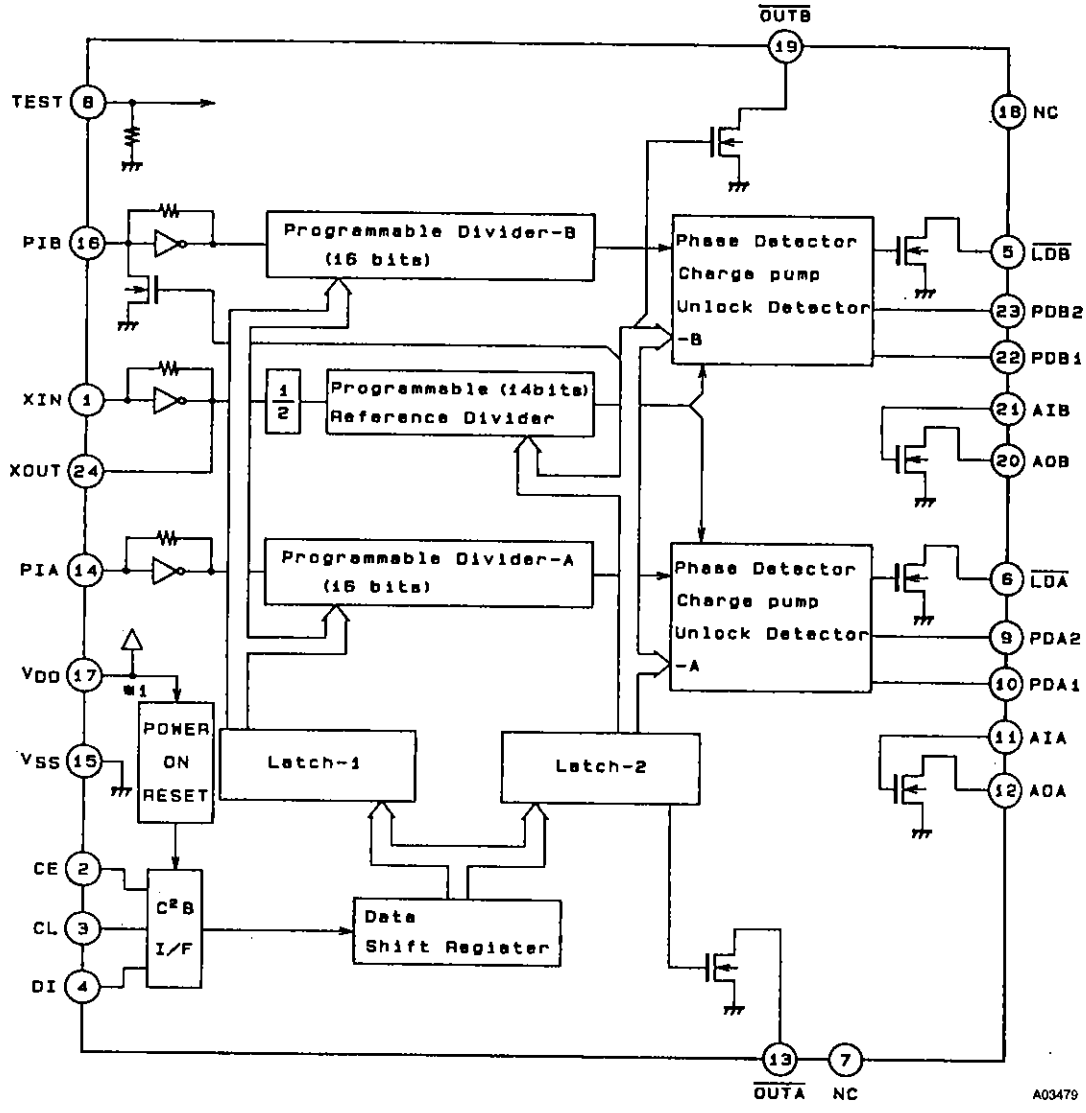


3112-MFP24S



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Block Diagram



*1. LC7152NM only

Pin Functions

Number	Name	Function
1	XIN	Crystal oscillator input
2	CE	Chip enable input
3	CL	Clock input
4	DI	Serial data input
5	$\overline{\text{LDB}}$	PLL-B unlock detector output
6	$\overline{\text{LDA}}$	PLL-A unlock detector output
7	NC	No connection
8	TEST	Test input
9	PDA2	PLL-A phase detector secondary output
10	PDA1	PLL-A phase detector main output
11	AIA	LPF transistor A input
12	AOA	LPF transistor A output

Number	Name	Function
13	$\overline{OUTA}$	General-purpose output port
14	PIA	PLL-A local-oscillator input
15	V_{SS}	Ground
16	PIB	PLL-B local-oscillator input
17	V_{DD}	3V supply
18	NC	No connection
19	$\overline{OUTB}$	General-purpose output port
20	AOB	LPF transistor B output
21	AIB	LPF transistor B input
22	PDB1	PLL-B phase detector main output
23	PDB2	PLL-B phase detector secondary output
24	XOUT	Crystal oscillator output

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
Maximum input voltage	V_{IN} max(1)	CE, CL, DI, AIA, AIB	–0.3 to +7.0	V
	V_{IN} max(2)	XIN, PIA, PIB, TEST	–0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_O max(1)	$\overline{LDA}$, $\overline{LDB}$	–0.3 to +7.0	V
	V_O max(2)	AOA, AOB, $\overline{OUTA}$, $\overline{OUTB}$	–0.3 to +15	V
	V_O max(3)	PDA1, PDA2, PDB1, PDB2, XOUT	–0.3 to V_{DD} + 0.3	V
Maximum output current	I_O max(1)	$\overline{LDA}$, $\overline{LDB}$, $\overline{OUTA}$, $\overline{OUTB}$	0 to +3	mA
	I_O max(2)	AOA, AOB	0 to +6	mA
Allowable power dissipation	Pd max	Ta ≤ 85°C, LC7152	350	mW
		Ta ≤ 85°C, LC7152M, 7152NM, 7152KM	160	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}(1)	V_{DD}	2.0	–	3.3	V
	V_{DD}(2)	V_{DD}: Serial data retention voltage, see Figure 4[1]	1.5	–	–	V
	V_{DD}(3)	V_{DD}: Power-on reset voltage, $t_R \geq 20ms$[1]	–	–	0.05	V
Input high-level voltage	V_{IH}(1)	CE, CL, DI: V_{DD} = 2.0V, (Note that V_{IH} can exceed V_{DD})	1.5	–	5.5	V
	V_{IH}(2)	CE, CL, DI: V_{DD} = 3.3V, (Note that V_{IH} can exceed V_{DD})	1.7	–	5.5	V
Input low-level voltage	V_{IL}(1)	CE, CL, DI: V_{DD} = 2.0V	0	–	0.4	V
	V_{IL}(2)	CE, CL, DI: V_{DD} = 3.3V	0	–	0.6	V
Output voltage	V_O(1)	$\overline{LDA}$, $\overline{LDB}$	0	–	5.5	V
	V_O(2)	AOA, AOB, $\overline{OUTA}$, $\overline{OUTB}$	0	–	13	V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input frequency	$f_{IN}(1)$	XIN: Sine wave, capacitively coupled	1.0	–	13	MHz
	$f_{IN}(2)$	PIA, PIB: Sine wave, capacitively coupled[2]	1.5	–	55	MHz
	$f_{IN}(3)$	PIA, PIB: Sine wave, capacitively coupled[3]	55	–	80	MHz
Input amplitude	$V_{IN}(1)$	XIN: Sine wave, capacitively coupled	200	–	600	mVrms
	$V_{IN}(2)$	PIA, PIB: Sine wave, capacitively coupled[2,3]	100	–	600	mVrms
Crystal oscillator frequency	$f_{X'tal}$	XIN, XOUT: CI ≤ 50Ω, C_L ≤ 16pF[4]	4	10.24	11	MHz

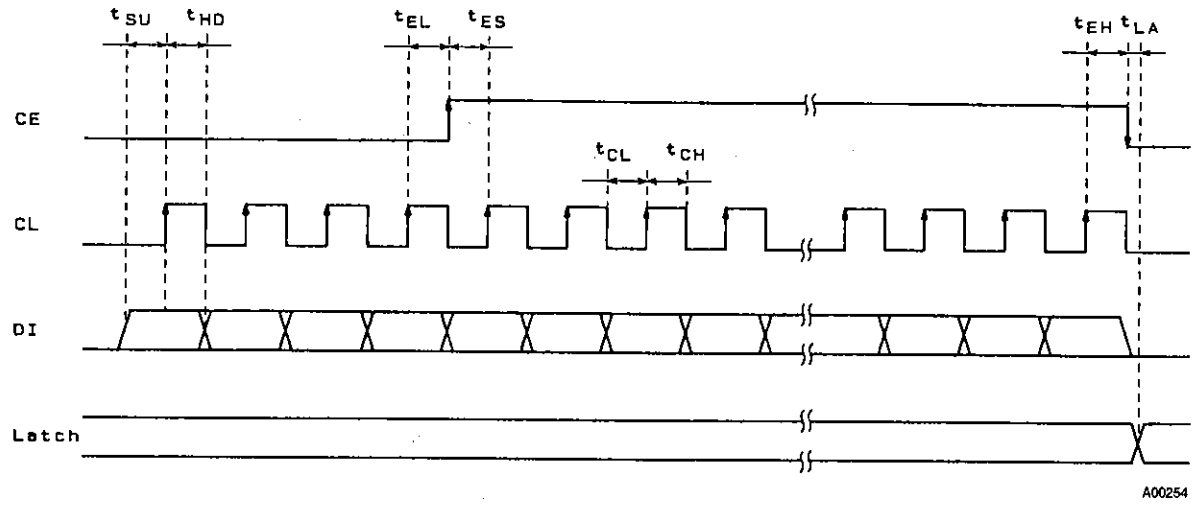
1. LC7152NM
2. 1.5 to 23MHz when FA/FB = 0, 20 to 55MHz when FA/FB = 1, V_{DD} = 2.0 to 3.3V, LC7152, 7152M, 7152NM, 7152KM. FA and FB are serial data input frequency select bits.
3. 55 to 80MHz when FA/FB = 1, V_{DD} = 2.7 to 3.3V, LC7152KM. FA and FB are serial data input frequency select bits.
4. CI is the crystal impedance and C_L is the load capacitance.

Electrical Characteristics within the allowable operating ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Output high-level voltage	$V_{OH}(1)$	PDA1, PDB1: I_O = 1mA	V_{DD} – 1.0	–	–	V
	$V_{OH}(2)$	PDA2, PDB2: I_O = 2mA	V_{DD} – 1.0	–	–	V
Output low-level voltage	$V_{OL}(1)$	PDA1, PDB1: I_O = 1mA	–	–	1.0	V
	$V_{OL}(2)$	PDA2, PDB2: I_O = 2mA	–	–	1.0	V
	$V_{OL}(3)$	$\overline{OUTA}$, $\overline{OUTB}$: I_O = 1mA	–	–	1.0	V
	$V_{OL}(4)$	$\overline{LDA}$, $\overline{LDB}$: I_O = 2mA	–	–	1.0	V
	$V_{OL}(5)$	AOA, AOB: I_O = 0.5mA, AIA = AIB = 1.2V	–	–	0.5	V
	$V_{OL}(6)$	AOA, AOB: I_O = 1mA, AIA = AIB = 1.3V	–	–	0.5	V
Output leakage current	$I_{OFF}(1)$	$\overline{LDA}$, $\overline{LDB}$: V_O = 5.5V	–	–	5.0	µA
	$I_{OFF}(2)$	PDA1, PDB1, PDA2, PDB2: V_O = 0/3.3V	–	0.01	10.0	nA
	$I_{OFF}(3)$	AOA, AOB, $\overline{OUTA}$, $\overline{OUTB}$: V_O = 13V	–	–	5.0	µA
Input high-level current	$I_{IH}(1)$	CE, CL, DI: V_I = 5.5V	–	–	5.0	µA
	$I_{IH}(2)$	XIN: V_I = 3.3V, V_{DD} = 3.3V	2.0	–	6.5	µA
	$I_{IH}(3)$	PIA, PIB: V_I = 3.3V, V_{DD} = 3.3V	3.5	–	10.0	µA
	$I_{IH}(4)$	AIA, AIB: V_I = 3.3V	–	0.01	10.0	nA
	$I_{IH}(5)$	TEST: V_I = 3.3V, V_{DD} = 3.3V	–	120	–	µA
Input low-level current	$I_{IL}(1)$	CE, CL, DI: V_I = 0V	–	–	5.0	µA
	$I_{IL}(2)$	XIN: V_I = 0V, V_{DD} = 3.3V	2.0	–	6.5	µA
	$I_{IL}(3)$	PIA, PIB: V_I = 0V, V_{DD} = 3.3V	3.5	–	10.0	µA
	$I_{IL}(4)$	AIA, AIB: V_I = 0V	–	0.01	10.0	nA
	$I_{IL}(5)$	TEST: V_I = 0V, V_{DD} = 3.3V	–	–	5.0	µA
Internal feedback resistance	$R_f(1)$	XIN: V_{DD} = 3.3V	–	1.0	–	MΩ
	$R_f(2)$	PIA, PIB: V_{DD} = 3.3V	–	600	–	kΩ
Internal pull-down resistance	Rd	TEST: V_{DD} = 3.3V	–	30	–	kΩ
Input capacitance	C_{IN}	XIN, PIA, PIB	–	2.5	–	pF
Supply current[1]	$I_{DD}(1)$	V_{DD} (= 2.0V): f_{IN} = 55MHz	–	3.0	8.0	mA
	$I_{DD}(2)$	V_{DD} (= 3.3V): f_{IN} = 55MHz	–	7.0	14.0	mA
Supply current[2]	$I_{DD}(4)$	V_{DD} (= 2.0V): f_{IN} = 55MHz	–	1.5	4.5	mA
	$I_{DD}(5)$	V_{DD} (= 3.3V): f_{IN} = 55MHz	–	3.9	8.0	mA

1. Dual PLL operation (both PLL-A and PLL-B), SB = 0, f_{XIN} = 10.24MHz (crystal), PIA and PIB input = 100mVrms at f_{IN}, all other inputs at V_{SS}, all other outputs open.
2. Standby mode: Single PLL operation (PLL-A operating and PLL-B stopped), SB = 1, f_{XIN} = 10.24MHz (crystal), PIA input = 100mVrms at f_{IN}, all other inputs at V_{SS}, all other outputs open.

Serial Data Input Timing



Parameter	Symbol	Conditions	min	max	Unit
Data setup time	t_{SU}	10.24MHz crystal	0.40	–	μs
		Other crystal frequencies	$4/f_{X'tal}$	–	–
Data hold time	t_{HD}	10.24MHz crystal	0.40	–	μs
		Other crystal frequencies	$4/f_{X'tal}$	–	–
Enable low-level pulse width	t_{EL}	10.24MHz crystal	0.40	–	μs
		Other crystal frequencies	$4/f_{X'tal}$	–	–
Enable setup time	t_{ES}	10.24MHz crystal	0.40	–	μs
		Other crystal frequencies	$4/f_{X'tal}$	–	–
Enable hold time	t_{EH}	10.24MHz crystal	0.40	–	μs
		Other crystal frequencies	$4/f_{X'tal}$	–	–
Clock low-level pulse width	t_{CL}	10.24MHz crystal	0.40	–	μs
		Other crystal frequencies	$4/f_{X'tal}$	–	–
Clock high-level pulse width	t_{CH}	10.24MHz crystal	0.40	–	μs
		Other crystal frequencies	$4/f_{X'tal}$	–	–
Latch propagation delay	t_{LA}	10.24MHz crystal	–	0.40	μs
		Other crystal frequencies	–	$4/f_{X'tal}$	–

Note. Data transfer occurs after the crystal oscillations normalize. Data transferred before oscillations normalize will not be recognized.

Functional Description

PLL-A and PLL-B Programmable Dividers

PLL-A and PLL-B input frequency ranges are set by Mode 2 command bits FA and FB, respectively. Their divider ratios, N_A and N_B, are set by Mode 1 command bits DA0 to DA15 and DB0 to DB15, respectively.

Programmable Reference Divider

The divider ratio, N_R, is set by Mode 2 command bits R0 to R13. The reference frequency is given by $f_{XIN}/(2 \times N_R)$.

Phase Detector

The phase detector output state as a function of the divider ratio and reference frequency is shown in Table 1.

Table 1. Phase detector output states

Condition[1]	PDA1, PDB1
$f_{osc}/N > f_{ref}$ (leading)	High
$f_{osc}/N < f_{ref}$ (lagging)	Low
$f_{osc}/N = f_{ref}$ (coincident)	High impedance

1. $N = N_A$ for PLL-A, and N_B for PLL-B

When PLL-A is unlocked, $\overline{LDA}$ is pulled low and both PDA1 and PDA2 are active. PLL-B operates identically to PLL-A. Mode 2 command bits UL0 and UL1 set the unlock phase-error threshold, and bits UE0 and UE1, the $\overline{LDA}$ and $\overline{LDB}$ output extension.

Dual Charge Pump

A typical dual charge pump configuration is shown in Figure 1. The phase detector secondary output is active after a change in frequency, and the phase error causes the PLL to unlock. In this case, the load resistance R1 becomes R1M||R1S, decreasing the LPF time constant and the time required to lock the PLL.

The phase detector secondary output is high impedance when the PLL is locked. In this case, R1 becomes R1M, increasing the LPF time constant and improving sideband and modulation response.

Test Mode

TEST is normally held low. However, when TEST is high and test bits T0 to T2 are set to 0, the signal on $\overline{OUTA}$ has a frequency of $f_{Xtal}/2$, allowing the crystal oscillator frequency to be monitored.

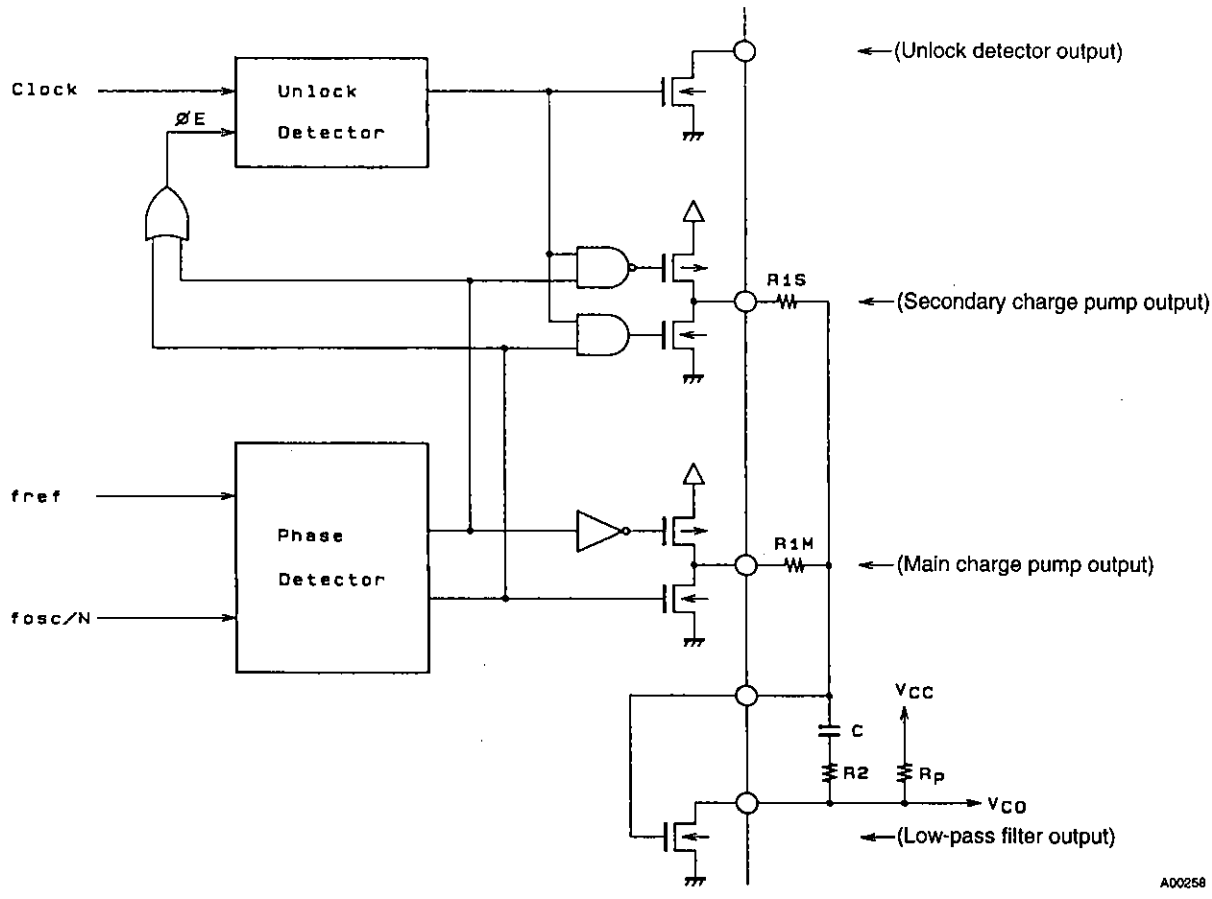


Figure 1. Dual charge pump circuit

Serial Input Data

Serial data should be input only after f_{Xtal} has become stable.

Mode 1 command format and functions

The Mode 1 command comprises the data bits which determine the PLL-A and PLL-B programmable divider ratios. The command format is shown in Figure 2. Bits DA0 to DA15 and bits DB0 to DB15 determine the PLL-A and PLL-B programmable divider ratios, respectively. Bit DA0 is the first bit received. The range of allowable divider ratios is N = 272 (0110H) to 65535 (FFFFH).

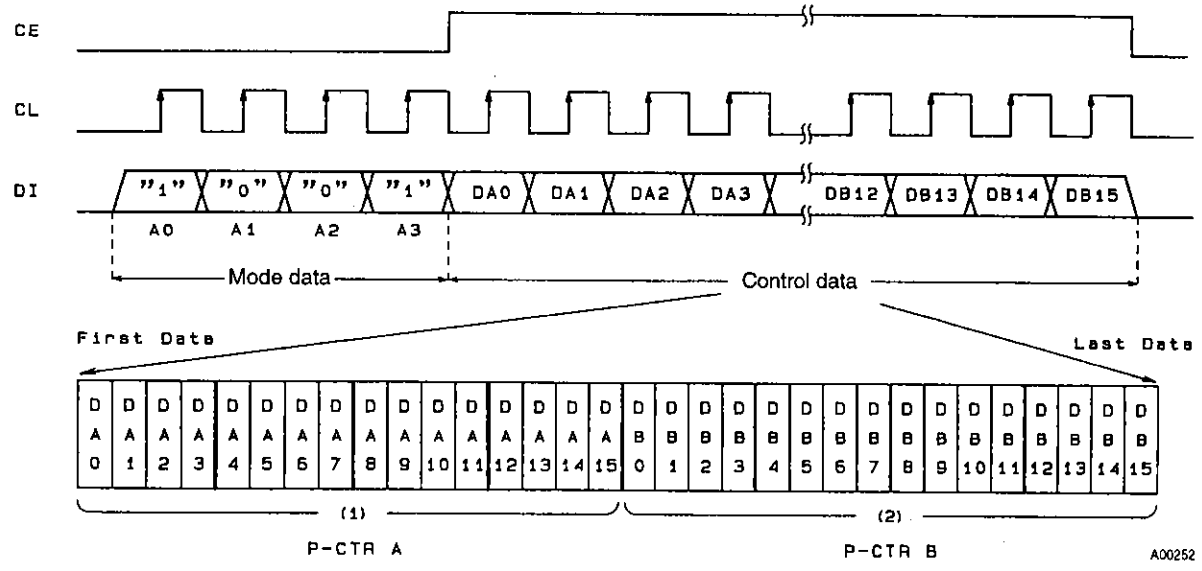


Figure 2. Mode 1 command (programmable divider data)

Mode 2 command format and functions

The Mode 2 command comprises the data bits which determine the reference frequency divider ratio and control functions. The command format is shown in Figure 3. Bit R0 is the first bit received.

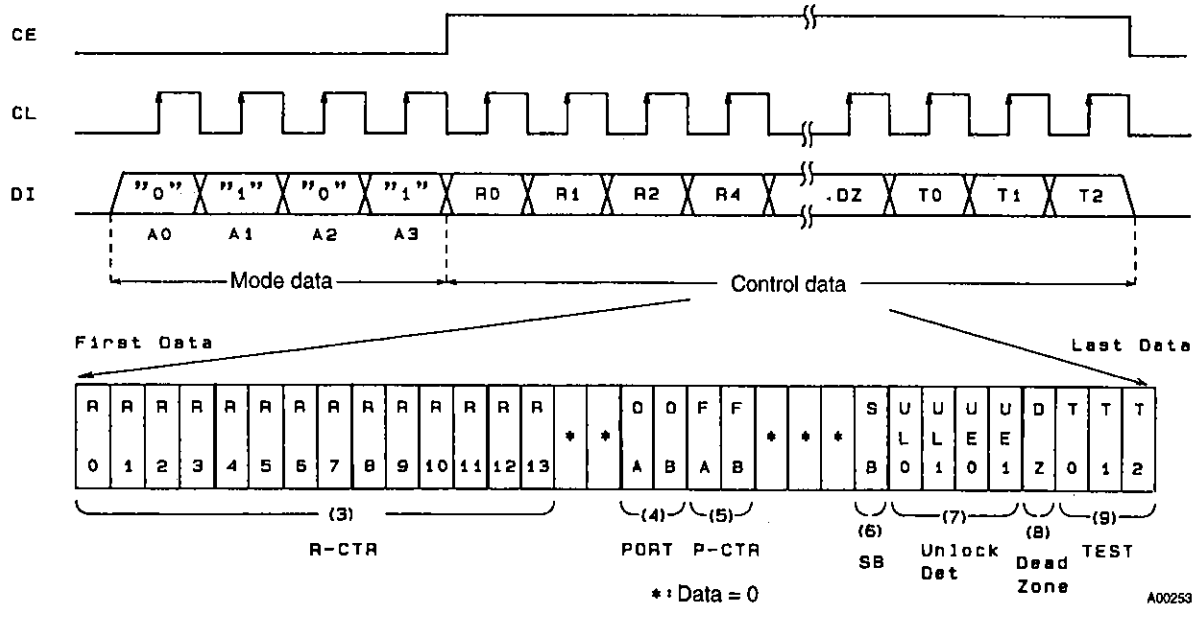


Figure 3. Mode 2 command (reference divider and control data)

Bits R0 to R13 determine the reference frequency ratio. The range of allowable divider ratios is N_R = 8 (0008H) to 16383 (3FFFH).

Bits OA and OB are the general-purpose output port control bits. They are latched and then inverted to control $\overline{OUTA}$ and $\overline{OUTB}$, respectively. If either bit is 1, the open-drain output is pulled low.

Bits FA and FB are the input frequency range select bits. The PIA and PIB frequency ranges, set by FA and FB, respectively, are shown in Table 2.

Table 2. Frequency ranges

FA (FB)	Input frequency range	Supply	Device
0	1.5 to 23.0MHz	2.0 to 3.3V	LC7152, 7152M LC7152NM, 7152KM
1	20 to 55MHz		
	55 to 80MHz	2.7 to 3.3V	LC7152KM

Bit SB is the standby mode control bit. When SB = 1, standby mode is selected. In standby mode, PLL-B is stopped, PIB is pulled low, and PDB1, PDB2 and $\overline{LDB}$ are high impedance. When SB = 0, normal operation is selected.

Bits UL0 and UL1 determine the unlock detection threshold. The PLL unlock detector output, $\overline{LDA}$ or $\overline{LDB}$, is pulled low when the phase differential between the reference and the divider inputs exceeds the threshold set by UL0 and UL1. The threshold for different crystal frequencies is shown in Table 3, from which the threshold for other frequencies can be calculated. The threshold is common to both PLLs. Note that a PLL will temporarily lose lock when either UL0 or UL1 is changed.

Table 3. Unlock detector thresholds

UL0	UL1	$\overline{LDA}$, $\overline{LDB}$ phase error threshold	Example phase error thresholds (μs)				
			f_{XIN} = 4MHz	f_{XIN} = 7.2MHz	f_{XIN} = 8MHz	f_{XIN} = 10.24MHz	f_{XIN} = 12.8MHz
0	0	0	0	0	0	0	0
1	0	$\pm 4/f_{XIN}$	±1.00	±0.55	±0.50	±0.39	±0.31
0	1	$\pm 16/f_{XIN}$	±4.00	±2.22	±2.00	±1.56	±1.20
1	1	$\pm 64/f_{XIN}$	±16.00	±8.88	±8.00	±6.25	±5.00

Bits UE0 and UE1 determine the unlock extension, or delay, before the unlock detector outputs, $\overline{LDA}$ and $\overline{LDB}$, can change state. The extension for different reference frequencies is shown in Table 4. However, if a phase error threshold of zero is set using UL0 and UL1, no output extension occurs.

Table 4. $\overline{LDA}$ and $\overline{LDB}$ output extension

UL0	UL1	$\overline{LDA}$, $\overline{LDB}$ output extension	Example output extensions (ms)		
			f_{ref} = 1kHz	f_{ref} = 5kHz	f_{ref} = 12.5kHz
0	0	$4/f_{ref}$	4.0[1]	0.8	0.32
1	0	$8/f_{ref}$	8.0	1.6	0.64
0	1	$32/f_{ref}$	32.0	6.4[1]	2.56
1	1	$64/f_{ref}$	64.0	12.8	5.12[1]

1. Typical value

Bit DZ is the dead-zone selection bit. It selects the phase-insensitive bandwidth, or dead zone, of the phase comparator. When DZ = 1, DZB mode is selected, and when DZ = 0, DZA mode. DZB mode has a larger dead zone than DZA mode.

Bits D0 to D2 are test bits. They should be set to for normal operation.

Power-on Reset (LC7152NM Only)

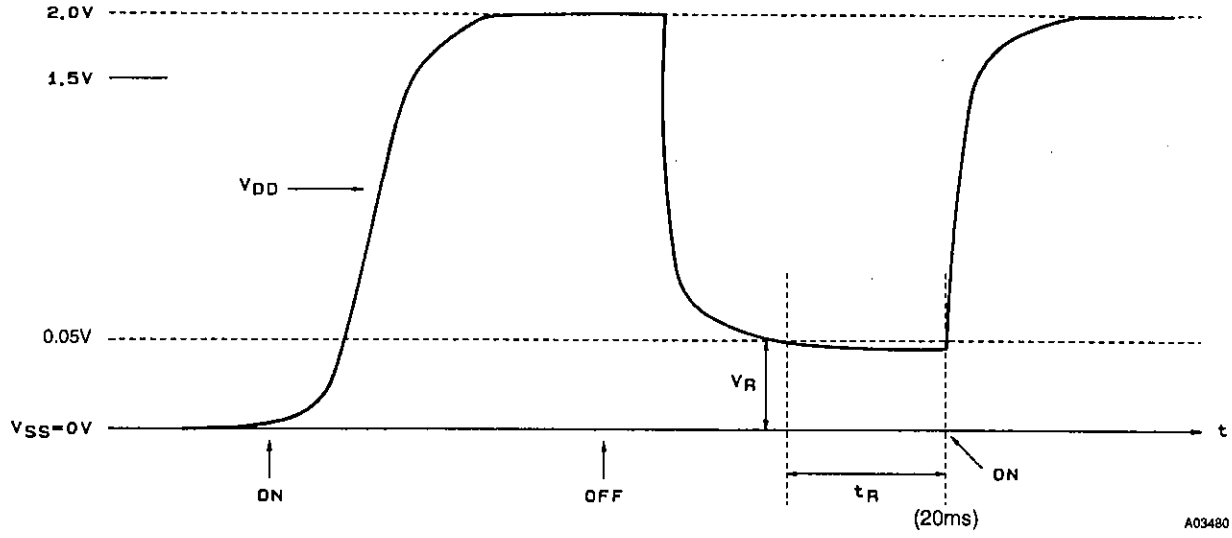


Figure 4. Power-on reset supply voltage

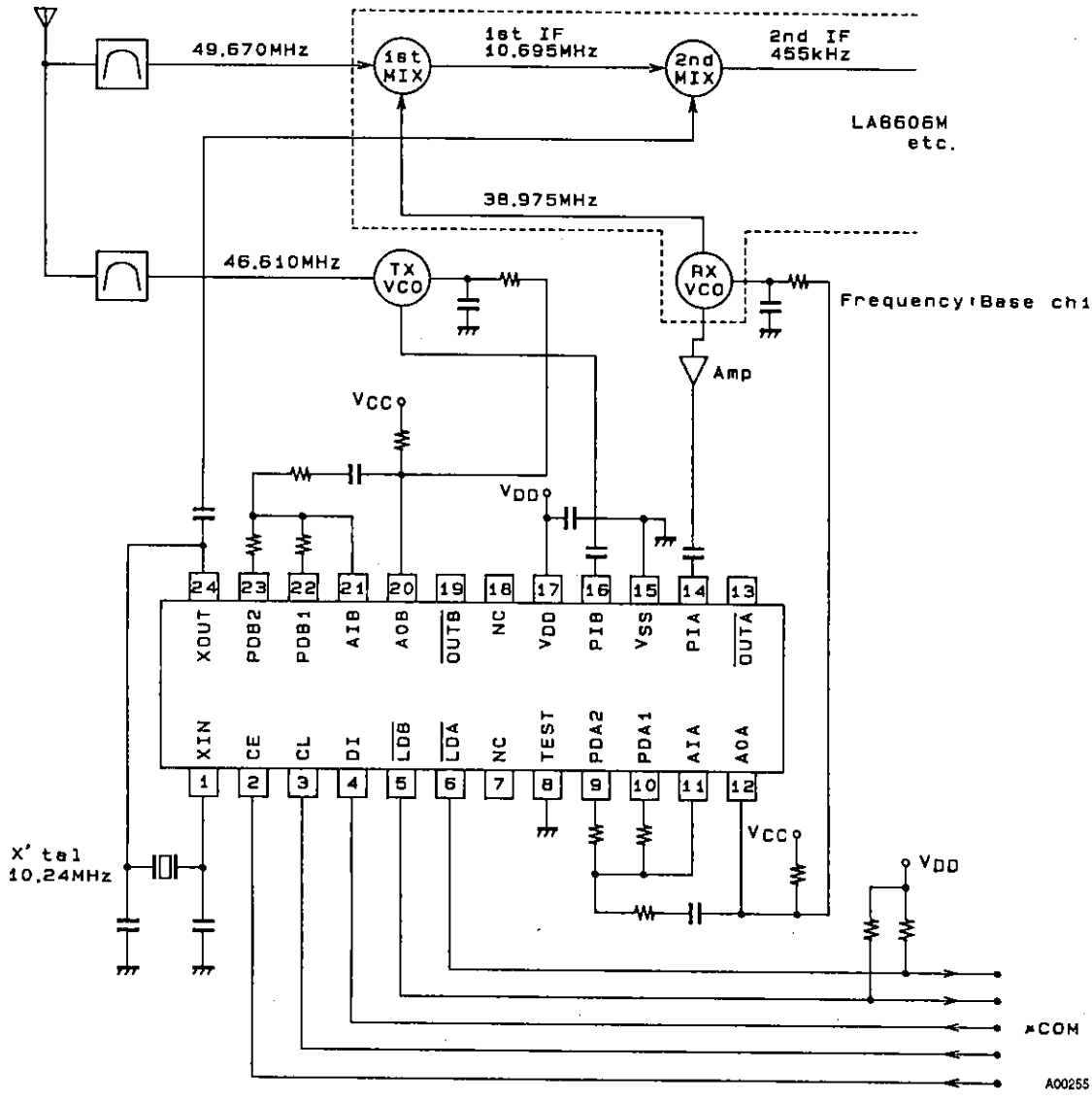
A power-on reset takes place when the supply voltage, V_{DD}, falls to a value $V_R \leq 0.05V$ for a period of $t_R \geq 20ms$ prior to rising to a value of 2.0V or greater, as shown in Figure 4. At supply voltages above 1.5V, the latch data is retained (and a power-on reset is not required).

Power-on reset serial data state

At power-on reset state, bits OA and OB are set to 0, which set $\overline{OUTA}$ and $\overline{OUTB}$ open circuit, and bit SB is set to 1.

Typical Application

A LC7152, 7152M, 7152NM, 7152KM cordless telephone application circuit is shown in Figure 5. The telephone is tuned to channel 1, which has a transmit VCO frequency of 46.610MHz and a receive VCO frequency of 38.975MHz.



NR-18 10.24 MHz crystal, C_L = 16pF/CI < 20Ω made by Nihon Dempa Kogyo Co., Ltd.

Figure 5. American 10-channel 46/49MHz cordless telephone base station

For f_{ref} = 5kHz, the divider ratios are as follows:

$$N_A = \frac{f_{VCO\text{-}A}}{f_{ref}} = \frac{\text{RX VCO}}{f_{ref}} = \frac{38.975\text{MHz}}{5\text{kHz}} = 7795\ (1E73H)$$

$$N_B = \frac{f_{VCO\text{-}B}}{f_{ref}} = \frac{\text{TX VCO}}{f_{ref}} = \frac{46.610\text{MHz}}{5\text{kHz}} = 9322\ (246AH)$$

$$N_R = \frac{f_{Xtal}}{f_{ref}} \div 2 = \frac{10.24\text{MHz}}{5\text{kHz}} \div 2 = 1024\ (400H)$$

The Mode 1 and Mode 2 commands are shown in Tables 5 and 6, respectively, and in Figures 6 and 7, respectively.

Table 5. Mode 1 command

Field	Value	Comment
DA0 to DA15	1E73H	PLL-A divider ratio of 7795
DB0 to DB15	246A	PLL-B divider ratio of 9322

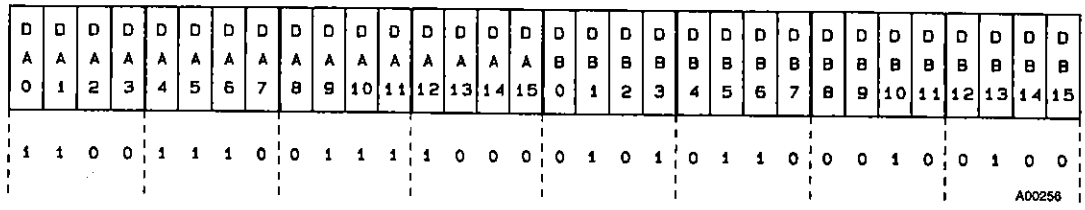


Figure 6. Mode 1: Latch 1 data

Table 6. Mode 2 command

Field	Value	Comment
R0 to R13	0400H	Reference divider ratio of 1024
OA	0	$\overline{OUTA}$ and $\overline{OUTB}$ left open.
OB	0	
FA	1	20 to 55MHz RX VCO input frequency range
FB	1	20 to 55MHz TX VCO input frequency range
SB	0 or 1	Standby mode selection
UL0, UL1	11	±6.25µs lock/unlock detection threshold
UE0, EU1	01	6.4ms $\overline{LDA}$ and $\overline{LDB}$ output extension
DZ	1	DZB dead-zone mode
T0 to T2	000	Test mode deselected

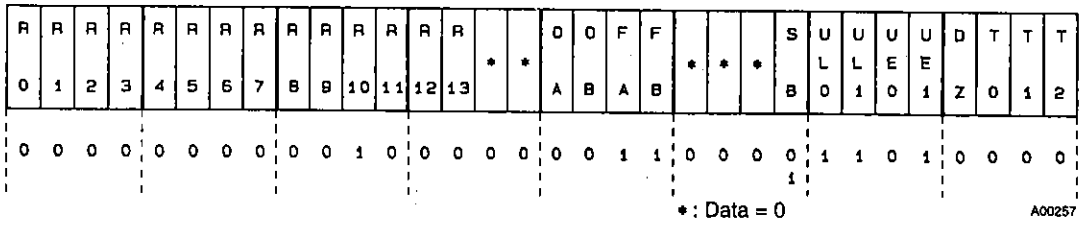


Figure 7. Mode 2: Latch 2 data

Device Comparison

Device	Operating frequency			Power-on reset circuit	Package
	FA/FB = 0	FA/FB = 1			
	1.5 to 23MHz	20 to 55MHz	55 to 80MHz		
LC7152	Yes	Yes	No	No	DIP24S
LC7152M	Yes	Yes	No	No	MFP24S
LC7152NM	Yes	Yes	No	Yes	MFP24S
LC7152KM	Yes	Yes	Yes (V_{DD} = 2.7 to 3.3V)	No	MFP24S

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