

Low-Charge Injection, 16-Channel, High-Voltage Analog Switch

Features

- High-Voltage CMOS technology for high performance
- 16-channel high voltage analog switch
- 3.3V input logic level compatible
- 20 MHz data shift clock frequency
- Very low quiescent power dissipation ($\sim 10 \mu\text{A}$)
- Low parasitic capacitance
- DC to 50 MHz small signal frequency response
- -60dB typical OFF-isolation at 5.0 MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Cascadable serial data register with latches
- Flexible operating supply voltages
- Integrated bleed resistors on the outputs (HV2701 only)

Applications

- Medical ultrasound imaging
- NDT metal flaw detection
- Piezoelectric transducer drivers
- Optical MEMS modules

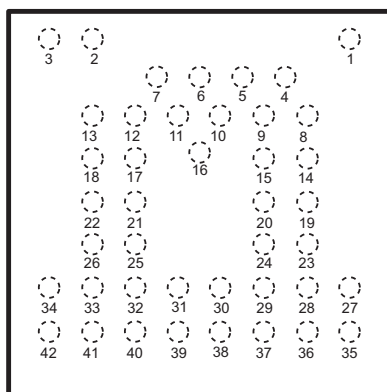
Description

HV2601/HV2701 are low-charge injection, 16-channel, high-voltage analog switch integrated circuits (ICs). These devices are designed for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging and other piezoelectric transducer drivers. HV2701 has integrated bleed resistors which eliminate voltage build-up on capacitive loads such as piezoelectric transducers.

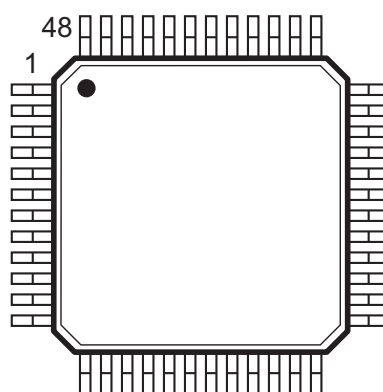
These ICs shift input data into a 16-bit shift register that can then be retained in a 16-bit latch. To reduce any possible clock feed-through noise, the latch enable bar should be left high until all bits are clocked in. Data is clocked in during the rising edge of the clock. Using High-Voltage CMOS technology, this device combines high-voltage, bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : $+40\text{V}/-160\text{V}$, $+100\text{V}/-100\text{V}$, and $+160\text{V}/-40\text{V}$.

Package Types



**42-Ball Bumped Die
(Top View)**

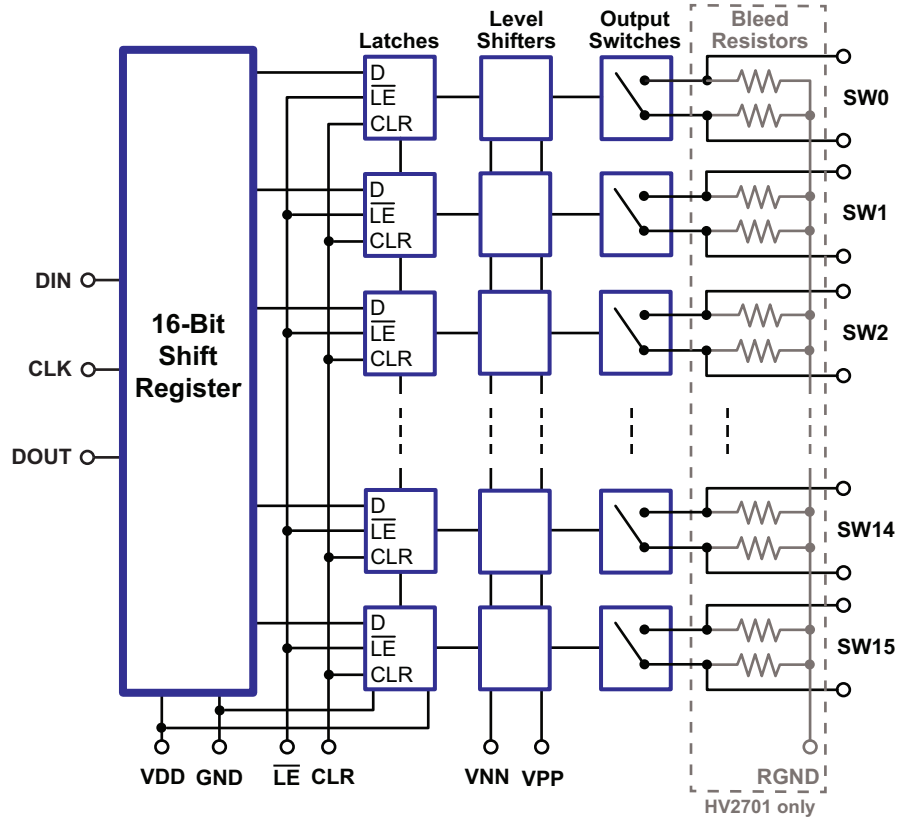


**48-Lead LQFP
(Top View)**

See [Table 2-1](#) and [Table 2-2](#) for pin information

HV2601 / HV2701

Block Diagram



Note: Bleed resistors and RGND apply to HV2701 only.

1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

V_{DD} logic supply	-0.5V to +7.0V
$V_{PP} - V_{NN}$ differential supply	220V
V_{PP} positive supply	-0.5V to $V_{NN} + 200V$
V_{NN} negative supply	+0.5V to -200V
Logic input voltage	-0.5V to $V_{DD} + 0.3V$
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation 42-Ball Bumped Die	1.5W
Power dissipation 48-Lead LQFP	1.0W

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Notes 1 – 3)

Symbol	Parameter	Value
V_{DD}	Logic power supply voltage	3.0V to 5.5V
V_{PP}	Positive high voltage supply	+40V to $V_{NN} + 200V$
V_{NN}	Negative high voltage supply	-40V to -160V
V_{IH}	High level input voltage	$0.9V_{DD}$ to V_{DD}
V_{IL}	Low level input voltage	0V to $0.1 V_{DD}$
V_{SIG}	Analog signal voltage peak-to-peak	$V_{NN} + 10V$ to $V_{PP} - 10V$
T_A	Operating free air temperature	0°C to 70°C

Note 1: Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.

2: V_{SIG} must be V_{NN} and V_{PP} or floating during power up/down transition.

3: Rise and fall times of power supplies V_{DD} , V_{PP} , and V_{NN} should not be less than 1.0msec.

HV2601 / HV2701

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise noted.

Parameter	Symbol	0°C		25°C			70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
Small signal switch ON-resistance	R_{ONS}	-	30	-	26	38	-	48	Ω	$I_{SIG} = 5.0 \text{ mA}$ $V_{PP} = +40V$
		-	25	-	22	27	-	32		$I_{SIG} = 200 \text{ mA}$ $V_{NN} = -160V$
		-	25	-	22	27	-	30		$I_{SIG} = 5.0 \text{ mA}$ $V_{PP} = +100V$
		-	18	-	18	24	-	27		$I_{SIG} = 200 \text{ mA}$ $V_{NN} = -100V$
		-	23	-	20	25	-	30		$I_{SIG} = 5.0 \text{ mA}$ $V_{PP} = +160V$
		-	22	-	16	25	-	27		$I_{SIG} = 200 \text{ mA}$ $V_{NN} = -40V$
Small signal switch ON-resistance matching	ΔR_{ONS}	-	20	-	5.0	20	-	20	%	$I_{SIG} = 5.0 \text{ mA}$, $V_{PP} = +100V$, $V_{NN} = -100V$
Large signal switch ON-resistance	R_{ONL}	-	-	-	15	-	-	-	Ω	$V_{SIG} = V_{PP} - 10V$, $I_{SIG} = 1.0A$
Value of output bleed resistor (HV2701 only)	R_{INT}	-	-	20	35	50	-	-	k Ω	Output Switch to R_{GND} $I_{RINT} = 0.5 \text{ mA}$
Switch OFF leakage per switch	I_{SOL}	-	5.0	-	1.0	10	-	15	μA	$V_{SIG} = V_{PP} - 10V$ and $V_{NN} + 10V$ (Note 1)
DC offset switch OFF	V_{OS}	-	300	-	100	300	-	300	mV	HV2601: 100 k Ω load HV2701: no load (Note 1)
DC offset switch ON		-	500	-	100	500	-	500	mV	
Quiescent V_{PP} supply current	I_{PPQ}	-	-	-	10	50	-	-	μA	All switches OFF
Quiescent V_{NN} supply current	I_{NNQ}	-	-	-	-10	-50	-	-	μA	All switches OFF
Quiescent V_{PP} supply current	I_{PPQ}	-	-	-	10	50	-	-	μA	All switches ON, $I_{SW} = 5.0 \text{ mA}$
Quiescent V_{NN} supply current	I_{NNQ}	-	-	-	-10	-50	-	-	μA	All switches ON, $I_{SW} = 5.0 \text{ mA}$
Switch output peak current	I_{SW}	-	3.0	-	3.0	2.0	-	2.0	A	V_{SIG} duty cycle < 0.1%
Output switching frequency	f_{SW}	-	-	-	-	50	-	-	kHz	Duty cycle = 50%
Average V_{PP} supply current	I_{PP}	-	6.5	-	-	7.0	-	8.0	mA	$V_{PP} = +40V$ $V_{NN} = -160V$
		-	4.0	-	-	5.5	-	5.5		$V_{PP} = +100V$ $V_{NN} = -100V$
		-	4.0	-	-	5.0	-	5.5		$V_{PP} = +160V$ $V_{NN} = -40V$
Average V_{NN} supply current	I_{NN}	-	6.5	-	-	7.0	-	8.0	mA	$V_{PP} = +40V$ $V_{NN} = -160V$
		-	4.0	-	-	5.0	-	5.5		$V_{PP} = +100V$ $V_{NN} = -100V$
		-	4.0	-	-	5.0	-	5.5		$V_{PP} = +160V$ $V_{NN} = -40V$
Average V_{DD} supply current	I_{DD}	-	4.0	-	-	4.0	-	4.0	mA	$f_{CLK} = 5.0 \text{ MHz}$, $V_{DD} = 5.0V$

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Over recommended operating conditions unless otherwise noted.

Parameter	Symbol	0°C		25°C			70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
Quiescent V_{DD} supply current	I_{DDQ}	-	10	-	-	10	-	10	μA	All logic inputs are static
Data out source current	I_{SOR}	0.45	-	0.45	0.70	-	0.40	-	mA	$V_{OUT} = V_{DD} - 0.7V$
Data out sink current	I_{SINK}	0.45	-	0.45	0.70	-	0.40	-	mA	$V_{OUT} = 0.7V$
Logic input capacitance	C_{IN}	-	10	-	-	10	-	10	pF	—

Note 1: See [Figure 3-1](#).

HV2601 / HV2701

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_{DD}=5.0V$, $t_R = t_F \leq 5.0$ ns, 50% duty cycle, $C_{LOAD} = 20$ pF, unless otherwise noted.										
Parameter	Symbol	0°C		25°C			70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
Set up time before $\overline{LE}$ rises	t_{SD}	25	-	25	-	-	25	-	ns	—
Time width of $\overline{LE}$	t_{WLE}	56	-	-	56	-	56	-	ns	$V_{DD} = 3.0V$
		12	-	-	12	-	12	-		$V_{DD} = 5.0V$
Clock delay time to data out	t_{DO}	50	100	50	78	100	50	100	ns	$V_{DD} = 3.0V$
		15	40	15	30	40	15	40		$V_{DD} = 5.0V$
Time width of CLR	t_{WCLR}	55	-	55	-	-	55	-	ns	—
Set up time data to clock	t_{SU}	21	-	-	21	-	21	-	ns	$V_{DD} = 3.0V$
		7.0	-	-	7.0	-	7.0	-		$V_{DD} = 5.0V$
Hold time data from clock	t_H	2.0	-	2.0	-	-	2.0	-	ns	$V_{DD} = 3.0$ or $5.0V$
Clock frequency	f_{CLK}	-	8.0	-	-	8.0	-	8.0	MHz	$V_{DD} = 3.0V$
		-	20	-	-	20	-	20		$V_{DD} = 5.0V$
Clock rise and fall times	t_R, t_F	-	50	-	-	50	-	50	ns	—
Turn ON time	T_{ON}	-	5.0	-	-	5.0	-	5.0	μs	$V_{SIG} = V_{PP}-10V$, $R_{LOAD} = 10k\Omega$ (Note 1)
Turn OFF time	T_{OFF}	-	5.0	-	-	5.0	-	5.0	μs	$V_{SIG} = V_{PP}-10V$, $R_{LOAD} = 10k\Omega$ (Note 1)
Maximum V_{SIG} slew rate	dv/dt	-	20	-	-	20	-	20	v/ns	$V_{PP} = +40V$, $V_{NN} = -160V$
		-	20	-	-	20	-	20		$V_{PP} = +100V$, $V_{NN} = -100V$
		-	20	-	-	20	-	20		$V_{PP} = +160V$, $V_{NN} = -40V$
OFF isolation	K_O	-30	-	-30	-33	-	-30	-	dB	$f = 5.0MHz$, $1.0k\Omega/15pF$ load (Note 1)
		-58	-	-58	-	-	-58	-		$f = 5.0MHz$, 50Ω load (Note 1)
Switch crosstalk	K_{CR}	-60	-	-60	-70	-	-60	-	dB	$f = 5.0MHz$, 50Ω load (Note 1)
Output switch isolation diode current	I_{ID}	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle (Note 1)
OFF capacitance SW to GND	$C_{SG(OFF)}$	5.0	17	5.0	12	17	5.0	17	pF	0V, $f = 1.0MHz$
ON capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, $f = 1.0MHz$
Output voltage spike	$+V_{SPK}$	-	-	-	-	150	-	-	mV	$V_{PP} = +40V$, $V_{NN} = -160V$, $R_{LOAD} = 50\Omega$ (Note 1)
	$-V_{SPK}$	-	-	-	-	150	-	-		$V_{PP} = +100V$, $V_{NN} = -100V$, $R_{LOAD} = 50\Omega$ (Note 1)
	$+V_{SPK}$	-	-	-	-	150	-	-		$V_{PP} = +160V$, $V_{NN} = -40V$, $R_{LOAD} = 50\Omega$ (Note 1)
	$-V_{SPK}$	-	-	-	-	150	-	-		$V_{PP} = +160V$, $V_{NN} = -40V$, $R_{LOAD} = 50\Omega$ (Note 1)
	$+V_{SPK}$	-	-	-	-	150	-	-		$V_{PP} = +160V$, $V_{NN} = -40V$, $R_{LOAD} = 50\Omega$ (Note 1)
	$-V_{SPK}$	-	-	-	-	150	-	-		$V_{PP} = +160V$, $V_{NN} = -40V$, $R_{LOAD} = 50\Omega$ (Note 1)
Charge injection	QC	-	-	-	820	-	-	-	pC	$V_{PP} = +40V$, $V_{NN} = -160V$, $V_{SIG} = 0V$ (Note 1)
		-	-	-	600	-	-	-		$V_{PP} = +100V$, $V_{NN} = -100V$, $V_{SIG} = 0V$ (Note 1)
		-	-	-	350	-	-	-		$V_{PP} = +160V$, $V_{NN} = -40V$, $V_{SIG} = 0V$ (Note 1)

Note 1: See Figure 3-1.

2.0 PIN DESCRIPTION

The locations of the pads/balls are listed in [Package Types](#).

TABLE 2-1: PIN DESCRIPTION: 42-BALL BUMPED DIE PACKAGE

Pin #	HV2601	HV2701	Description
1	NC	RGND	No connect/Ground for bleed resistor
2	V _{PP}	V _{PP}	Positive supply voltage
3	V _{NN}	V _{NN}	Negative supply voltage
4	D _{OUT}	D _{OUT}	Data out logic output
5	CLR	CLR	Latch clear logic input
6	CLK	CLK	Clock logic input for shift register
7	GND	GND	Ground
8	SW15A	SW15A	Analog switch 15 terminal A
9	SW15B	SW15B	Analog switch 15 terminal B
10	$\overline{\text{LE}}$	$\overline{\text{LE}}$	Latch-enable logic input, low active
11	V _{DD}	V _{DD}	Logic supply voltage
12	SW0A	SW0A	Analog switch 0 terminal A
13	SW0B	SW0B	Analog switch 0 terminal B
14	SW14A	SW14A	Analog switch 14 terminal A
15	SW14B	SW14B	Analog switch 14 terminal B
16	D _{IN}	D _{IN}	Data in logic input
17	SW1A	SW1A	Analog switch 1 terminal A
18	SW1B	SW1B	Analog switch 1 terminal B
19	SW13A	SW13A	Analog switch 13 terminal A
20	SW13B	SW13B	Analog switch 13 terminal B
21	SW2A	SW2A	Analog switch 2 terminal A
22	SW2B	SW2B	Analog switch 2 terminal B
23	SW12A	SW12A	Analog switch 12 terminal A
24	SW12B	SW12B	Analog switch 12 terminal B
25	SW3A	SW3A	Analog switch 3 terminal A
26	SW3B	SW3B	Analog switch 3 terminal B
27	SW11A	SW11A	Analog switch 11 terminal A
28	SW11B	SW11B	Analog switch 11 terminal B
29	SW9B	SW9B	Analog switch 9 terminal B
30	SW8B	SW8B	Analog switch 8 terminal B
31	SW7A	SW7A	Analog switch 7 terminal A
32	SW6A	SW6A	Analog switch 6 terminal A
33	SW4A	SW4A	Analog switch 4 terminal A
34	SW4B	SW4B	Analog switch 4 terminal B
35	SW10B	SW10B	Analog switch 10 terminal B
36	SW10A	SW10A	Analog switch 10 terminal A
37	SW9A	SW9A	Analog switch 9 terminal A
38	SW8A	SW8A	Analog switch 8 terminal A
39	SW7B	SW7B	Analog switch 7 terminal B
40	SW6B	SW6B	Analog switch 6 terminal B
41	SW5B	SW5B	Analog switch 5 terminal B
42	SW5A	SW5A	Analog switch 5 terminal A

HV2601 / HV2701

TABLE 2-2: PIN DESCRIPTION: 48-LEAD LQFP

Pin #	HV2601	HV2701	Description
1	NC	NC	No connect
2	NC	NC	No connect
3	SW4B	SW4B	Analog switch 4 terminal B
4	SW4A	SW4A	Analog switch 4 terminal A
5	SW3B	SW3B	Analog switch 3 terminal B
6	SW3A	SW3A	Analog switch 3 terminal A
7	SW2B	SW2B	Analog switch 2 terminal B
8	SW2A	SW2A	Analog switch 2 terminal A
9	SW1B	SW1B	Analog switch 1 terminal B
10	SW1A	SW1A	Analog switch 1 terminal A
11	SW0B	SW0B	Analog switch 0 terminal B
12	SW0A	SW0A	Analog switch 0 terminal A
13	V _{NN}	V _{NN}	Negative supply voltage
14	NC	NC	No connect
15	V _{PP}	V _{PP}	Positive supply voltage
16	NC	NC	No connect
17	GND	GND	Ground
18	V _{DD}	V _{DD}	Logic supply voltage
19	D _{IN}	D _{IN}	Data in logic input
20	CLK	CLK	Clock logic input for shift register
21	$\overline{\text{LE}}$	$\overline{\text{LE}}$	Latch-enable logic input, low active
22	CLR	CLR	Latch clear logic input
23	D _{OUT}	D _{OUT}	Data out logic output
24	NC	RGND	No connect/Ground for bleed resistor
25	SW15B	SW15B	Analog switch 15 terminal B
26	SW15A	SW15A	Analog switch 15 terminal A
27	SW14B	SW14B	Analog switch 14 terminal B
28	SW14A	SW14A	Analog switch 14 terminal A
29	SW13B	SW13B	Analog switch 13 terminal B
30	SW13A	SW13A	Analog switch 13 terminal A
31	SW12B	SW12B	Analog switch 12 terminal B
32	SW12A	SW12A	Analog switch 12 terminal A
33	SW11B	SW11B	Analog switch 11 terminal B
34	SW11A	SW11A	Analog switch 11 terminal A
35	NC	NC	No connect
36	NC	NC	No connect
37	SW10B	SW10B	Analog switch 10 terminal B
38	SW10A	SW10A	Analog switch 10 terminal A
39	SW9B	SW9B	Analog switch 9 terminal B
40	SW9A	SW9A	Analog switch 9 terminal A
41	SW8B	SW8B	Analog switch 8 terminal B
42	SW8A	SW8A	Analog switch 8 terminal A
43	SW7B	SW7B	Analog switch 7 terminal B

TABLE 2-2: PIN DESCRIPTION: 48-LEAD LQFP

Pin #	HV2601	HV2701	Description
44	SW7A	SW7A	Analog switch 7 terminal A
45	SW6B	SW6B	Analog switch 6 terminal B
46	SW6A	SW6A	Analog switch 6 terminal A
47	SW5B	SW5B	Analog switch 5 terminal B
48	SW5A	SW5A	Analog switch 5 terminal A

3.0 DETAILED DESCRIPTION

3.1 Application Information

FIGURE 3-1: TEST CIRCUITS

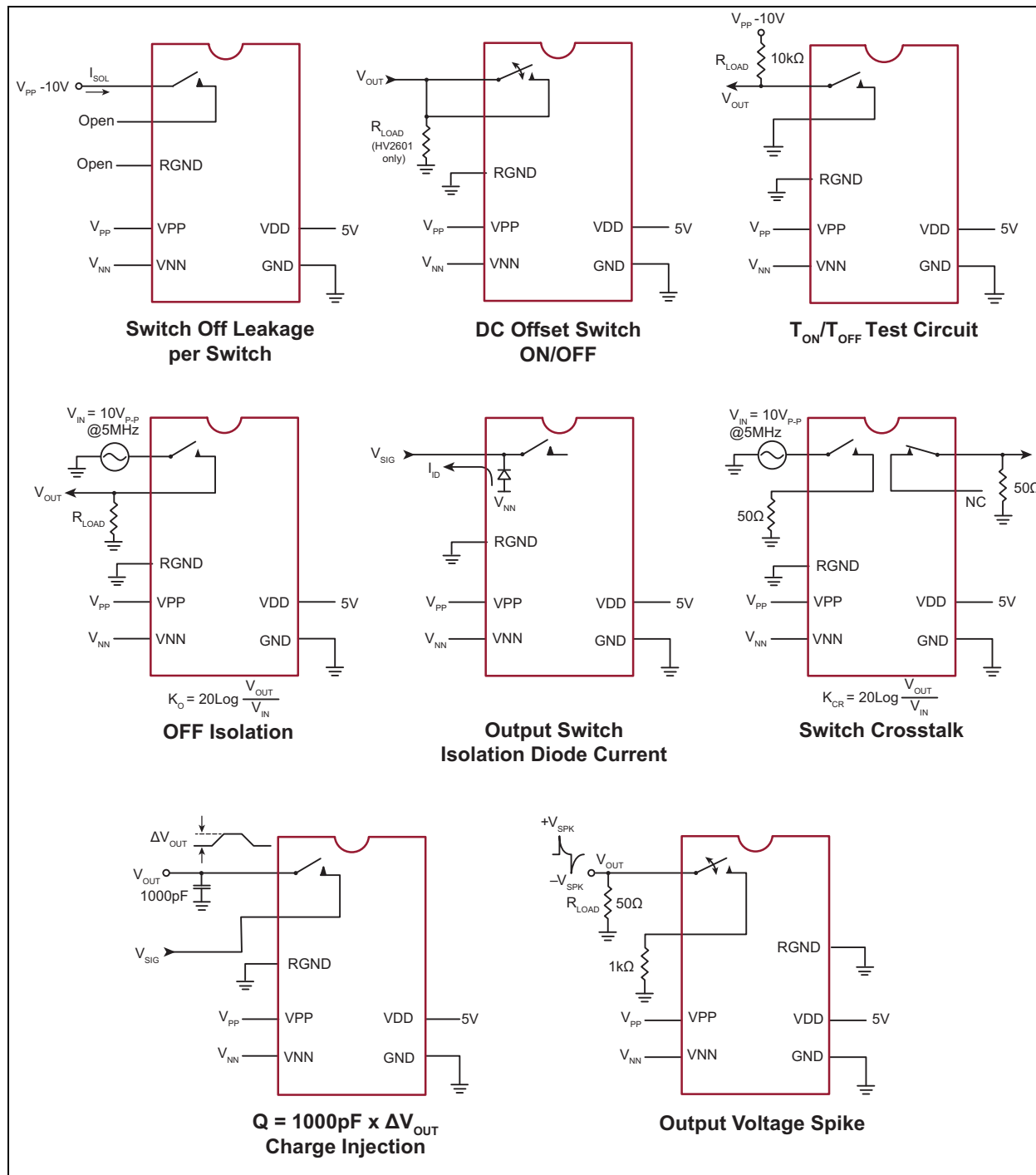


TABLE 3-1: LOGIC FUNCTION TABLE

D0	D1	...	D7	D8	...	D15	LE	CLR	SW0	SW1	...	SW7	SW8	...	SW15
L	-		-	-		-	L	L	OFF	-		-	-		-
H	-		-	-		-	L	L	ON	-		-	-		-
-	L		-	-		-	L	L	-	OFF		-	-		-
-	H		-	-		-	L	L	-	ON		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		L	-		-	L	L	-	-		OFF	-		-
-	-		H	-		-	L	L	-	-		ON	-		-
-	-	...	-	L	...	-	L	L	-	-	...	-	OFF	...	-
-	-		-	H		-	L	L	-	-		-	ON		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		L	L	L	-	-		-	-		OFF
-	-		-	-		H	L	L	-	-		-	-		ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Note 1: The 16 switches operate independently.

2: Serial data is clocked in on the L to H transition of the CLK.

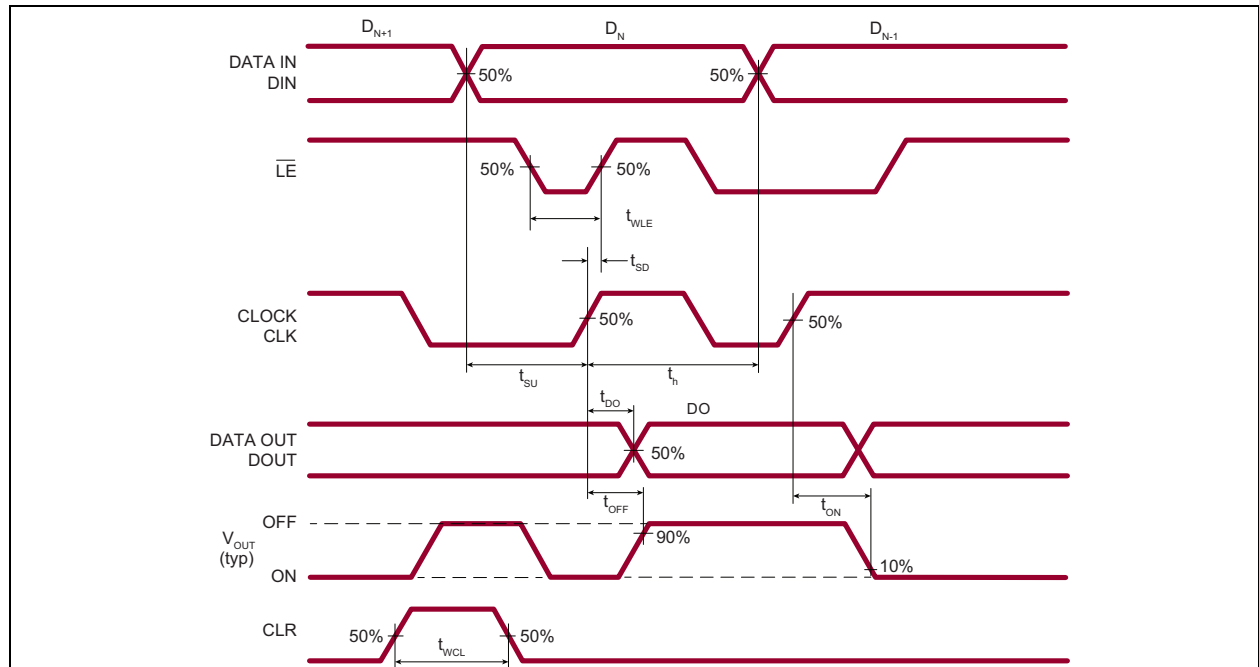
3: All 16 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift registers data flow through the latch.

4: D_{OUT} is high when data in the shift register 15 is high.

5: Shift registers clocking has no effect on the switch states if $\overline{LE}$ is high.

6: The CLR clear input overrides all other inputs.

FIGURE 3-2: LOGIC TIMING WAVEFORMS

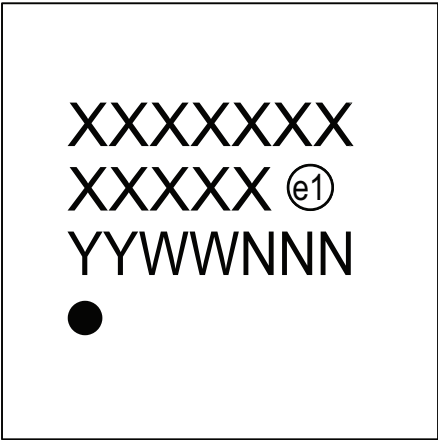


HV2601 / HV2701

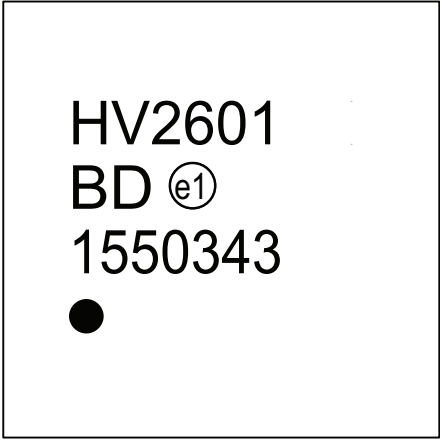
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

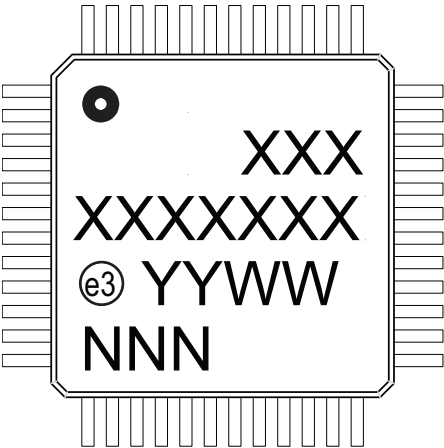
42-ball Bumped Die



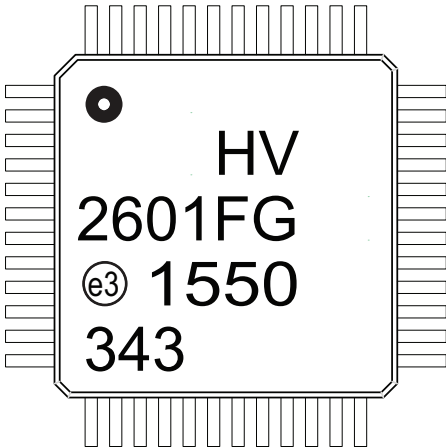
Example



48-lead LQFP



Example

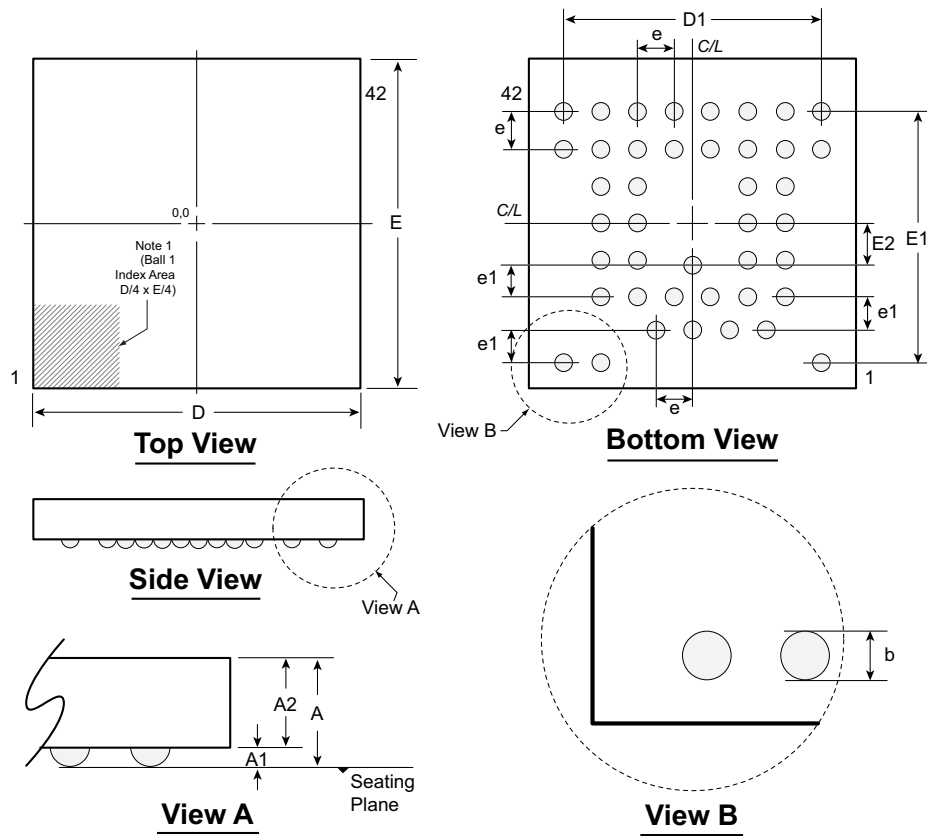


Legend: XX...X Product Code or Customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code
(e3) Pb-free JEDEC® designator for Matte Tin (Sn)
* This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

42-Ball Bumped Die Package Outline (BD)

5.29x5.30mm body, 1.02mm height (max), 0.52 / 0.60mm pitch



Notes: For the most current package drawings, See the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

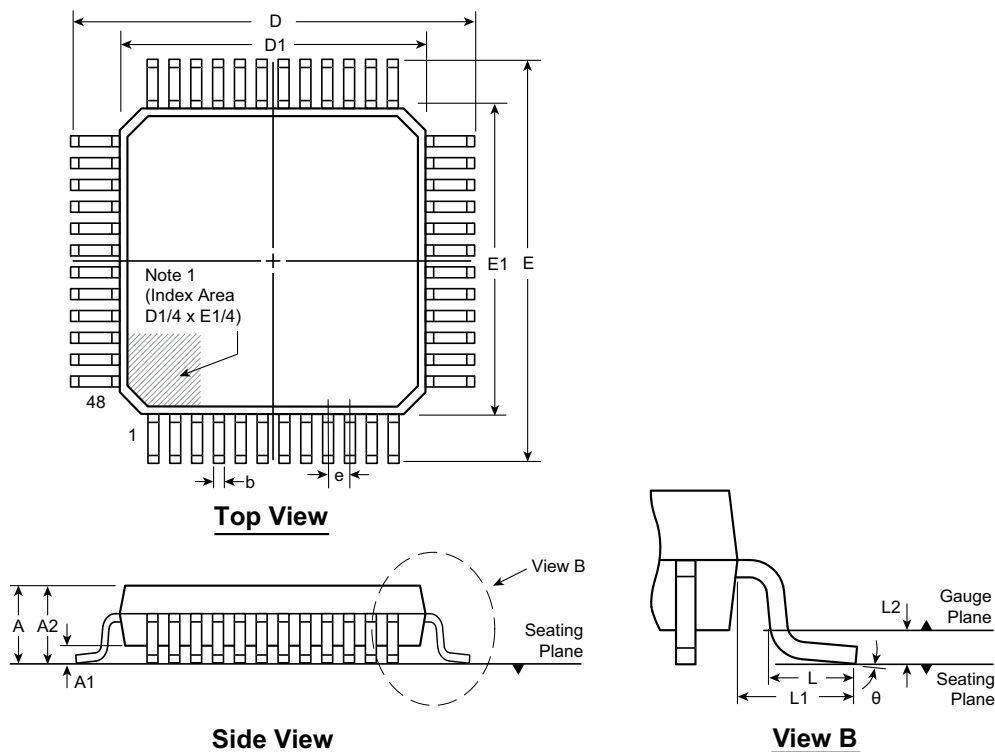
- Ball 1 identifier must be located in the index area indicated. Ball 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	E2	e	e1
Dimension (mm)	MIN	0.91	0.21	0.70	0.29	5.19	4.20 BSC	5.20	4.04 BSC	0.68 BSC	0.60 BSC
	NOM	0.965	0.24	0.725	0.32	5.29		5.30			
	MAX	1.02	0.27	0.75	0.35	5.39		5.40			

Note: For more information about ball coordinates, contact Microchip sales.

48-Lead LQFP Package Outline (FG)

7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75			7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (December 2015)

- Converted Supertex Doc #s DSFP-HV2601 and DSFP-HV2701 to Microchip DS20005391B.
- Combined HV2601/HV2701 into one document.
- Revised **Section 4.0 “Packaging Information”**
- Removed package GA from the data sheet.
- Made minor text changes throughout.

Revision B (March 2016)

- Moved **“Block Diagram”** to page 2 and made a minor change for clarity.
- Removed Confidential status from document.

HV2601 / HV2701

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package		Environmental		Media Type
Device: HV2601 = 16-Channel HV Analog Switch HV2701 = 16-Channel HV Analog Switch with Bleed Resistors Package: BD = 42-Ball Bumped Die FG = 48-lead LQFP Environmental G = Lead (Pb)-free/ROHS-compliant package (not used for BD packages) Media Type: (blank) = 250/Tray for FG package M931 = 1000/Reel for FG package M936 = 2500/Reel for BD package					
Examples: a) HV2601FG-G: 48-lead LQFP package, 250/Tray b) HV2601FG-G-M931: 48-lead LQFP package, 1000/Reel c) HV2701BD-M936 42-ball Bumped Die, 2500/Reel					

Note: HV2601BD and HV2701BD are RoHS-compliant products

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KeeLoq, KeeLoq logo, Klear, LANCheck, LINK MD, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, ETHERSYNCH, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and QUIET-WIRE are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, RightTouch logo, REAL ICE, Ripple Blocker, Serial Quad I/O, SQL, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2015-2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-0342-5

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820