ON Semiconductor®

PCS3P25811 and PCS3P25812 and PCS3P25814

Spread Spectrum Clock Generator

Features

- Generates a 1x (PCS3P25811), 2x (PCS3P25812) and 4x(PCS3P25814) low EMI spread spectrum clock of the input frequency
- Provides up to 15dB of EMI suppression
- Input Frequency: 4MHz - 32MHz
- Output Frequency:
  - PCS3P25811: 4MHz - 32MHz
  - PCS3P25812: 8MHz - 64MHz
  - PCS3P25814: 16MHz - 128MHz
- Selectable spread options: Down Spread and Center Spread
- Low Power Dissipation:
  - 3.3V: 20mW (typ) @ 6MHz
  - 3.3V: 24mW (typ) @ 12MHz
  - 3.3V: 30mW (typ) @ 24MHz
- Low inherent Cycle-to-Cycle Jitter
- Supply Voltage: 2.8V to 3.6V
- LVCMOS Input and output
- Functional and Pinout compatible to Cypress CY25811, CY25812 and CY25814
- 8-pin SOIC, and 8L 2mmX2mm WDFN (TDFN) Packages

Product Description

The PCS3P25811/12/14 devices are versatile spread spectrum frequency modulators designed specifically for a wide range of input clock frequencies from 4MHz to 32MHz.

The PCS3P25811/12/14 reduce electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. It allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The PCS3P25811/12/14 can generate an EMI reduced clock from crystal, ceramic resonator, or system clock.

The PCS3P25811/12/14 modulate the output of a single PLL in order to “spread” the bandwidth of a synthesized cock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation.’

The PCS3P25811/12/14 use the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all-digital method.

The PCS3P25811/12/14 have 2 pins S0 and S1 to control the selection of Center Spread, Down Spread and No-Spread functions. Additionally there is a 3 level logic contol FSEL, for selecting one of the three different frequency ranges within the operating frequency range. Refer *Input/Output Frequency Range Selection Table*.

The PCS3P25811/12/14 operate from a 2.8V to 3.6V supply and are available in 8 pin SOIC, and 8L 2mmX2mm WDFN packages.

Applications

The PCS3P25811/12/14 are targeted towards EMI management in applications such as LCD Panels, MFPs, Digital copiers, Networking, PC peripheral devices, consumer electronics, and embedded controller systems.

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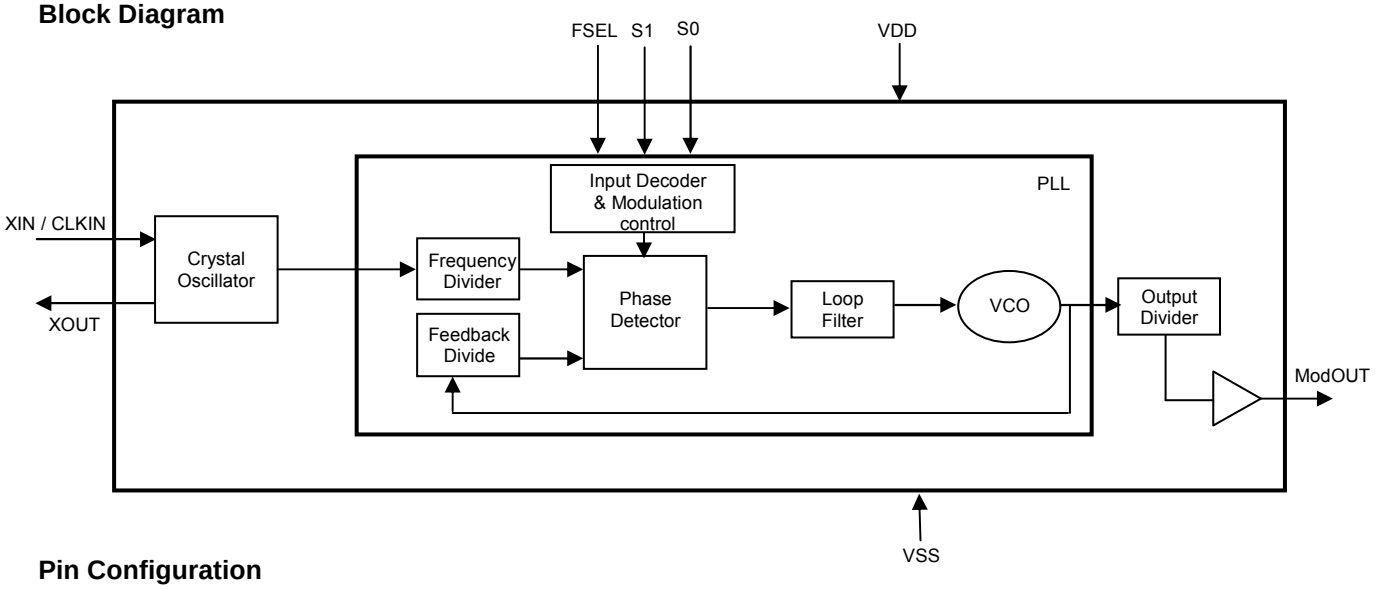
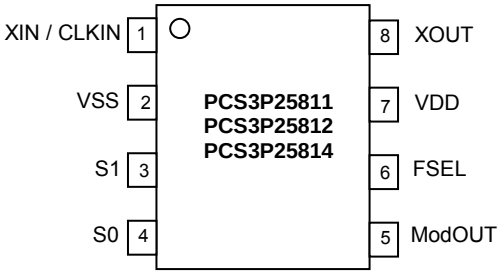
PCS3P25811/D

Block Diagram



Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	XIN / CLKIN	I	Crystal connection or External Clock input.
2	VSS	P	Ground to entire chip.
3	S1	I	Digital 3 level logic input (1-M-0) used to select Center, Down and No spread options. (Refer to *Frequency Deviation Selection Table).* Default=M.
4	S0	I	Digital 3 level logic input (1-M-0) used to select Center, Down and No spread options. (Refer to *Frequency Deviation Selection Table).* Default=M.
5	ModOUT	O	Spread Spectrum Clock Output.
6	FSEL	I	Frequency range select. Digital 3 level logic input (1-M-0) used to select Input Clock frequency range (Refer to *Input/Output Frequency Range Selection Table*). Default=M.
7	VDD	P	Power supply for the entire chip (2.8V to 3.6V).
8	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.

Input/Output Frequency Range Selection Table

FSEL (pin 6)	Part Number						Modulation Rate
	PCS3P25811 (1x)		PCS3P25812 (2x)		PCS3P25814 (4x)		
	Input (MHz)	Output (MHz)	Input (MHz)	Output (MHz)	Input (MHz)	Output (MHz)	
0	4-8	4-8	4-8	8-16	4-8	16-32	Input Frequency / 128
1	8-16	8-16	8-16	16-32	8-16	32-64	Input Frequency / 256
M	16-32	16-32	16-32	32-64	16-32	64-128	Input Frequency / 512

Output Frequency Deviation Selection Table

CLKIN (MHz)	FSEL	S1=0 S0=0	S1=0 S0=M	S1=0 S0=1	S1=M S0=0	S1=1 S0=1	S1=1 S0=0	S1=M S0=1	S1=1 S0=M	S1=M S0=M
		Center	Center	Center	Center	Down	Down	Down	Down	No Spread
4-5	0	±1.4	±1.2	±0.6	±0.5	-3	-2.2	-1.9	-0.7	0
5-6	0	±1.3	±1.1	±0.5	±0.4	-2.7	-1.9	-1.7	-0.6	0
6-7	0	±1.2	±0.9	±0.5	±0.4	-2.5	-1.8	-1.5	-0.6	0
7-8	0	±1.1	±0.9	±0.4	±0.3	-2.3	-1.7	-1.4	-0.5	0
8-10	1	±1.4	±1.2	±0.6	±0.5	-3	-2.2	-1.9	-0.7	0
10-12	1	±1.3	±1.1	±0.5	±0.4	-2.7	-1.9	-1.7	-0.6	0
12-14	1	±1.2	±0.9	±0.5	±0.4	-2.5	-1.8	-1.5	-0.6	0
14-16	1	±1.1	±0.9	±0.4	±0.3	-2.3	-1.7	-1.4	-0.5	0
16-20	M	±1.4	±1.2	±0.6	±0.5	-3	-2.2	-1.9	-0.7	0
20-24	M	±1.3	±1.1	±0.5	±0.4	-2.7	-1.9	-1.7	-0.6	0
24-28	M	±1.2	±0.9	±0.5	±0.4	-2.5	-1.8	-1.5	-0.6	0
28-32	M	±1.1	±0.9	±0.4	±0.3	-2.3	-1.7	-1.4	-0.5	0

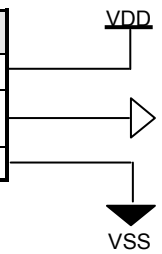
Note: Frequency Deviation given in the table is for the Input Frequency Range covering PCS3P25811/12 /14.

3 Level Digital Logic

S0, S1, and FSEL digital inputs are designed to sense 3 different logic levels designated as High “1”, Low “0” and Middle “M”. With this 3-Level digital input logic 9 different logic states can be detected.

S0, S1 and FSEL pins include an on chip 100K (50K/50K) resistor divider. No external application resistors are needed to implement the 3-Level logic levels as shown below:

Logic	Control Pins
1	FSEL, S0, S1 to VDD
M	FSEL, S0, S1 UNCONNECTED
0	FSEL, S0, S1 to VSS



Operating Conditions

Symbol	Parameter	Min	Max	Unit
VDD	Voltage on any pin with respect to VSS	2.8	3.6	V
T_A	Operating temperature	0	+70	℃
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD 22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter			Min	Typ	Max	Unit
VDD	Supply Voltage			2.8	3.3	3.6	V
V_{IL}	Input low voltage (S0, S1, FSEL Inputs)	Commercial Temp.		0		$0.15V_{DD}$	V
		Industrial Temp.		0		$0.13\ V_{DD}$	
V_{IM}	Input Middle Voltage (S0, S1, FSEL Inputs)			0.4VDD		$0.60V_{DD}$	V
V_{IH}	Input high voltage (S0, S1, FSEL Inputs)			0.85VDD		V_{DD}	V
V_{OL}	Output low voltage (ModOUT Output)		I_{OL}= 4mA			0.4	V
			I_{OL}= 10mA			1.2	
V_{OH}	Output high voltage (ModOUT Output)		I_{OH}= -4mA	2.4			V
			I_{OH}= -6mA	2			
C_{IN}	Input Capacitance (XIN And XOUT)			6		9	pF
I_{DD}	Dynamic supply current (Unloaded Output)	Commercial Temp	XIN / CLKIN = 12MHz			8	mA
			XIN / CLKIN = 24MHz			10	
			XIN / CLKIN = 32MHz			13	
		Industrial Temp	XIN / CLKIN = 12MHz			10	mA
			XIN / CLKIN = 24MHz			12	
			XIN / CLKIN = 32MHz			15	
I_{CC}	Static supply current (XIN / CLKIN pulled to VSS)					0.5	mA

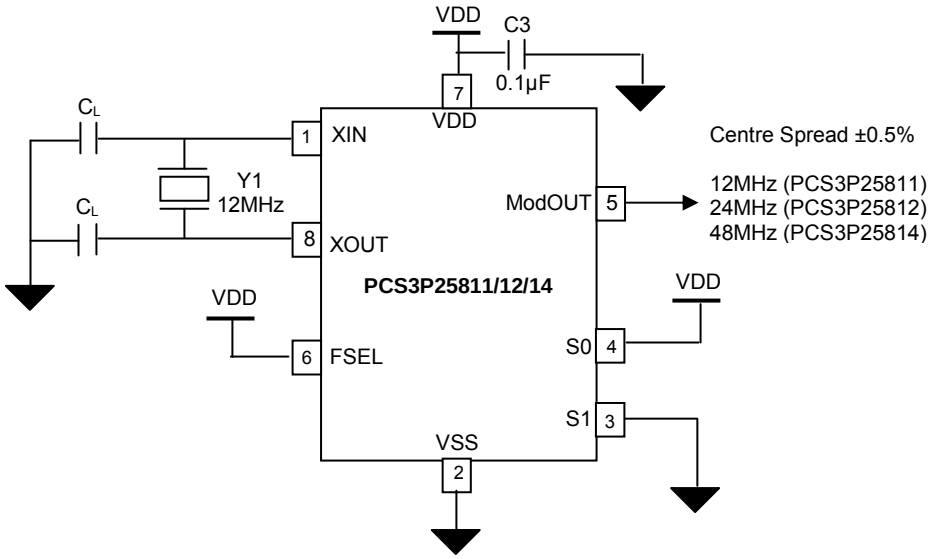
Note. The voltage on any input or I/O pin cannot exceed the power pin during power up. All parameters are specified at Commercial and Industrial temperature unless stated otherwise.

AC Electrical Characteristics

Symbol	Parameter			Min	Typ	Max	Unit
f_{IN}	Input Clock frequency for PCS3P25811/12/14			4		32	MHz
f_{OUT}	ModOUT Clock frequency for PCS3P25811			4		32	MHz
	ModOUT Clock frequency for PCS3P25812			8		64	MHz
	ModOUT Clock frequency for PCS3P25814			16		128	MHz
t_{LH}[1, 2]	ModOUT Rise time (Measured from 20% to 80%)	PCS3P25811/12/14		2		5	nS
		PCS3P25814 When FSEL=M		1		2.2	
t_{HL}[1, 2]	ModOUT Fall time (Measured from 80% to 20%)	PCS3P25811/12/14		2		4.4	nS
		PCS3P25814 When FSEL=M		1		2.2	
T_{DCIN}	Input Clock Duty Cycle(XIN / CLKIN)			40		60	%
T_{DCOUT}[1, 2]	Output Clock Duty Cycle (ModOUT)			40		60	%
T_{JC}[2]	Cy-Cy Jitter, For ModOUT with Spread ON (*For Commercial temperature*)	PCS3P25811	4MHz			600	pS
			8MHz			450	
		PCS3P25812	16MHz			400	
			32MHz			380	
		PCS3P25814	64MHz			380	
			128MHz			380	
	Cy-Cy Jitter, For ModOUT with Spread ON (*For Industrial temperature*)	PCS3P25811 PCS3P25812 PCS3P25814	CLKIN = 6MHz			500	pS
			CLKIN = 12MHz			400	
			CLKIN = 24MHz			380	
t_{ON}[2]	PLL Lock Time (Stable power supply, valid input clock to valid Clock on ModOUT)		Commercial Temp.			2	mS
			Industrial Temp.			3	

Notes: 1.Parameters are specified with 15pF loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Application Schematic

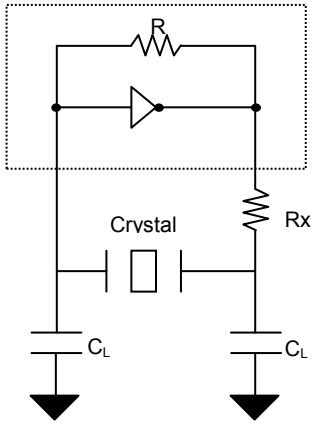


Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	12MHz
Frequency tolerance	± 30 ppm or better at 25℃
Operating temperature range	-25℃ to +85℃
Storage temperature	-40℃ to +85℃
Load capacitance(C_P)	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω

Note: Note: C_L is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

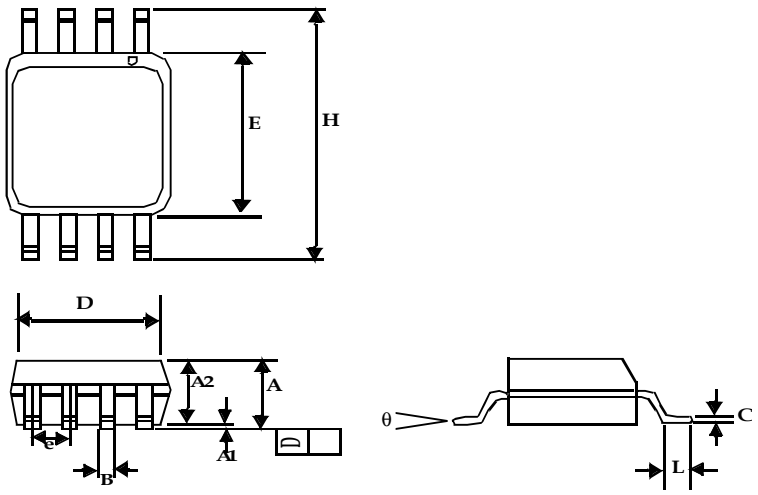
Typical Crystal Interface Circuit



$C_L = 2*(C_P – C_S)$,
Where C_P = Load capacitance of crystal
C_S = Stray capacitance due to $C_{IN,}$ PCB, Trace etc.

Package Information

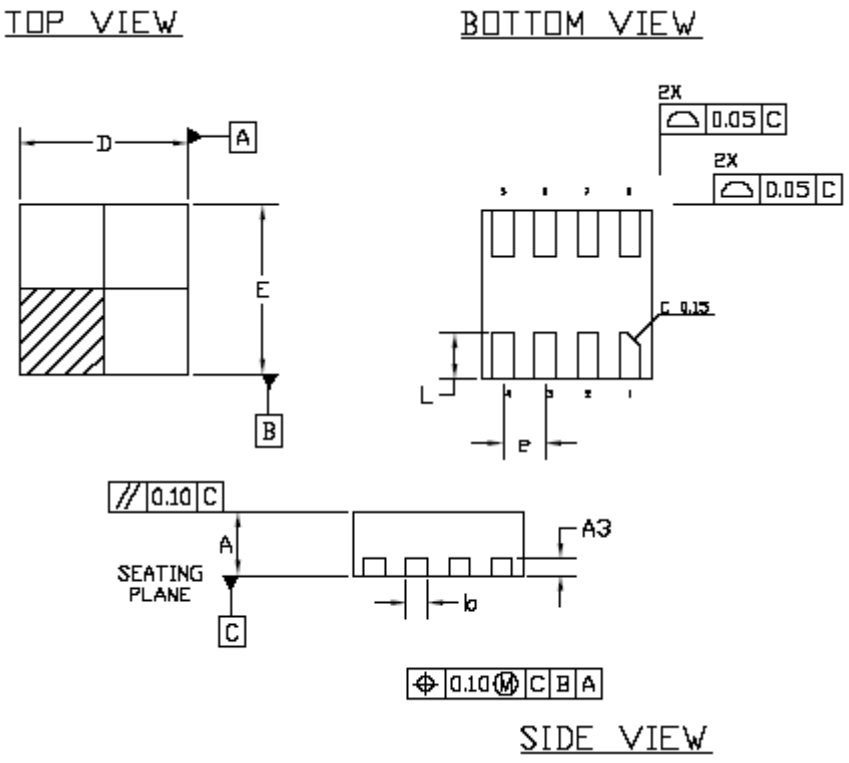
8-Pin SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

Note: Controlling dimensions are millimeters.
SOIC: 0.074 grams unit weight.

8L 2mmX2mm WDFN package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.027	0.0315	0.70	0.80
A3	0.008 BSC		0.203 BSC	
b	0.008	0.012	0.20	0.30
D	0.077	0.080	1.95	2.05
E	0.077	0.080	1.95	2.05
e	0.020 BSC		0.50 BSC	
L	0.020	0.024	0.50	0.60

Ordering Code

Part Number	Marking	Package Type	Temperature
PCS3P25811AG08SR	CGL	8-pin SOIC – Tape & Reel, Green	0℃ to +70℃
P3P25812AG-08SR	CIL	8-pin SOIC – Tape & Reel, Green	0℃ to +70℃
P3P25814AG-08SR	CKL	8-pin SOIC – Tape & Reel, Green	0℃ to +70℃
P3P25811AG-08CR	CG	8L-WDFN (2mmX2mm) - Tape & Reel, Green	0℃ to +70℃
P3P25812AG-08CR	CI	8L-WDFN (2mmX2mm) - Tape & Reel, Green	0℃ to +70℃
P3P25814AG-08CR	CK	8L-WDFN (2mmX2mm) - Tape & Reel, Green	0℃ to +70℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

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