LMV3xxA Low-Voltage Rail-to-Rail Output Operational Amplifiers

1 Features

- Low Input Offset Voltage: ±1 mV
- Rail-to-Rail Output
- Unity-Gain Bandwidth: 1 MHz
- Low Broadband Noise: 30 nV/√Hz
- Low Input Bias Current: 10 pA
- Low Quiescent Current: 80 µA/Ch
- Unity-Gain Stable
- Internal RFI and EMI Filter
- Operational at Supply Voltages as Low as 2.5 V
- Easier to Stabilize With Higher Capacitive Load Due to Resistive Open-Loop Output Impedance
- Extended Temperature Range: –40°C to +125°C

2 Applications

- Smoke Detectors
- Motion Detectors
- Wearable Devices
- Large and Small Appliances
- EPOS
- Barcode Scanners
- Sensor Signal Conditioning
- Power Modules
- Personal Electronics
- Active Filters
- HVAC: Heating, Ventilating, and Air Conditioning
- Motor Control: AC Induction
- Low-Side Current Sensing

3 Description

The LMV3xxA family includes single - (LMV321A), dual - (LMV358A), and quad-channel (LMV324A) low-voltage (2.5 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail output swing capabilities. These op amps provide a cost-effective solution for space-constrained applications such as large appliances, smoke detectors, and personal electronics where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive of the LMV3xxA family is 500 pF, and the resistive open-loop output impedance makes stabilization easier with much higher capacitive loads. These op amps are designed specifically for low-voltage operation (2.5 V to 5.5 V) with performance specifications similar to the LMV3xx devices.

The robust design of the LMV3xxA family simplifies circuit design. The op amps feature unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions.

The LMV3xxA family is available in industry-standard packages such as SOIC, MSOP, SOT-23 and TSSOP packages.

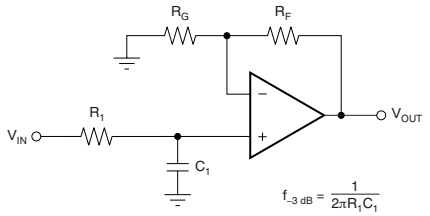
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV321A	SOT-23 (5)(2)	1.60 mm × 2.90 mm
	SC70 (5)(2)	1.25 mm × 2.00 mm
LMV358A	SOIC (8)	3.91 mm × 4.90 mm
	TSSOP (8)(2)	3.00 mm x 4.40 mm
	VSSOP (8)	3.00 mm × 3.00 mm
LMV324A	SOIC (14)(2)	8.65 mm × 3.91 mm
	TSSOP (14)(2)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Package is for preview only.

Single-Pole, Low-Pass Filter



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information: LMV321A ... 6
6.5 Thermal Information: LMV358A ... 6
6.6 Thermal Information: LMV324A ... 6
6.7 Electrical Characteristics ... 7
6.8 Typical Characteristics ... 8
7 Detailed Description ... 14
7.1 Overview ... 14
7.2 Functional Block Diagram ... 14
7.3 Feature Description ... 15
7.4 Device Functional Modes ... 15
8 Application and Implementation ... 16
8.1 Application Information ... 16
8.2 Typical Application ... 16
9 Power Supply Recommendations ... 21
9.1 Input and ESD Protection ... 21
10 Layout ... 22
10.1 Layout Guidelines ... 22
10.2 Layout Example ... 22
11 Device and Documentation Support ... 23
11.1 Documentation Support ... 23
11.2 Related Links ... 23
11.3 Receiving Notification of Documentation Updates 23
11.4 Community Resources ... 23
11.5 Trademarks ... 23
11.6 Electrostatic Discharge Caution ... 23
11.7 Glossary ... 23
12 Mechanical, Packaging, and Orderable Information ... 23

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2018) to Revision B — **Page**

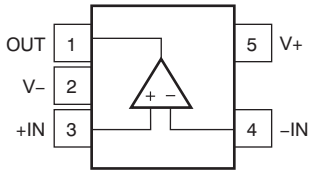
- Added SOT-23 package to *Device Information* table ... 1
- Added SC70 package to *Device Information* table ... 1
- Added TSSOP-8 package to *Device Information* table ... 1
- Added SOIC-14 package to *Device Information* table ... 1
- Added TSSOP-14 package to *Device Information* table ... 1
- Added *Thermal Information: LMV321A* ... 6
- Added *Thermal Information: LMV324A* ... 6

Changes from Original (December 2017) to Revision A — **Page**

- Changed device status from Advance Information to Production Data/Mixed Status ... 1
- Added TSSOP to LMV358A D, DGK, PW Packages to *Pin Configuration and Functions* table ... 3
- Added DGK and PW package to *Thermal Information* table ... 6

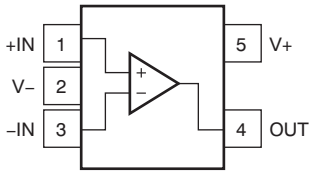
5 Pin Configuration and Functions

LMV321A DBV Package(1)
5-Pin SOT-23
Top View



(1) Package is preview only.

LMV321A DCK Package(1)
5-Pin SC70
Top View

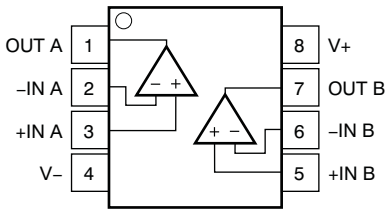


(1) Package is preview only.

Pin Functions: LMV321A

PIN			I/O	DESCRIPTION
NAME	DBV	DCK		
–IN	4	3	I	Inverting input
+IN	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	—	Negative (lowest) supply or ground (for single-supply operation)
V+	5	5	—	Positive (highest) supply

LMV358A D, DGK, PW Packages
8-Pin SOIC, VSSOP, TSSOP(1)
Top View

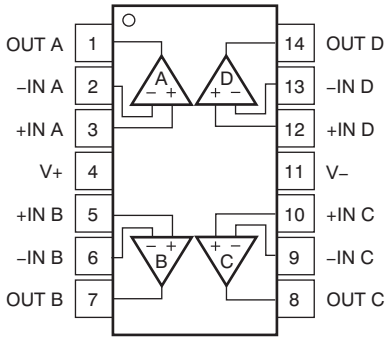


(1) Package is preview only.

Pin Functions: LMV358A

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

LMV324A D, PW Packages(1)
14-Pin SOIC, TSSOP
Top View



(1) Packages are preview only.

Pin Functions: LMV324A

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, ([V+] – [V–])			0	6	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	V
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		mA
Operating, T_A			–55	150	°C
Operating junction temperature, T_J				150	°C
Storag temperaturee, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	2.5	5.5	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information: LMV321A

THERMAL METRIC (1)		LMV321A		UNIT
		DBV (SOT-23)(2)	DCK (SC70)(2)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	232.8	239.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	153.8	148.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100.9	82.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	77.2	54.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100.4	81.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Package is preview only.

6.5 Thermal Information: LMV358A

THERMAL METRIC(1)		LMV358A			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)(2)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.4	201.2	205.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.3	85.7	106.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89.5	122.9	133.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	47.3	21.2	34.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	89	121.4	132.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Package is preview only.

6.6 Thermal Information: LMV324A

THERMAL METRIC(1)		LMV324A		UNIT
		D (SOIC)(2)	PW (TSSOP)(2)	
		14 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.1	148.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.8	68.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.5	92.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	16.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.1	91.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Package is preview only.

6.7 Electrical Characteristics

For V_S = (V+) – (V–) = 2.5 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25 °C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	Vs = 5 V		±1	±4	mV
		Vs = 5 V, T_A = –40°C to 125°C			±5	mV
dV_{OS}/dT	V_{OS} vs temperature	T_A = –40°C to 125°C		±1		µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.5 to 5.5 V, V_{CM} = (V–)	78	100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V–) – 0.1		(V+) – 1	V
CMRR	Common-mode rejection ratio	V_S = 2.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C		86		dB
		V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C		95		dB
		V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V T_A = –40°C to 125°C	63	77		dB
		V_S = 2.5 V, (V–) – 0.1 V < V_{CM} < (V+)+ 0.1 V T_A = –40°C to 125°C		68		dB
INPUT BIAS CURRENT						
I_B	Input bias current	Vs = 5 V		±10		pA
I_{OS}	Input offset current			±3		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz, Vs = 5 V		5.1		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz, Vs = 5 V		33		$nV/\sqrt{Hz}$
		f = 10 kHz, Vs = 5 V		30		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz, Vs = 5 V		25		$fA/\sqrt{Hz}$
INPUT CAPACITANCE						
C_{ID}	Differential			1.5		pF
C_{IC}	Common-mode			5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	100	115		dB
		V_S = 2.5 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ		98		dB
		V_S = 2.5 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 2 kΩ		112		dB
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		128		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	Vs = 5 V		1		MHz
φ_m	Phase margin	V_S = 5.5 V, G = 1		76		degrees
SR	Slew rate	Vs = 5 V		1.7		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V Step , G = +1, C_L = 100 pF		3		µs
		To 0.01%, V_S = 5 V, 2-V Step , G = +1, C_L = 100 pF		4		µs
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.9		µs
THD+N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz, 80 kHz measurement BW		0.005		%
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ		20	50	mV
		V_S = 5.5 V, R_L = 2 kΩ		40	75	mV
I_{SC}	Short-circuit current	Vs = 5.5 V		±40		mA
Z_O	Open-loop output impedance	Vs = 5 V, f = 1 MHz		1200		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.5 (±1.25)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5 V		80	125	µA
		I_O = 0 mA, V_S = 5.5 V, T_A = –40°C to 125°C			150	µA
	Power-on time	V_S = 0 V to 5 V, to 90% I_Q level		50		µs

6.8 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

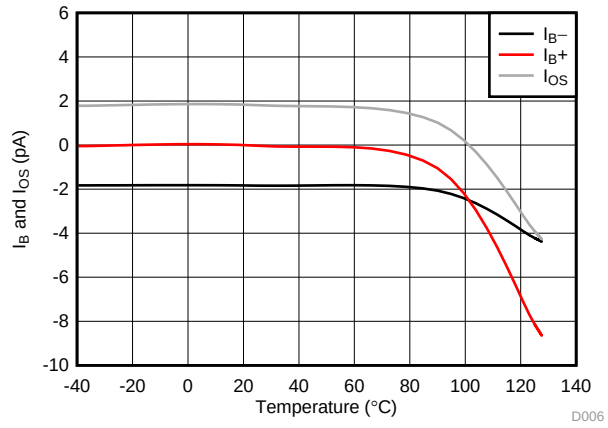


Figure 1. I_B and I_{OS} vs Temperature

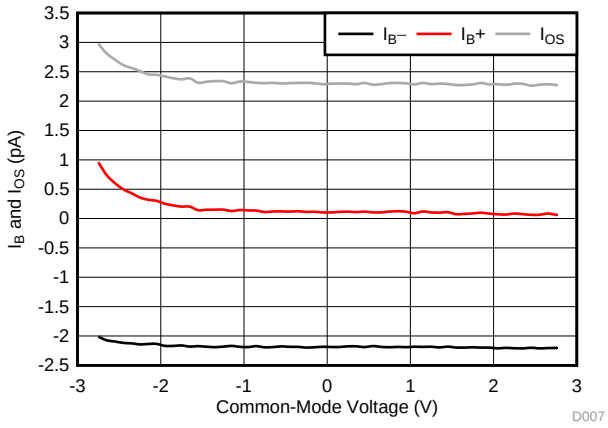


Figure 2. I_B and I_{OS} vs Common-Mode Voltage

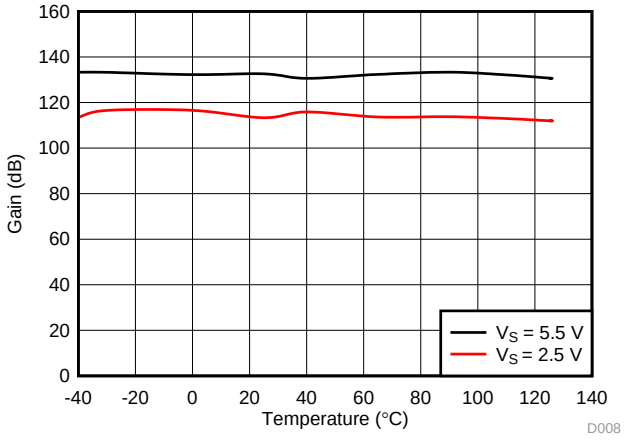
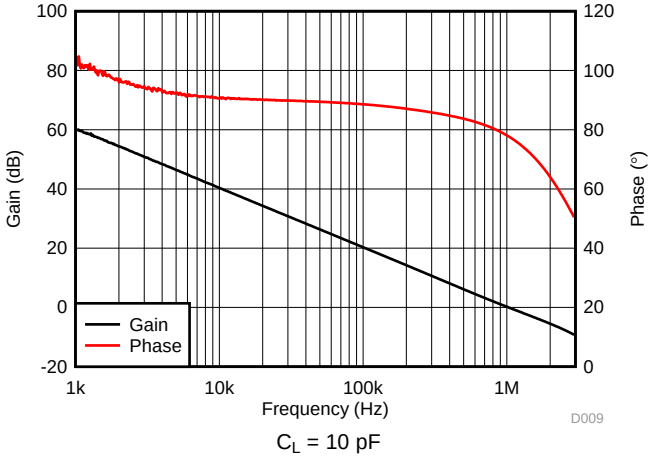


Figure 3. Open-Loop Gain vs Temperature



C_L = 10 pF

Figure 4. Open-Loop Gain and Phase vs Frequency

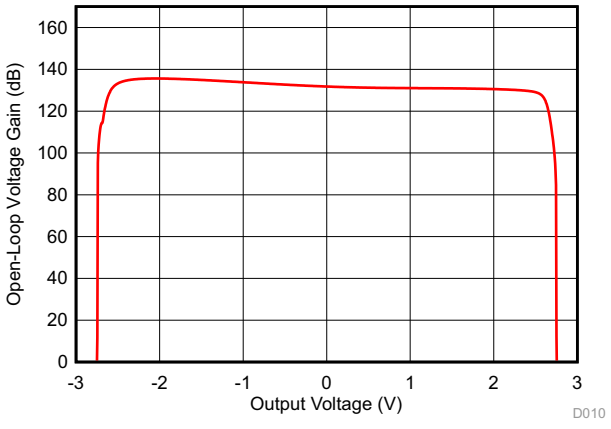
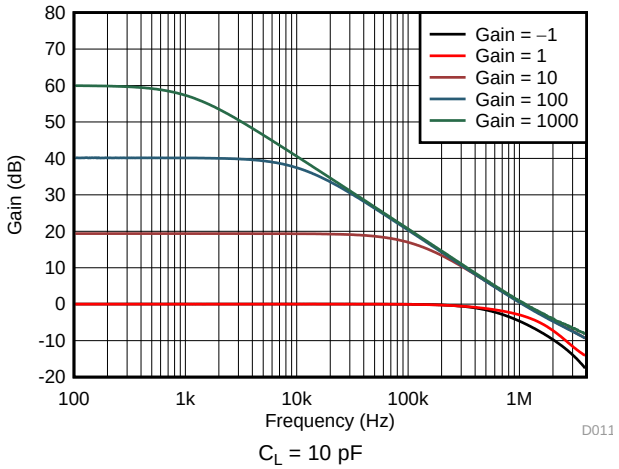


Figure 5. Open-Loop Gain vs Output Voltage



C_L = 10 pF

Figure 6. Closed-Loop Gain vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

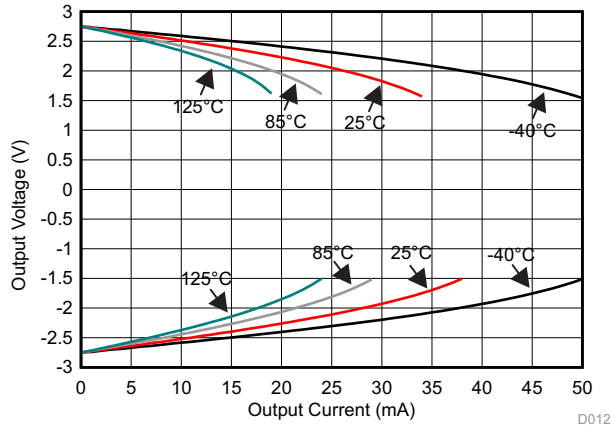


Figure 7. Output Voltage vs Output Current (Claw)

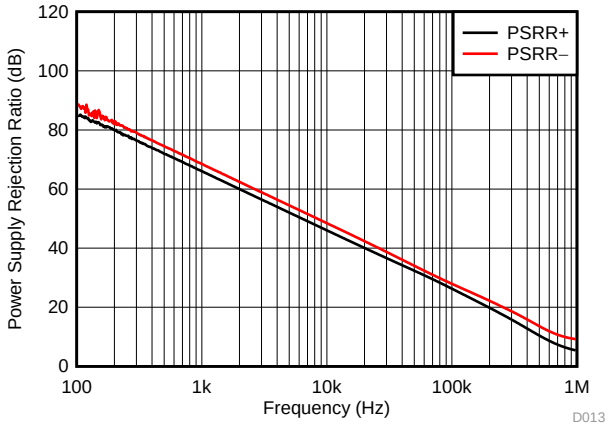
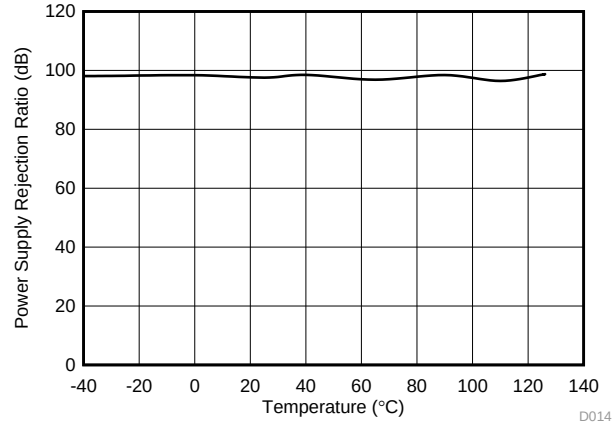


Figure 8. PSRR vs Frequency



V_S = 1.8 V to 5.5 V

Figure 9. DC PSRR vs Temperature

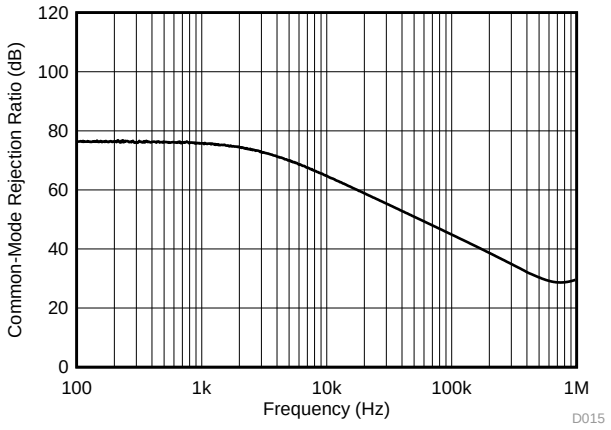
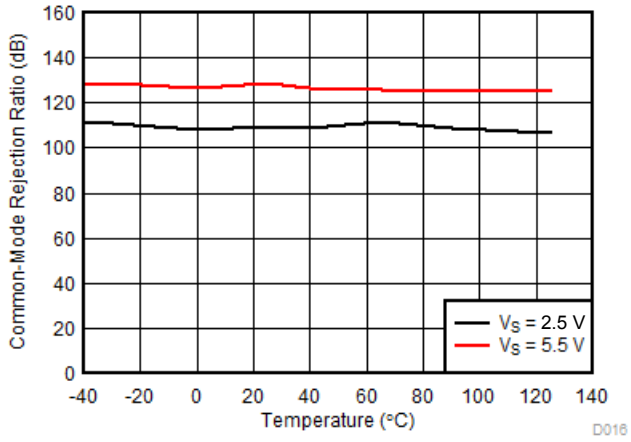


Figure 10. CMRR vs Frequency



V_{CM} = (V–) – 0.1 V to (V+) – 1.4 V

Figure 11. DC CMRR vs Temperature

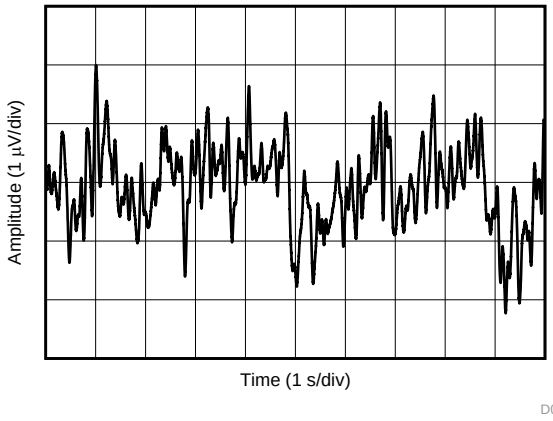


Figure 12. 0.1 Hz to 10 Hz Integrated Voltage Noise

Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

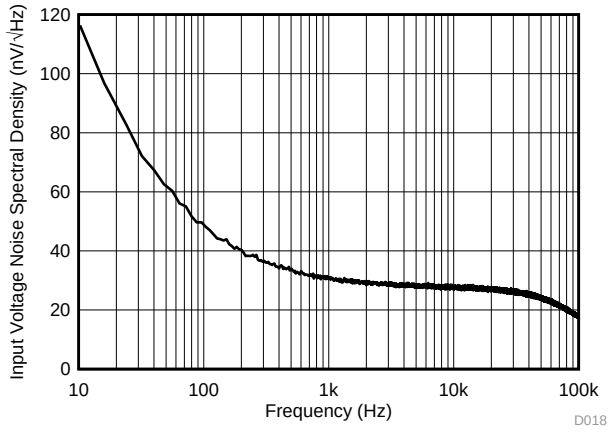
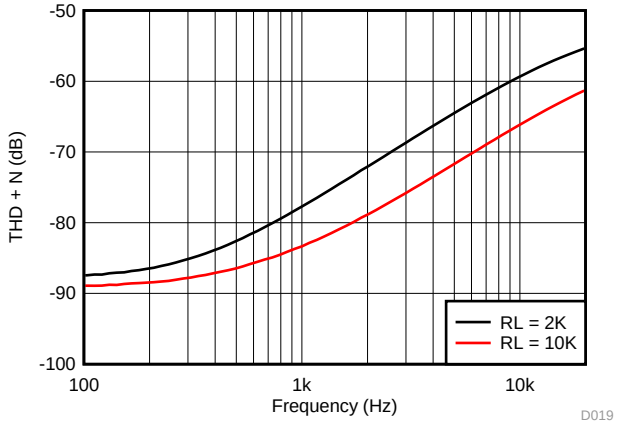
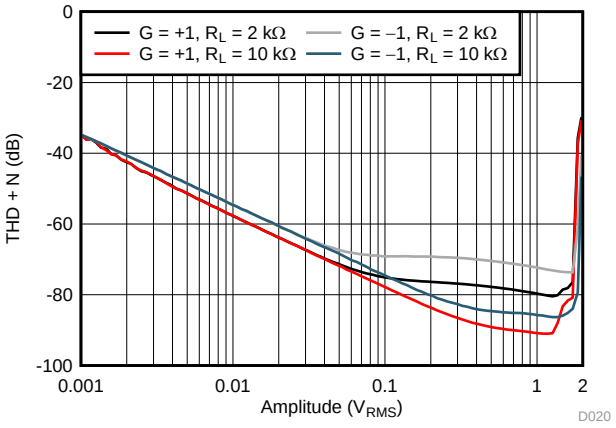


Figure 13. Input Voltage Noise Spectral Density



V_S = 5.5 V, V_{CM} = 2.5 V, G = 1, BW = 80 kHz, V_{OUT} = 0.5 V_{RMS}

Figure 14. THD + N vs Frequency



V_S = 5.5 V, V_{CM} = 2.5 V, f = 1 kHz, G = 1, BW = 80 kHz

Figure 15. THD + N vs Amplitude

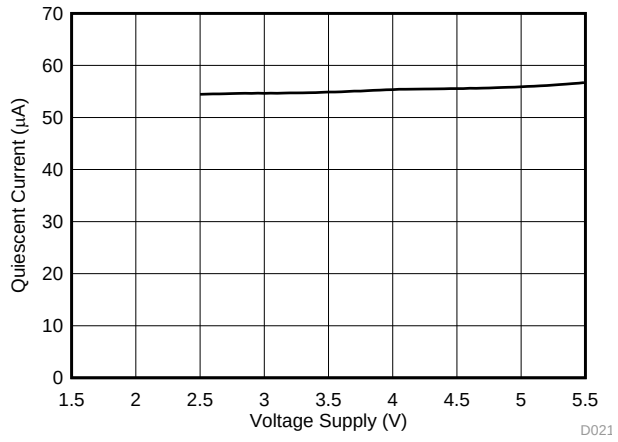


Figure 16. Quiescent Current vs Supply Voltage

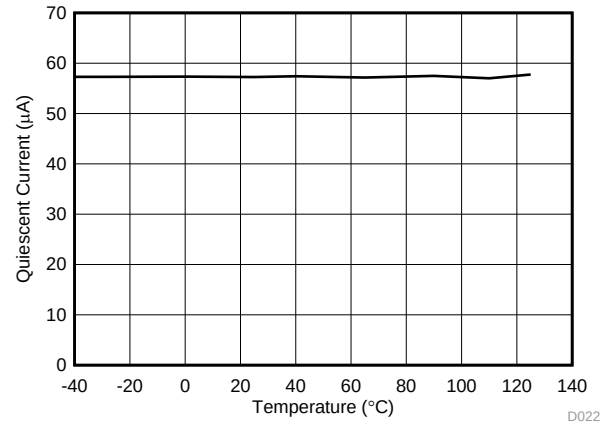


Figure 17. Quiescent Current vs Temperature

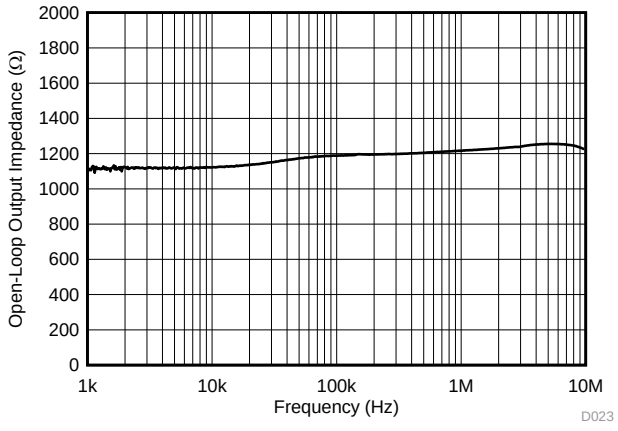
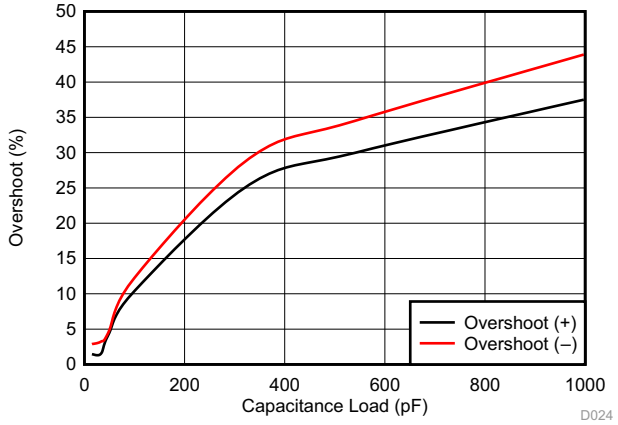


Figure 18. Open-Loop Output Impedance vs Frequency

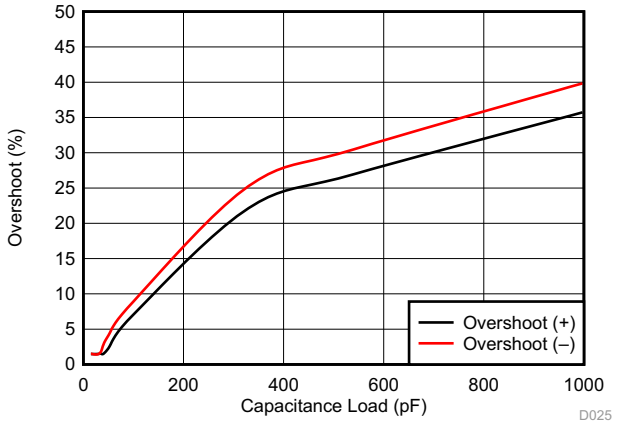
Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = 1, V_{IN} = 100 mVpp

Figure 19. Small Signal Overshoot vs Capacitive Load



G = –1, V_{IN} = 100 mVpp

Figure 20. Small Signal Overshoot vs Capacitive Load

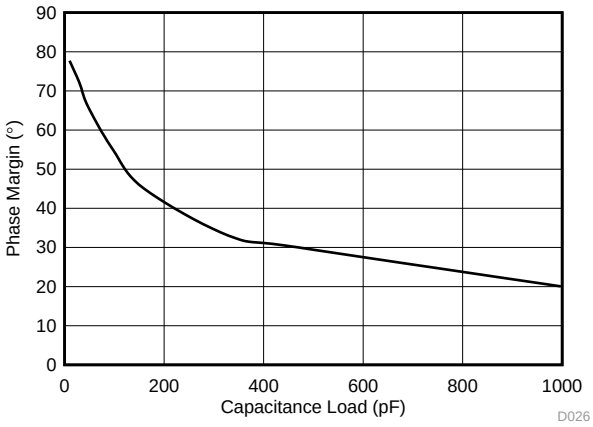
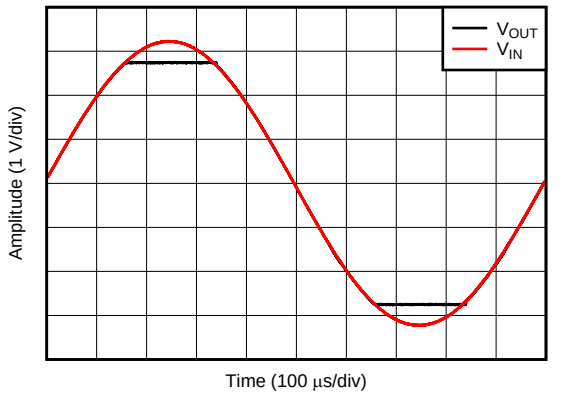
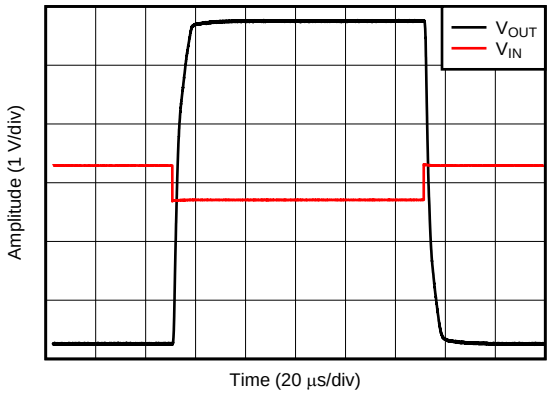


Figure 21. Phase Margin vs Capacitive Load



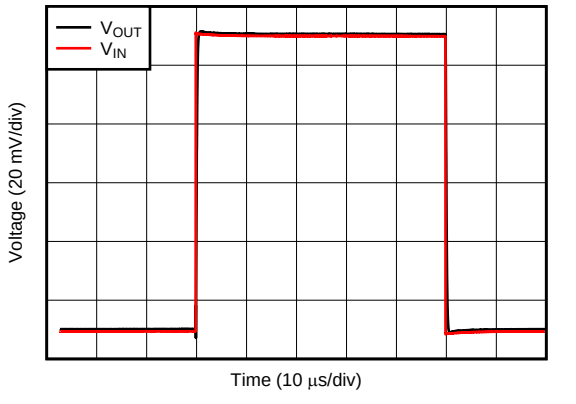
G = 1, V_{IN} = 6.5 V_{PP}

Figure 22. No Phase Reversal



G = –10, V_{IN} = 600 mV_{PP}

Figure 23. Overload Recovery

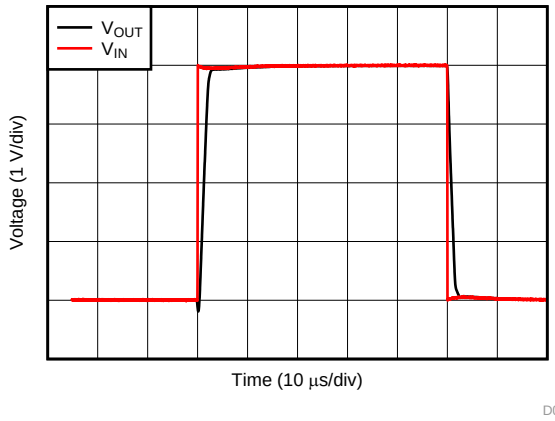


G = 1, V_{IN} = 100 mV_{PP} , C_L = 10 pF

Figure 24. Small-Signal Step Response

Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

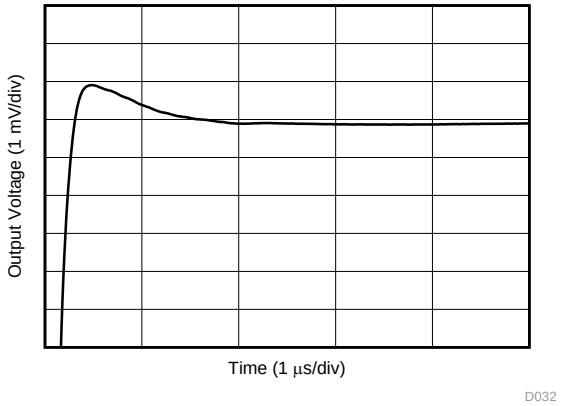


G = 1, V_{IN} = 4 V_{PP} , C_L = 10 pF

Figure 25. Large-Signal Step Response

G = 1, C_L = 100 pF, 2-V step

Figure 26. Large-Signal Settling Time (Negative)



G = 1, C_L = 100 pF, 2-V step

Figure 27. Large-Signal Settling Time (Positive)

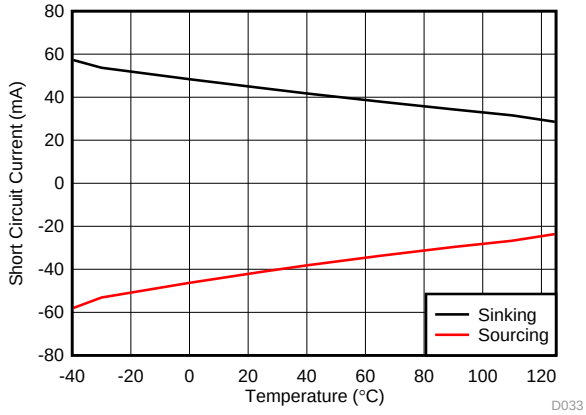


Figure 28. Short-Circuit Current vs Temperature

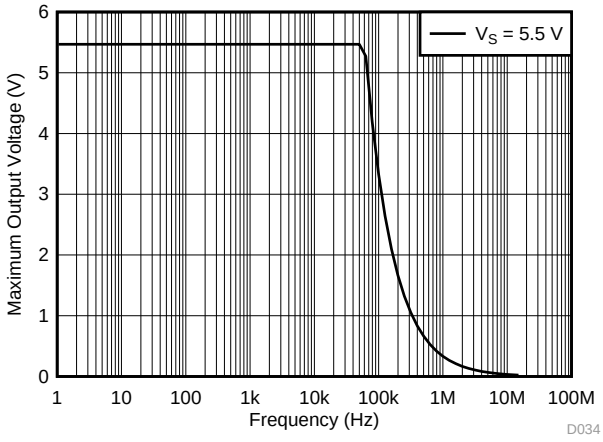


Figure 29. Maximum Output Voltage vs Frequency

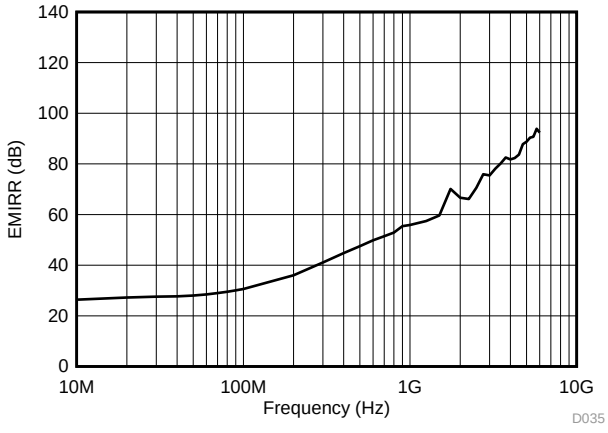


Figure 30. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

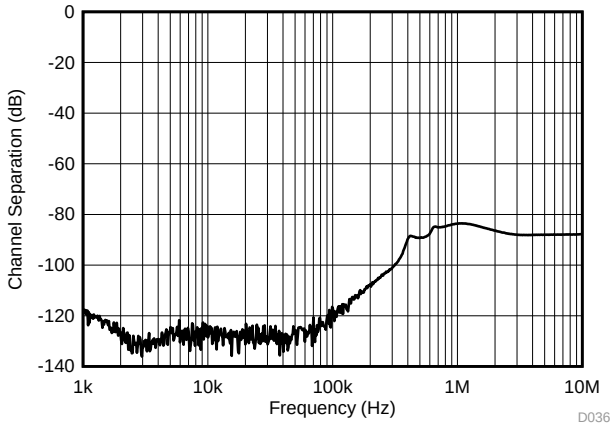


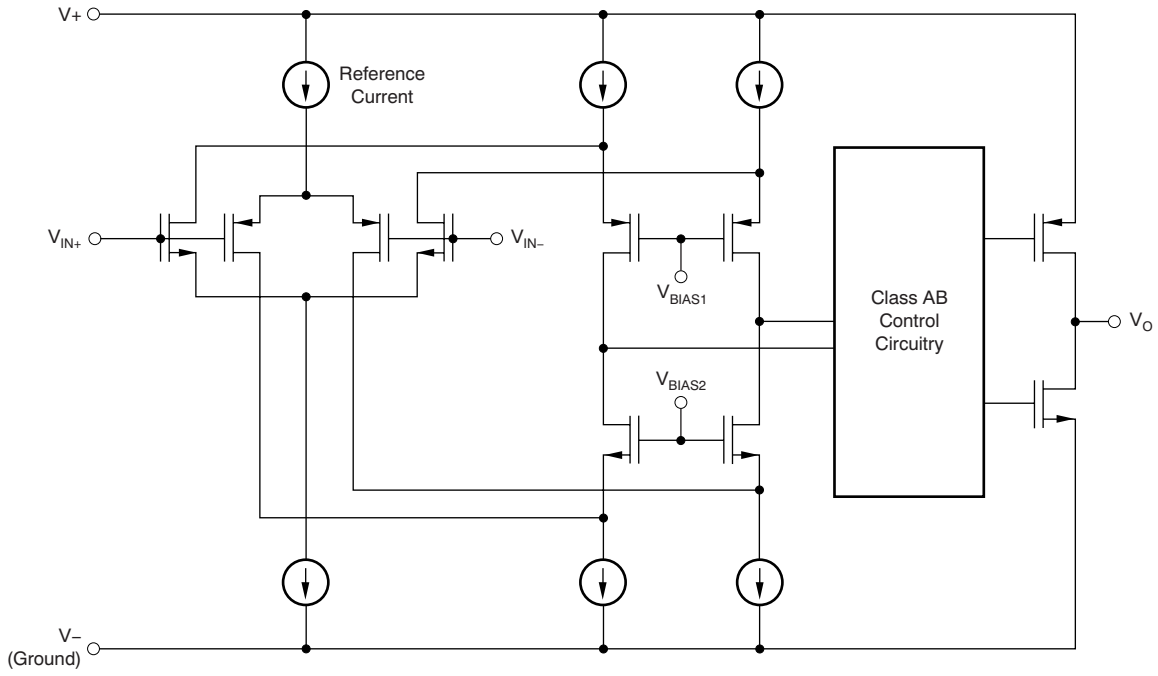
Figure 31. Channel Separation

7 Detailed Description

7.1 Overview

The LMV3xxA series is a family of low-power, rail-to-rail output op amps. These devices operate from 2.5 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes the negative rail and allows the LMV3xxA series to be used in many single-supply applications. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling analog-to-digital converters (ADCs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The LMV3xxA series of op amps are ensured for operation from 2.5 V to 5.5 V. In addition, many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the section.

7.3.2 Input Common Mode Range

The input common-mode voltage range of the LMV3xxA family extends 100 mV beyond the negative supply rail and within 1 V below the positive rail for the full supply voltage range of 2.5 V to 5.5 V. This performance is achieved with a P-channel differential pair, as shown in the *Functional Block Diagram*. Additionally, a complementary N-channel differential pair has been included in parallel to eliminate issues with phase reversal that are common with previous generations of op amps. However, the N-channel pair is not optimized for operation. TI recommends limiting any voltages applied at the inputs to less than V_{CC}– 1V to ensure that the op amp conforms to the specifications detailed in the *Electrical Characteristics* table.

7.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the LMV3xxA series delivers a robust output drive capability. A class-AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 20 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

7.3.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the LMV3xxA series is approximately 850 ns.

7.4 Device Functional Modes

The LMV3xxA family has a single functional mode. The devices are powered on as long as the power-supply voltage is between and 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV3xxA is a family of low-power, rail-to-rail output operational amplifiers specifically designed for portable applications. The devices operate from 2.5 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving less than or equal to 10-kΩ loads connected to any point between V+ and V–. The input common-mode voltage range includes the negative rail, and allows the LMV3xxA to be used in many single-supply applications.

8.2 Typical Application

8.2.1 LMV3xxA Low-Side, Current Sensing Application

Figure 32 shows the LMV3xxA configured in a low-side current sensing application.

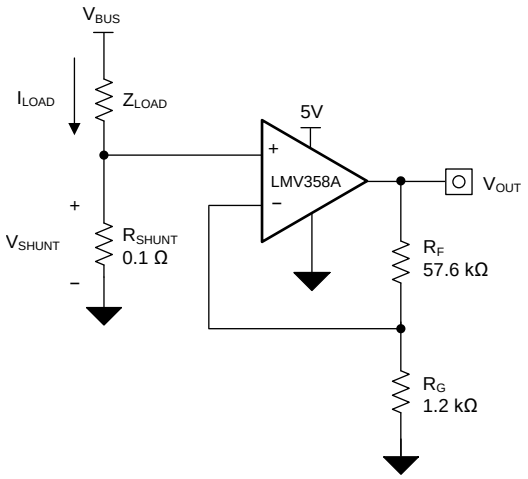


Figure 32. LMV3xxA in a Low-Side, Current-Sensing Application

Typical Application (continued)

8.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in is given in Equation 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current ($_{ILOAD}$) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is shown using Equation 2:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{2}$$

Using Equation 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the LMV3xxA to produce an output voltage of approximately 0 V to 4.9 V. The gain needed by the LMV3xxA to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \tag{3}$$

Using Equation 3, the required gain is calculated to be 49 V/V, which is set with resistors RF and RG. Equation 4 sizes the resistors RF and RG, to set the gain of the LMV3xxA to 49 V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \tag{4}$$

Selecting RF as 57.6 kΩ and RG as 1.2 kΩ provides a combination that equals 49 V/V. Figure 33 shows the measured transfer function of the circuit shown in Figure 32.

8.2.1.3 Application Curve

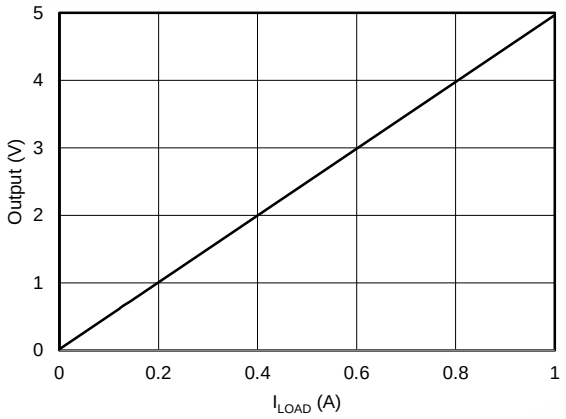


Figure 33. Low-Side, Current-Sense Transfer Function

Typical Application (continued)

8.2.2 Single-Supply Photodiode Amplifier

Photodiodes are used in many applications to convert light signals to electrical signals. The current through the photodiode is proportional to the light energy applied to the current, and is commonly in the range of a few hundred picoamps to a few tens of microamps. An amplifier in a transimpedance configuration is typically used to convert the low-level photodiode current to a voltage signal for processing in an MCU. The circuit shown in Figure 34 is an example of a single-supply photodiode amplifier circuit using the LMV358A.

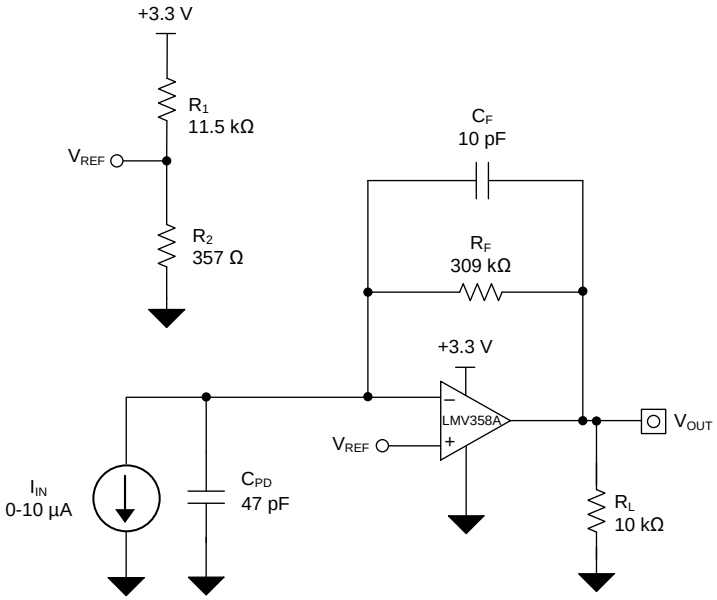


Figure 34. Single-Supply Photodiode Amplifier Circuit

Typical Application (continued)

8.2.2.1 Design Requirements

The design requirements for this design are:

- Supply Voltage: 3.3 V
- Input: 0 µA to 10 µA
- Output: 0.1 V to 3.2 V
- Bandwidth: 50 kHz

8.2.2.2 Detailed Design Procedure

The transfer function between the output voltage (V_{OUT}), the input current, (I_{IN}) and the reference voltage (V_{REF}) is defined in Equation 5.

$$V_{OUT} = I_{IN} \times R_F + V_{REF} \tag{5}$$

Where:

$$V_{REF} = V_+ \times \left(\frac{R_1 \times R_2}{R_1 + R_2} \right) \tag{6}$$

Set V_{REF} to 100 mV to meet the minimum output voltage level by setting R1 and R2 to meet the required ratio calculated in Equation 7.

$$\frac{V_{REF}}{V_+} = \frac{0.1\ V}{3.3\ V} = 0.0303 \tag{7}$$

The closest resistor ratio to meet this ratio sets R1 to 11.5 kΩ and R2 to 357 Ω.

The required feedback resistance can be calculated based on the input current and desired output voltage.

$$R_F = \frac{V_{OUT} - V_{REF}}{I_{IN}} = \frac{3.2\ V - 0.1\ V}{10\ \mu A} = 310 \frac{kV}{A} \approx 309\ k\Omega \tag{8}$$

Calculate the value for the feedback capacitor based RF and the desired –3-dB bandwidth, (f-3dB) using Equation 9.

$$C_F = \frac{1}{2 \times \pi \times R_F \times f_{-3dB}} = \frac{1}{2 \times \pi \times 309\ k\Omega \times 50\ kHz} = 10.3\ pF \approx 10\ pF \tag{9}$$

The minimum op amp bandwidth required for this application is based on the value of R_F, C_F, and the capacitance on the IN– pin of the LMV358A which is equal to the sum of the photodiode shunt capacitance, (CPD) the common-mode input capacitance, (CCM) and the differential input capacitance (CD) as Equation 10 shows.

$$C_{IN} = C_{PD} + C_{CM} + C_D = 47\ pF + 5\ pF + 1\ pF = 53\ pF \tag{10}$$

The minimum op amp bandwidth is calculated in Equation 11.

$$f_{=BGW} \geq \frac{C_{IN} + C_F}{2 \times \pi \times R_F \times {C_F}^2} \geq 324\ kHz \tag{11}$$

The 1-MHz bandwidth of the LMV3xxA meets the minimum bandwidth requirement and remains stable in this application configuration.

Typical Application (continued)

8.2.2.3 Application Curves

The measured current-to-voltage transfer function for photodiode amplifier circuit is shown in Figure 35. The measured DC performance of the photodiode amplifier circuit is shown in Figure 36.

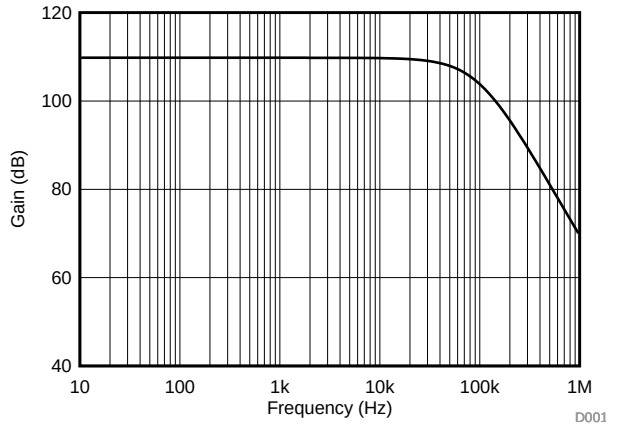


Figure 35. Photodiode Amplifier Circuit AC Gain Results

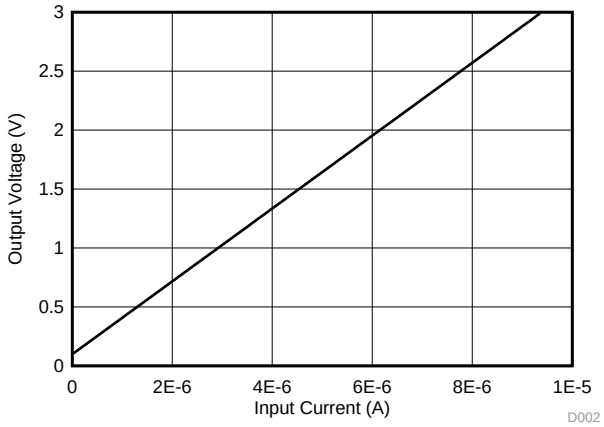


Figure 36. Photodiode Amplifier Circuit DC Results

9 Power Supply Recommendations

The LMV3xxA series is specified for operation from 2.5 V to 5.5 V (±1.25 V to ±2.75 V); many specifications apply from –40°C to +125°C. The section presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V may permanently damage the device; see the table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

9.1 Input and ESD Protection

The LMV3xxA series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10-mA, as stated in the table. Figure 37 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

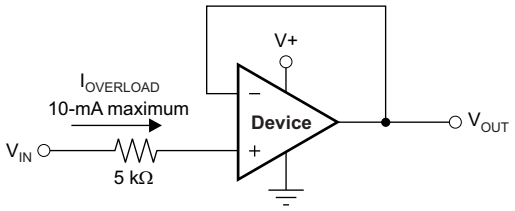


Figure 37. Input Current Protection

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in Figure 39. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

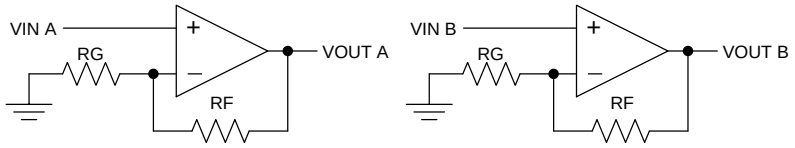


Figure 38. Schematic Representation for Figure 39

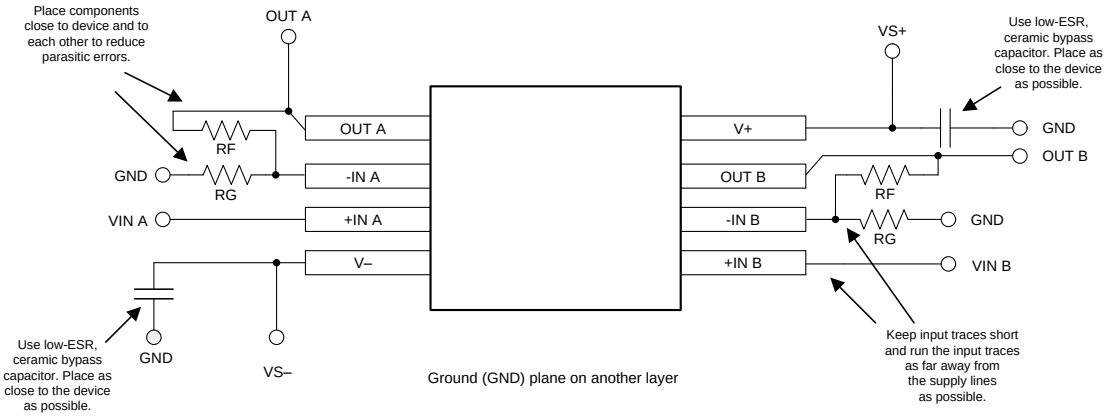


Figure 39. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV321A	Click here	Click here	Click here	Click here	Click here
LMV358A	Click here	Click here	Click here	Click here	Click here
LMV324A	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV321AIDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
LMV321AIDCKR	PREVIEW	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 125		
LMV324AIDR	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 125		
LMV324AIPWR	PREVIEW	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 125		
LMV358AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1MAX	Samples
LMV358AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1MAX	Samples
LMV358AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	MV358A	Samples
PLMV321AIDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PLMV321AIDCKR	ACTIVE	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PLMV324AIDR	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 125		
PLMV324AIPWR	ACTIVE	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

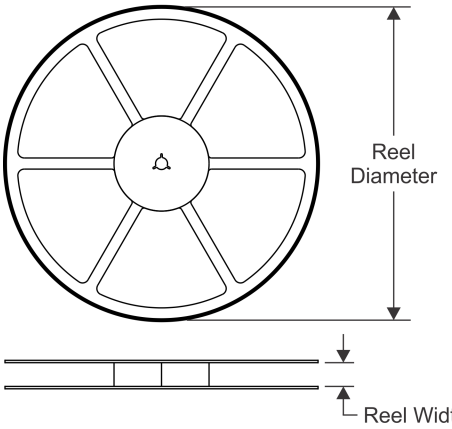
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

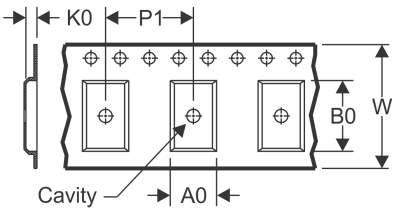
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

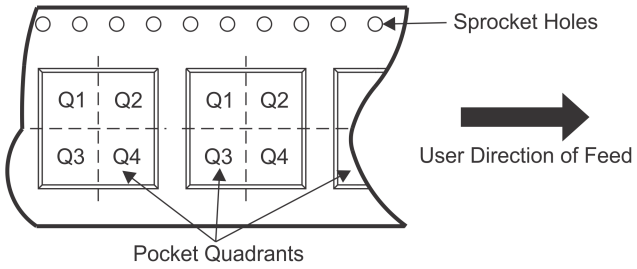


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

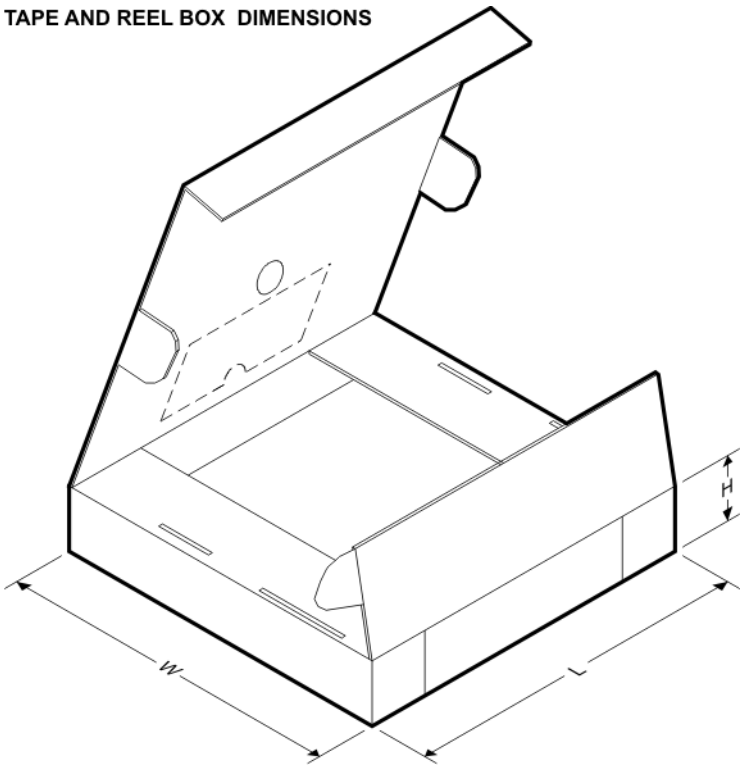
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV358AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358AIDR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1

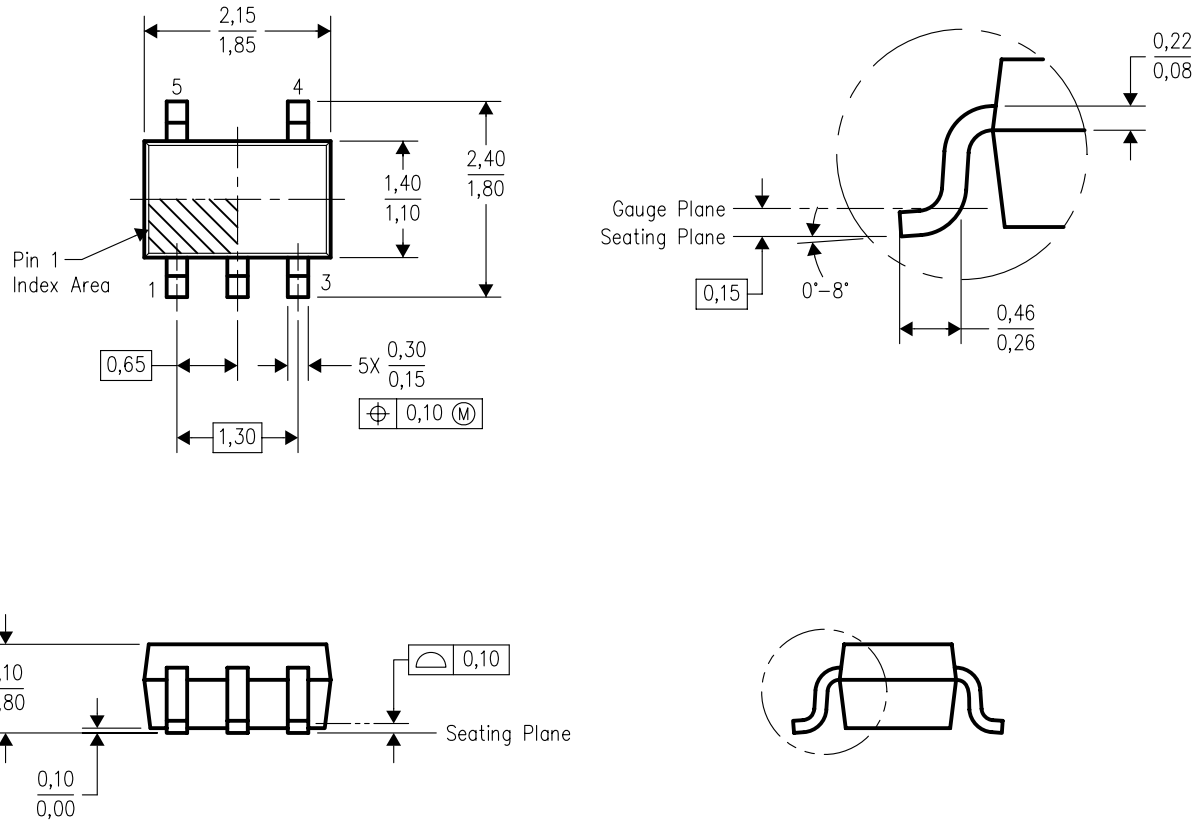
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV358AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LMV358AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
LMV358AIDR	SOIC	D	8	2500	336.6	336.6	41.3

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE

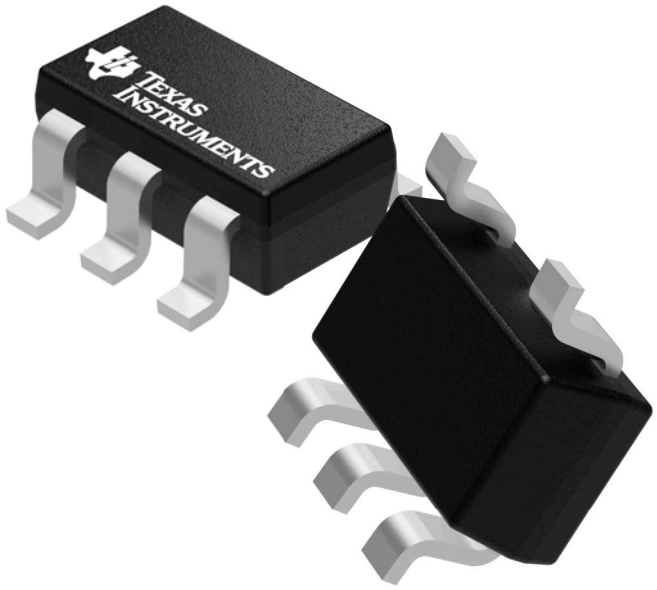


4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



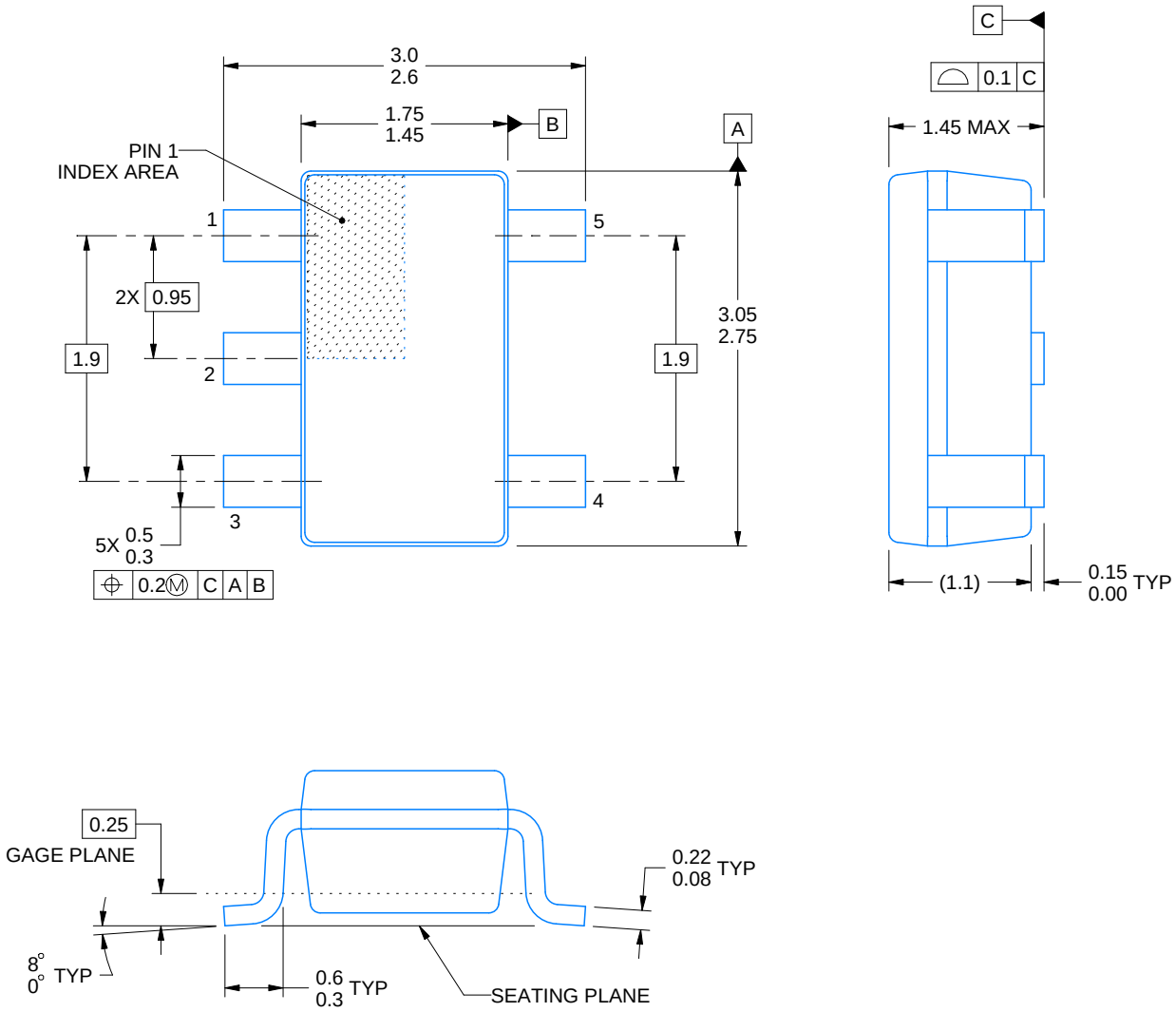
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

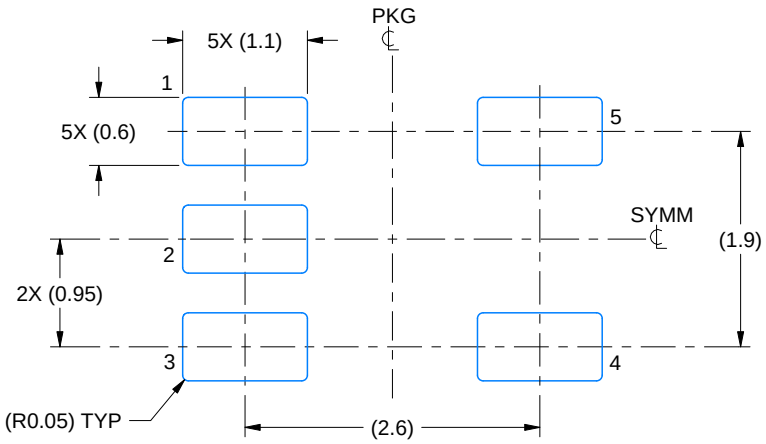
SMALL OUTLINE TRANSISTOR



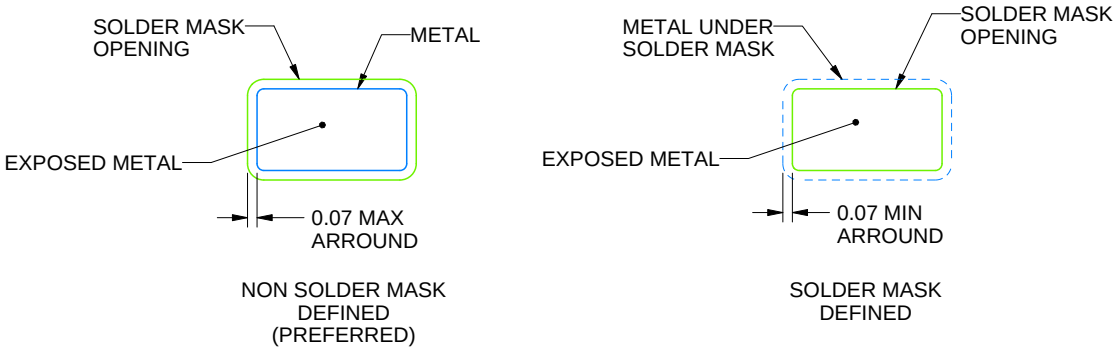
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

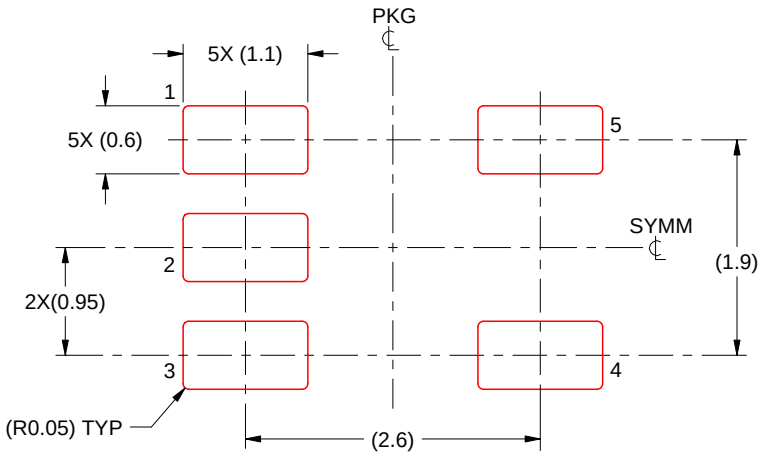


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



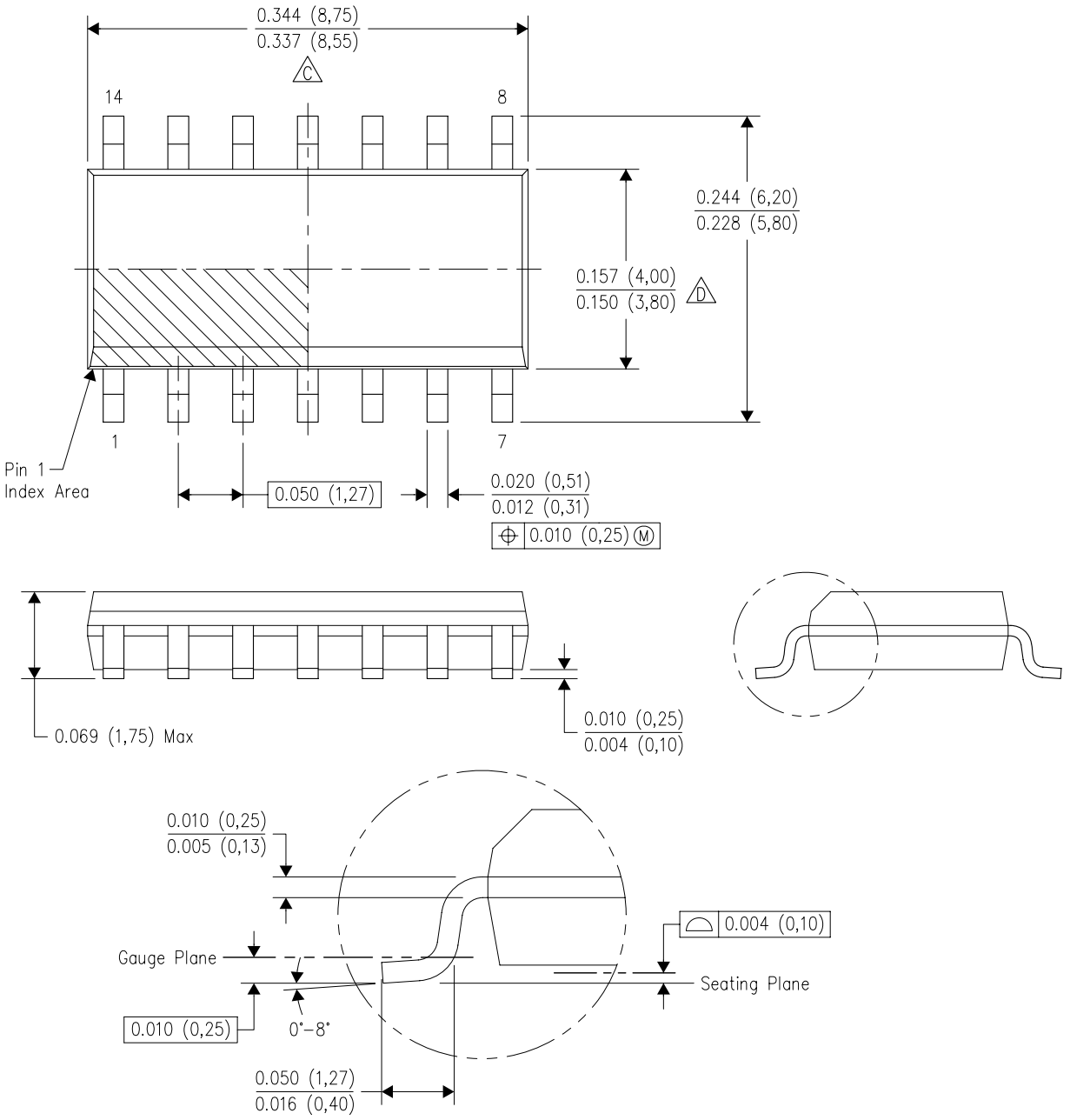
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

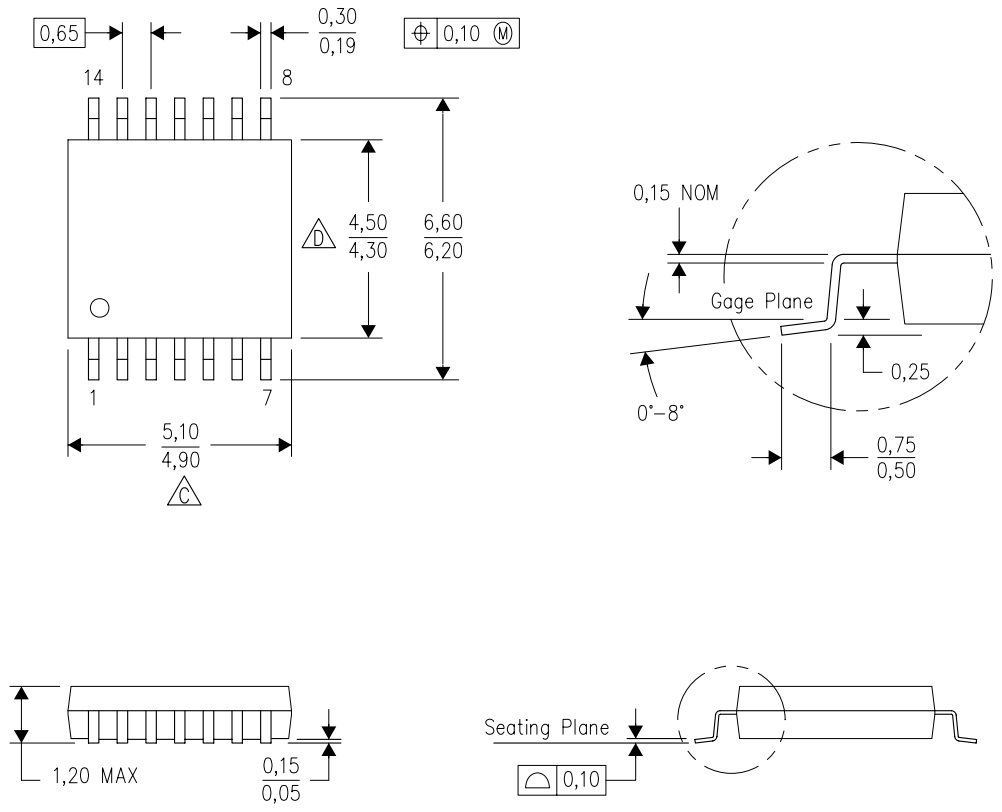
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

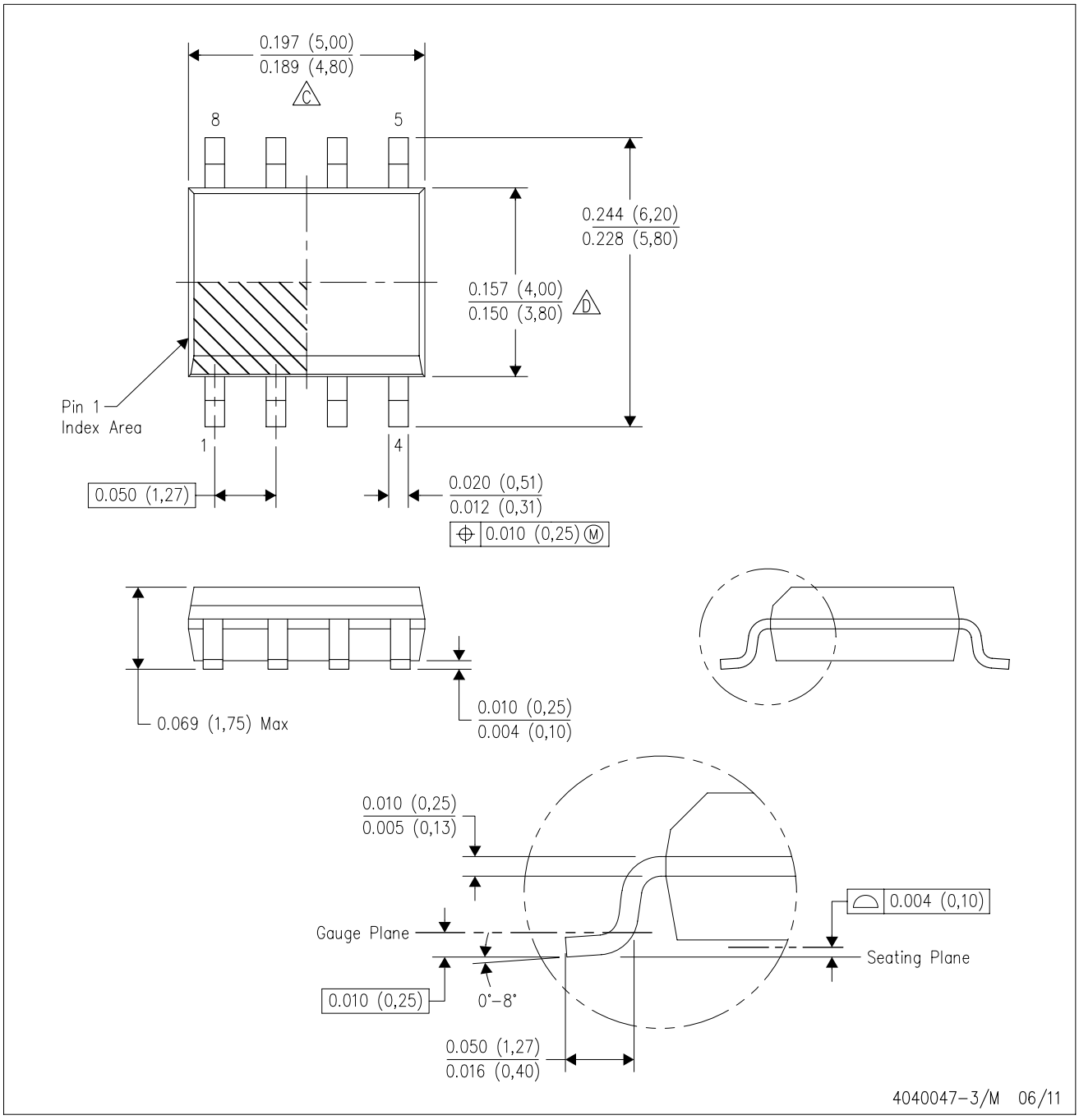
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

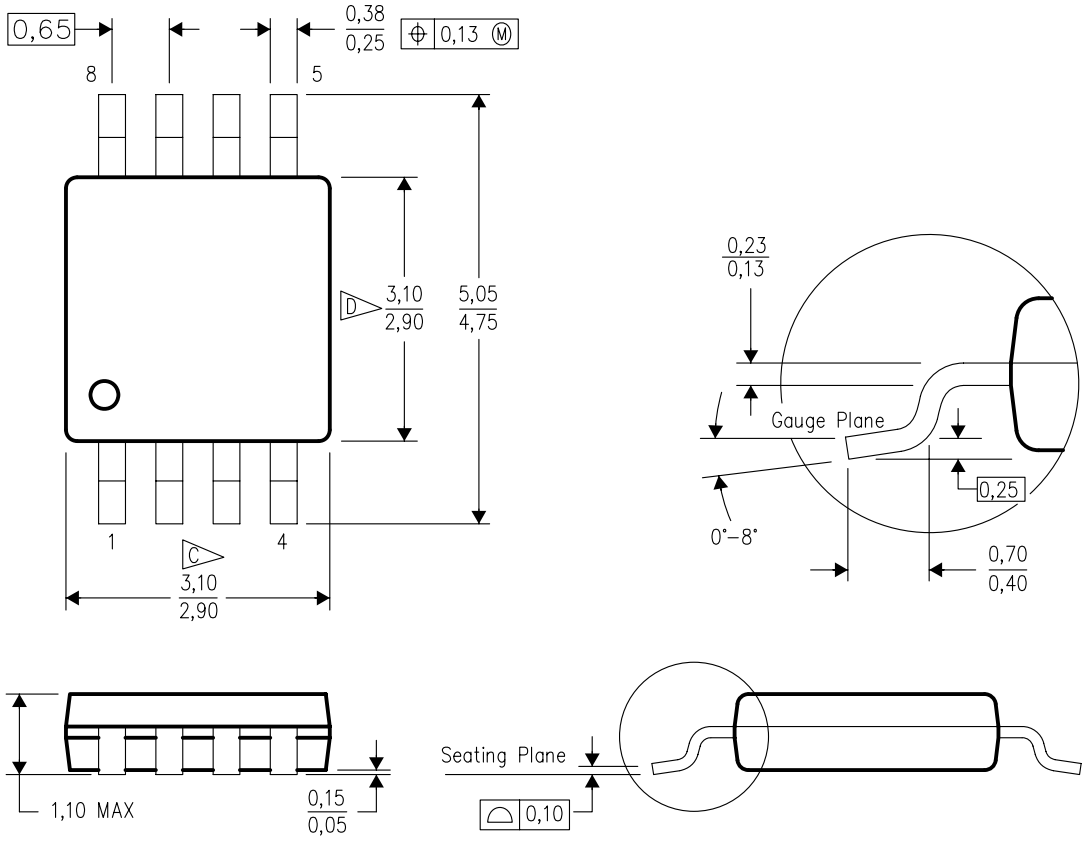
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

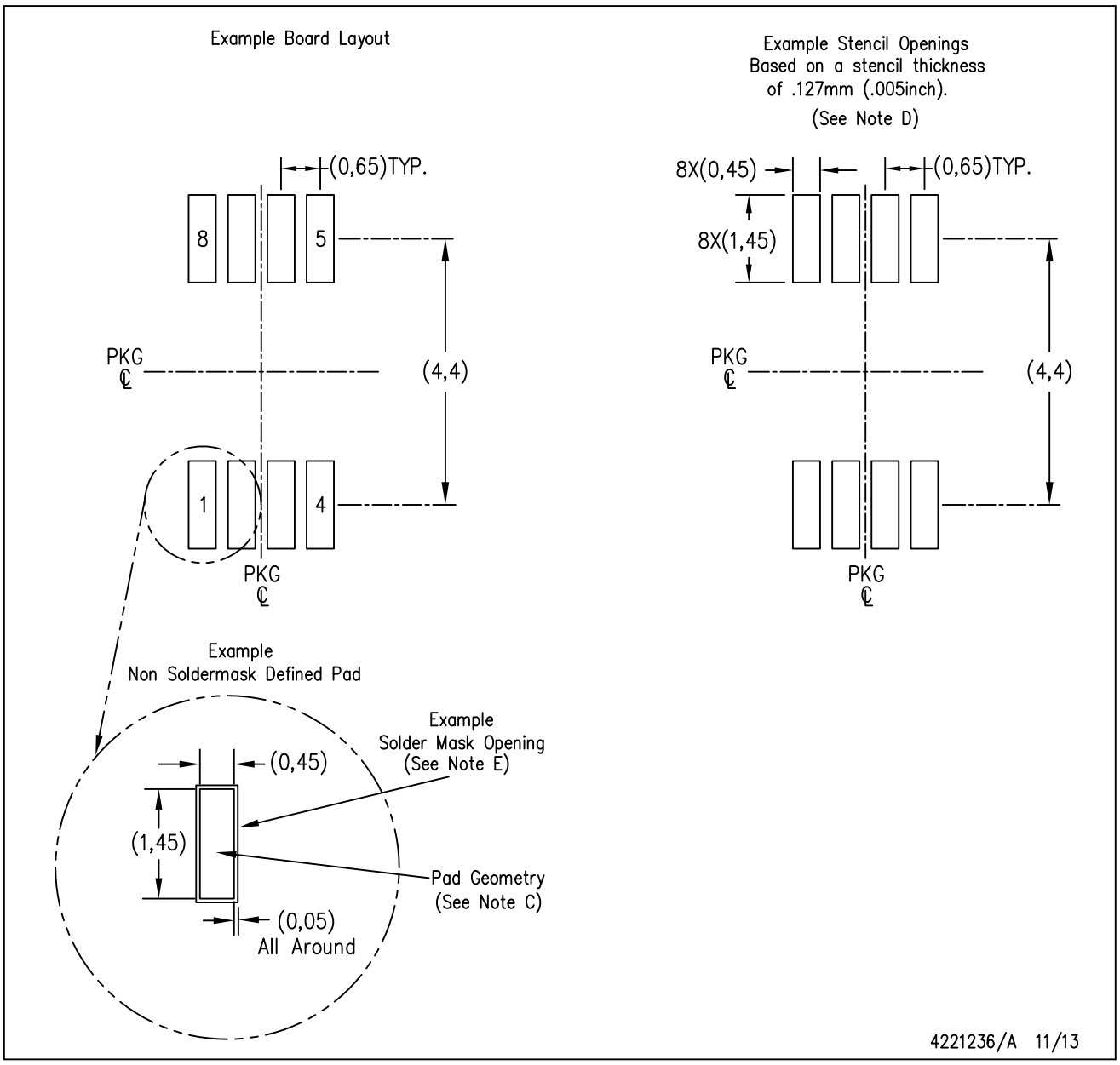
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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