

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

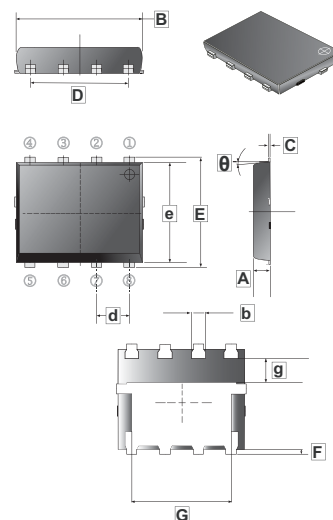
DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

FEATURES

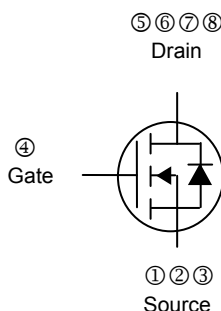
- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe SOP-8PP saves board space.
- Fast switching speed.
- High performance trench technology.

SOP-8PP



PRODUCT SUMMARY

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$V_{DS}(V)$	$R_{DS(on)} (m\Omega)$	$I_D(A)$
200	400@ $V_{GS}=10V$	3.0
	450@ $V_{GS}=4.5V$	2.8



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	1.00	1.10	θ	0°	12°
B	5.70	5.80	b	0.33	0.51
C	0.20	0.30	d	1.27BSC	
D	3.61	3.98	e	1.35	1.75
E	5.40	6.10	g	1.10	-
F	0.08	0.20			
G	3.60	3.99			

ABSOLUTE MAXIMUM RATINGS AND THERMAL DATA($T_A = 25^\circ C$ unless otherwise specified)

PARAMETER	SYMBOL	RATING	UNIT
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	20	V
Continuous Drain Current ^A	I_D	$T_A=25^\circ C$	3
		$T_A=70^\circ C$	2.4
Pulsed Drain Current ^B	I_{DM}	50	A
Continuous Source Current (Diode Conduction) ^A	I_S	2.3	A
Power Dissipation ^A	P_D	$T_A=25^\circ C$	5.0
		$T_A=70^\circ C$	3.2
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 150	$^\circ C$
THERMAL RESISTANCE DATA			
Maximum Junction to Ambient ^A	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	25
	Steady State		65
			$^\circ C / W$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	-	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS} = 0\text{V}$, $V_{GS} = 12\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS} = 160\text{V}$, $V_{GS} = 0\text{V}$
		-	-	5		$V_{DS} = 160\text{V}$, $V_{GS} = 0\text{V}$, $T_J=55^\circ\text{C}$
On-State Drain Current ^A	$I_{D(ON)}$	40	-	-	A	$V_{DS} = 5\text{V}$, $V_{GS} = 10\text{V}$
Drain-Source On-Resistance ^A	$R_{DS(ON)}$	-	-	400	m Ω	$V_{GS} = 10\text{V}$, $I_D = 3\text{A}$
		-	-	450		$V_{GS} = 4.5\text{V}$, $I_D = 2.8\text{A}$
Forward Transconductance ^A	g_{FS}	-	40	-	S	$V_{DS} = 15\text{V}$, $I_D = 3\text{A}$
Diode Forward Voltage	V_{SD}	-	0.7	-	V	$I_S = 2.3\text{A}$, $V_{GS} = 0\text{V}$
Dynamic ^b						
Total Gate Charge	Q_g	-	15	-	nC	$I_D = 6\text{A}$
Gate-Source Charge	Q_{gs}	-	3	-		$V_{DS} = 15\text{V}$
Gate-Drain Charge	Q_{gd}	-	5	-		$V_{GS} = 4.5\text{V}$
Turn-On Delay Time	$T_{d(ON)}$	-	15	-	nS	$I_D = 1\text{A}$, $V_{DD} = 15\text{V}$ $V_{GEN} = 10\text{V}$ $R_L = 6\Omega$
Rise Time	T_r	-	10	-		
Turn-Off Delay Time	$T_{d(OFF)}$	-	54	-		
Fall Time	T_f	-	26	-		

Notes

- a. Pulse test : $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.