CS4270

24-Bit, 192 kHz Stereo Audio CODEC

D/A Features

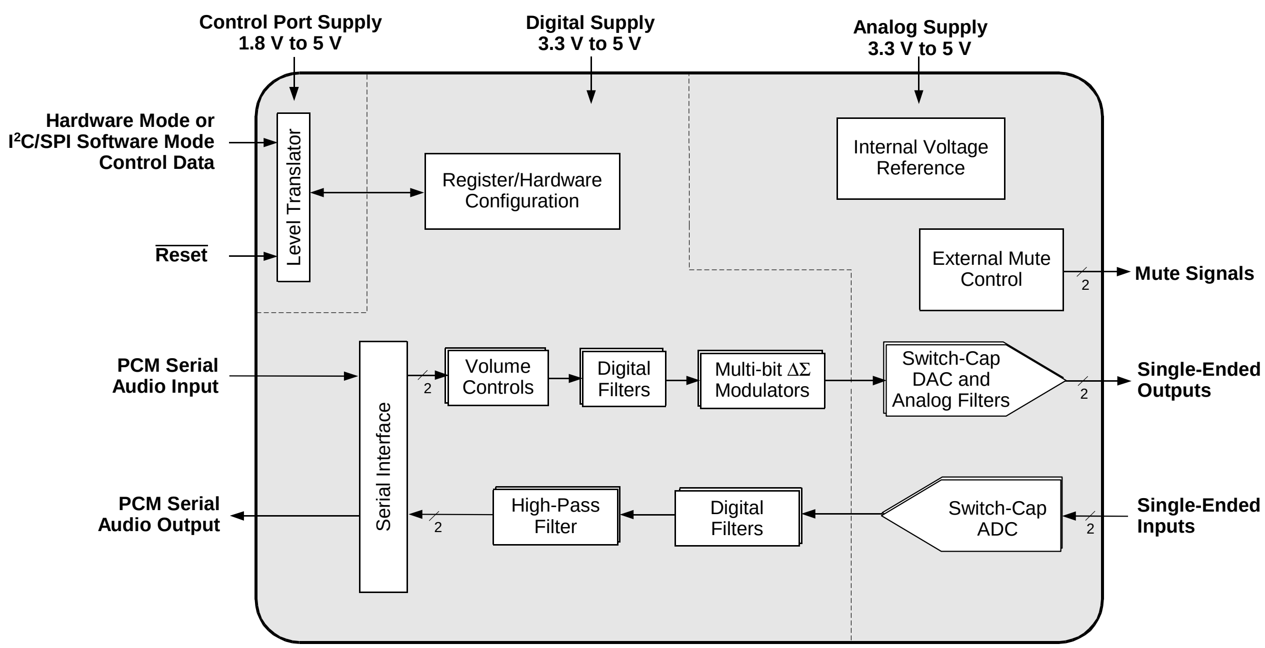
- High Performance
  - 105 dB Dynamic Range
  - -95 dB THD+N
- Selectable Serial Audio Interface Formats
  - Left-Justified up to 24-bit
  - I²S up to 24-bit
  - Right-Justified 16-, and 24-Bit
- Control Output for External Muting
- On-Chip Digital De-Emphasis
- Popguard® Technology
- Multi-bit ΔΣ Conversion
- Digital Volume Control
- Single-Ended Output

A/D Features

- High Performance
  - 105 dB Dynamic Range
  - -95 dB THD+N
- Multi-bit ΔΣ Conversion
- High-Pass Filter to Remove DC Offsets
- Selectable Serial Audio Interface Formats
  - Left-Justified up to 24-bit
  - I²S up to 24-bit
- Single-Ended Input

System Features

- Direct Interface with Logic Levels 1.8 V to 5 V
- Internal Digital Loopback
- Stand-Alone or Control Port Functionality
- Single-Ended Analog Architecture
- Supports all Audio Sample Rates from 4 kHz to 216 kHz
- 3.3 V or 5 V Core Supply



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Stand-Alone Mode Feature Set

- System Features
  - Serial Audio Port Master or Slave Operation
  - Single-, Double-, or Quad-Speed Operation
- D/A Features
  - Auto-Mute on Static Samples
  - 44.1 kHz 50/15 µs De-emphasis Available
  - Selectable Serial Audio Interface Formats
    - Left-Justified up to 24-bit
    - I²S up to 24-bit
- A/D Features
  - High-Pass Filter
  - Selectable Serial Audio Interface Formats
    - Left-Justified up to 24-bit
    - I²S up to 24-bit

Software Mode Feature Set

- System Features
  - Serial Audio Port Master or Slave Operation
  - Internal Digital Loopback Available
- D/A Features
  - Selectable Auto-mute
  - 44.1-kHz De-emphasis Filters
  - Configurable Muting Controls
  - Volume Control
  - Selectable Serial Audio Interface Formats
    - Left-Justified up to 24-bit
    - I²S up to 24-bit
    - Right-Justified 16, and 24-bit
- A/D Features
  - Selectable High-Pass Filter or DC Offset Calibration
  - Selectable Serial Audio Interface Formats
    - Left-Justified up to 24-bit
    - I²S up to 24-bit

General Description

The CS4270 is a high-performance, integrated audio CODEC. The CS4270 performs stereo analog-to-digital (A/D) and digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 216 kHz.

Standard 50/15 µs de-emphasis is available for sampling rates of 44.1 kHz for compatibility with digital audio programs mastered using the 50/15 µs pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS4270 and other devices operating over a wide range of logic levels.

Independently addressable high-pass filters are available for the right and left channel of the A/D. This allows the A/D to be used in a wide variety of applications where one audio channel and one DC measurement channel is desired.

The CS4270 is available in a 24-pin TSSOP package in both Commercial (-10° to +70° C) and Automotive grades (-40° to +85° C). The CDB4270 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 47 for complete ordering information.

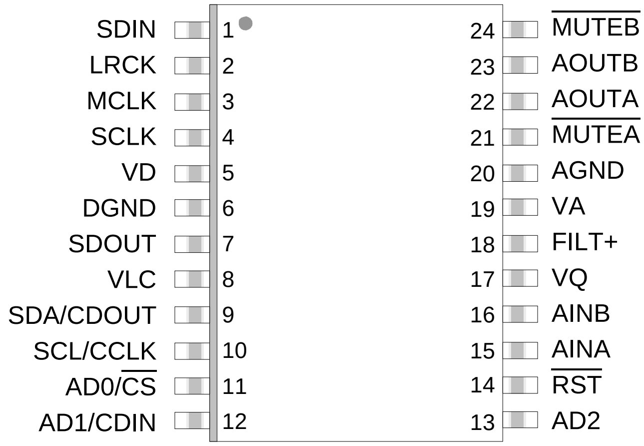
The CS4270's wide dynamic range, negligible distortion, and low noise make it ideal for applications such as DVD-recorders, digital televisions, set-top boxes, effects processors, and automotive audio systems.

TABLE OF CONTENTS

LIST OF FIGURES

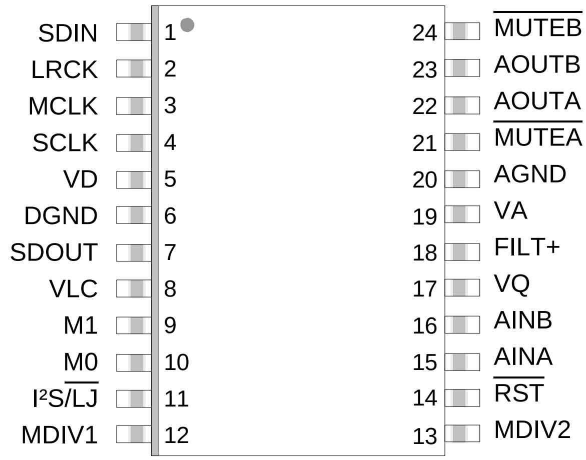
LIST OF TABLES

1. PIN DESCRIPTIONS - SOFTWARE MODE



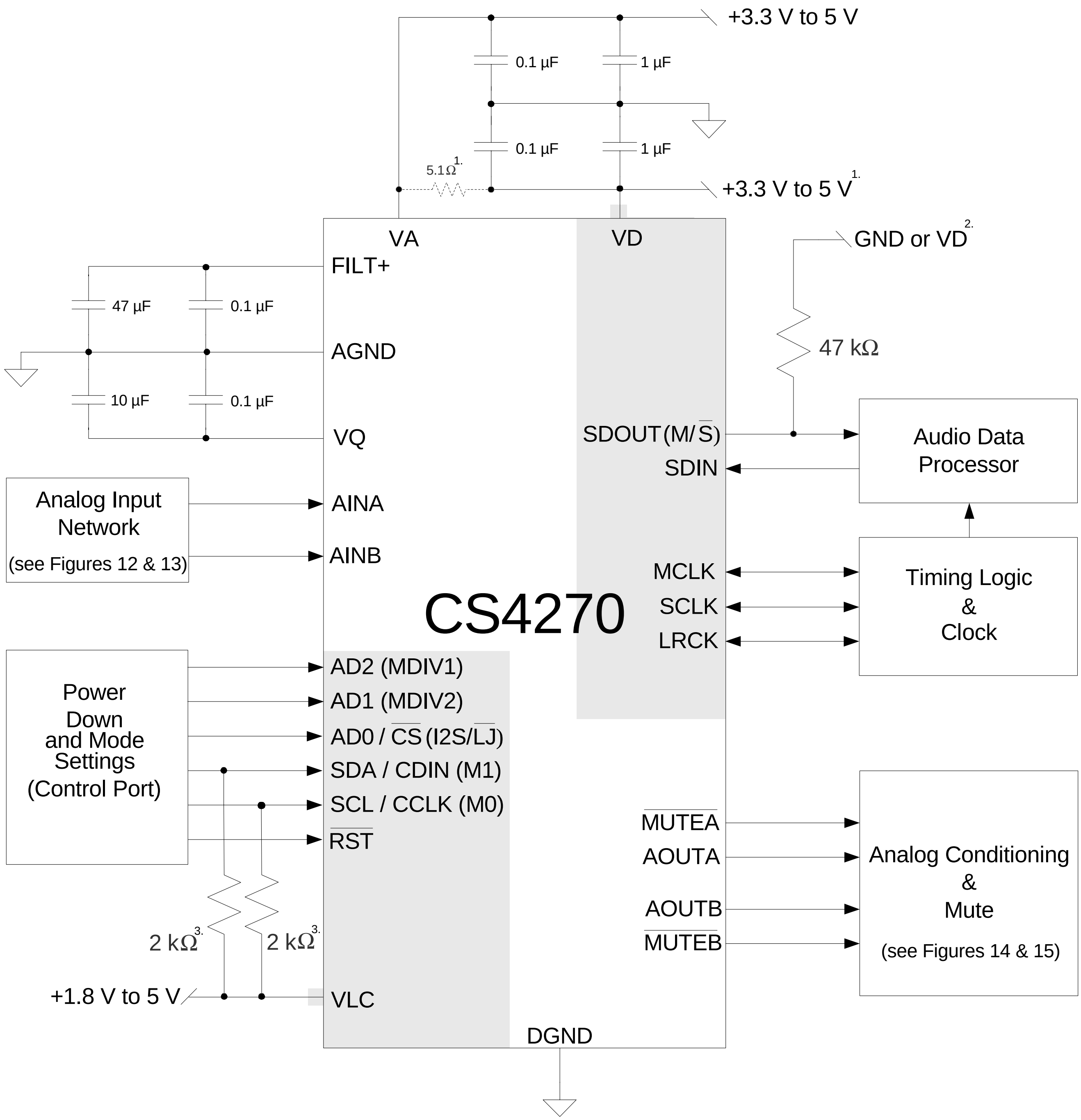
Pin Name	#	Pin Description
SDIN	1	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
LRCK	2	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	3	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
SCLK	4	**Serial Clock** (*Input*/*Output*) - Serial clock for the serial audio interface.
VD	5	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	6	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
SDOUT	7	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
VLC	8	**Control Port Power** (*Input*) - Determines the signal level for the Control Port.
SDA/CDOUT	9	**Serial Control Data** (*Input*/*Output*) - SDA is a data I/O in I²C® Mode. CDOUT is the output data line for the Control Port interface in SPI® Mode.
SCL/CCLK	10	**Serial Control Port Clock** (*Input*) - Serial clock for the serial Control Port.
AD0/$\overline{\text{CS}}$	11	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** *(Input)* - AD0 is a chip address pin in I²C Mode. $\overline{\text{CS}}$ is the chip select signal for SPI format.
AD1/CDIN	12	**Address Bit 1 (I²C) / Serial Control Data** (*Input*) - AD1 is a chip address pin in I²C Mode. CDIN is the input data line for the Control Port interface in SPI Mode.
AD2	13	**Address Bit 2 (I²C)** (*Input*) - AD2 is a chip address pin in I²C Mode.
$\overline{\text{RST}}$	14	**Reset** (*Input*) - The device enters a low power mode when low.
AINA AINB	15 16	**Analog Input** (*Input*) - The full-scale analog input level is specified in the ADC Analog Characteristics specification table.
VQ	17	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
VA	19	**Analog Power** (*Input*) - Positive power for the analog sections.
AGND	20	**Analog Ground** (*Input*) - Ground reference. Must be connected to analog ground.
$\overline{\text{MUTEA}}$ $\overline{\text{MUTEB}}$	21 24	**Mute Control** *(Output)* - Each pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
AOUTA AOUTB	22 23	**Analog Audio Output** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table.

2. PIN DESCRIPTIONS - STAND-ALONE MODE



Pin Name	#	Pin Description
SDIN	1	**Serial Audio Data Input (*Input*)** - Input for two's complement serial audio data.
LRCK	2	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	3	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
SCLK	4	**Serial Clock (*Input*/*Output*)** - Serial clock for the serial audio interface.
VD	5	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	6	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
SDOUT (M/$\overline{\text{S}}$)	7	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data. This pin must be pulled-up or pulled-down to select Master or Slave Mode.
VLC	8	**Control Port Power** (*Input*) - Determines the signal level for the Control Port.
M1 M0	9 10	**Mode Selection** (*Input*) - Determines the operational mode of the device.
I²S/$\overline{\text{LJ}}$	11	**Serial Audio Interface Select** *(Input)* - Selects either the Left-Justified or I²S format for the Serial Audio Interface.
MDIV1 MDIV2	12 13	**MCLK Divide** (*Input*) - Configures MCLK divider to divide by 1, 1.5, 2, or 4.
$\overline{\text{RST}}$	14	**Reset** (*Input*) - The device enters a low power mode when low.
AINA AINB	15 16	**Analog Input** (*Input*) - The full-scale analog input level is specified in the ADC Analog Characteristics specification table.
VQ	17	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
VA	19	**Analog Power (*Input*)** - Positive power for the analog sections.
AGND	20	**Analog Ground** (*Input*) - Ground reference. Must be connected to analog ground.
$\overline{\text{MUTEA}}$ $\overline{\text{MUTEB}}$	21 24	**Mute Control** *(Output)* - Each pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
AOUTA AOUTB	22 23	**Analog Audio Output** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table.

3. TYPICAL CONNECTION DIAGRAM



1. If using separate supplies for VA and VD, 5.1 Ω resistor not needed. See "Grounding and Power Supply Decoupling."

2. Use a 47 kΩ pull-down to select Slave Mode or 47 kΩ pull-up to VD to select Master Mode. See "Master/Slave Mode Selection."

3. Use pull-up resistors in Software Mode. In Hardware Mode, use pull-up or pull-down. See "Mode Selection & De-Emphasis."

Figure 1. CS4270 Typical Connection Diagram

4. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Analog	VA	3.1	5.0	5.25	V
	Digital	VD	3.1	3.3	5.25	V
	Control Port Interface	VLC	1.7	3.3	5.25	V
Ambient Operating Temperature (Power Applied)	Commercial	T_A	-10	-	+70	°C
	Automotive		-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V, All voltages with respect to ground.) (Note 1)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Analog	VA	-0.3	-	+6.0	V
	Digital	VD	-0.3	-	+6.0	V
	Control Port Interface	VLC	-0.3	-	+6.0	V
Input Current	(Note 2)	I_{in}	-10	-	+10	mA
Analog Input Voltage		V_{IN}	AGND-0.7	-	VA+0.7	V
Digital Input Voltage	Control Port Interface	V_{IND-C}	-0.3	-	VLC+0.3	V
	Digital Interface	V_{IND-D}	-0.3		VD+0.3	V
Ambient Operating Temperature (Power Applied)		T_{AC}	-50	-	+95	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes:

1. Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SRC latch-up.

THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Allowable Junction Temperature			-	-	135	°C
Junction to Ambient Thermal Impedance (Note 3)						
	(Multi-layer PCB) TSSOP	θ_{JA-M}	-	70	-	°C/W
	(Single-layer PCB) TSSOP	θ_{JA-S}	-	105	-	°C/W

3. θ_{JA} is specified according to JEDEC specifications for multi-layer PCBs.

DAC ANALOG CHARACTERISTICS - COMMERCIAL GRADE

(Full-Scale Output Sine Wave, 997 Hz (Note 4), Fs = 48/96/192 kHz; Test load R_L = 3 kΩ, C_L = 10 pF (see Figure 2). Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.)

Parameter			VA = 5 V Min	VA = 5 V Typ	VA = 5 V Max	VA = 3.3 V Min	VA = 3.3 V Typ	VA = 3.3 V Max	Unit
Dynamic Range	18 to 24-Bit	A-weighted	99	105	-	97	103	-	dB
		unweighted	96	102	-	94	100	-	dB
	16-Bit	A-weighted	90	96	-	90	96	-	dB
		unweighted	87	93	-	87	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-89	-83	-	-89	-83	dB
		-20 dB	-	-76	-70	-	-76	-70	dB
		-60 dB	-	-36	-30	-	-36	-30	dB
	16-Bit	0 dB	-	-87	-81	-	-87	-81	dB
		-20 dB	-	-67	-61	-	-67	-61	dB
		-60 dB	-	-27	-21	-	-27	-21	dB

DAC ANALOG CHARACTERISTICS - AUTOMOTIVE GRADE

(Full-Scale Output Sine Wave, 997 Hz (Note 4), Fs = 48/96/192 kHz; Test load R_L = 3 kΩ, C_L = 10 pF (see Figure 2). Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.)

Parameter			VA = 5 V Min	VA = 5 V Typ	VA = 5 V Max	VA = 3.3 V Min	VA = 3.3 V Typ	VA = 3.3 V Max	Unit
Dynamic Range	18 to 24-Bit	A-weighted	95	105	-	93	103	-	dB
		unweighted	92	102	-	90	100	-	dB
	16-Bit	A-weighted	86	96	-	86	96	-	dB
		unweighted	83	93	-	83	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-89	-79	-	-89	-79	dB
		-20 dB	-	-76	-66	-	-76	-66	dB
		-60 dB	-	-36	-26	-	-36	-26	dB
	16-Bit	0 dB	-	-87	-77	-	-87	-77	dB
		-20 dB	-	-67	-57	-	-67	-57	dB
		-60 dB	-	-27	-17	-	-27	-17	dB

4. One-half LSB of triangular PDF dither added to data.

DAC ANALOG CHARACTERISTICS - ALL MODES

Parameter		Symbol	Min	Typ	Max	Unit
Interchannel Isolation	(1 kHz)		-	100	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	0.25	dB
Gain Drift			-100		+100	ppm/°C
Analog Output						
Full Scale Output Voltage			0.6•VA	0.65•VA	0.7•VA	Vpp
Max DC Current draw from AOUTA or AOUTB		I_{OUTmax}	-	10	-	µA
Max AC-Load Resistance (see Figure 3)		R_L	-	3	-	kΩ
Max Load Capacitance (see Figure 3)		C_L	-	100	-	pF
Output Impedance of AOUTA and AOUTB		Z_{OUT}	-	100	-	Ω

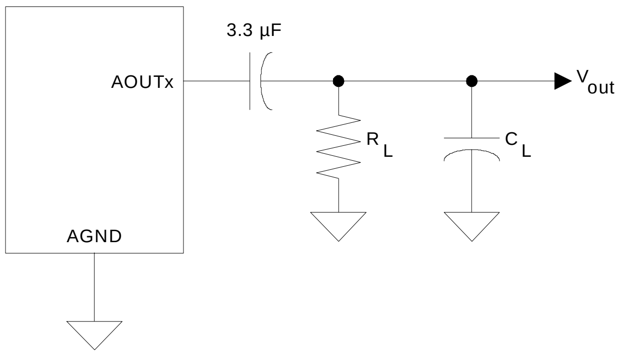


Figure 2. Output Test Load

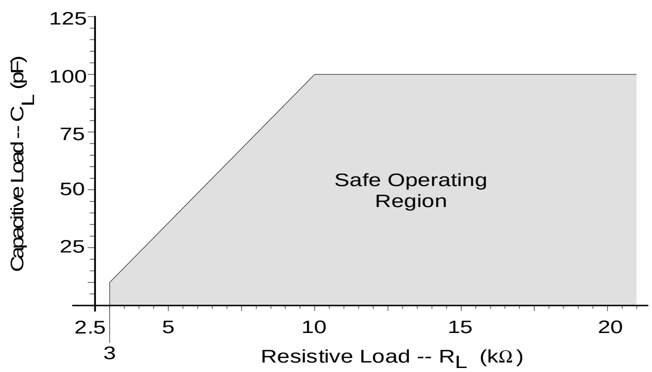


Figure 3. Maximum Loading

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.) (See Note 5)

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Passband (Note 6)	to -0.1 dB corner to -3 dB corner		0 0	- -	.35 .4992	Fs Fs
Frequency Response 10 Hz to 20 kHz			-.175	-	+.01	dB
StopBand			.5465	-	-	Fs
StopBand Attenuation	(Note 7)		50	-	-	dB
Group Delay		tgd	-	10/Fs	-	s
De-emphasis Error (Note 8)	Fs = 32 kHz Fs = 44.1 kHz Fs = 48 kHz		- - -	- - -	+1.5/+0 +.05/-.25 -.2/-.4	dB dB dB
Double-Speed Mode						
Passband (Note 6)	to -0.1 dB corner to -3 dB corner		0 0	- -	.22 .501	Fs Fs
Frequency Response 10 Hz to 20 kHz			-.15	-	+.15	dB
StopBand			.5770	-	-	Fs
StopBand Attenuation	(Note 7)		55	-	-	dB
Group Delay		tgd	-	5/Fs	-	s
Quad-Speed Mode						
Passband (Note 6)	to -0.1 dB corner to -3 dB corner		0 0	- -	0.110 0.469	Fs Fs
Frequency Response 10 Hz to 20 kHz			-.12	-	+0	dB
StopBand			0.7	-	-	Fs
StopBand Attenuation	(Note 7)		51	-	-	dB
Group Delay		tgd	-	2.5/Fs	-	s

5. Amplitude vs. Frequency plots of this data are available in Section 9. “Filter Plots” on page 41. See Figures 24 through 47.
6. Response is clock dependent and will scale with Fs.
7. For Single-Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
   For Double-Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.
   For Quad-Speed Mode, the Measurement Bandwidth is 0.7 Fs to 1 Fs.
8. De-emphasis is available only in Single-Speed Mode.

ADC ANALOG CHARACTERISTICS - COMMERCIAL GRADE

Measurement bandwidth is 10 Hz to 20 kHz unless otherwise specified. Figure 18 input circuit, 1 kHz sine wave in.

Dynamic Performance for Commercial Grade			VA = 5 V			VA = 3.3 V			
Single-Speed Mode	**Fs = 48 kHz**	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Dynamic Range	A-weighted unweighted		99 96	105 102	- -	96 93	102 99	- -	dB dB
Total Harmonic Distortion + Noise	(Note 9) -1 dB -20 dB -60 dB	THD+N	- - -	-95 -82 -42	-90 - -	- - -	-92 -79 -39	-87 - -	dB dB dB
Double-Speed Mode	**Fs = 96 kHz**								
Dynamic Range	A-weighted unweighted 40 kHz bandwidth unweighted		99 96 -	105 102 99	- - -	96 93 -	102 99 96	- - -	dB dB dB
Total Harmonic Distortion + Noise	(Note 9) -1 dB -20 dB -60 dB 40 kHz bandwidth -1 dB	THD+N	- - - -	-95 -82 -42 -95	-90 - - -	- - - -	-92 -79 -39 -87	-87 - - -	dB dB dB dB
Quad-Speed Mode	**Fs = 192 kHz**								
Dynamic Range	A-weighted unweighted 40 kHz bandwidth unweighted		99 96 -	105 102 99	- - -	96 93 -	102 99 96	- - -	dB dB dB
Total Harmonic Distortion + Noise	(Note 9) -1 dB -20 dB -60 dB 40 kHz bandwidth -1 dB	THD+N	- - - -	-95 -82 -42 -95	-90 - - -	- - - -	-92 -79 -39 -87	-87 - - -	dB dB dB dB

Dynamic Performance for Commercial Grade - All Modes					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Interchannel Isolation		-	90	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error		-3	-	+3	%
Gain Drift		-	±100	-	ppm/°C
Analog Input Characteristics					
Full-Scale Input Voltage		0.53*VA	0.56*VA	0.58*VA	Vpp
Input Impedance		-	300	-	kΩ

9. Referred to the typical full-scale input voltage.

ADC ANALOG CHARACTERISTICS - AUTOMOTIVE GRADE

Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Figure 18 input circuit, 1 kHz sine wave in.

Dynamic Performance for Automotive Grade			VA = 5 V			VA = 3.3 V			
Single-Speed Mode	**Fs = 48 kHz**	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Dynamic Range	A-weighted unweighted		97 94	105 102	- -	94 91	102 99	- -	dB dB
Total Harmonic Distortion + Noise	(Note 10) -1 dB -20 dB -60 dB	THD+N	- - -	-95 -82 -42	-90 - -	- - -	-92 -79 -39	-87 - -	dB dB dB
Double-Speed Mode	**Fs = 96 kHz**								
Dynamic Range	A-weighted unweighted 40 kHz bandwidth unweighted		97 94 -	105 102 99	- - -	94 91 -	102 99 96	- - -	dB dB dB
Total Harmonic Distortion + Noise	(Note 10) -1 dB -20 dB -60 dB 40 kHz bandwidth -1 dB	THD+N	- - - -	-95 -82 -42 -95	-90 - - -	- - - -	-92 -79 -39 -87	-87 - - -	dB dB dB dB
Quad-Speed Mode	**Fs = 192 kHz**								
Dynamic Range	A-weighted unweighted 40 kHz bandwidth unweighted		97 94 -	105 102 99	- - -	94 91 -	102 99 96	- - -	dB dB dB
Total Harmonic Distortion + Noise	(Note 10) -1 dB -20 dB -60 dB 40 kHz bandwidth -1 dB	THD+N	- - - -	-95 -82 -42 -95	-90 - - -	- - - -	-92 -79 -39 -87	-87 - - -	dB dB dB dB

Dynamic Performance for Automotive Grade - All Modes					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Interchannel Isolation		-	90	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error		-3	-	+3	%
Gain Drift		-	±100	-	ppm/°C
Analog Input Characteristics					
Full-Scale Input Voltage		0.53*VA	0.56*VA	0.58*VA	Vpp
Input Impedance		-	300	-	kΩ

10. Referred to the typical full-scale input voltage.

ADC DIGITAL FILTER CHARACTERISTICS

(Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified) (Note 11)

Parameter	Symbol	Min	Typ	Max	Unit
Single-Speed Mode					
Passband (-0.1 dB) (Note 12)		0	-	0.49	Fs
Passband Ripple		-	-	0.035	dB
Stopband (Note 12)		0.57	-	-	Fs
Stopband Attenuation		70	-	-	dB
Group Delay	t_{gd}	-	12/Fs	-	s
Double-Speed Mode					
Passband (-0.1 dB) (Note 12)		0	-	0.49	Fs
Passband Ripple		-	-	0.05	dB
Stopband (Note 12)		0.56	-	-	Fs
Stopband Attenuation		69	-	-	dB
Group Delay	t_{gd}	-	9/Fs	-	s
Quad-Speed Mode					
Passband (-0.1 dB) (Note 12)		0	-	0.26	Fs
Passband Ripple		-	-	0.05	dB
Stopband (Note 12)		0.50	-	-	Fs
Stopband Attenuation		60	-	-	dB
Group Delay	t_{gd}	-	5/Fs	-	s
High-Pass Filter Characteristics					
Frequency Response -3.0 dB -0.13 dB (Note 13)		-	1 20	- -	Hz Hz
Phase Deviation @ 20 Hz (Note 13)		-	10	-	deg
Passband Ripple		-	-	0	dB

11. Plots of this data are contained in Section 9. "Filter Plots" on page 41. See Figures 24 through 47.
12. The filter frequency response scales precisely with Fs.
13. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

DC ELECTRICAL CHARACTERISTICS

(T_A = 25° C; AGND=DGND=0, all voltages with respect to ground; MLCK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply						
Power Supply Current (Normal Operation)	VA = 5 V	I_A	-	31	40	mA
	VA = 3.3 V	I_A	-	27	35	mA
	VD, VLC = 5 V	I_D	-	29	38	mA
	VD, VLC = 3.3 V	I_D	-	20	29	mA
Power Supply Current (Power-Down Mode) (Note 14)	VA = 5 V	I_A	-	1.51	-	mA
	VD, VLC = 5 V	I_D	-	0.45	-	mA
Power Consumption VA = 5 V, VD = VLC= 3.3 V	Normal Operation	-	-	221	296	mW
VA = 5 V, VD = VLC = 5 V	Normal Operation	-	-	255	-	mW
	Power-Down Mode (Note 14)	-	-	9.8	323	mW
Power Supply Rejection Ratio (1 kHz)	(Note 15)	PSRR	-	55	-	dB
Common Mode Voltage						
Nominal Common Mode Voltage		VQ	-	VA/2	-	VDC
Maximum DC Current Source/Sink from VQ			-	1	-	µA
VQ Output Impedance			-	25	-	kΩ
Positive Voltage Reference						
FILT+ Nominal Voltage		FILT+	-	VA	-	VDC
Maximum DC Current Source/Sink from FILT+			-	10	-	µA
FILT+ Output Impedance			-	18	-	kΩ
Mute Control						
MUTEA, MUTEB Low-Level Output Voltage			-	0	-	V
MUTEA, MUTEB High-Level Output Voltage			-	VA	-	V
Maximum MUTEA & MUTEB Drive Current			-	3	-	mA

14. Power Down Mode is defined as $\overline{RST}$ = Low with all clocks and data lines held static.

15. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS

Parameter (Note 16)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Serial Port	V_{IH}	0.7xVD	-	-	V
	Control Port		0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	V_{IL}	-	-	0.2xVD	V
	Control Port		-	-	0.2xVLC	V
High-Level Output Voltage at I_o = 2 mA	Serial Port	V_{OH}	VD - 1.0	-	-	V
	Control Port		VLC - 1.0	-	-	V
	MUTEA, MUTEB		VA - 1.0	-	-	V
Low-Level Output Voltage at I_o = 2 mA		V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-10	-	10	µA

16. Serial Port signals include: SCLK, LRCK, SDOUT, SDIN
Control Port signals include: SDA/CDOUT, SCL/CCLK, AD1/CDIN, AD0/$\overline{CS}$, $\overline{RST}$

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

(Logic "0" = AGND = 0 V; Logic "1" = VD, C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rate	Single-Speed Mode Double-Speed Mode Quad-Speed Mode	Fs Fs Fs	4 50 100	- - -	54 108 216	kHz kHz kHz
MCLK Specifications						
MCLK Frequency (Note 17)	tand-Alone Mode Control Port Mode	f_{mclk} f_{mclk}	1.024 1.024	- -	55.296 55.296	MHz MHz
MCLK Duty Cycle			40	50	60	ns
Master Mode						
LRCK Duty Cycle			-	50	-	%
SCLK Period (Note 18)		t_{sclkw}	-	$\frac{1}{(64)Fs}$	-	s
SCLK Duty Cycle			-	50	-	%
SCLK falling to LRCK edge		t_{mslr}	-20	-	20	ns
SCLK falling to SDOUT valid		t_{sdo}	-	-	32	ns
SDIN valid to SCLK rising setup time		t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time		t_{sdih}	20	-	-	ns
Slave Mode						
LRCK Duty Cycle			40	50	60	%
SCLK Period (Note 17)	Single-Speed Mode Double-Speed Mode Quad-Speed Mode	t_{sclkw} t_{sclkw} t_{sclkw}	$\frac{1}{(128)Fs}$ $\frac{1}{(64)Fs}$ $\frac{1}{(64)Fs}$	- - -	- - -	s s s
SCLK Duty Cycle			45	50	55	ns
SCLK falling to LRCK edge		t_{slrd}	-20	-	20	ns
SDOUT valid before SCLK rising		t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising		t_{hld}	5	-	-	ns
SDIN valid to SCLK rising setup time		t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time		t_{sdih}	20	-	-	ns

17. In Control Port Mode, MCLK Frequency and Functional Mode Select bits must be configured according to Table 5, Table 8, and Table 12.

18. $t_{sclkw} = t_{sclkh} + t_{sclkl}$ in Figures 5 and 7.

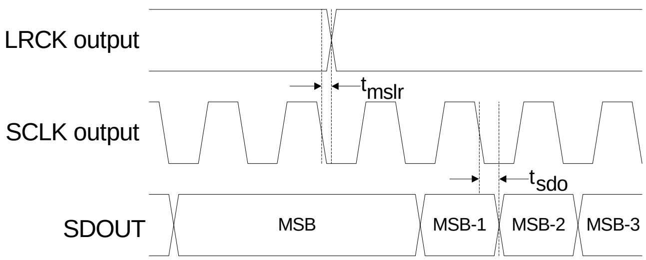


Figure 4. Master Mode, Left-Justified SAI

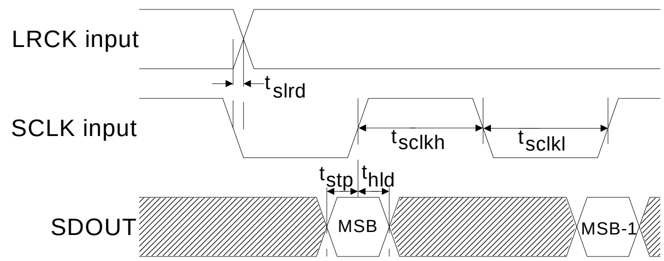


Figure 5. Slave Mode, Left-Justified SAI

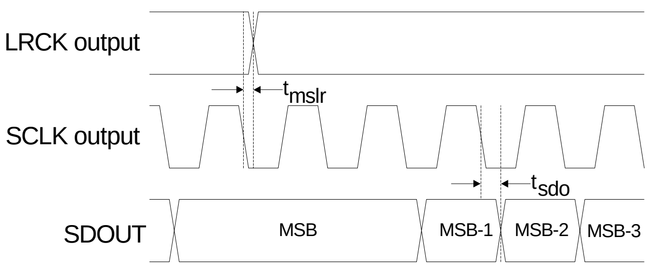


Figure 6. Master Mode, I²S SAI

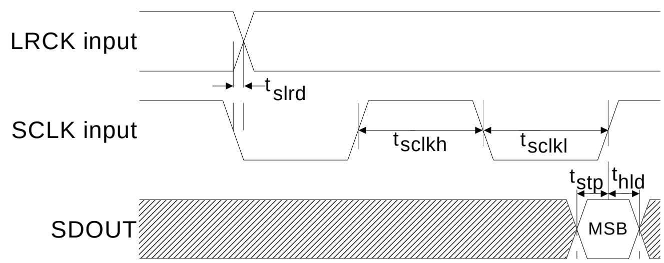


Figure 7. Slave Mode, I²S SAI

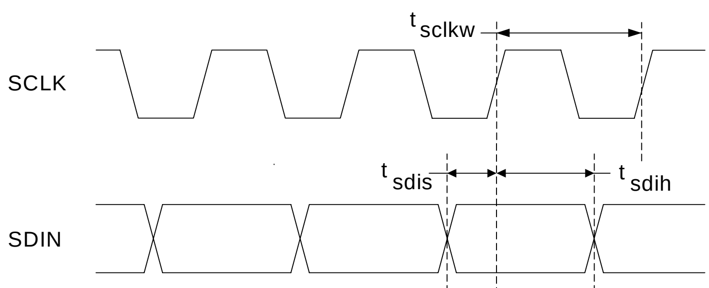


Figure 8. Master and Slave Mode SDIN vrs. SCLK

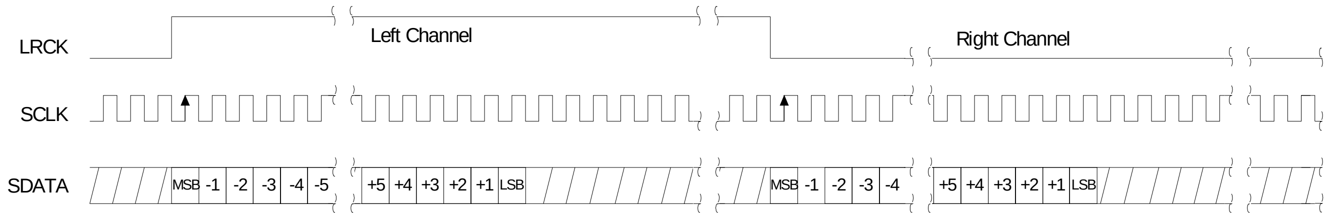


Figure 9. Format 0, Left-Justified up to 24-Bit Data

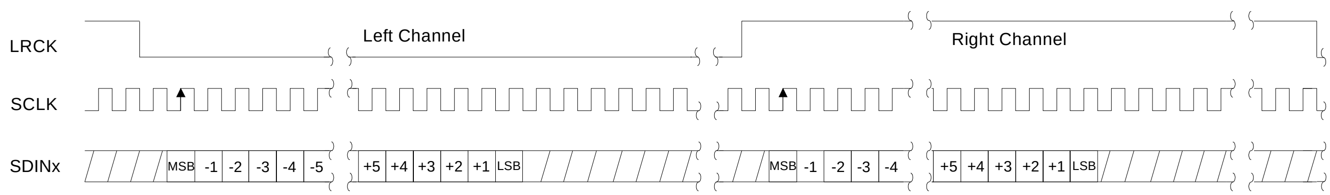


Figure 10. Format 1, I²S up to 24-Bit Data

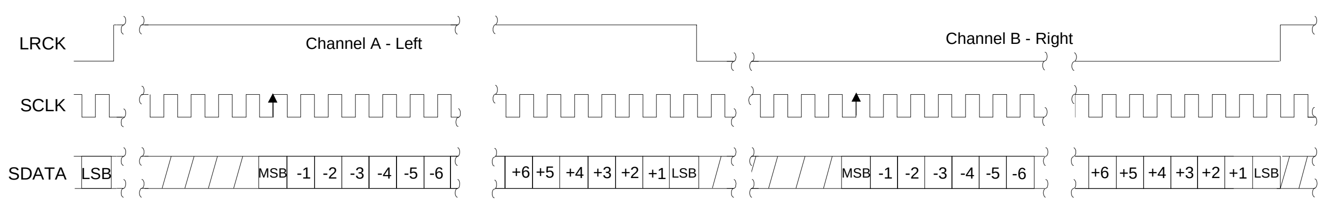


Figure 11. Format 2, Right-Justified 16-Bit Data. (Available in Control Port Mode only)
Format 3, Right-Justified 24-Bit Data. (Available in Control Port Mode only)

SWITCHING CHARACTERISTICS - I²C MODE CONTROL PORT

(Inputs: logic 0 = DGND, logic 1 = VLC)

Parameter	Symbol	Min	Max	Unit
I²C Mode				
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 19)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	1	µs
Fall Time of Both SDA and SCL Lines	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

19. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

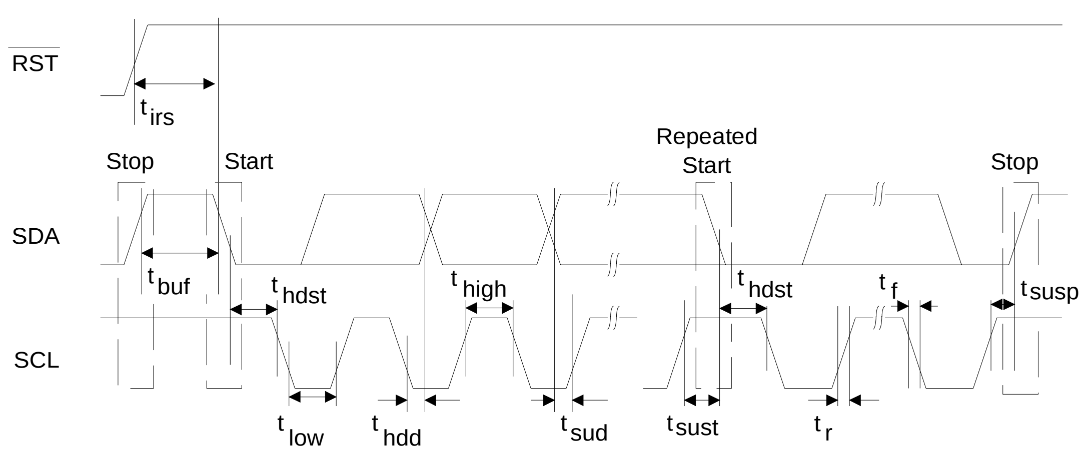


Figure 12. I²C Mode Control Port Timing

SWITCHING CHARACTERISTICS - SPI[TM] CONTROL PORT

(Inputs: logic 0 = DGND, logic 1 = VLC)

Parameter	Symbol	Min	Max	Unit
SPI Mode				
CCLK Clock Frequency	f_{sclk}	-	6	MHz
$\overline{\text{RST}}$ Rising Edge to CS Falling	t_{srs}	500	-	ns
CCLK Edge to $\overline{\text{CS}}$ Falling (Note 20)	t_{spi}	500	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions	t_{csh}	1.0	-	µs
$\overline{\text{CS}}$ Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	82	-	ns
CCLK High Time	t_{sch}	82	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 21)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 22)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 22)	t_{f2}	-	100	ns

20. t_{spi} only needed before first falling edge of $\overline{\text{CS}}$ after $\overline{\text{RST}}$ rising edge. t_{spi} = 0 at all other times.
21. Data must be held for sufficient time to bridge the transition time of CCLK.
22. For F_{SCK} < 1 MHz

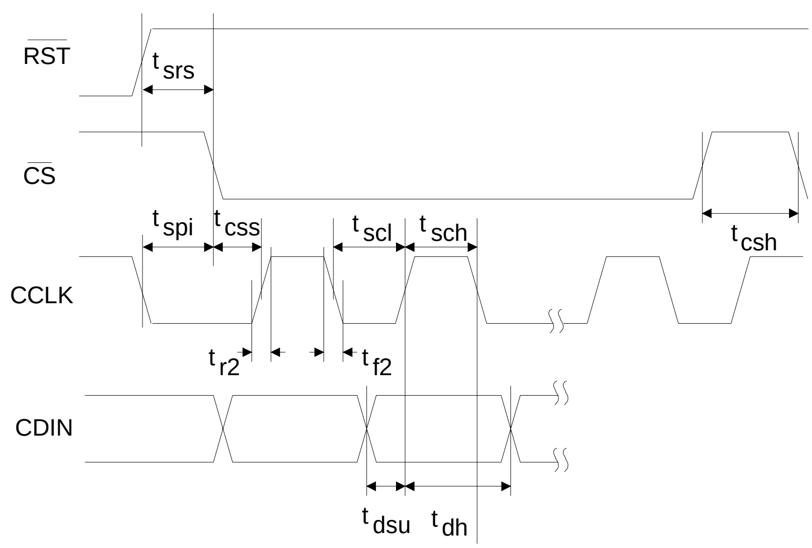


Figure 13. SPI Control Port Timing

5. APPLICATIONS

5.1 Stand-Alone Mode

5.1.1 Recommended Power-Up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

5.1.2 Master/Slave Mode

The CS4270 supports operation in either Master Mode or Slave Mode.

In Master Mode, LRCK and SCLK are outputs and are synchronously generated on-chip. LRCK is equal to Fs and SCLK is equal to 64x Fs.

In Slave Mode, LRCK and SCLK are inputs, requiring external generation that is synchronous to MCLK. It is recommended that SCLK be 48x or 64x Fs to maximize system performance.

In Stand-Alone Mode, the CS4270 will enter Slave Mode when SDOUT (M/$\overline{S}$) is pulled low through a 47 kΩ resistor. Master Mode may be accessed by placing a 47 kΩ pull-up to VD on the SDOUT (M/$\overline{S}$) pin.

Configuration of clock ratios in each of these modes is outlined in Table 2.

5.1.3 System Clocking

The CS4270 will operate at sampling frequencies from 4 kHz to 216 kHz. This range is divided into three speed modes as shown in Table 1

.

Mode	Sampling Frequency
Single-Speed	4-54 kHz
Double-Speed	50-108 kHz
Quad-Speed	100-216 kHz

Table 1. Speed Modes

5.1.4 Clock Ratio Selection

Depending on whether the CS4270 is in Master or Slave Mode, different MCLK/LRCK and SCLK/LRCK ratios may be used. These ratios are shown in the Table 2.

Master Mode					
	MCLK/LRCK	SCLK/LRCK	LRCK	MDIV2	MDIV1
Single-Speed	256	64	Fs	0	0
	384	64	Fs	0	1
	512	64	Fs	1	0
	1024	64	Fs	1	1
Double-Speed	128	64	Fs	0	0
	192	64	Fs	0	1
	256	64	Fs	1	0
	512	64	Fs	1	1
Quad-Speed	64	64	Fs	0	0
	96	64	Fs	0	1
	128	64	Fs	1	0
	256	64	Fs	1	1
Slave Mode					
	MCLK/LRCK	SCLK/LRCK	LRCK	MDIV2	MDIV1
Single-Speed	256	32, 48, 64, 128	Fs	0	0
	384	32, 48, 64, 96	Fs	0	1
	512	32, 48, 64, 128	Fs	1	0
	1024	32, 48, 64, 96	Fs	1	1
Double-Speed	128	32, 48, 64	Fs	0	0
	192	32, 48, 64	Fs	0	1
	256	32, 48, 64	Fs	1	0
	512	32, 48, 64	Fs	1	1
Quad-Speed	64	32, 48, 64	Fs	0	0
	96	32, 48, 64	Fs	0	1
	128	32, 48, 64	Fs	1	0
	256	32, 48, 64	Fs	1	1

Table 2. Clock Ratios - Stand-Alone Mode

5.1.5 Interpolation Filter

In Stand-Alone Mode, the fast roll-off interpolation filter is used. Filter specifications can be found in Section 4. Plots of the data are contained in Section 9. “Filter Plots” on page 41.

5.1.6 High-Pass Filter

The operational amplifiers in the input circuitry driving the CS4270 may generate a small DC offset into the ADC. The CS4270 includes a high-pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system. In Stand-Alone Mode, the high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter This function cannot be disabled in Stand-Alone Mode.

5.1.7 Mode Selection & De-Emphasis

The sample rate, Fs, can be adjusted from 4 kHz to 216 kHz and De-emphasis, optimized for 44.1 kHz, is available in Single-Speed Mode. In Stand-Alone Master Mode, the CS4270 must be set to the proper mode via the mode pins, M1 and M0. In Slave Mode, the CS4270 auto-detects Speed Mode and the M0 pin becomes De-emphasis select. Stand-alone definitions of the mode pins are shown in Table 3.

Mode 1	Mode 0	Mode	Sample Rate (Fs)	De-Emphasis
0	0	Single-Speed Mode	4 kHz - 54 kHz	Off
0	1	Single-Speed Mode	4 kHz - 54 kHz	44.1 kHz
1	0	Double-Speed Mode	50 kHz - 108 kHz	Off
1	1	Quad-Speed Mode	100 kHz - 216 kHz	Off

Table 3. CS4270 Stand-Alone Mode Control

5.1.8 Serial Audio Interface Format Selection

Either I²S or Left-Justified serial audio data format may be selected in Stand-Alone Mode. The selection will affect both the input and output format. Placing a 10 kΩ pull-up to VD on the I²S/$\overline{\text{LJ}}$ pin will select the I²S format, while placing a 10 kΩ pull-down to DGND on the I²S/$\overline{\text{LJ}}$ pin will select the Left-Justified format.

5.2 Control Port Mode

5.2.1 Recommended Power-Up Sequence - Access to Control Port Mode

1. Pull $\overline{\text{RST}}$ low until the power supply, MCLK, and LRCK are stable.
2. Release $\overline{\text{RST}}$. The Control Port will be accessible.
3. Set the power down bit (register 0x02h, bit 0) to “1” for 1 ms minimum within 10 ms after releasing $\overline{\text{RST}}$ and then set to “0” prior to reading or writing to other registers.
4. Initiate a SPI or I²C transaction as described in Section 6.1 or Section 6.2, respectively.

5.2.2 Master / Slave Mode Selection

The CS4270 supports operation in either Master Mode or Slave Mode.

In Master Mode, LRCK and SCLK are outputs and are synchronously generated on-chip. LRCK is equal to Fs and SCLK is equal to 64x Fs.

In Slave Mode, LRCK and SCLK are inputs, requiring external generation that is synchronous to MCLK. It is recommended that SCLK be 48x or 64x Fs to maximize system performance.

Configuration of clock ratios in each of these modes will be outlined in the Table 10 and Table 9.

In Control Port Mode the CS4270 will default to Slave Mode. The user may change this default setting by changing the status of the M/$\overline{\text{S}}$ bits in the Functional Control Register (03h).

5.2.3 System Clocking

The CS4270 will operate at sampling frequencies from 4 kHz to 216 kHz. This range is divided into three speed modes as shown in Table 4.

Mode	Sampling Frequency
Single-Speed	4-54 kHz
Double-Speed	50-108 kHz
Quad-Speed	100-216 kHz

Table 4. Speed Modes

5.2.4 Clock Ratio Selection

In Control Port Master Mode, the user must configure the mode bits (MCLK Freq<2:0>) to set the speed mode and select the appropriate clock ratios. Depending on whether the CS4270 is in Master or Slave Mode, different MCLK/LRCK and SCLK/LRCK ratios may be used. These ratios as well as the Control Port Register Bits are shown in Table 5, Table 9 and Section 8.3 on page 36.

Master Mode						
	MCLK/LRCK	SCLK/LRCK	LRCK	MCLK Freq<2>	MCLK Freq<1>	MCLK Freq<0>
Single-Speed	256	64	Fs	0	0	0
	384	64	Fs	0	0	1
	512	64	Fs	0	1	0
	768	64	Fs	0	1	1
	1024	64	Fs	1	0	0
Double-Speed	128	64	Fs	0	0	0
	192	64	Fs	0	0	1
	256	64	Fs	0	1	0
	384	64	Fs	0	1	1
	512	64	Fs	1	0	0
Quad-Speed	64	64	Fs	0	0	0
	96	64	Fs	0	0	1
	128	64	Fs	0	1	0
	192	64	Fs	0	1	1
	256	64	Fs	1	0	0
Slave Mode						
	MCLK/LRCK	SCLK/LRCK	LRCK	MCLK Freq<2>	MCLK Freq<1>	MCLK Freq<0>
Single-Speed	256	32, 64, 128	Fs	0	0	0
	384	32, 48, 64, 96, 128	Fs	0	0	1
	512	32, 64, 128	Fs	0	1	0
	768	32, 48, 64, 96, 128	Fs	0	1	1
	1024	32, 64, 128	Fs	1	0	0

Table 5. Clock Ratios - Control Port Mode

Double-Speed	128	32, 48, 64	Fs	0	0	0
	192	32, 48, 64	Fs	0	0	1
	256	32, 48, 64	Fs	0	1	0
	384	32, 48, 64	Fs	0	1	1
	512	32, 64	Fs	1	0	0
Quad-Speed	64	32	Fs	0	0	0
	96	48, 64	Fs	0	0	1
	128	32, 64	Fs	0	1	0
	192	48, 64	Fs	0	1	1
	256	32, 64	Fs	1	0	0

Table 5. Clock Ratios - Control Port Mode (Continued)

5.2.5 Internal Digital Loopback

In Control Port Mode, the CS4270 supports an internal digital loopback mode in which the output of the ADC is routed to the input of the DAC. This mode may be activated by setting the Digital Loopback bit in the ADC & DAC Ctrl register (04h).

When this bit is set, the status of the DAC_DIF(4:3) bits in register 04h will be disregarded by the CS4270. Any changes made to the DAC_DIF(4:3) bits while the Digital Loopback bit is set will have no impact on operation until the Digital Loopback bit is released, at which time the Digital Interface Format of the DAC will operate according to the format selected in the DAC_DIF(4:3) bits. While the Digital Loopback bit is set, data will be present on the SDOUT pin in the format selected in the ADC_DIF(0) bit in register 04h.

5.2.6 Auto-Mute

The Auto-Mute function is controlled by the status of the Auto Mute bit in the Mute register. When set, the DAC output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting are done independently for each channel. The common mode on the output will be retained and the Mute Control pin for that channel will become active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and ZeroCross bits in the Transition and Control register. The Auto Mute bit is set by default.

5.2.7 High-Pass Filter and DC Offset Calibration

The input circuitry driving the CS4270 may generate a small DC offset into the A/D converter. The CS4270 includes a high-pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. The high-pass filter can be enabled if the hpf_freeze bit is set during normal operation, the current value of the DC offset for the corresponding channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS4270 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS4270.

5.2.8 De-Emphasis

One de-emphasis mode is available via the Control Port and is optimized for 44.1 kHz sampling rate.

5.2.9 Oversampling Modes

The CS4270 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the FM_&_M/S_Mode[1:0] bits in the Functional Mode register (03h). Single-Speed Mode supports input sample rates up to 54 kHz and uses a 128x oversampling ratio. Double-Speed Mode supports input sample rates up to 108 kHz and uses an oversampling ratio of 64x. Quad-Speed Mode supports input sample rates up to 216 kHz and uses an oversampling ratio of 32x. See Table 10 for Control Port Mode settings.

5.3 De-Emphasis Filter

The CS4270 includes on-chip digital de-emphasis. Figure 14 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs. Please see Section 5.1.7 for the desired de-emphasis control for Stand-Alone Mode and Section 5.2.8 for Control Port Mode.

The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 µs pre-emphasis equalization as a means of noise reduction.

De-emphasis is only available in Single-Speed Mode.

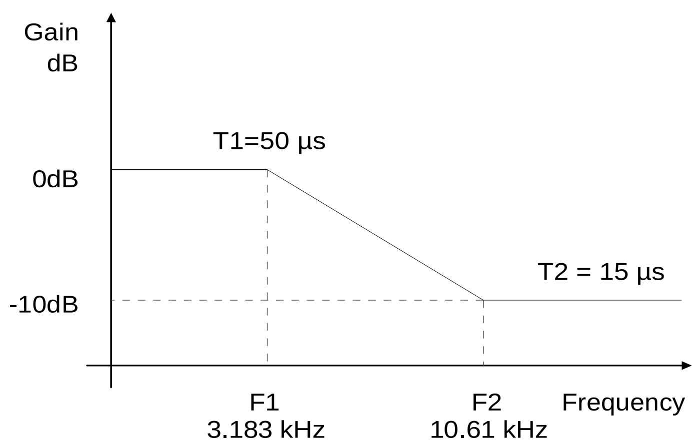


Figure 14. De-Emphasis Curve

5.4 Analog Connections

5.4.1 Input Connections

The analog modulator samples the input at 6.144 MHz.The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are multiples of the input sampling frequency (n × 6.144 MHz), where n=0,1,2,... Refer to Figure 15 which shows the recommended topology of the analog input network. The capacitor values chosen not only provide the appropriate filtering of noise at the modulator sampling frequency, but also act as a charge source for the internal sampling circuits. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity.

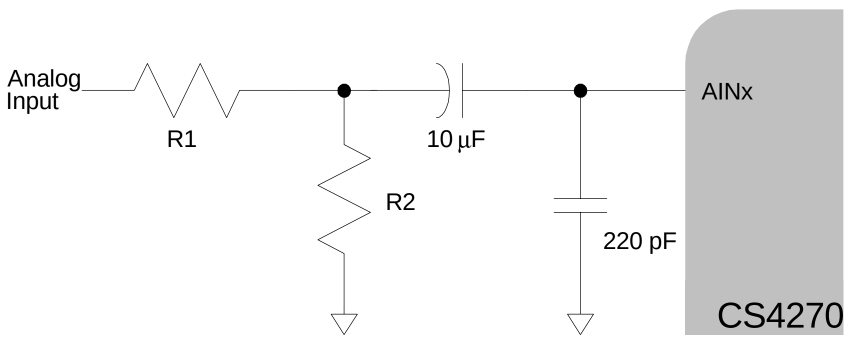


Figure 15. CS4270 Recommended Analog Input Network

Three parameters determine the values of resistors R1 and R2 as shown in Figure 15 source impedance, attenuation, and input impedance. Table 6 shows the design equation used to determine these values.

Source Impedance: Source impedance is defined as the impedance as seen from the ADC looking back into the signal network. The ADC achieves optimal THD+N performance when source impedance is minimized and THD+N degrades for source impedance greater than 1 kΩ. See Figure 16 and 17 below.

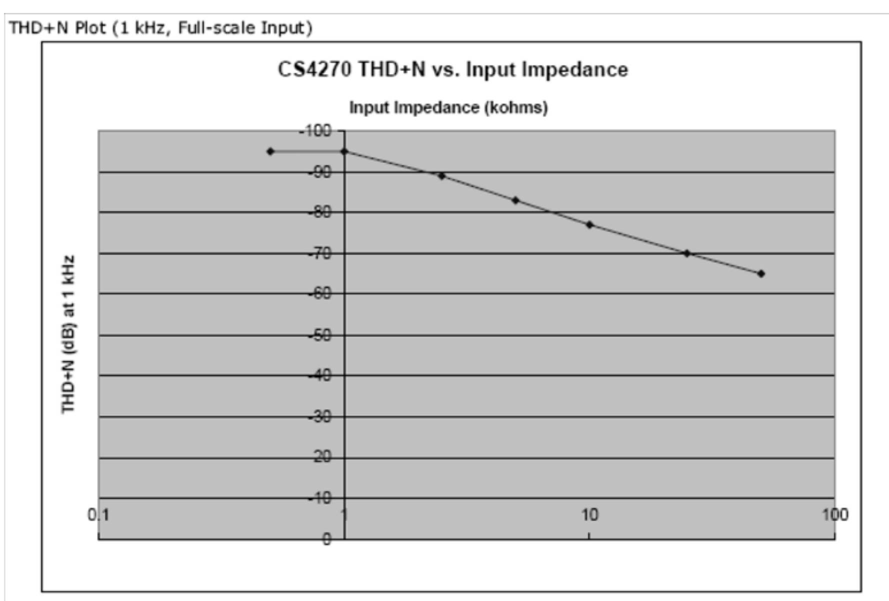


Figure 16. A/D THD+N Performance vrs. Input Source Resistance

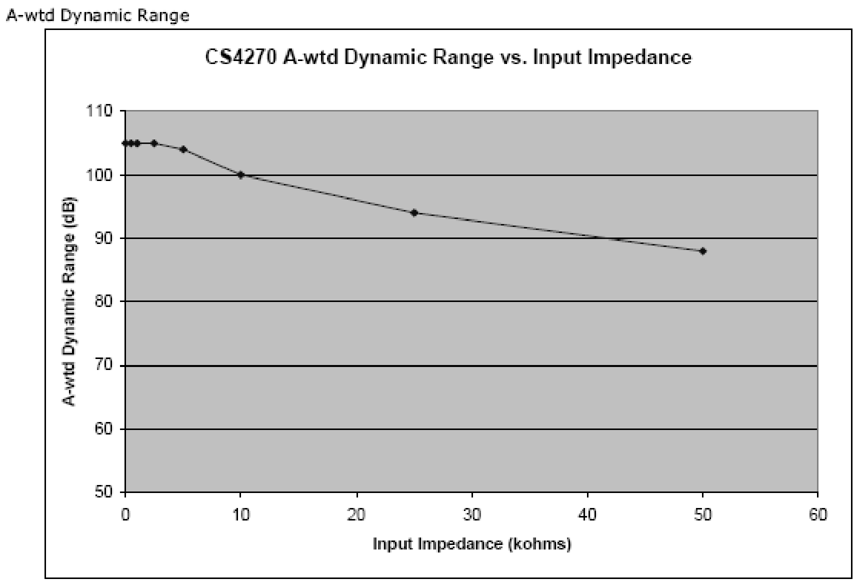


Figure 17. A/D Dynamic Range vrs. Input Source Resistance

Attenuation: The required attenuation factor depends on the magnitude of the input signal. For VA = 5 V, the full-scale input voltage equals 1 Vrms. The full-scale input voltage scales with VA as indicated on pages 13 and 14. The user should select values for R1 and R2 such that the magnitude of the incoming signal multiplied by the attenuation factor is less than or equal to the full-scale input voltage of the device.

Input Impedance: Input impedance is the impedance from the signal source to the ADC analog input pins. Table 6 shows the input parameters and the associated design equations.

Source Impedance	$\frac{(R1 \times R2)}{R1 + R2}$
Attenuation Factor	$\frac{(R2)}{(R1 + R2)}$
Input Impedance	$(R1 + R2)$

Table 6. Analog Input Design Parameters

Figure 18 illustrates an example configuration using two 2 kΩ resistors in place of R1 and R2. This circuit will attenuate a typical line level voltage, 2 Vrms, to the full-scale input of the ADC, 1 Vrms when VA = 5 V and is the maximum source impedance for the ADC specifications listed in this Data Sheet.

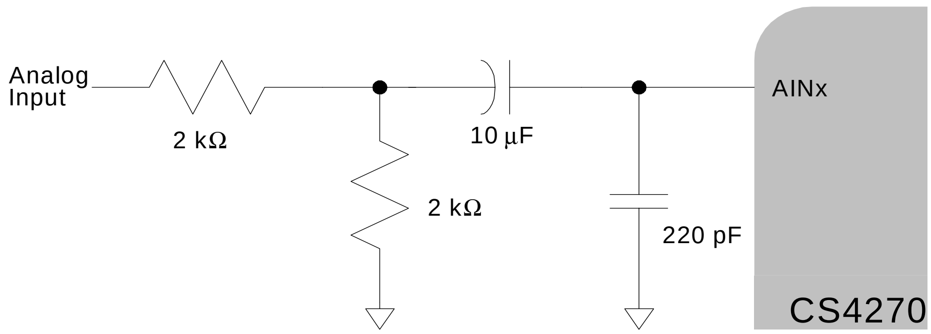
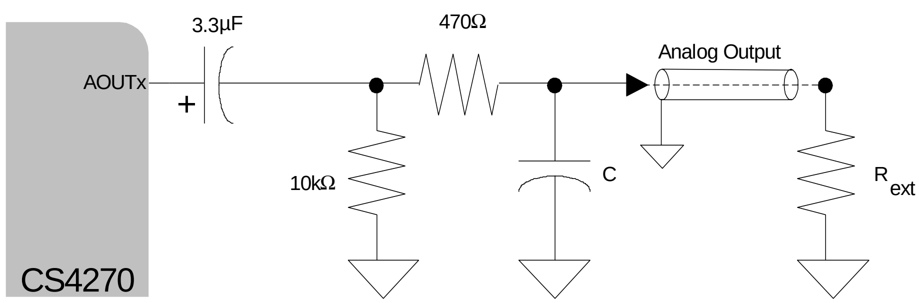


Figure 18. CS4270 Example Analog Input Network

5.4.2 Output Connections

The analog output filter present in the CS4270 is a switched-capacitor filter followed by a continuous time low pass filter. Its response, combined with that of the digital interpolator, is given in Figures 24 - 47. The recommended external analog circuitry is shown in Figure 19.



$$C = \frac{R_{ext} + 470}{4\pi F_S (R_{ext} \bullet 470)}$$ For best 20 kHz response

Figure 19. CS4270 Recommended Analog Output Filter

5.5 Mute Control

The Mute Control pins become active during power-up initialization, reset, muting, when the MCLK to LRCK ratio is incorrect, and during power-down. The MUTE pins are intended to be used as control for an external mute circuit in order to add off-chip mute capability.

The CS4270 also features Auto-Mute, which is enabled by default. The Auto-Mute function causes the MUTE pin corresponding to an individual channel to activate following the reception of 8192 consecutive static-level audio samples on the respective channel. A single transition of data on the channel will cause the corresponding MUTE pin to deactivate.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. The MUTE pins are active-low. See Figure 20 for a suggested active-low mute circuit.

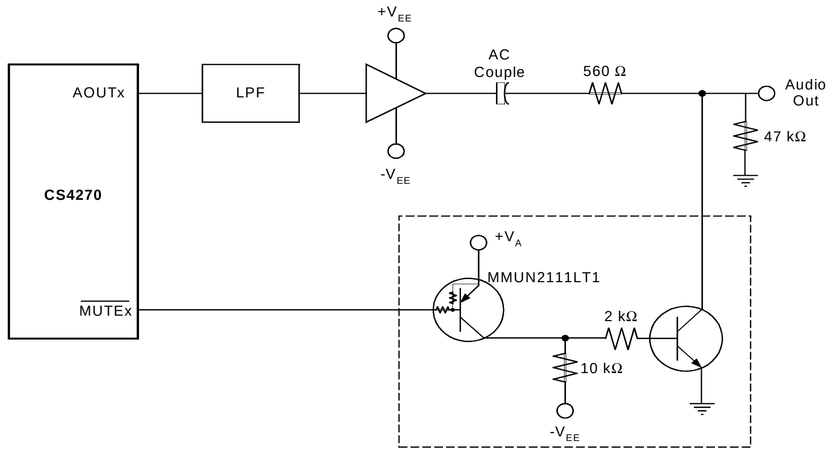


Figure 20. Suggested Active-Low Mute Circuit

5.6 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all of the CS4270's in the system. If only one MCLK source is needed, one solution is to place one CS4270 in Master Mode, and slave all of the other CS4270's to the one master. If multiple MCLK sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS4270 reset with the inactive edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

5.7 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4270 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA and VD connected to clean supplies. VD, which powers the digital filter, may be run from the system digital supply (VD) or may be powered from the analog supply (VA) via a resistor. In this case, no additional devices should be powered from VD. Power supply decoupling capacitors should be as near to the CS4270 as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the modulators. The VREF and VCOM decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from VREF and AGND. The CDB4270 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the CS4270 digital outputs only to CMOS inputs.

6. CONTROL PORT INTERFACE

The Control Port is used to load all the internal settings of the CS4270. The operation of the Control Port may be completely asynchronous to the audio sample rate. However, to avoid potential interference problems, the Control Port pins should remain static if no operation is required.

The Control Port has 2 modes: SPI and I²C, with the CS4270 operating as a slave to control messages in both modes. If I²C operation is desired, AD0/$\overline{CS}$ should be tied to VLC or DGND. If the CS4270 ever detects a high to low transition on AD0/$\overline{CS}$ after power-up, SPI Mode will be selected.

Upon release of the $\overline{RST}$ pin, the CS4270 will wait approximately 10 ms before it begins its start-up sequence. The part defaults to Stand-Alone Mode, in which all operational modes are controlled as described in Section 5.1 on page 22. If the user initiates communication to the part through the SPI or I²C interface, the part enters Control-Port Mode and all operational modes are controlled by the Control Port registers. If system requirements do not allow writing to the Control Port immediately following the release of $\overline{RST}$, the SDIN line should be held at logic “0” until the proper serial mode can be selected.

6.1 SPI™ Mode

In SPI Mode, $\overline{CS}$ is the CS4270 chip select signal, CCLK is the Control Port bit clock, CDIN is the input data line from the microcontroller and the chip address is 1001111. All control signals are inputs and data is clocked in on the rising edge of CCLK.

Figure 21 shows the operation of the Control Port in SPI Mode. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address, and must be 1001111. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into the register designated by the MAP. See Table 9 on page 36.

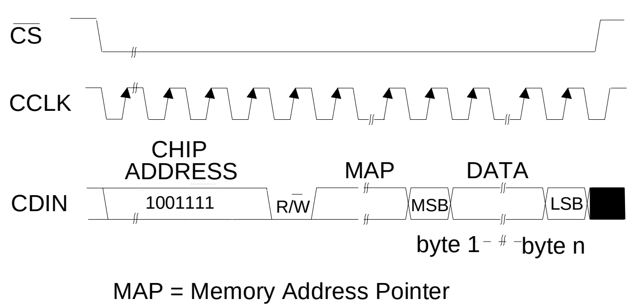


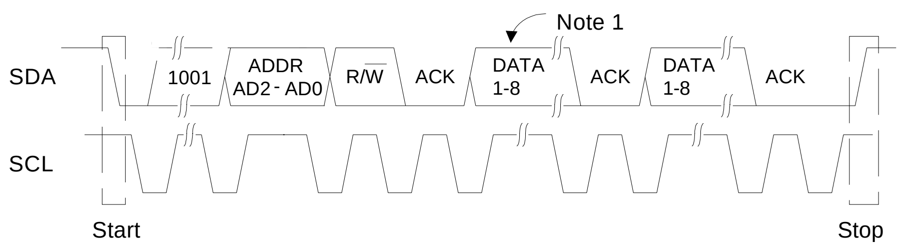
Figure 21. Control Port Timing, SPI Mode

The CS4270 has MAP auto increment capability, enabled by the INCR bit in the MAP. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set, then MAP will auto increment after each byte is written, allowing block writes to successive registers.

6.2 I²C® Mode

In I²C Mode, SDA is a bi-directional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 22. There is no CS pin. Pins AD0, AD1, and AD2 form the partial chip address and should be tied to VLC or DGND as required. The upper 4 bits of the 7-bit address field must be 1001. To communicate with the CS4270, the three lower bits of the chip address field should match the setting on the AD0, AD1, and AD2 pins. The eighth bit of the address byte is the R/W bit (high for a read, low for a write). The next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. If the operation is a write, the MAP is then followed by the data to be written. If the operation is a read, then the contents of the register pointed to by the MAP will be output after the chip address.

The CS4270 has MAP auto increment capability, enabled by the INCR bit in the MAP. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set, then MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 22. Control Port Timing, I²C Mode

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

INCR - Auto MAP Increment Enable
Default = ‘0’.
0 - Disabled
1 - Enabled

MAP(3:0) - Memory Address Pointer
Default = ‘0000’.

Table 7. Memory Address Pointer

7. REGISTER QUICK REFERENCE

This table shows the register names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
01h	ID	id<3>	id<2>	id<1>	id<0>	rev<3>	rev<2>	rev<1>	rev<0>
		1	1	0	0	0	0	0	1
02h	Power Control	Freeze	Reserved	PDN_ADC	Reserved	Reserved	Reserved	PDN_DAC	PDN
		0	0	0	0	0	0	0	0
03h	Funct Mode	Reserved	Reserved	FM_&_M/S_Mode1	FM_&_M/S_Mode0	MCLK freq<2>	MCLK freq<1>	MCLK freq<0>	PopGuard Disable
		0	0	1	1	0	0	0	0
04h	Serial Format	ADC HPF Freeze A	ADC HPF Freeze B	Digital Loopback	DAC_DIF1	DAC_DIF0	Reserved	Reserved	ADC_DIF0
		0	0	0	0	0	0	0	0
05h	Transition Control	DAC Single Vol	soft_dac	zc_dac	Invert ADC ch B	Invert ADC ch A	Invert DAC ch B	Invert DAC ch A	De-Emph
		0	1	1	0	0	0	0	0
06h	Mute	Reserved	Reserved	Auto Mute	Mute ADC SP ch B	Mute ADC SP ch A	Mute Polarity	Mute DAC ch B	Mute DAC ch A
		0	0	1	0	0	0	0	0
07h	Vol Ctrl AOUTA	dacA vol<7>	dacA vol<6>	dacA vol<5>	dacA vol<4>	dacA vol<3>	dacA vol<2>	dacA vol<1>	dacA vol<0>
		0	0	0	0	0	0	0	0
08h	Vol Ctrl AOUTB	dacB vol<7>	dacB vol<6>	dacB vol<5>	dacB vol<4>	dacB vol<3>	dacB vol<2>	dacB vol<1>	dacB vol<0>
		0	0	0	0	0	0	0	0

8. REGISTER DESCRIPTION

** All registers are read/write in I²C Mode and SPI Mode, unless otherwise noted**

8.1 Chip ID - Address 01h

7	6	5	4	3	2	1	0
id<3>	id<2>	id<1>	id<0>	rev<3>	rev<2>	rev<1>	rev<0>

Function:

This register is Read-Only. Bits 7 through 4 are the part number ID which is 1100b (01h) and the remaining bits (b3:b0) are for the chip revision.

8.2 Power Control - Address 02h

7	6	5	4	3	2	1	0
Freeze	Reserved	PDN_ADC	Reserved	Reserved	Reserved	PDN_DAC	PDN

8.2.1 Freeze (Bit 7)

Function:

This function allows modifications to be made to certain Control Port bits without the changes taking effect until the Freeze bit is disabled. To make multiple changes to these bits take effect simultaneously, set the Freeze bit, make all changes, then clear the Freeze bit. The bits affected by the Freeze function are listed below:

- Register 05h (Bits 7:0)
- Register 06h (Bits 7:0)
- Register 07h (Bits 7:0)
- Register 08h (Bits 7:0)

8.2.2 PDN_ADC (Bit 5)

Function:

The ADC portion of the device will enter a low-power state whenever this bit is set.

8.2.3 PDN_DAC (Bit 1)

Function:

The DAC portion of the device will enter a low-power state whenever this bit is set.

8.2.4 Power Down (Bit 0)

Function:

The device will enter a low-power state whenever this bit is set. The contents of the control registers are retained when the device is in power-down.

8.3 Mode Control - Address 03h

7	6	5	4	3	2	1	0
Reserved	Reserved	FM_&_M/S_ Mode1	FM_&_M/S_ Mode0	MCLK freq<2>	MCLK freq<1>	MCLK freq<0>	Popguard Disable

8.3.1 ADC Functional Mode & Master / Slave Mode (Bits 5:4)

Function:

In Control Port Master Mode, the user must configure the CS4270 Speed Mode with these bits. In Control Port Slave Mode, the CS4270 auto-detects speed mode.

FM_&_M/S_ Mode1	FM_&_M/S_ Mode0	**Mode**
0	0	Single-Speed Mode: 4 to 54 kHz sample rates
0	1	Double-Speed Mode: 50 to 108 kHz sample rates
1	0	Quad-Speed Mode: 100 to 216 kHz sample rates
1	1	Slave Mode (default)

Table 8. Functional Mode Selection

8.3.2 Ratio Select (Bits 3:1)

Function:

These bits are used to select the clocking ratios.

MCLK freq<2>	**MCLK freq<1>**	**MCLK freq<0>**	**Mode**
0	0	0	Divide by 1 (default)
0	0	1	Divide by 1.5
0	1	0	Divide by 2
0	1	1	Divide by 3
1	0	0	Divide by 4

Table 9. MCLK Divider Configuration

8.3.3 Popguard Disable (Bit 0)

Function:

Disables Popguard when set. Popguard is enabled by default.

8.4 ADC and DAC Control - Address 04h

7	6	5	4	3	2	1	0
ADC HPF Freeze A	ADC HPF Freeze B	Digital Loopback	DAC_DIF1	DAC_DIF0	Reserved	Reserved	ADC_DIF0

8.4.1 ADC HPF Freeze A (Bit 7)

Function:

When this bit is set, the internal high-pass filter for the selected channel will be disabled.The current DC offset value will be frozen and continuously subtracted from the conversion result. Section 5.2.7 “High-Pass Filter and DC Offset Calibration” on page 26.

8.4.2 ADC HPF Freeze B (Bit 6)

Function:

When this bit is set, the internal high-pass filter for the selected channel will be disabled.The current DC offset value will be frozen and continuously subtracted from the conversion result. Section 5.2.7 “High-Pass Filter and DC Offset Calibration” on page 26.

8.4.3 Digital Loopback (Bit 5)

Function:

When this bit is set, an internal digital loopback from the ADC to the DAC will be enabled. Please refer to Section 5.2.5 “Internal Digital Loopback” on page 26.

8.4.4 DAC Digital Interface Format (Bits 4:3)

Function:

The DAC Digital Interface Format and the options are detailed in Table 10 and Figures 9 through 11.

DAC_DIF1	DAC_DIF0	Description	Format	Figure
0	0	Left-Justified, up to 24-bit data (default)	0	9
0	1	I²S, up to 24-bit data	1	10
1	1	Right-Justified, 16-bit Data	2	11
1	0	Right-Justified, 24-bit Data	3	11

Table 10. DAC Digital Interface Formats

8.4.5 ADC Digital Interface Format (Bit 0)

Function:

The required relationship between LRCK, SCLK and SDOUT for the ADC is defined by the ADC Digital Interface Format. The options are detailed in Table 11 and may be seen in Figures 9 and 10.

ADC_DIF	Description	Format	Figure
0	Left-Justified, up to 24-bit data (default)	0	9
1	I²S, up to 24-bit data	1	10

Table 11. ADC Digital Interface Formats

8.5 Transition Control - Address 05h

7	6	5	4	3	2	1	0
DAC Single Volume	soft_dac	zc_dac	invert ADC ch B	invert ADC ch A	invert DAC ch B	invert DAC ch A	De-emph

8.5.1 DAC Single Volume (Bit 7)

Function:

The AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTA and AOUTB are determined by the A Channel Volume Control Byte (07h) and the B Channel Byte (08h) is ignored when this function is enabled. Volume and muting functions are affected by the Soft Ramp and ZeroCross functions below.

8.5.2 Soft Ramp or Zero Cross Enable (Bits 6:5)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods. See Table 12 on page 38.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 9 on page 36.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 9 on page 36.

Soft	ZeroCross	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled
1	1	Soft Ramp and Zero Cross enabled (default)

Table 12. Soft Cross or Zero Cross Mode Selection

8.5.3 Invert Signal Polarity (Bits 4:1)

Function:

When set, this bit activates an inversion of the signal polarity for the appropriate channel. This is useful if a board layout error has occurred or in other situations where a 180 degree phase shift is desirable.

8.5.4 De-Emphasis Control (Bit 0)

Function:

Implementation of the standard 50/15 µs digital de-emphasis filter on the DAC output requires reconfiguration of the digital filter to maintain the proper filter response for 44.1 kHz sample rate. Figure 23 shows the filter response. **NOTE:** De-emphasis is available only in Single-Speed Mode.

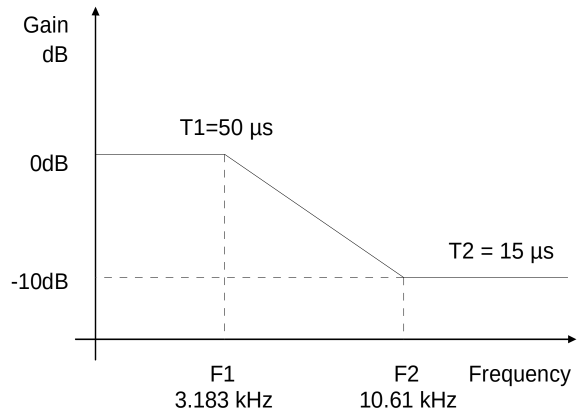


Figure 23. De-Emphasis Curve

8.6 Mute Control - Address 06h

7	6	5	4	3	2	1	0
Reserved	Reserved	Auto Mute	Mute ADC SP ch B	Mute ADC SP ch A	mute polarity	Mute DAC SP ch B	Mute DAC SP ch B

8.6.1 Auto-Mute (Bit 5)

Function:

When set, enables the Auto-Mute function. Section 5.2.6 “Auto-Mute” on page 26.

8.6.2 ADC Channel A & B Mute (Bits 4:3)

Function:

When this bit is set, the output of the ADC for the selected channel will be muted.

8.6.3 Mute Polarity (Bit 2)

Function:

The MUTEA and MUTEB pins (pins 24 and 21) are active low by default. When this bit is set, these pins are active high.

8.6.4 DAC Channel A & B Mute (Bits 1:0)

Function:

When this bit is set, the output of the DAC for the selected channel will be muted.

8.7 DAC Channel A Volume Control - Address 07h

7	6	5	4	3	2	1	0
dacA vol<7>	dacA vol<6>	dacA vol<5>	dacA vol<4>	dacA vol<3>	dacA vol<2>	dacA vol<1>	dacA vol<0>

Function:

See Section 8.8 DAC Channel B Volume Control - Address 08h.

8.8 DAC Channel B Volume Control - Address 08h

7	6	5	4	3	2	1	0
dacB vol<7>	dacB vol<6>	dacB vol<5>	dacB vol<4>	dacB vol<3>	dacB vol<2>	dacB vol<1>	dacB vol<0>

Function:

The digital volume control allows the user to attenuate the signal in 0.5 dB increments from 0 to -127 dB. The vol<0> bit activates a 0.5 dB attenuation when set, and no attenuation when cleared. The Vol[7:1] bits activate attenuation equal to their decimal value (in dB). Example volume settings are decoded as shown in Table 13. The volume changes are implemented as dictated by the DACSoft and DACZero-Cross bits in the Transition Control register (see Section 8.5.2).

Binary Code	Volume Setting
00000000	0 dB
00000001	-0.5 dB
00101000	-20 dB
00101001	-20.5 dB
11111110	-127 dB
11111111	-127.5 dB

Table 13. Digital Volume Control

9. FILTER PLOTS

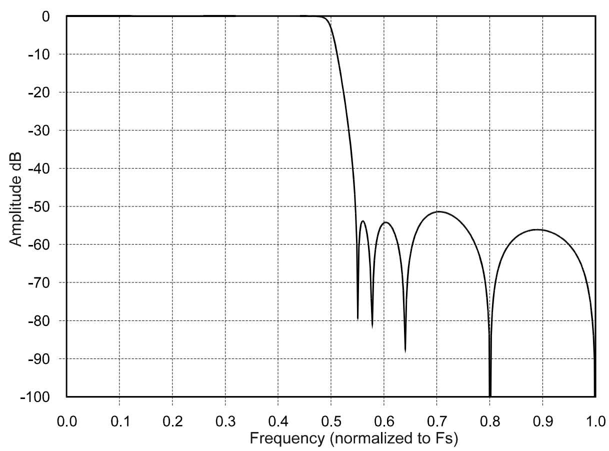


Figure 24. DAC Single-Speed Stopband Rejection

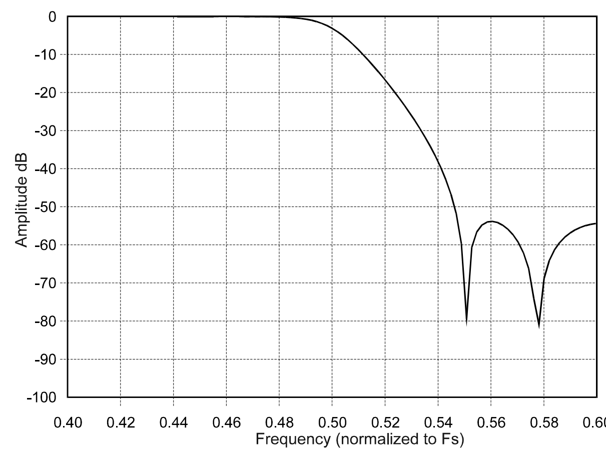


Figure 25. DAC Single-Speed Transition Band

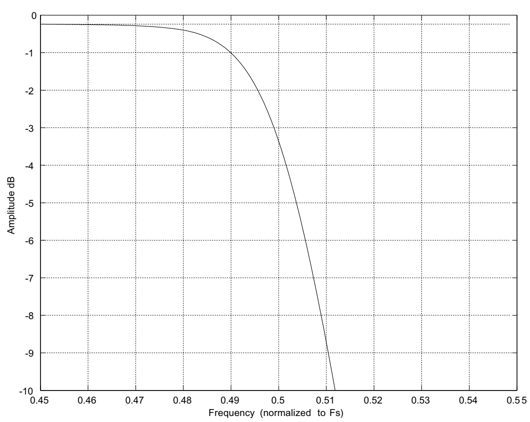


Figure 26. DAC Single-Speed Transition Band (detail)

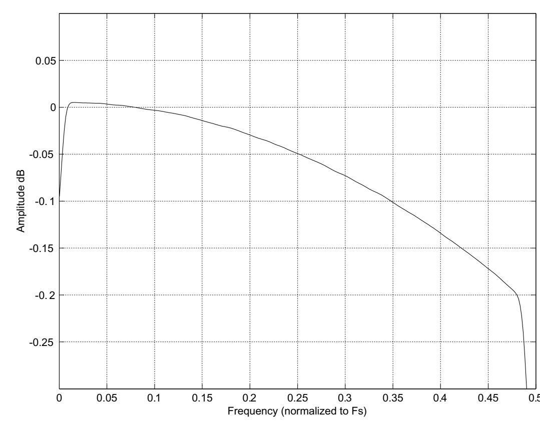


Figure 27. DAC Single-Speed Passband Ripple

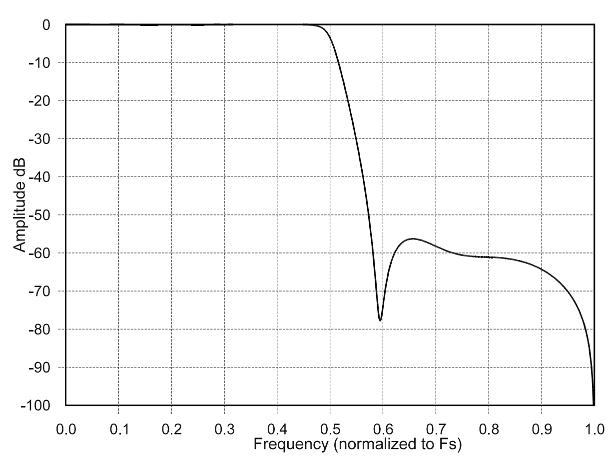


Figure 28. DAC Double-Speed Stopband Rejection

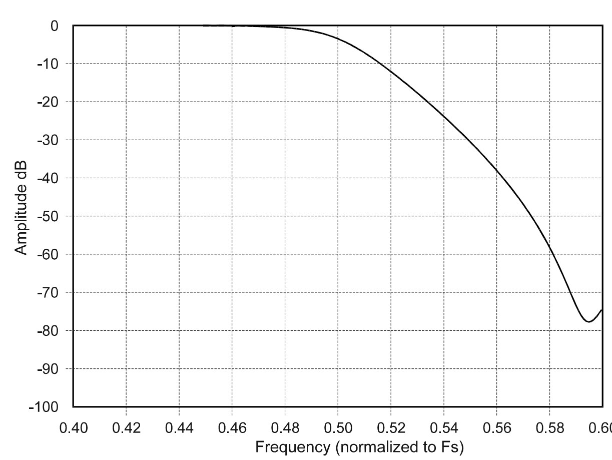


Figure 29. DAC Double-Speed Transition Band

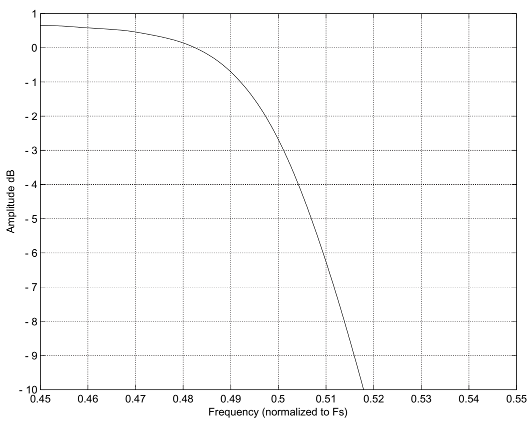


Figure 30. DAC Double-Speed Transition Band (detail)

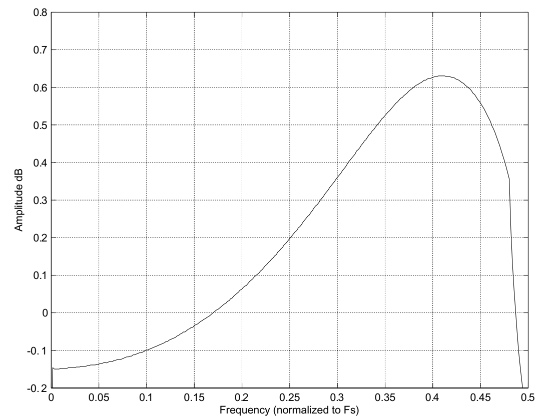


Figure 31. DAC Double-Speed Passband Ripple

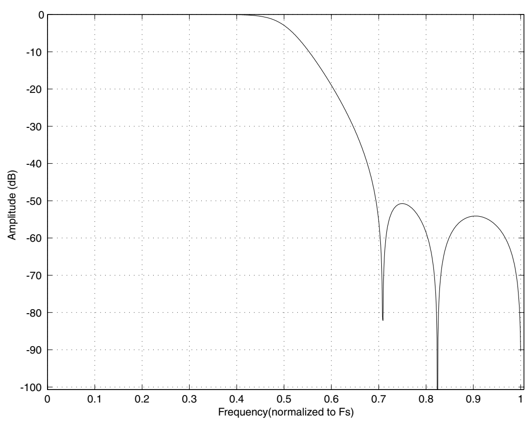


Figure 32. DAC Quad-Speed Stopband Rejection

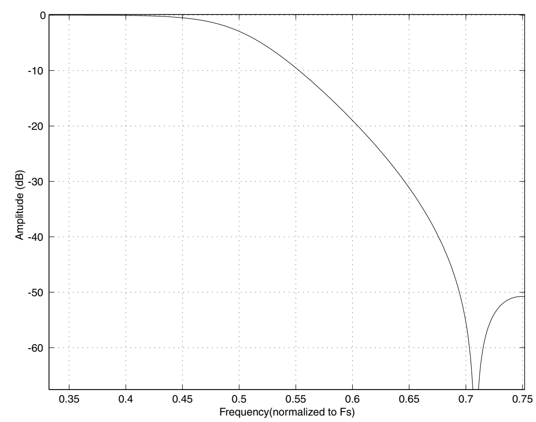


Figure 33. DAC Quad-Speed Transition Band

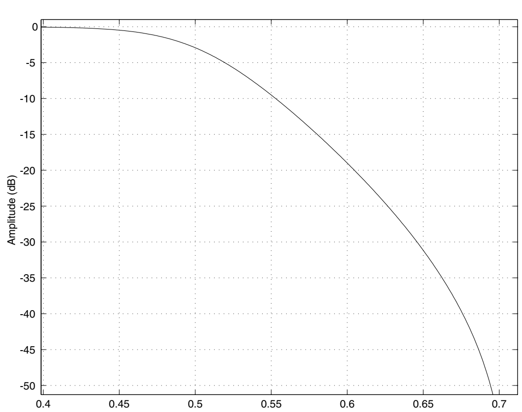


Figure 34. DAC Quad-Speed Transition Band (detail)

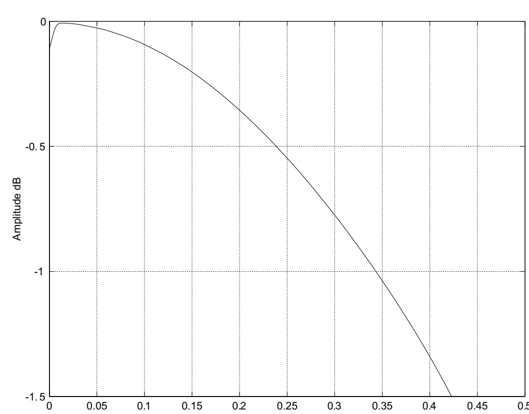


Figure 35. DAC Quad-Speed Passband Ripple

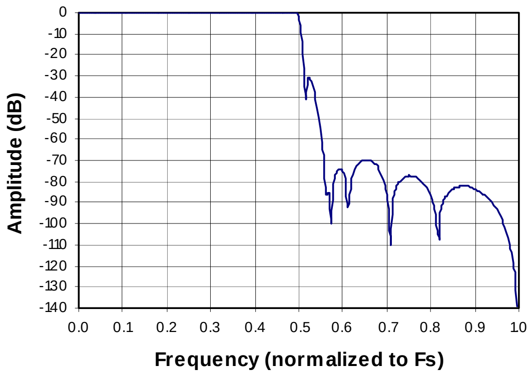


Figure 36. ADC Single-Speed Stopband Rejection

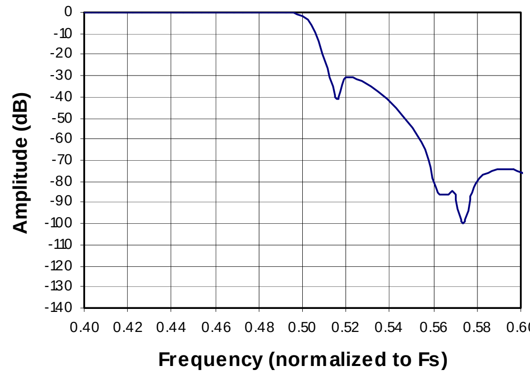


Figure 37. ADC Single-Speed Stopband (detail)

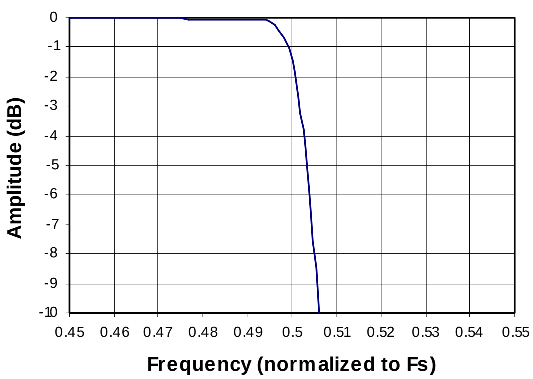


Figure 38. ADC Single-Speed Transition Band (detail)

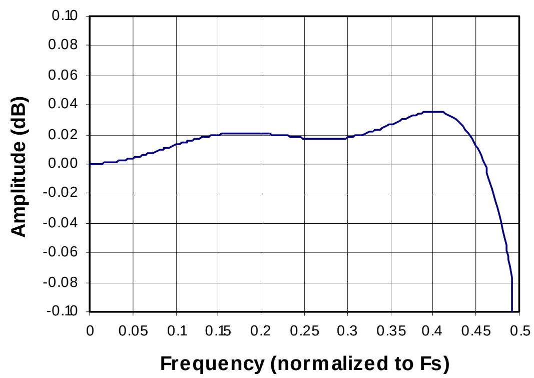


Figure 39. ADC Single-Speed Passband Ripple

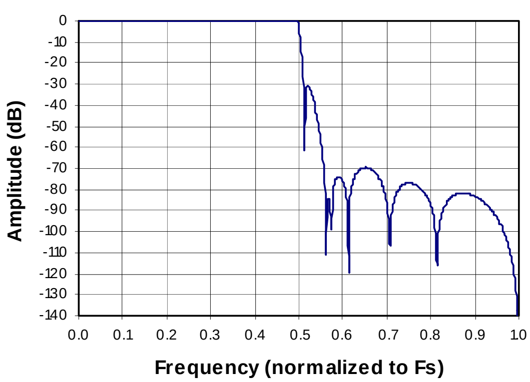


Figure 40. ADC Double-Speed Stopband Rejection

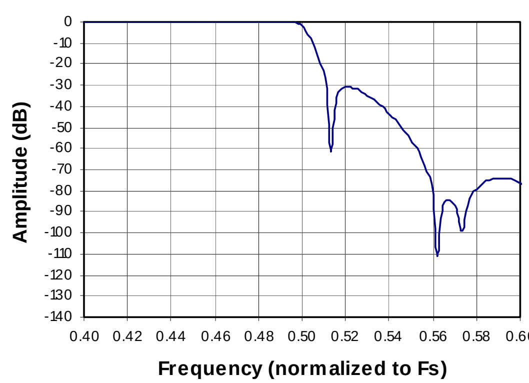


Figure 41. ADC Double-Speed Stopband (detail)

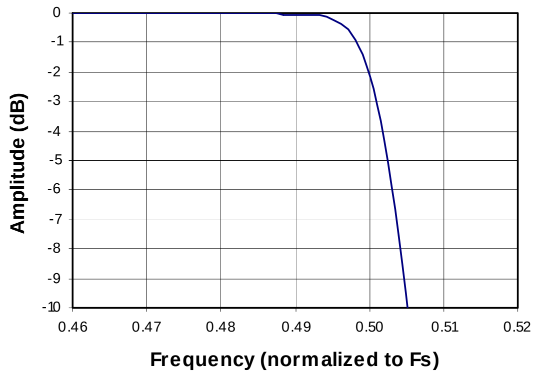


Figure 42. ADC Double-Speed Transition Band (detail)

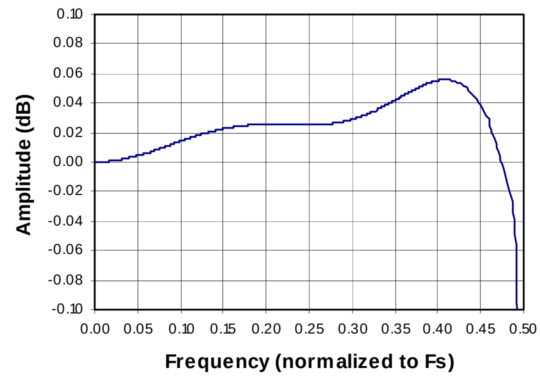


Figure 43. ADC Double-Speed Passband Ripple

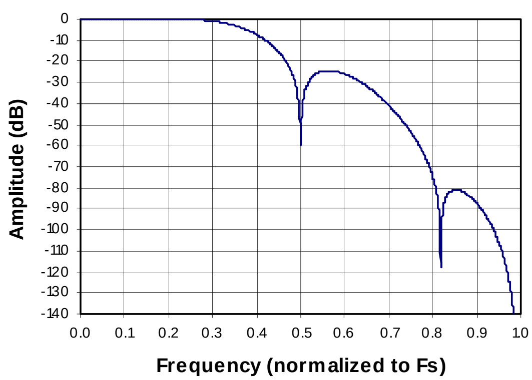


Figure 44. ADC Quad-Speed Stopband Rejection

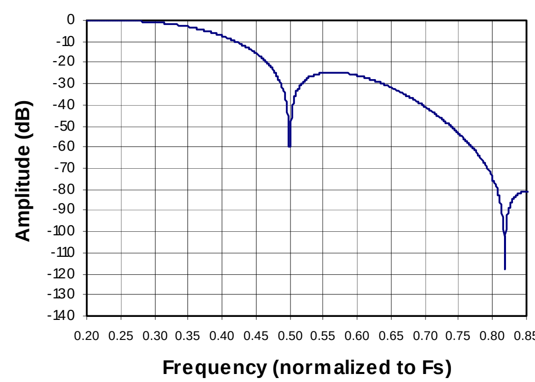


Figure 45. ADC Quad-Speed Stopband (detail)

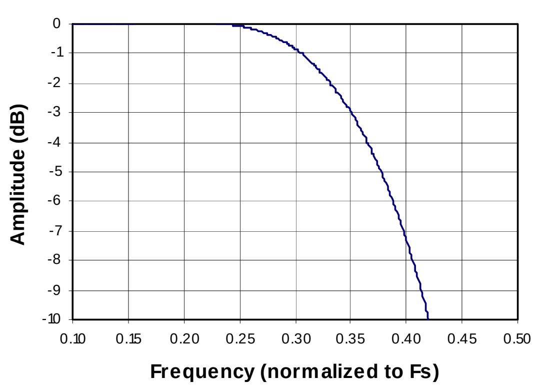


Figure 46. ADC Quad-Speed Transition Band (detail)

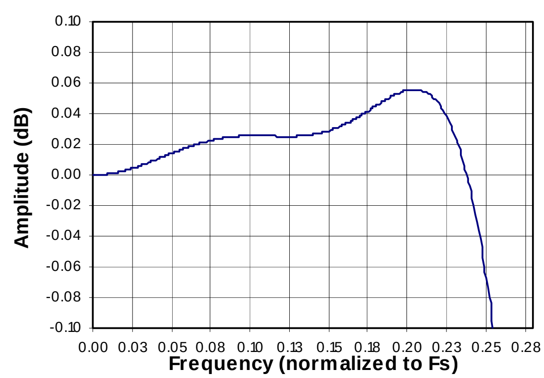


Figure 47. ADC Quad-Speed Passband Ripple

10. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

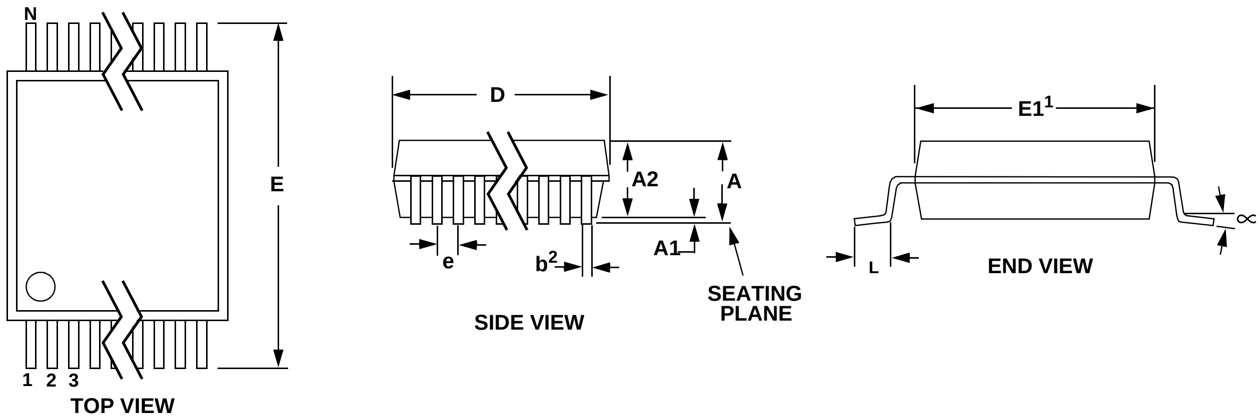
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

11.PACKAGE DIMENSIONS

24L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	--	--	0.47	--	--	1.20	
A1	0.00197	0.00394	0.00591	0.05	0.10	0.15	
A2	0.03150	0.0394	0.04137	0.80	1.00	1.05	
b	0.00748	0.00965	0.01182	0.19	0.245	0.30	2,3
D	0.30338 BSC	0.30732 BSC	0.31126 BSC	7.70 BSC	7.80 BSC	7.90 BSC	1
E	0.24822	0.25216	0.25610	6.30	6.40	6.50	
E1	0.16942	0.17336	0.17730	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.01970	0.02364	0.02955	0.50	0.60	0.75	
µ	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes:

1. “D” and “E1” are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension “b” does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of “b” dimension at maximum material condition. Dambar intrusion shall not reduce dimension “b” by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

12.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4270	24-Bit 192 kHz Stereo Audio CODEC	24-TSSOP	YES	Commercial	-10° to +70° C	Rail	CS4270-CZZ
						Tape & Reel	CS4270-CZZR
CS4270	24-Bit 192 kHz Stereo Audio CODEC	24-TSSOP	YES	Automotive	-40° to +85° C	Rail	CS4270-DZZ
						Tape & Reel	CS4270-DZZR
CDB4270	CS4270 Evaluation Board	-	-	-	-	-	CDB4270

13.REVISION HISTORY

Release	Changes
A1	Initial Release

Release	Changes
PP1	– Update Release after B0 chip validation – Changed value of A/D shunt capacitor from 2200 pF to 220 pF in Figure 18 – Added "single ended input" to "A/D Features" on page 1 and "single ended output" to "D/A Features" on page 1 – Added "3.3 V or 5 V core supply" to "System Features" on page 1 – Added package/grade & ordering info to "General Description" on page 2 – Changed note 2. in Figure 1 – Moved ordering info to Section 12 – Moved Typical Connection Diagram to Section 3 – Removed SOIC data from Thermal Characteristics Table on page 9 – Changed DAC THD+N specs in "DAC Analog Characteristics - Commercial Grade" on page 10 and "DAC Analog Characteristics - Automotive Grade" on page 10 – Changed DAC Full Scale Output Voltage specs in "DAC Analog Characteristics - all Modes" on page 11 – Revised specifications in "DAC Combined Interpolation & on-Chip Analog FIlter Response" on page 12 – Changed A/D THD+N and Full Scale Input Voltage specs in "ADC Analog Characteristics - Commercial Grade" on page 13 and "ADC Analog Characteristics - Automotive Grade" on page 14 – Specified A/D input circuit for performance specs in "ADC Analog Characteristics - Commercial Grade" on page 13 and "ADC Analog Characteristics - Automotive Grade" on page 14 – Revised specifications in "ADC Digital Filter CharacteristicS" on page 15 – Changed PSRR spec in "DC Electrical Characteristics" on page 16 – Revised Serial Audio Port specifications and acronyms in "Switching Characteristics - Serial Audio Port" on page 17 – Replaced serial port timing diagrams with Figure 4, Figure 5, Figure 6, Figure 7 and Figure 8, revised Note 17 and Note 18. – Revised power up sequence text in "Recommended Power-Up Sequence - Access to Control Port Mode" on page 24 – Changed text in "Input Connections" on page 28 to specify maximum source impedance for A/D performance specifications in the A/D Specification Tables – Added "A/D THD+N Performance vrs. Input Source Resistance" on page 28 and "A/D Dynamic Range vrs. Input Source Resistance" on page 29 – Revised text in "Input Connections" on page 28 that describes A/D input attenuator (resistor divider) circuit – Replaced Figure 18 on page 30 – Moved Parameter Definitions to Section 10 – Moved "Filter Plots" to Section 9 and updated all plots – Moved "Package Dimensions" to Section 11 and updated dimensions data

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com.