CMOS Digital Integrated Circuits Silicon Monolithic

TC7WZ74FK

1. Functional Description

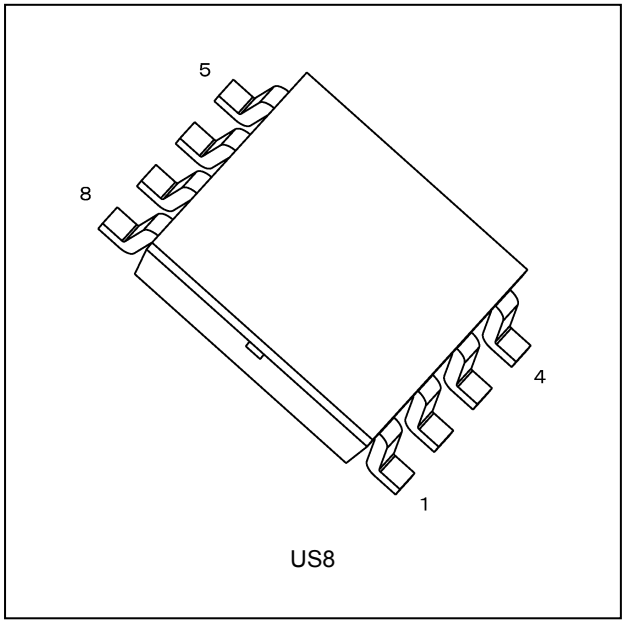
- D-Type Flip Flop with Preset and Clear

2. Features

(1) AEC-Q100 (Rev. H) (Note 1)
(2) Wide operating temperature range: T_{opr} = -40 to 125 °C (Note 2)
(3) High output current: ±24 mA (min) (V_{CC} = 3.0 V)
(4) High speed operation: t_{pd} = 2.8 ns (typ.) (V_{CC} = 5.0 V, C_L = 50 pF)
(5) Wide operating voltage range: V_{CC} = 1.65 to 5.5 V
(6) 5.5 V tolerant inputs
(7) 5.5 V power down protection output
(8) Matches the performance of TC74LCX series when operated at 3.3 V V_{CC}

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.
Note 2: For devices with the ordering part number ending in J(CT. T_{opr} = -40 to 85 °C for the other devices.

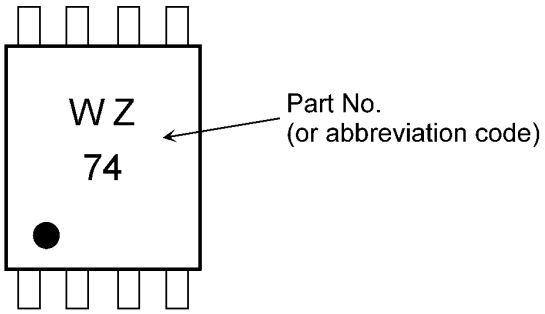
3. Packaging



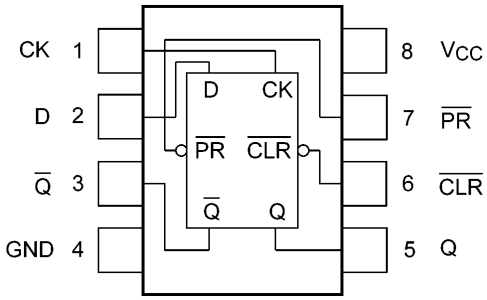
US8

Start of commercial production
2001-04

4. Marking and Pin Assignment

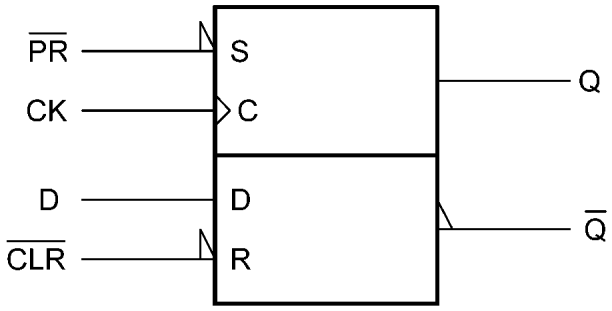


Marking



Pin Assignment (Top view)

5. IEC Logic Symbol



6. Truth Table

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	$\overline{Q}_n$	No Change

X: Don't care

7. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 6.0	V
Input voltage	V_{IN}		-0.5 to 6.0	V
DC output voltage	V_{OUT}	(Note 1)	-0.5 to 6.0	V
		(Note 2)	-0.5 to V_{CC} + 0.5	
Input diode current	I_{IK}		-20	mA
Output diode current	I_{OK}	(Note 3)	-20	
DC output current	I_{OUT}		±50	
V_{CC}/ground current	I_{CC}		±50	mA
Power dissipation	P_D		200	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: V_{CC} = 0 V
Note 2: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.
Note 3: V_{OUT} < GND

8. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CC}		—	1.65 to 5.5	V
		(Note 1)	—	1.5 to 5.5	
Input voltage	V_{IN}		—	0 to 5.5	V
Output voltage	V_{OUT}	(Note 2)	—	0 to 5.5	V
		(Note 3)	—	0 to V_{CC}	
Operating temperature	T_{opr}	(Note 4)	—	-40 to 125	°C
		(Note 5)	—	-40 to 85	
Input rise and fall time	dt/dv		V_{CC} = 1.8 ± 0.15 V, 2.5 ± 0.2 V	0 to 20	ns/V
			V_{CC} = 3.3 ± 0.3 V	0 to 10	
			V_{CC} = 5.0 ± 0.5 V	0 to 5	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 1: Data retention only
Note 2: V_{CC} = 0 V
Note 3: High (H) or Low (L) state.
Note 4: For devices with the ordering part number ending in J(CT.
Note 5: For devices except those with the ordering part number ending in J(CT.

9. Electrical Characteristics

9.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		1.65 to 1.8	V_{CC} × 0.75	—	—	V
				2.3 to 5.5	V_{CC} × 0.70	—	—	
Low-level input voltage	V_{IL}	—		1.65 to 1.8	—	—	V_{CC} × 0.25	V
				2.3 to 5.5	—	—	V_{CC} × 0.30	
High-level output voltage	V_{OH}	V_{IN} = V_{IL} or V_{IH}	I_{OH} = -100 μA	1.65	1.55	1.65	—	V
				2.3	2.2	2.3	—	
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			I_{OH} = -4 mA	1.65	1.29	1.52	—	
			I_{OH} = -8 mA	2.3	1.9	2.15	—	
			I_{OH} = -16 mA	3.0	2.4	2.8	—	
			I_{OH} = -24 mA	3.0	2.3	2.68	—	
			I_{OH} = -32 mA	4.5	3.8	4.2	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 100 μA	1.65	—	0.0	0.1	V
				2.3	—	0.0	0.1	
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			I_{OL} = 4 mA	1.65	—	0.08	0.24	
			I_{OL} = 8 mA	2.3	—	0.1	0.3	
			I_{OL} = 16 mA	3.0	—	0.15	0.4	
			I_{OL} = 24 mA	3.0	—	0.22	0.55	
			I_{OL} = 32 mA	4.5	—	0.22	0.55	
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±1	μA
Power-OFF leakage current	I_{OFF}	V_{IN} or GND = 5.5 V		0	—	—	1	μA
Quiescent supply current	I_{CC}	V_{IN} = 5.5 V or GND		1.65 to 5.5	—	—	1	μA

9.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		1.65 to 1.8	V_{CC} × 0.75	—	V
				2.3 to 5.5	V_{CC} × 0.70	—	
Low-level input voltage	V_{IL}	—		1.65 to 1.8	—	V_{CC} × 0.25	V
				2.3 to 5.5	—	V_{CC} × 0.30	
High-level output voltage	V_{OH}	V_{IN} = V_{IL} or V_{IH}	I_{OH} = -100 μA	1.65	1.55	—	V
				2.3	2.2	—	
				3.0	2.9	—	
				4.5	4.4	—	
			I_{OH} = -4 mA	1.65	1.29	—	
			I_{OH} = -8 mA	2.3	1.9	—	
			I_{OH} = -16 mA	3.0	2.4	—	
			I_{OH} = -24 mA	3.0	2.3	—	
			I_{OH} = -32 mA	4.5	3.8	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 100 μA	1.65	—	0.1	V
				2.3	—	0.1	
				3.0	—	0.1	
				4.5	—	0.1	
			I_{OL} = 4 mA	1.65	—	0.24	
			I_{OL} = 8 mA	2.3	—	0.3	
			I_{OL} = 16 mA	3.0	—	0.4	
			I_{OL} = 24 mA	3.0	—	0.55	
			I_{OL} = 32 mA	4.5	—	0.55	
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±10	μA
Power-OFF leakage current	I_{OFF}	V_{IN} or V_{OUT} = 5.5 V		0	—	10	μA
Quiescent supply current	I_{CC}	V_{IN} = 5.5 V or GND		1.65 to 5.5	—	10	μA

9.3. DC Characteristics (Note) (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		1.65 to 1.8	V_{CC} × 0.75	—	V
				2.3 to 5.5	V_{CC} × 0.70	—	
Low-level input voltage	V_{IL}	—		1.65 to 1.8	—	V_{CC} × 0.25	V
				2.3 to 5.5	—	V_{CC} × 0.30	
High-level output voltage	V_{OH}	V_{IN} = V_{IL} or V_{IH}	I_{OH} = -100 μA	1.65	1.55	—	V
				2.3	2.2	—	
				3.0	2.9	—	
				4.5	4.4	—	
			I_{OH} = -4 mA	1.65	0.95	—	
			I_{OH} = -8 mA	2.3	1.7	—	
			I_{OH} = -16 mA	3.0	2.2	—	
			I_{OH} = -24 mA	3.0	2.0	—	
			I_{OH} = -32 mA	4.5	3.4	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 100 μA	1.65	—	0.1	V
				2.3	—	0.1	
				3.0	—	0.1	
				4.5	—	0.1	
			I_{OL} = 4 mA	1.65	—	0.7	
			I_{OL} = 8 mA	2.3	—	0.45	
			I_{OL} = 16 mA	3.0	—	0.6	
			I_{OL} = 24 mA	3.0	—	0.8	
			I_{OL} = 32 mA	4.5	—	0.8	
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±20	μA
Power-OFF leakage current	I_{OFF}	V_{IN} or V_{OUT} = 5.5 V		0	—	100	μA
Quiescent supply current	I_{CC}	V_{IN} = 5.5 V or GND		1.65 to 5.5	—	100	μA

Note: For devices with the ordering part number ending in J(CT.

9.4. AC Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Maximum clock frequency	f_{MAX}		R_L = 500 Ω	1.8 ± 0.15	50	51	—	—	MHz
				2.5 ± 0.2		130	—	—	
				3.3 ± 0.3		200	—	—	
				5.0 ± 0.5		200	—	—	
Propagation delay time (CK-Q,$\overline{Q}$)	t_{PLH},t_{PHL}		R_L = 1 MΩ	1.8 ± 0.15	15	2.5	10.0	18.0	ns
				2.5 ± 0.2		2.0	4.9	7.5	
				3.3 ± 0.3		1.5	3.3	4.8	
				5.0 ± 0.5		1.0	2.4	3.5	
			R_L = 500 Ω	3.3 ± 0.3	50	2.0	4.3	5.7	
				5.0 ± 0.5		1.5	2.8	4.0	
Propagation delay time ($\overline{CLR}$,$\overline{PR}$-Q,$\overline{Q}$)	t_{PLH},t_{PHL}		R_L = 1 MΩ	1.8 ± 0.15	15	2.5	10.0	17.0	ns
				2.5 ± 0.2		2.0	5.0	7.3	
				3.3 ± 0.3		1.5	3.4	4.8	
				5.0 ± 0.5		1.5	2.2	3.5	
			R_L = 500 Ω	3.3 ± 0.3	50	2.0	4.3	5.7	
				5.0 ± 0.5		1.0	3.1	3.9	
Minimum setup time	t_S		R_L = 500 Ω	2.5 ± 0.2	50	3.4	—	—	ns
				3.3 ± 0.3		2.1	—	—	
				5.0 ± 0.5		1.5	—	—	
Minimum hold time	t_h		R_L = 500 Ω	2.5 ± 0.2	50	2.4	—	—	ns
				3.3 ± 0.3		1.4	—	—	
				5.0 ± 0.5		1.0	—	—	
Minimum pulse width (CK)	$t_{W(L)}$,$t_{W(H)}$		R_L = 500 Ω	2.5 ± 0.2	50	3.0	—	—	ns
				3.3 ± 0.3		3.0	—	—	
				5.0 ± 0.5		3.0	—	—	
Minimum pulse width ($\overline{CLR}$,$\overline{PR}$)	$t_{W(L)}$		R_L = 500 Ω	2.5 ± 0.2	50	3.0	—	—	ns
				3.3 ± 0.3		3.0	—	—	
				5.0 ± 0.5		3.0	—	—	
Minimum removal time	t_{rem}		R_L = 500 Ω	2.5 ± 0.2	50	3.6	—	—	ns
				3.3 ± 0.3		2.2	—	—	
				5.0 ± 0.5		1.3	—	—	
Input capacitance	C_{IN}		—	0 to 5.5	—	—	3.0	10	pF
Output capacitance	C_{OUT}		—	0 to 5.5	—	—	5.0	—	pF
Power dissipation capacitance	C_{PD}	(Note 1)	—	3.3	—	—	30	—	pF
				5.5		—	47	—	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

9.5. AC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Maximum clock frequency	f_{MAX}	RL = 500 Ω	1.8 ± 0.15	50	38	—	MHz
			2.5 ± 0.2		100	—	
			3.3 ± 0.3		150	—	
			5.0 ± 0.5		180	—	
Propagation delay time (CK-Q,$\overline{Q}$)	t_{PLH},t_{PHL}	RL = 1 MΩ	1.8 ± 0.15	15	2.1	23.0	ns
			2.5 ± 0.2		1.7	9.0	
			3.3 ± 0.3		1.3	5.6	
			5.0 ± 0.5		1.0	3.9	
		RL = 500 Ω	3.3 ± 0.3	50	1.5	7.0	
			5.0 ± 0.5		1.3	4.4	
Propagation delay time ($\overline{CLR}$,$\overline{PR}$-Q,$\overline{Q}$)	t_{PLH},t_{PHL}	RL = 1 MΩ	1.8 ± 0.15	15	2.1	21.0	ns
			2.5 ± 0.2		1.7	8.8	
			3.3 ± 0.3		1.3	5.6	
			5.0 ± 0.5		1.0	3.9	
		RL = 500 Ω	3.3 ± 0.3	50	1.5	7.0	
			5.0 ± 0.5		1.0	4.3	
Minimum setup time	t_S	RL = 500 Ω	2.5 ± 0.2	50	4.1	—	ns
			3.3 ± 0.3		2.5	—	
			5.0 ± 0.5		1.7	—	
Minimum hold time	t_h	RL = 500 Ω	2.5 ± 0.2	50	2.9	—	ns
			3.3 ± 0.3		1.5	—	
			5.0 ± 0.5		1.1	—	
Minimum pulse width (CK)	$t_{W(L)}$,$t_{W(H)}$	RL = 500 Ω	2.5 ± 0.2	50	3.6	—	ns
			3.3 ± 0.3		3.3	—	
			5.0 ± 0.5		3.2	—	
Minimum pulse width ($\overline{CLR}$,$\overline{PR}$)	$t_{W(L)}$	RL = 500 Ω	2.5 ± 0.2	50	3.6	—	ns
			3.3 ± 0.3		3.3	—	
			5.0 ± 0.5		3.2	—	
Minimum removal time	t_{rem}	RL = 500 Ω	2.5 ± 0.2	50	4.4	—	ns
			3.3 ± 0.3		2.5	—	
			5.0 ± 0.5		1.4	—	

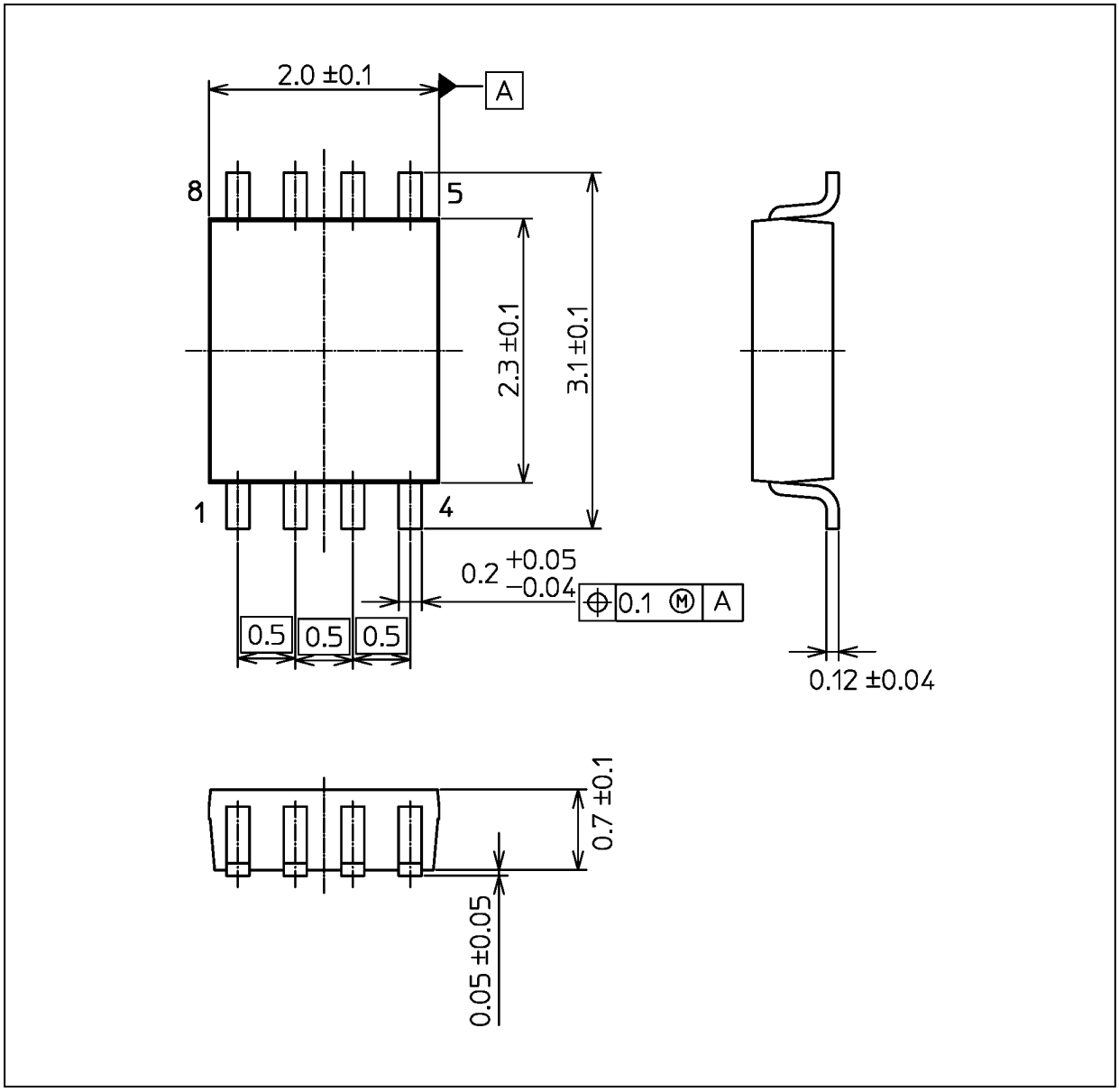
9.6. AC Characteristics (Note)
(Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Maximum clock frequency	f_{MAX}	RL = 500 Ω	1.8 ± 0.15	50	34	—	MHz
			2.5 ± 0.2		90	—	
			3.3 ± 0.3		135	—	
			5.0 ± 0.5		162	—	
Propagation delay time (CK-Q,$\overline{Q}$)	t_{PLH},t_{PHL}	RL = 1 MΩ	1.8 ± 0.15	15	2.1	26.0	ns
			2.5 ± 0.2		1.7	10.0	
			3.3 ± 0.3		1.3	6.2	
			5.0 ± 0.5		1.0	4.3	
		RL = 500 Ω	3.3 ± 0.3	50	1.5	8.8	
			5.0 ± 0.5		1.3	4.9	
Propagation delay time ($\overline{CLR}$,$\overline{PR}$-Q,$\overline{Q}$)	t_{PLH},t_{PHL}	RL = 1 MΩ	1.8 ± 0.15	15	2.1	24.0	ns
			2.5 ± 0.2		1.7	9.7	
			3.3 ± 0.3		1.3	6.2	
			5.0 ± 0.5		1.0	4.3	
		RL = 500 Ω	3.3 ± 0.3	50	1.5	7.7	
			5.0 ± 0.5		1.0	4.8	
Minimum setup time	t_S	RL = 500 Ω	2.5 ± 0.2	50	4.1	—	ns
			3.3 ± 0.3		2.5	—	
			5.0 ± 0.5		1.7	—	
Minimum hold time	t_h	RL = 500 Ω	2.5 ± 0.2	50	2.9	—	ns
			3.3 ± 0.3		1.5	—	
			5.0 ± 0.5		1.1	—	
Minimum pulse width (CK)	$t_{W(L)}$,$t_{W(H)}$	RL = 500 Ω	2.5 ± 0.2	50	3.6	—	ns
			3.3 ± 0.3		3.3	—	
			5.0 ± 0.5		3.2	—	
Minimum pulse width ($\overline{CLR}$,$\overline{PR}$)	$t_{W(L)}$	RL = 500 Ω	2.5 ± 0.2	50	3.6	—	ns
			3.3 ± 0.3		3.3	—	
			5.0 ± 0.5		3.2	—	
Minimum removal time	t_{rem}	RL = 500 Ω	2.5 ± 0.2	50	4.4	—	ns
			3.3 ± 0.3		2.5	—	
			5.0 ± 0.5		1.4	—	

Note: For devices with the ordering part number ending in J(CT.

Package Dimensions

Unit: mm



Weight: 0.01 g (typ.)

Package Name(s)
JEDEC: SOT-765
Nickname: US8

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