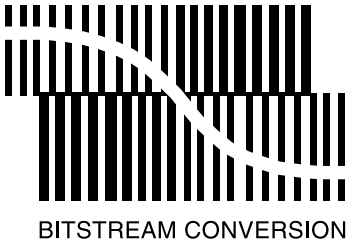
DATA SHEET



UDA1324TS
Ultra low-voltage stereo filter DAC

Preliminary specification
Supersedes data of 1999 Oct 12
File under Integrated Circuits, IC01

2000 Jan 20

Philips
Semiconductors

PHILIPS

Ultra low-voltage stereo filter DAC UDA1324TS

FEATURES

General

- Low power consumption
- Ultra low power supply voltage from 1.9 to 2.7 V
- Selectable control via L3 microcontroller interface or via static pin control
- System clock frequencies of $256f_s$, $384f_s$ and $512f_s$ selectable via L3 interface or $256f_s$ and $384f_s$ via static pin control
- Supports sampling frequencies (f_s) from 16 to 48 kHz
- Integrated digital filter plus non inverting Digital-to-Analog Converter (DAC)
- No analog post filtering required for DAC
- Slave mode only applications
- Easy application
- Small package size (SSOP16).

Multiple format input interface

- L3 mode: I^2S-bus, MSB-justified or LSB-justified 16, 18 and 20 bits format compatible
- Static pin mode: I^2S-bus or LSB-justified 16, 18 and 20 bits format compatible
- $1f_s$ input format data rate.

DAC digital sound processing

- Digital logarithmic volume control in L3 mode
- Digital de-emphasis selection for 32, 44.1 and 48 kHz sampling frequencies in L3 mode or 44.1 kHz sampling frequency in static pin mode
- Soft mute control in static pin mode or in L3 mode.

Advanced audio configuration

- Stereo line output (volume control in L3 mode)
- High linearity, wide dynamic range and low distortion.

BITSTREAM CONVERSION

APPLICATIONS

- Portable digital audio equipment.

GENERAL DESCRIPTION

The UDA1324TS is a single-chip stereo DAC employing bitstream conversion techniques. The ultra low-voltage requirements make the device eminently suitable for use in portable digital audio equipment which incorporates playback functions.

The UDA1324TS supports the I^2S-bus data format with word lengths of up to 20 bits, the MSB-justified data format with word lengths of up to 20 bits and the LSB-justified serial data format with word lengths of 16, 18 and 20 bits.

The UDA1324TS can be used in two modes: L3 mode or static pin mode.

In the L3 mode, all digital sound processing features must be controlled via the L3 interface, including the selection of the system clock setting.

In the two static modes, the UDA1324TS can be operated in the $256f_s$ and $384f_s$ system clock mode. Muting, de-emphasis for 44.1 kHz and four digital input formats (I^2S-bus or LSB-justified 16, 18 and 20 bits) can be selected via static pins. The L3 interface cannot be used in this application mode, so volume control is not available in this mode.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1324TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		1.9	2.0	2.7	V
V_{DDD}	digital supply voltage		1.9	2.0	2.7	V
I_{DDA}	analog supply current	V_{DDA} = 2.0 V	–	3.0	–	mA
I_{DDD}	digital supply current	V_{DDD} = 2.0 V	–	1.5	–	mA
DAC; note 1						
$V_{o(rms)}$	output voltage (RMS value)	note 2	–	500	–	mV
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB	–	–83	–78	dB
		at –60 dB; A-weighted	–	–36	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	–	97	–	dB
α_{cs}	channel separation		–	100	–	dB
T_{amb}	ambient temperature		–40	–	+70	°C

Notes

1. The analog performance figures are measured at 2.0 V supply voltage.
2. The DAC output voltage scales linearly with the power supply voltage.

BLOCK DIAGRAM

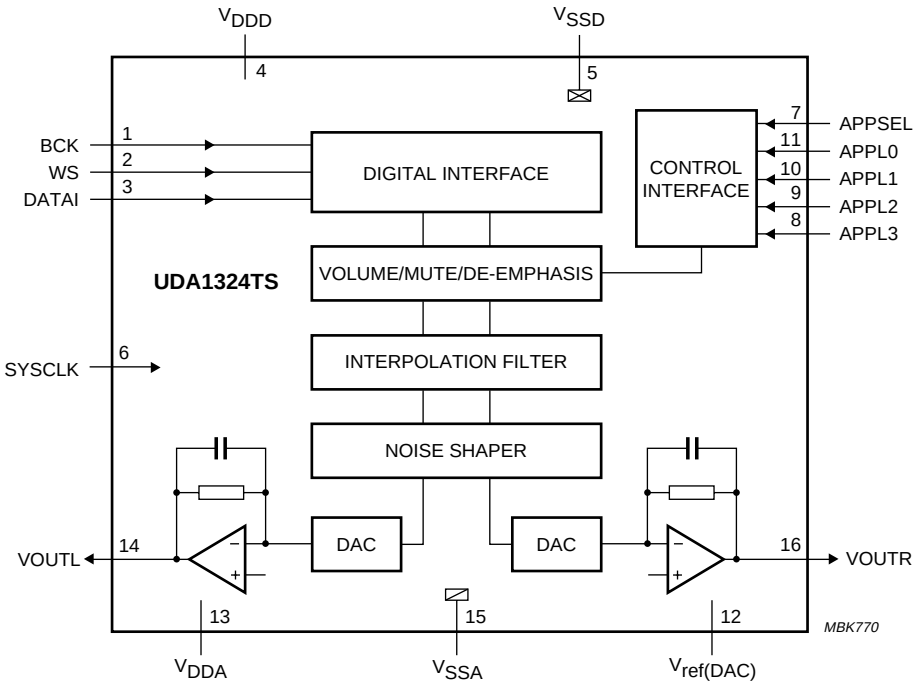


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATAI	3	data input
V_{DDD}	4	digital supply voltage
V_{SSD}	5	digital ground
SYSCLK	6	system clock input: $256f_s$, $384f_s$ and $512f_s$
APPSEL	7	application mode select input
APPL3	8	application input pin 3
APPL2	9	application input pin 2
APPL1	10	application input pin 1
APPL0	11	application input pin 0
$V_{ref(DAC)}$	12	DAC reference voltage
V_{DDA}	13	analog supply voltage for DAC
VOUTL	14	left channel output
V_{SSA}	15	analog ground for DAC
VOUTR	16	right channel output

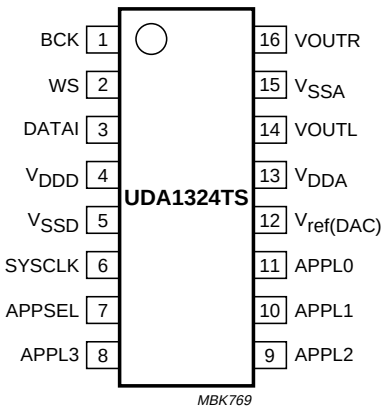


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

System clock

The UDA1324TS operates in the slave mode only. Therefore, in all applications the system devices must provide the system clock. The system frequency (f_{sys}) is selectable and depends on the application mode.
The options are: $256f_s$, $384f_s$ and $512f_s$ for the L3 mode and $256f_s$ or $384f_s$ for the static pin mode. The system clock must be locked in frequency to the digital interface input signals.

The UDA1324TS supports sampling frequencies (f_s) from 16 to 48 kHz.

Application modes

The application mode can be set with the three-level pin APPSEL (see Table 1):

- L3 mode
- Static pin mode with $f_{sys} = 384f_s$
- Static pin mode with $f_{sys} = 256f_s$.

Table 1 Selecting application mode and system clock frequency via pin APPSEL

VOLTAGE ON PIN APPSEL	MODE	f_{sys}
V_{SSD}	L3 mode	$256f_s$, $384f_s$ or $512f_s$
$0.5V_{DDD}$	static pin mode	$384f_s$
V_{DDD}		$256f_s$

The function of an application input pin (active HIGH) depends on the application mode (see Table 2).

Table 2 Functions of application input pins

PIN	FUNCTION	
	L3 MODE	STATIC PIN MODE
APPL0	TEST	MUTE
APPL1	L3CLOCK	DEEM
APPL2	L3MODE	SF0
APPL3	L3DATA	SF1

For example, in the static pin mode the output signal can be soft muted by setting pin APPL0 to HIGH.
De-emphasis can be switched on for 44.1 kHz by setting pin APPL1 to HIGH; setting pin APPL1 to LOW will disable de-emphasis.

In the L3 mode, pin APPL0 must be set to LOW. It should be noted that when the L3 mode is used, an initialization must be performed when the IC is powered-up.

Digital interface

DATA FORMATS

The digital interface of the UDA1324TS supports multiple format inputs (see Fig.3).

Left and right data-channel words are time multiplexed.

The WS signal must have a 50% duty factor for all LSB-justified formats.

The BCK clock can be up to $64f_s$, or in other words the BCK frequency is 64 times the Word Select (WS) frequency or less: $f_{BCK} \leq 64 \times f_{WS}$.

Important: the WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital interface.

The UDA1324TS also accepts double speed data for double speed data monitoring purposes.

L3 MODE

- I^2S-bus format with data word length of up to 20 bits
- MSB-justified format with data word length up to 20 bits
- LSB-justified format with data word length of 16, 18 or 20 bits.

STATIC PIN MODE

- I^2S-bus format with data word length of up to 20 bits
- LSB-justified format with data word length of 16, 18 or 20 bits.

These four formats are selectable via the static pin codes SF0 and SF1 (see Table 3).

Table 3 Input format selection using SF0 and SF1

FORMAT	SF0	SF1
I^2S-bus	0	0
LSB-justified 16 bits	0	1
LSB-justified 18 bits	1	0
LSB-justified 20 bits	1	1

Interpolation filter

The digital filter interpolates from $1f_s$ to $128f_s$ by cascading a recursive filter and a FIR filter (see Table 4).

Table 4 Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	±0.1
Stop band	$>0.55f_s$	–50
Dynamic range	0 to $0.45f_s$	108

Noise shaper

The 3rd-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream Digital-to-Analog Converter (FSDAC).

Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage capable of driving a line output.

The output voltage of the FSDAC scales linearly with the power supply voltage.

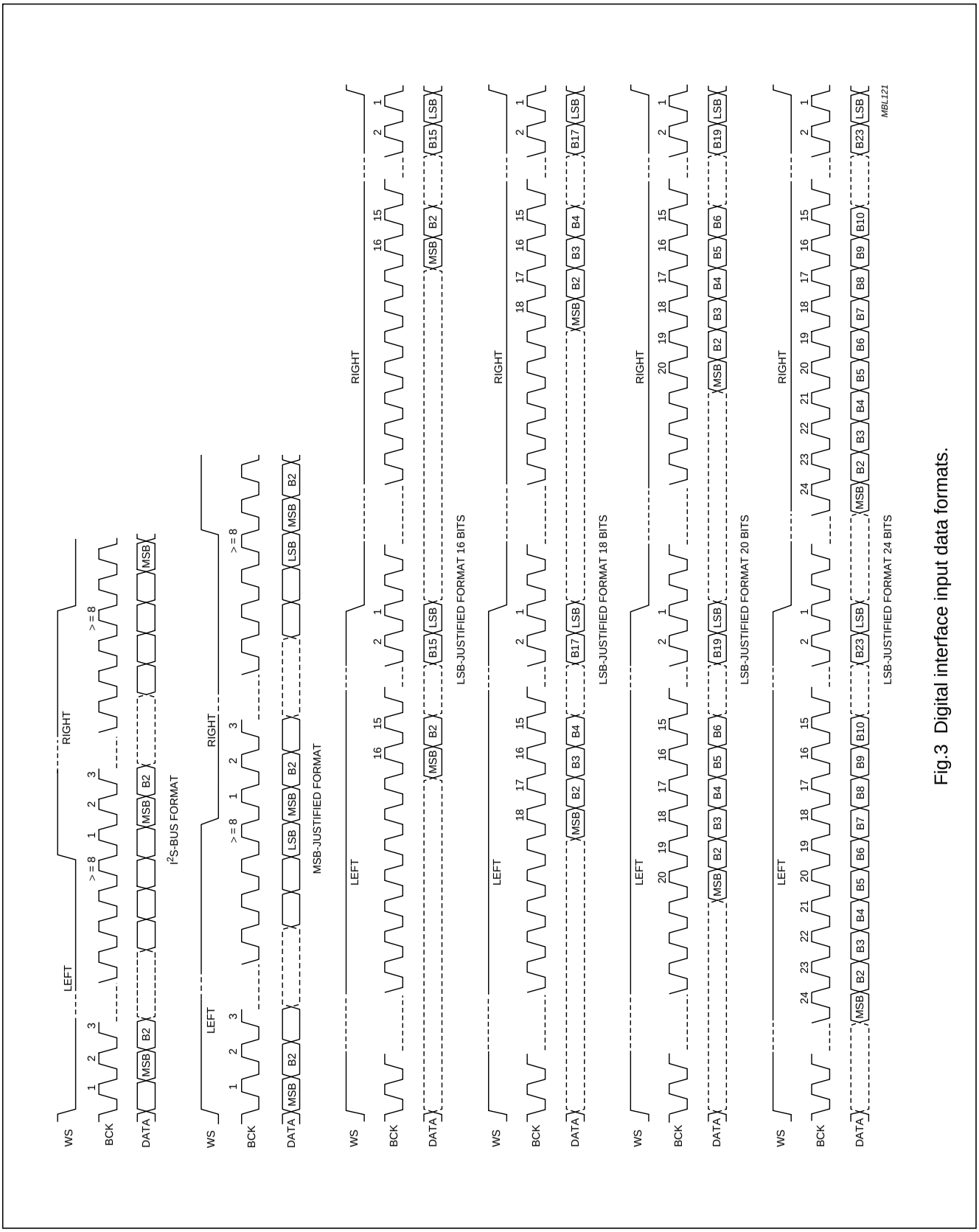


Fig.3 Digital interface input data formats.

L3 INTERFACE

The following system and digital sound processing features can be controlled in the L3 mode of the UDA1324TS:

- System clock frequency
- Data input format
- De-emphasis for 32, 44.1 and 48 kHz
- Volume
- Soft mute.

The exchange of data and control information between the microcontroller and the UDA1324TS is accomplished through a serial interface comprising the following signals:

- L3DATA
- L3MODE
- L3CLOCK.

Information transfer through the microcontroller bus is organized in accordance with the L3 interface format, in which two different modes of operation can be distinguished: address mode and data transfer mode.

Address mode

The address mode (see Fig.4) is required to select a device communicating via the L3 interface and to define the destination registers for the data transfer mode.

Data bits 7 to 2 represent a 6-bit device address where bit 7 is the MSB. The address of the UDA1324TS is 000101 (bit 7 to bit 2). If the UDA1324TS receives a different address, it will deselect its microcontroller interface logic.

Data transfer mode

The selected address remains active during subsequent data transfers until the UDA1324TS receives a new address command.

The fundamental timing of data transfers (see Fig.5) is essentially the same as the address mode. The maximum input clock frequency and data rate is $64f_s$.

Data transfer can only be in one direction, consisting of input to the UDA1324TS to program sound processing and other functional features. All data transfers are by 8-bit bytes. Data will be stored in the UDA1324TS after reception of a complete byte.

A multi-byte transfer is illustrated in Fig.6.

Registers

The sound processing and other feature values are stored in independent registers. The first selection of the registers is achieved by the choice of data type that is transferred. This is performed in the address mode using bit 1 and bit 0 (see Table 5).

Table 5 Selection of data transfer

BIT 1	BIT 0	TRANSFER
0	0	data (volume, de-emphasis, mute)
0	1	not used
1	0	status (system clock frequency, data input format)
1	1	not used

The second selection is performed by the 2 MSBs of the data byte (bit 7 and bit 6). The other bits in the data byte (bit 5 to bit 0) represent the value that is placed in the selected registers.

The ‘status’ settings are given in Table 6 and the ‘data’ settings are given in Table 7.

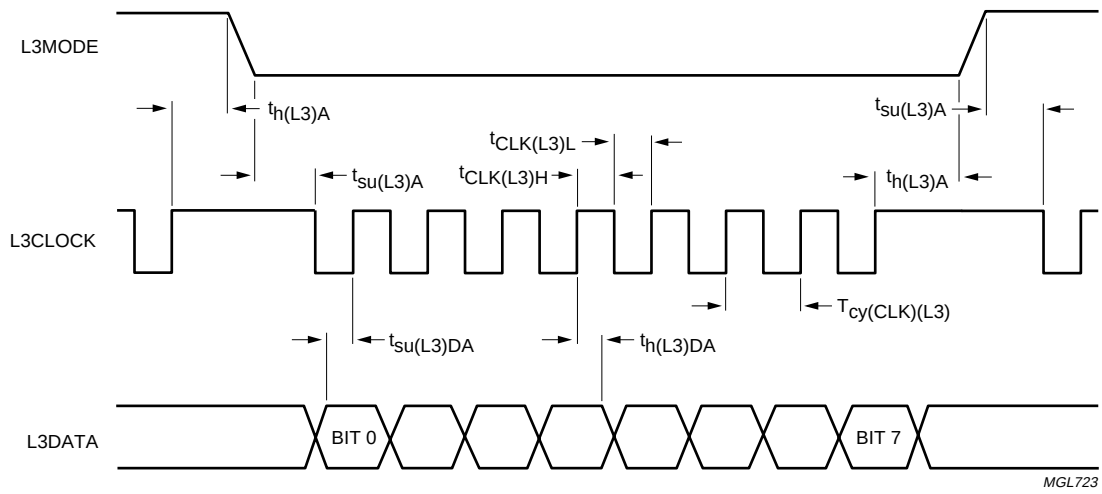


Fig.4 Timing address mode.

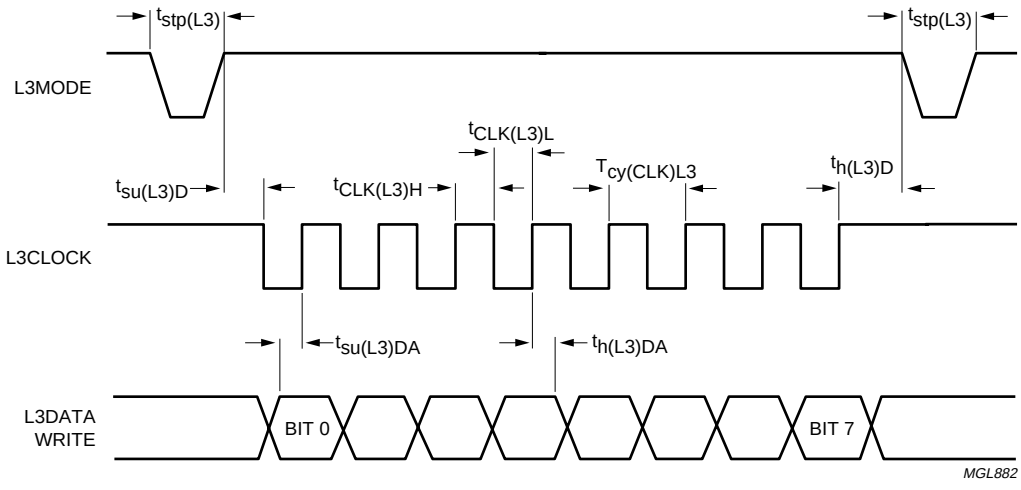


Fig.5 Timing data transfer mode.

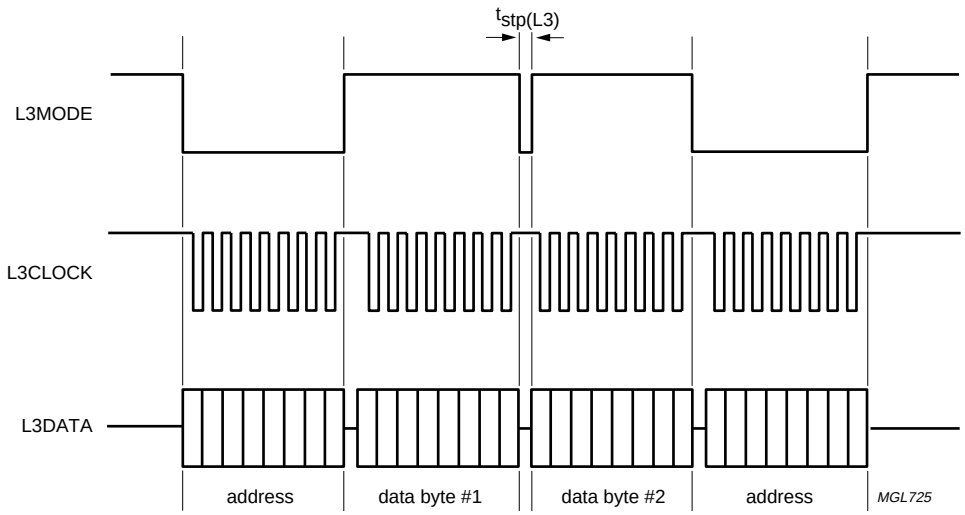


Fig.6 Multibyte data transfer.

Programming the features

When the data transfer of type ‘status’ is selected, the features for the system clock frequency and the data input format can be controlled.

Table 6 Data transfer of type ‘status’

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	SC1	SC0	IF2	IF1	IF0	0	SC = system clock frequency (2 bits); see Table 8
								IF = data input format (3 bits); see Table 9
1	0	0	0	0	0	0	0	not used

When the data transfer of type ‘data’ is selected, the features for volume, de-emphasis and mute can be controlled.

Table 7 Data transfer of type ‘data’

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	VC5	VC4	VC3	VC2	VC1	VC0	VC = volume control (6 bits); see Table 11
0	1	0	0	0	0	0	0	not used
1	0	0	DE1	DE0	MT	0	0	DE = de-emphasis (2 bits); see Table 10
								MT = mute (1 bit); see Table 12
1	1	0	0	0	0	0	1	default setting

SYSTEM CLOCK FREQUENCY

The system clock frequency is a 2-bit value to select the external clock frequency.

Table 8 System clock settings

SC1	SC0	FUNCTION
0	0	$512f_s$
0	1	$384f_s$
1	0	$256f_s$
1	1	not used

DATA FORMAT

The data format is a 3-bit value to select the used data format.

Table 9 Data input format settings

IF2	IF1	IF0	FORMAT
0	0	0	I^2S-bus
0	0	1	LSB-justified 16 bits
0	1	0	LSB-justified 18 bits
0	1	1	LSB-justified 20 bits
1	0	0	MSB-justified
1	0	1	not used
1	1	0	not used
1	1	1	not used

DE-EMPHASIS

De-emphasis is a 2-bit value to enable the digital de-emphasis filter.

Table 10 De-emphasis settings

DE1	DE0	FUNCTION
0	0	no de-emphasis
0	1	de-emphasis, 32 kHz
1	0	de-emphasis, 44.1 kHz
1	1	de-emphasis, 48 kHz

VOLUME CONTROL

The volume control is a 6-bit value to program the volume attenuation from 0 to −60 dB and −∞ dB in steps of 1 dB.

Table 11 Volume settings

VC5	VC4	VC3	VC2	VC1	VC0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	−1
0	0	0	0	1	1	−2
:	:	:	:	:	:	:
1	1	0	0	1	1	−51
1	1	0	1	0	0	
1	1	0	1	0	1	−52
1	1	0	1	1	0	
1	1	0	1	1	1	−54
1	1	1	0	0	0	
1	1	1	0	0	1	−57
1	1	1	0	1	0	
1	1	1	0	1	1	
1	1	1	1	0	0	−60
1	1	1	1	0	1	
1	1	1	1	1	0	−∞
1	1	1	1	1	1	

MUTE

Mute is a 1-bit value to enable the digital mute.

Table 12 Mute setting

MT	FUNCTION
0	no muting
1	muting

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	–	5.0	V
V_{DDA}	analog supply voltage	note 1	–	5.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage	note 2	–3000	+3000	V
		note 3	–300	+300	V
$I_{sc(DAC)}$	short-circuit current of DAC	note 4			
		output short-circuited to $V_{SSA(DAC)}$	–	450	mA
		output short-circuited to $V_{DDA(DAC)}$	–	300	mA

Notes

1. All supply connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor, except pin 14 which can withstand ESD pulses of –2500 to +2500 V.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.
4. Short-circuit test at T_{amb} = 0 °C and V_{DDA} = 3 V. DAC operation after short-circuiting cannot be warranted.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	190	K/W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611-E”*.

DC CHARACTERISTICS

V_{DDD} = V_{DDA} = 2.0 V; T_{amb} = 25 °C; R_L = 5 kΩ; all voltages referenced to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage	note 1	1.9	2.0	2.7	V
V_{DDD}	digital supply voltage	note 1	1.9	2.0	2.7	V
I_{DDA}	analog supply current	operating	–	3.0	–	mA
I_{DDD}	digital supply current	operating	–	1.5	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital inputs: pins BCK, WS, DATAI, SYSCLK, APPL0, APPL1, APPL2 and APPL3						
V_{IH}	HIGH-level input voltage		$0.8V_{DDD}$	–	–	V
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DDD}$	V
$\|I_{LI}\|$	input leakage current		–	–	1	μA
C_I	input capacitance		–	–	10	pF
Three-level input: pin APPSEL						
V_{IH}	HIGH-level input voltage		$0.8V_{DDD}$	–	V_{DDD} + 0.5	V
V_{IM}	MIDDLE-level input voltage		$0.3V_{DDD}$	–	$0.7V_{DDD}$	V
V_{IL}	LOW-level input voltage		–0.5	–	$0.2V_{DDD}$	V
DAC						
$V_{ref(DAC)}$	reference voltage	referenced to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1%; R_L = 5 kΩ	–	0.16	–	mA
R_O	output resistance		–	0.15	2.0	Ω
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 2	–	–	50	pF

Notes

1. All supply connections must be made to the same external power supply unit.
2. When the DAC drives a capacitive load above 50 pF, a series resistance of 100 Ω must be used to prevent oscillations in the output operational amplifier.

AC CHARACTERISTICS

$V_{DDD} = V_{DDA}$ = 2.0 V; f_i = 1 kHz; T_{amb} = 25 °C; R_L = 5 kΩ; all voltages referenced to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DAC						
$V_{o(rms)}$	output voltage (RMS value)		–	500	–	mV
ΔV_o	unbalance voltage between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB	–	–83	–78	dB
		at –60 dB; A-weighted	–	–36	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	–	97	–	dB
α_{cs}	channel separation		–	100	–	dB
PSRR	power supply ripple rejection ratio	f_{ripple} = 1 kHz; V_{ripple} = 100 mV (p-p)	–	50	–	dB

TIMING

V_{DDD} = V_{DDA} = 1.9 to 2.7 V; T_{amb} = –40 to +85 °C; R_L = 5 kΩ; all voltages referenced to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock (see Fig.7)						
T_{sys}	system clock cycle time	$f_{sys} = 256f_s$	78	88	244	ns
		$f_{sys} = 384f_s$	52	59	162	ns
		$f_{sys} = 512f_s$	39	44	122	ns
t_{CWL}	LOW-level system clock pulse width	f_{sys} < 19.2 MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		$f_{sys} \geq$ 19.2 MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns
t_{CWH}	HIGH-level system clock pulse width	f_{sys} < 19.2 MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		$f_{sys} \geq$ 19.2 MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns
Digital interface with I²S-bus (see Fig.8)						
$T_{cy(BCK)}$	bit clock cycle time		300	–	–	ns
t_{BCKH}	bit clock HIGH time		100	–	–	ns
t_{BCKL}	bit clock LOW time		100	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{su(DATAI)}$	data input set-up time		20	–	–	ns
$t_{h(DATAI)}$	data input hold time		0	–	–	ns
$t_{su(WS)}$	word select set-up time		20	–	–	ns
$t_{h(WS)}$	word select hold time		10	–	–	ns
Control L3 interface (see Figs 4 and 5)						
$T_{cy(CLK)L3}$	L3CLOCK cycle time		500	–	–	ns
$t_{CLK(L3)H}$	L3CLOCK HIGH time		250	–	–	ns
$t_{CLK(L3)L}$	L3CLOCK LOW time		250	–	–	ns
$t_{su(L3)A}$	L3MODE set-up time for address mode		190	–	–	ns
$t_{h(L3)A}$	L3MODE hold time for address mode		190	–	–	ns
$t_{su(L3)D}$	L3MODE set-up time for data transfer mode		190	–	–	ns
$t_{h(L3)D}$	L3MODE hold time for data transfer mode		190	–	–	ns
$t_{su(L3)DA}$	L3DATA set-up time for data transfer and address mode		190	–	–	ns
$t_{h(L3)DA}$	L3DATA hold time for data transfer and address mode		30	–	–	ns
$t_{stp(L3)}$	L3MODE stop time for data transfer mode		190	–	–	ns

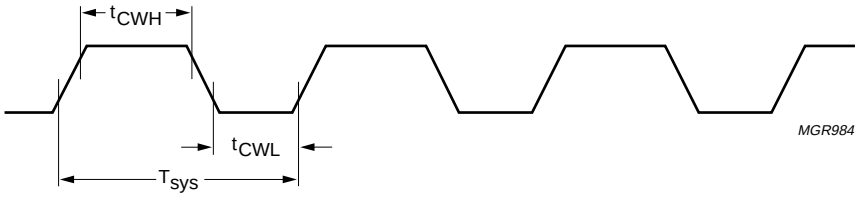


Fig.7 System clock timing.

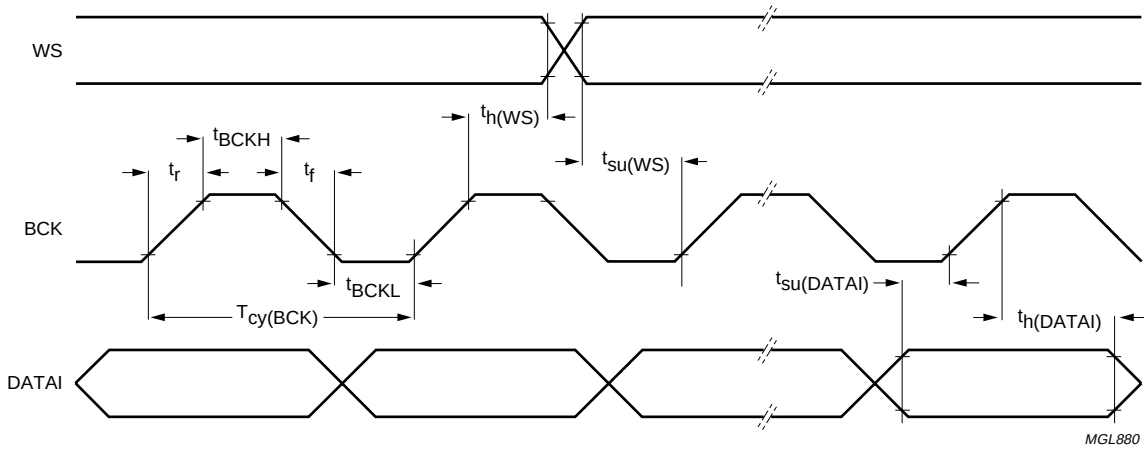


Fig.8 I^2S-bus timing.

APPLICATION INFORMATION

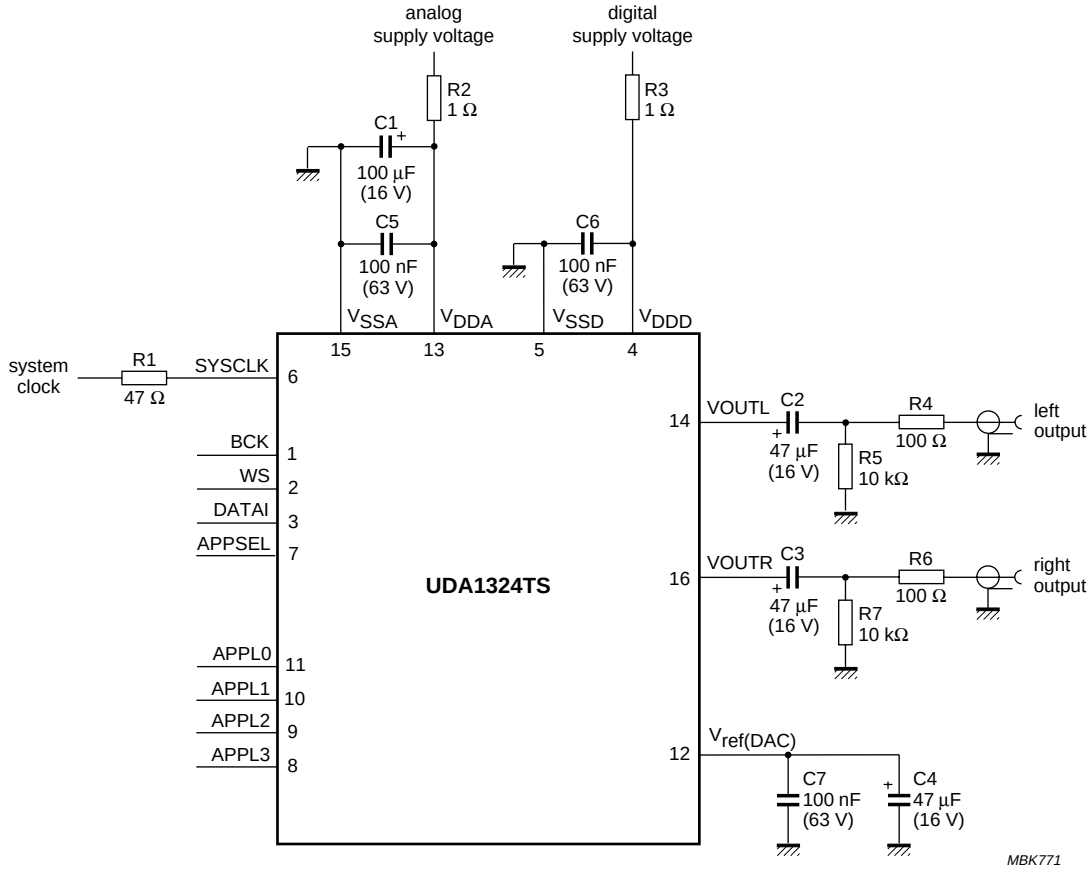
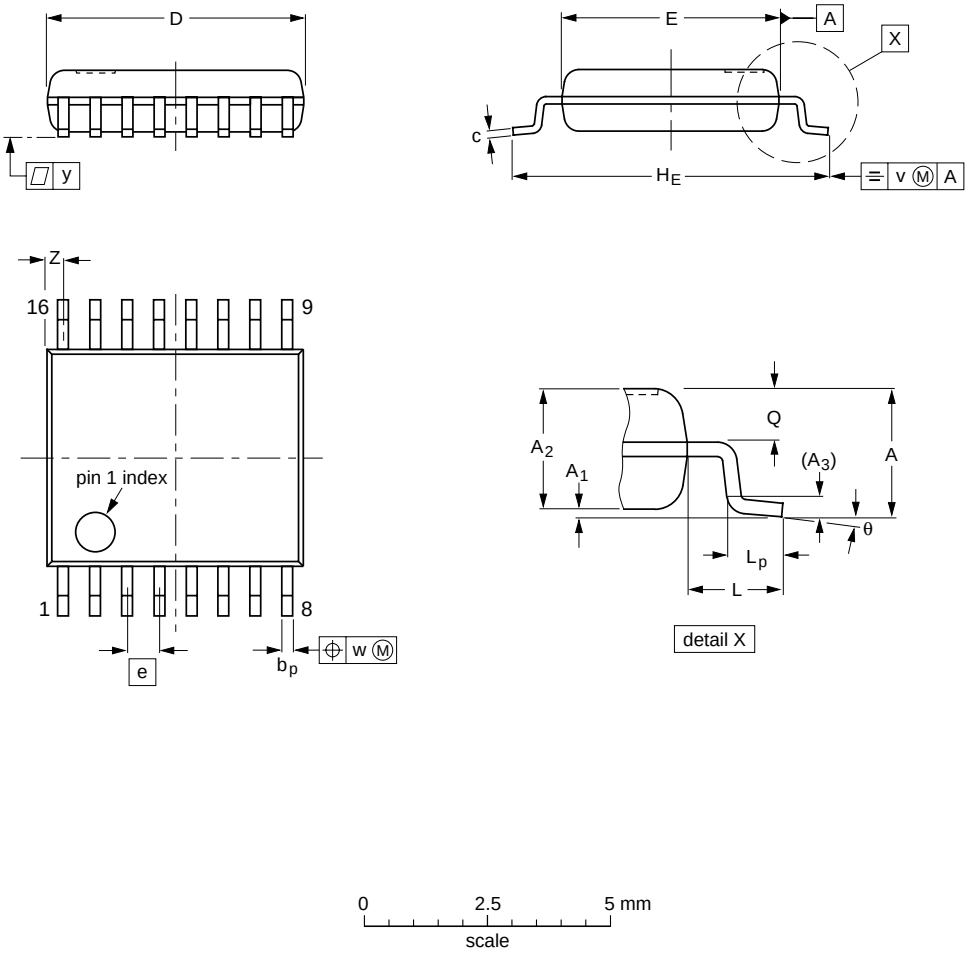


Fig.9 Application diagram.

PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm **SOT369-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1		MO-152				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
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Printed in The Netherlands 545002/25/03/pp20 Date of release: 2000 Jan 20 Document order number: 9397 750 06676

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