NATURAL PFC LED LIGHTING DRIVER CONTROLLER

Check for Samples: TPS92210

FEATURES

- **Flexible Operation Modes**
  - **Constant On-Time Enables Single Stage PFC Implementation**
  - **Peak Primary Current**
- **Cascoded MOSFET Configuration**
  - **Fully Integrated Current Control Without Sense Resistor**
  - **Fast and Easy Startup**
- **Discontinuous Conduction Mode or Transition Mode Operation**
- **Transformer Zero Energy Detection**
  - **Enables Valley Switching Operation**
  - **Helps to Achieve High Efficiency and Low EMI**
- **Open LED Detection**
- **Advanced Overcurrent Protection**
- **Output Overvoltage Protection**
- **Line Surge Ruggedness**
- **Internal Over-Temperature Protection**
- **8-Pin SOIC (D) Package**

APPLICATIONS

- **TRIAC Dimmable LED Lighting Designs**
- **Residential LED Lighting Drivers for Retrofit A19 (E27/26, E14), PAR30/38, GU10, MR16, BR**
- **Drivers for Down and Architectural Wall Sconces, Pathway and Overhead Lighting**
- **Commercial Troffers and Downlights**

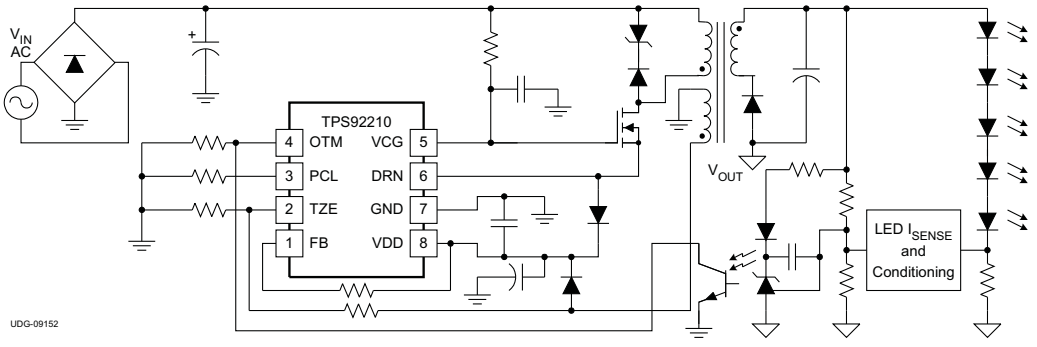
DESCRIPTION

The TPS92210 is a natural power factor correction (PFC) light emmitting diode (LED) lighting driver controller with advanced energy features to provide high efficiency control for LED lighting applications.

A PWM modulation algorithm varies both the switching frequency and primary current while maintaining discontinuous or transition mode operation in all regions of operation. The TPS92210 cascode architecture enables low switching loss in the primary side and when combined with the discontinuous conduction mode (DCM) operation ensures that there is no reverse recovery loss in the output rectifier. These innovations result in efficiency, reliability or system cost improvements over a conventional flyback architecture.

The TPS92210 offers a predictable maximum power threshold and a timed response to an overload, allowing safe handling of surge power requirements. The overload fault response is user-programmed for retry or latch mode. Additional protection features include open-LED detection by output overvoltage protection and thermal shutdown.

The TPS92210 is offered in the 8-pin SOIC (D) package. Operating junction temperature range is –40°C to 125°C



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

OPERATING TEMPERATURE RANGE, T_A	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	TRANSPORT MEDIA	QUANTITY
–40°C to 125°C	SOIC	TPS92210DR	8	Tape and Reel	2500
		TPS92210D		Tube	75

ABSOLUTE MAXIMUM RATINGS(1)

All voltages are with respect to GND, –40°C < T_J = T_A < 125°C, all currents are positive into and negative out of the specified terminal (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage range	VDD	–0.5	25	V
	DRN, during conduction	–0.5	2.0	
	DRN, during non-conduction		20	
	VCG (2)	–0.5	16	
	TZE, OTM, PCL (3)	–0.5	7	
	FB (3)	–0.5	1.0	
	VDD – VCG	–7	10	
Continuous input current	I_{VCG} (2)		10	mA
Input current range	I_{TZE}, I_{OTM}, I_{PCL}, I_{FB} (3)	–3	1	
Output current	DRN		-4	A
	DRN, pulsed 200ns, 2% duty cycle	–6	1.5	
Operating junction temperature	T_J	–40	150	°C
Storage temperature range	T_{stg}	–65	150	°C
Lead temperature	Soldering, 10 s		260	°C

(1) These are stress ratings only. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability

(2) Voltage on VCG is internally clamped. The clamp level varies with operating conditions. In normal use, VCG is current fed with the voltage internally limited

(3) In normal use, pins OTM, PCL, TZE, and FB are connected to resistors to GND and internally limited in voltage swing

THERMAL INFORMATION

THERMAL METRIC[1]		TPS92210 D 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	117.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	63.7	
θ_{JB}	Junction-to-board thermal resistance[4]	57.8	
ψ_{JT}	Junction-to-top characterization parameter[5]	15.3	
ψ_{JB}	Junction-to-board characterization parameter[6]	57.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted, all voltages are with respect to GND, –40°C < T_J = T_A < 125°C. Components reference Figure 17.

			MIN	MAX	UNIT
VDD	Input voltage		9	20	V
VCG	Input voltage from low-impedance source		9	13	
I_{VCG}	Input current from a high-impedance source		10	2000	µA
R_{OTM}	Resistor to GND	Shutdown/retry mode	25	100	kΩ
		Latch-off mode	150	750	
R_{PCL}	Resistor to GND		24.3	100	kΩ
R_{TZE1}	Resistor to auxiliary winding		50	200	kΩ
C_{VCG}	VCG capacitor		33	200	nF
C_{BP}	VDD bypass capacitor, ceramic		0.1	1.0	µF

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MAX	UNIT
ESD Rating, Human Body Model (HBM)	1.5	kV
ESD Rating, Charged Device Model (CDM)	500	V

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: V_{VDD} = 12 V, V_{VCG} = 12 V, V_{TZE} = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1-µF capacitor exists between VDD and GND, a 0.1-µF capacitor exists between VCG and GND, R_{PCL}= 33.2 kΩ, R_{OTM}= 380 kΩ, –40°C < T_A< +125°C, $T_J = T_A$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD and VCG SUPPLY						
$VCG_{(OPERATING)}$	VCG Voltage, Operating	VDD = 14 V, I_{VCG} = 2.0 mA	13	14	15	V
$VCG_{(DISABLED)}$	VCG Voltage, PWM Disabled	VDD = 12 V, I_{VCG} = 15 µA, I_{FB} = 350 µA	15	16	17	V
ΔVCG	Rise in VCG Clamping Voltage During UVLO, LPM, or Fault	$VCG_{(DISABLED)}$ – $VCG_{(OPERATING)}$	1.75	2	2.15	V
$I_{VCG(SREG)}$	VCG Shunt Regulator Current	VCG = ($VCG_{(DISABLED)}$ – 100 mV), VDD = 12 V		6	10	µA
$ΔVCG_{(SREG)}$	VCG Shunt Load Regulation	10 µA ≤ I_{VCG} ≤ 5 mA, I_{FB} = 350 µA		125	200	mV
$VCG_{(LREG)}$	VCG LDO Regulation Voltage	VDD = 20 V, I_{VCG} = – 2 mA		13		V
$VCG_{(LREG, DO)}$	VCG LDO Dropout Voltage	VDD – VCG, VDD = 11 V, I_{VCG} = – 2 mA	1.5	2	2.5	V
$VDD_{(ON)}$	UVLO Turn-on Threshold		9.7	10.2	10.7	V
$VDD_{(OFF)}$	UVLO Turn-off Threshold		7.55	8	8.5	V
$ΔVDD_{(UVLO)}$	UVLO Hysteresis		1.9	2.2	2.5	V
$I_{VDD(OPERATING)}$	Operating Current	VDD= 20 V	2.5	3	3.7	mA
$I_{VDD(LPM)}$	Idle Current Between Bursts	I_{FB} = 350 µA		550	900	µA
$I_{VDD(UVLO)}$	Current for VDD < UVLO	VDD = $VDD_{(on)}$ – 100 mV, increasing		225	300	µA
$R_{DS,ON(VDD)}$	VDD Switch on Resistance, DRN to VDD	VCG = 12 V, VDD == 7V, I_{DRN} = 50 mA		4	10	Ω
$VDD_{(FAULT\ RESET)}$	VDD for Fault Latch Reset		5.6	6	6.4	V
MODULATION						
$t_{SW(HF)}$ (1)	Minimum switching period, frequency modulation (FM) mode	I_{FB} = 0 µA, (1)	7.125	7.5	7.875	µs
$t_{SW(LF)}$ (1)	Maximum switching period, reached at end of frequency modulation (FM) range	I_{FB} = $I_{FB,\ CNR3}$ – 20 µA, (1)	31	34	38	µs
$I_{DRN(peak,max)}$	Maximum peak driver current over amplitude modulation (AM) range	I_{FB} = 0 µA, R_{PCL} = 33. 2 kΩ	2.85	3	3.15	A
		I_{FB} = 0 µA, R_{PCL} = 100 kΩ	0.8	0.9	1.0	A
$I_{DRN(peak,min)}$	Minimum peak driver current reached at end of AM modulation range	$I_{FB,\ CNR2}$ + 10 µA, R_{PCL} = 33.2 kΩ	0.7	0.85	1.1	A
		$I_{FB,\ CNR2}$ + 10 µA, R_{PCL} = 100 kΩ	0.2	0.33	0.5	A
K_P	Maximum power constant	$I_{DRN(peak,max)}$ = 3 A	0.54	0.60	0.66	W/µH
$I_{DRN(peak,absmin)}$	Minimum peak driver independent of R_{PCL} or AM control	R_{PCL} = OPEN	0.3	0.45	0.6	A
$t_{BLANK(ILIM)}$	Leading ddge current limit blanking time	I_{FB} = 0 µA, R_{PCL} = 100 kΩ, 1.2-A pull-up on DRN		220		ns
V_{PCL}	PCL Voltage	I_{FB} = 0 µA	2.94	3	3.06	V
		I_{FB} = ($I_{FB,CNR3}$ – 20 µA) (1)	0.95	1	1.1	
$I_{FB,CNR1}$ (2)	I_{FB} range for FM modulation	I_{FB} increasing, t_{SW} = $t_{SW(LF)}$, and $I_{DRN(PK,)}$ = $I_{DRN,PK(MAX)}$	145	165	195	µA
$I_{FB,CNR2}$ – $I_{FB,CNR1}$ (2)	I_{FB} range for AM modulation	t_{SW} = $t_{SW(LF)}$, $I_{DRN\ PK}$ ranges from $I_{DRN,PK(MAX)}$ to $I_{DRN,PK(MIN)}$	35	45	65	µA
$I_{FB,CNR3}$ – $I_{FB,CNR2}$ (2)	I_{FM} range for low power mode(LPM) modulation	I_{FB} increasing until PWM action is disabled entering a burst-off state	45	70	90	µA
$I_{FB,\ LPM-HYST}$ (2)	I_{FB} hysteresis during LPM modulation to enter burst on and off states	I_{FB} decreasing from above $I_{FB,CNR3}$	10	25	40	µA
FB	Voltage of FB	I_{FB} = 10 µA	0.34	0.7	0.84	V

(1) t_{SW} sets a minimum switching period. Following the starting edge of a PWM on time, under normal conditions, the next on time is initiated following the first valley switching at TZE after t_{SW}. The value of t_{SW} is modulated by I_{FB} between a minimum of $t_{SW(HF)}$ and a maximum of $t_{SW(LF)}$ In normal operation, $t_{SW(HF)}$ sets the maximum operating frequency of the power supply and $t_{SW(LF)}$ sets the minimum operating frequency of the power supply.

(2) Refer to Figure 24.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated: V_{VDD} = 12 V, V_{VCG} = 12 V, V_{TZE} = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1-µF capacitor exists between VDD and GND, a 0.1-µF capacitor exists between VCG and GND, R_{PCL}= 33.2 kΩ, R_{OTM}= 380 kΩ, –40°C < T_A< +125°C, $T_J = T_A$

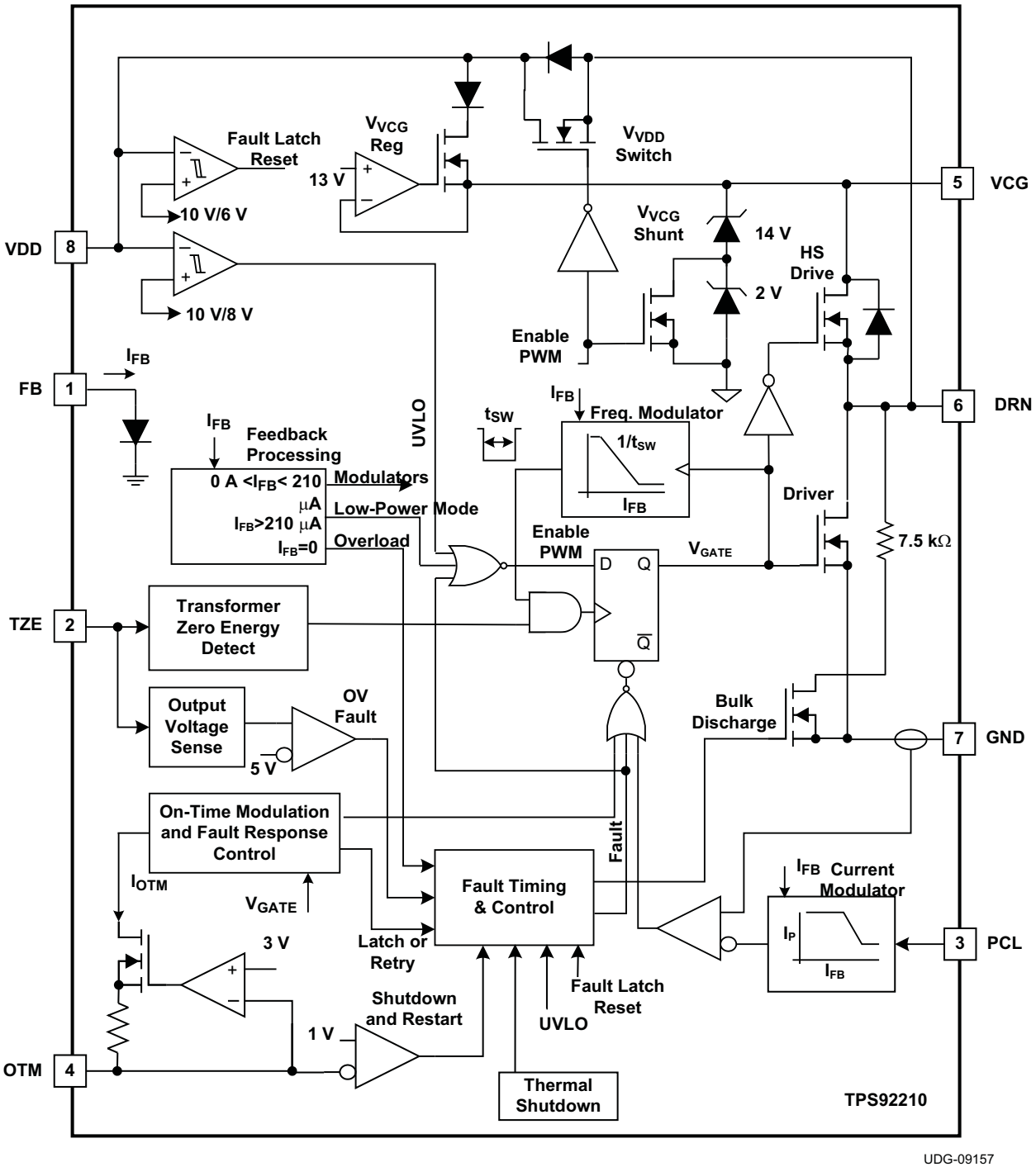
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRANSFORMER ZERO ENERGY DETECTION						
$TZE_{(TH)}$	TZE zero crossing threshold	TZE high to low generates switching period (t_{SW} has expired)	5	20	50	mV
$TZE_{(CLAMP)}$	TZE low clamp voltage	I_{TZE} = –10 µA	-220	-160	-100	mV
$TZE_{(START)}$	TZE voltage threshold to enable the internal start timer	Driver switching periods generated at start timer rate	0.1	0.15	0.2	V
$t_{DLY(TZ2D)}$	Delay from zero crossing to Driver turn-on	150-Ω pull-up to 12-V on DRN		150		ns
$t_{WAIT(TZE)}$	Wait time for zero energy detection	Driver turn-on edge generated following t_{SW} with previous zero current detected	2	2.4	2.8	µs
t_{ST}	Starter time-out period	TZE = 0 V	150	240	300	µs
DRIVER						
$R_{DS(on)(DRN)}$	Driver on-resistance	I_{DRN} = 4.0 A		90	190	mΩ
$I_{DRN(OFF)}$	Driver off-leakage current	I_{DRN} = 12 V		1.5	20	µA
$R_{DS(on)(HSDRV)}$	HSDRV on-resistance	HS Driver Current = 50 mA		6	11	Ω
$I_{DRN,DSCH}$	DRN Bulk Discharge	VDD open, DRN = 12 V, Fault latch set	2	2.8	3.6	mA
OVERVOLTAGE FAULT						
$TZE_{(OVP)}$	Overvoltage fault threshold at TZE	Fault latch set	4.85	5	5.15	V
$t_{BLANK,OVP}$	TZE blanking and OVP sample time from the turn-off edge of DRN		0.6	1	1.7	µs
$I_{TZE(bias)}$	TZE Input bias current	TZE = 5 V	–0.1		–0.1	µA
OVERLOAD FAULT						
$I_{FB(OL)}$	Current to trigger overload delay timer		0	1.5	3	µA
t_{OL}	Delay to overload fault	I_{FB} = 0 A continuously	200	250	300	ms
t_{RETRY}	Retry delay in retry mode or after shutdown command	R_{OTM} = 76 kΩ		750		ms
$R_{OTM(TH)}$	Boundary R_{OTM} between latch-off and retry modes	See (3)	100	120	150	kΩ
SHUTDOWN THRESHOLD						
$V_{OTM(SR)}$	Shutdown/retry threshold	OTM high to low	0.7	1	1.3	V
$I_{OTM,PU}$	OTM current when OTM is pulled low	$V_{OTM} = V_{OTM(SR)}$	–600	–450	–300	µA
MAXIMUM ON TIME						
t_{OTM}	Latch-off	R_{OTM} = 383 kΩ	3.43	3.83	4.23	µs
	Shutdown/retry	R_{OTM} = 76 kΩ	3.4	3.8	4.2	µs
V_{OTM}	OTM voltage		2.7	3	3.3	V
THERMAL SHUTDOWN						
T_{SD} (4)	Shutdown temperature	T_J, temperature rising (4)		165		°C
T_{SD_HYS} (4)	Hysteresis	T_J, temperature falling, degrees below t_{SD} (4)		15		°C

(3) A latch-off or a shutdown/retry fault response to a sustained overload is selected by the range of R_{OTM}. To select the latch-off mode, R_{OTM} should be greater than 150 kΩ and t_{OTM} is given by $R_{OTM} \times (1.0 \times 10^{-11})$. To select the shutdown/retry mode, R_{OTM} should be less than 100 kΩ and t_{OTM} is given by $R_{OTM} \times (5.0 \times 10^{-11})$.

(4) Thermal shutdown occurs at temperatures higher than the normal operating range. Device performance at or near thermal shutdown temperature is not specified or assured.

DEVICE INFORMATION

Functional Block Diagram



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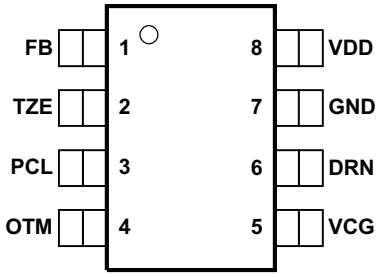
PIN CONFIGURATION



PIN DESCRIPTIONS

TERMINAL		I/O	DESCRIPTION
NAME	No.		
DRN	6	O	The DRN pin is the drain of the internal low voltage power MOSFET of the TPS92210 and carries the peak primary inductor current, $I_{PEAK(pri)}$. Connect this pin to the source of the external cascode power MOSFET. A schottky diode between DRN and VDD is used to provide initial bias at startup.
FB	1	I	The FB pin is regulated at 0.7 V and only detects current input (FB current,I_{FB}) which commands the operating mode of TPS92210. For peak-current mode control, this pin is connected to the emitter of the feedback opto coupler. In constant on-time control, the minimum switching period is programmed by forcing a constant current into this pin.
GND	7	—	This GND pin is the current return terminal for both the analog and power signals in the TPS92210. This terminal carries the full drain current, I_{DRN}, which is equal to the peak primary current, $I_{PEAK(pri)}$, in addition to the bias supply current (I_{VDD}) , and the gate voltage current (I_{VCG}).
OTM	4	I	the OTM pin is internally regulated at 3 V and used to program the on-time of the cascode (flyback) switch by connecting a resistor (R_{OTM}) from this pin to the quiet return of GND. The collector of the opto-coupler is connected to this pin for constant-on time control. The range of impedance connected at this pin determines the system fault response (latch-off or shutdown/retry) to overload and brownout fault conditions. An external shutdown/retry response can be initiated by pulling this pin low below 1 V.
PCL	3	I	The PCL pin programs the peak primary inductor current that is reached each switching cycle. The primary current is sensed with the $R_{DS(on)}$ of the internal MOSFET and is programmed by setting a threshold by connecting a low power resistor from this pin to the quiet return of GND.
TZE	2	I	A resistive divider between the primary-side auxiliary winding and this pin is used to detect when the transformer is demagnetized resulting in *transformer zero energy*. The ratio of the resistive divider at this pin can also be used to program the output overvoltage protection (OVP) feature.
VCG	5	—	The VCG pin provides the bias voltage for the gate of the cascode MOSFET. Place a 0.1-µF ceramic capacitor between VCG and GND, as close as possible to the high-voltage MOSFET. This pin also provides start-up bias through a resistor R_{SU}, which is connected between this pin and the bulk voltage.
VDD	8	—	VDD is the bias supply pin for the TPS92210. It can be derived from an external source, or an auxiliary winding. Place a 0.1-µF ceramic capacitor between VDD and GND, as close to the device as possible. This pin also enables and disables the general functions of the TPS92210 using the UVLO feature.

TYPICAL CHARACTERISTICS

Unless otherwise stated: V_{VDD} = 12 V, V_{VCG} = 12 V, V_{TZE} = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1µF capacitor tied between VDD and GND, a 0.1-µF capacitor tied between VCG and GND, R_{PCL} = 33.2 kΩ, R_{OTM} = 380 kΩ, –40°C < T_A < +125°C, T_J = T_A

BIAS SUPPLY CURRENT
vs
BIAS SUPPLY VOLTAGE DURING OPERATION

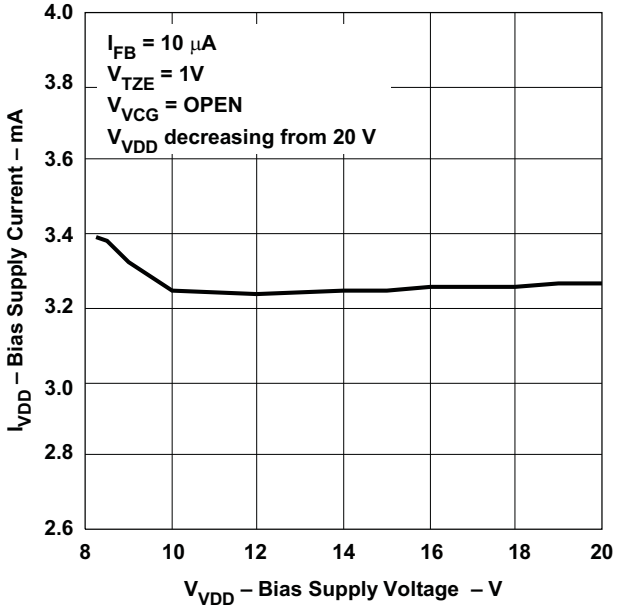


Figure 1.

BIAS SUPPLY CURRENT
vs
BIAS SUPPLY VOLTAGE DURING LOW POWER MODE

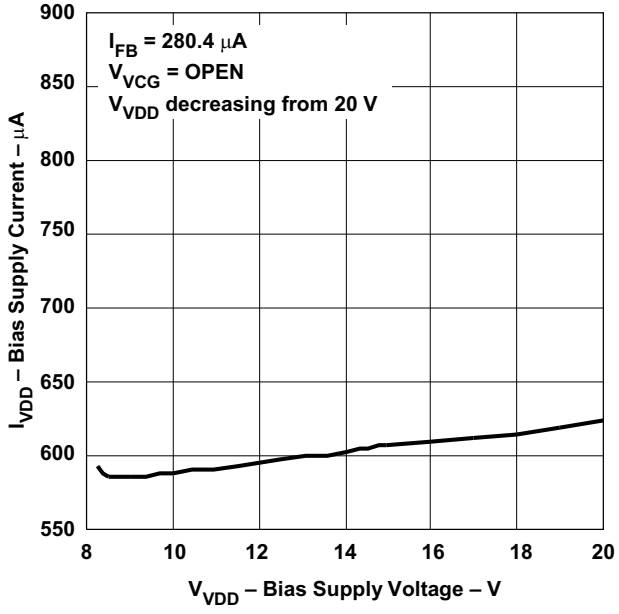


Figure 2.

BIAS SUPPLY CURRENT
vs
TEMPERATURE DURING LOW POWER MODE

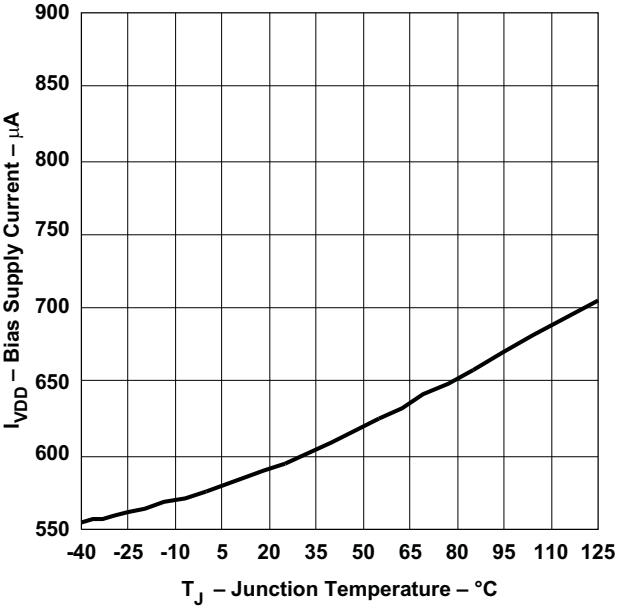


Figure 3.

OPERATIONAL I_{VDD} – BIAS CURRENT
vs
BIAS VOLTAGE

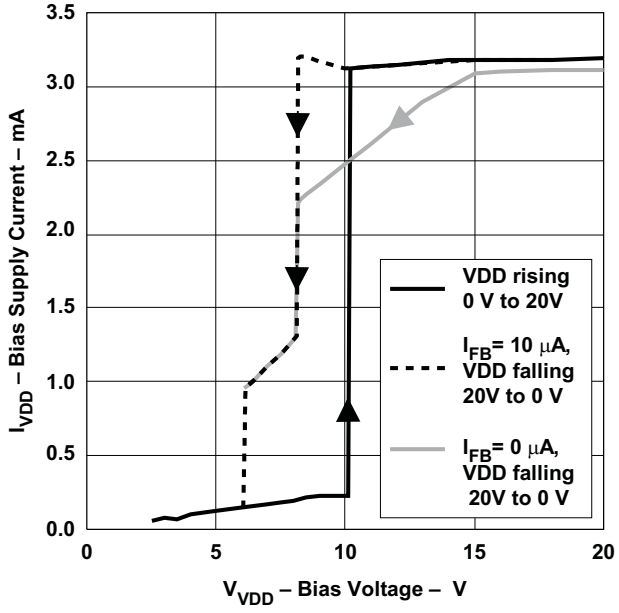


Figure 4.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated: V_{VDD} = 12 V, V_{VCG} = 12 V, V_{TZE} = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1µF capacitor tied between VDD and GND, a 0.1-µF capacitor tied between VCG and GND, R_{PCL} = 33.2 kΩ, R_{OTM} = 380 kΩ, –40°C < T_A < +125°C, T_J = T_A

OSCILLATOR FREQUENCY vs FEEDBACK CURRENT

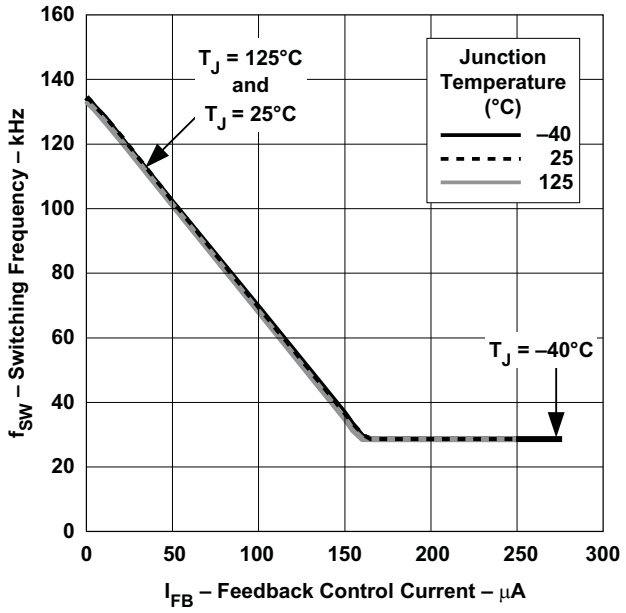


Figure 5.

MINIMUM SWITCHING PERIOD vs TEMPERATURE

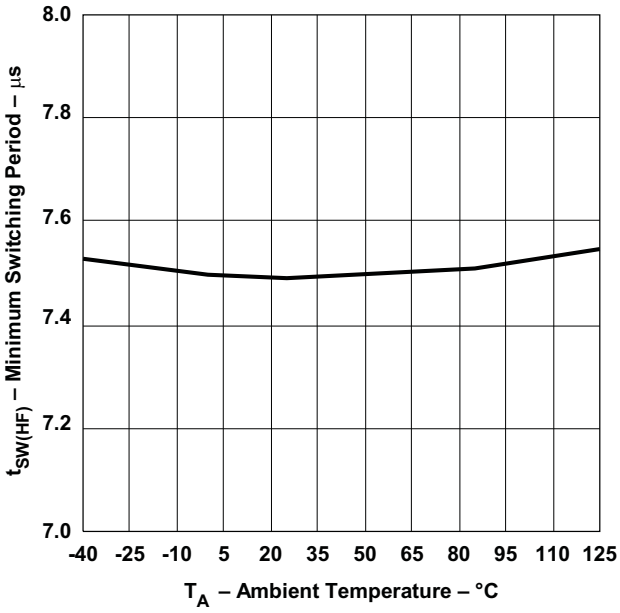


Figure 6.

SWITCHING PERIOD vs AMBIENT TEMPERATURE

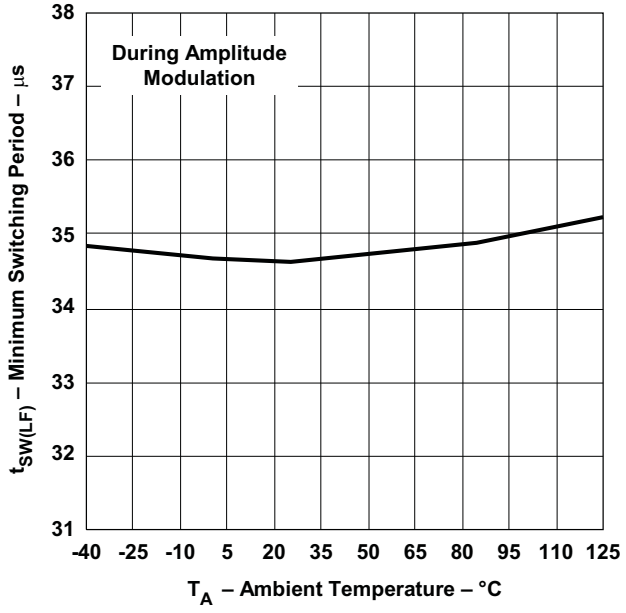


Figure 7.

PEAK DRN CURRENT vs FEEDBACK CURRENT

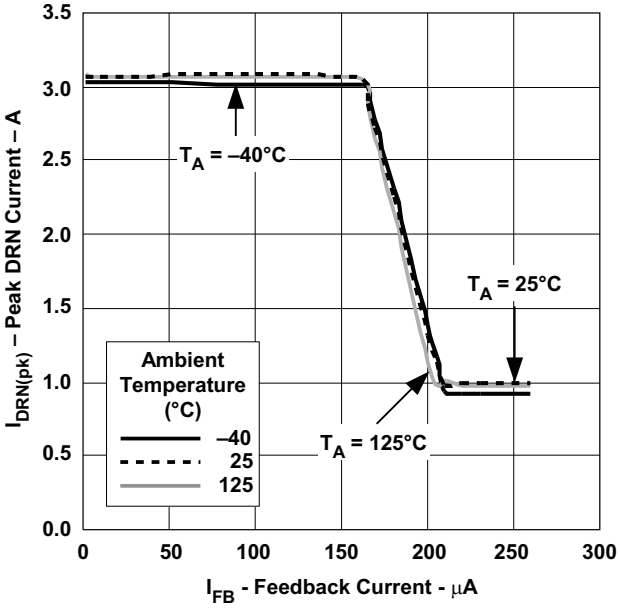


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated: V_{VDD} = 12 V, V_{VCG} = 12 V, V_{TZE} = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1µF capacitor tied between VDD and GND, a 0.1-µF capacitor tied between VCG and GND, R_{PCL} = 33.2 kΩ, R_{OTM} = 380 kΩ, –40°C < T_A < +125°C, T_J = T_A

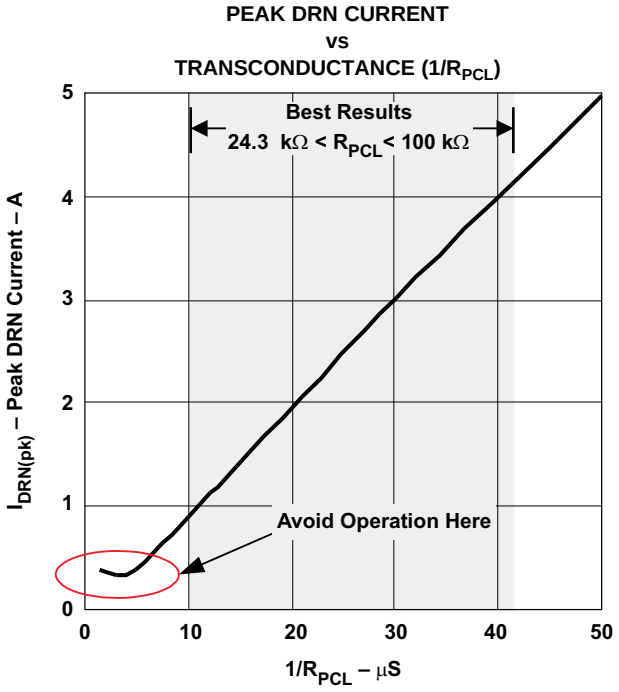


Figure 9.

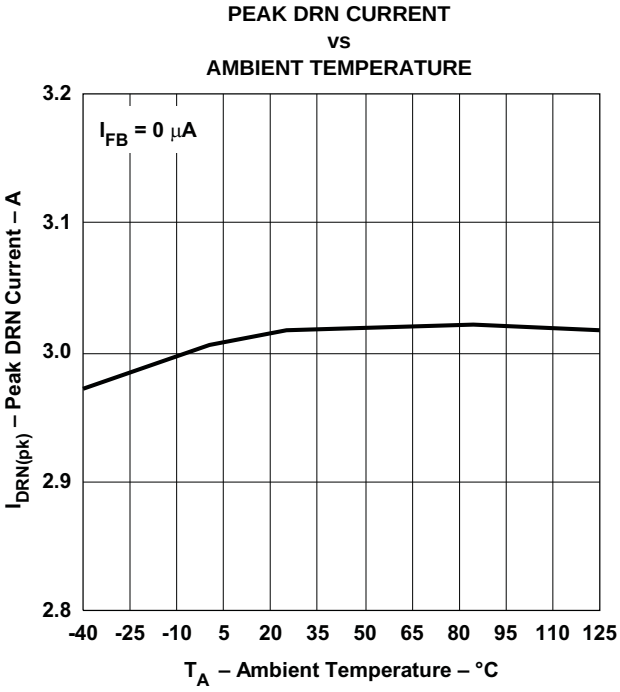


Figure 10.

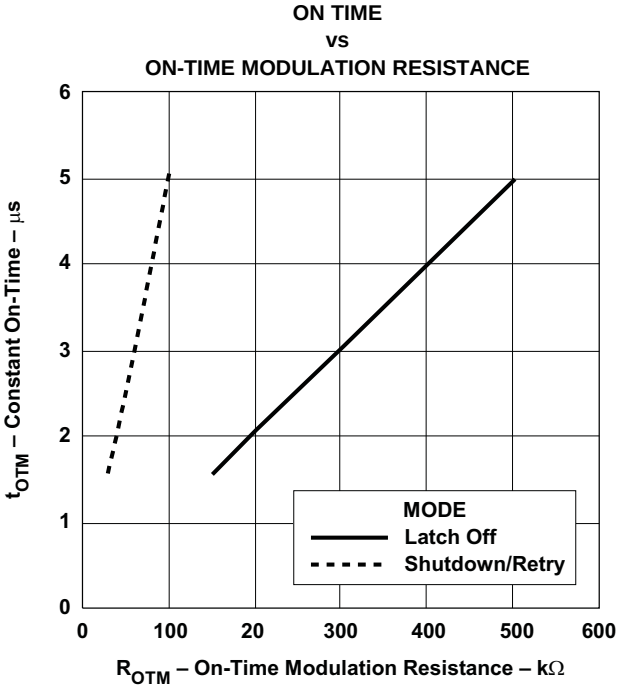


Figure 11.

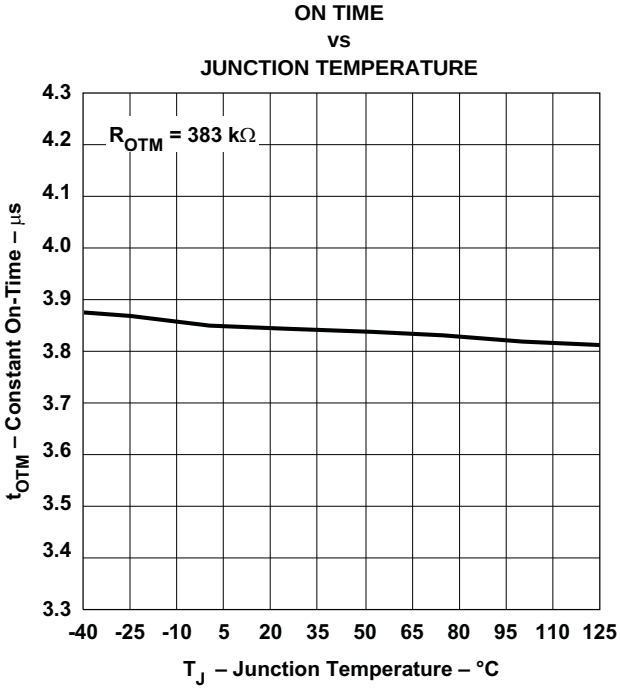


Figure 12.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated: V_{VDD} = 12 V, V_{VCG} = 12 V, V_{TZE} = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1µF capacitor tied between VDD and GND, a 0.1-µF capacitor tied between VCG and GND, R_{PCL} = 33.2 kΩ, R_{OTM} = 380 kΩ, –40°C < T_A < +125°C, T_J = T_A

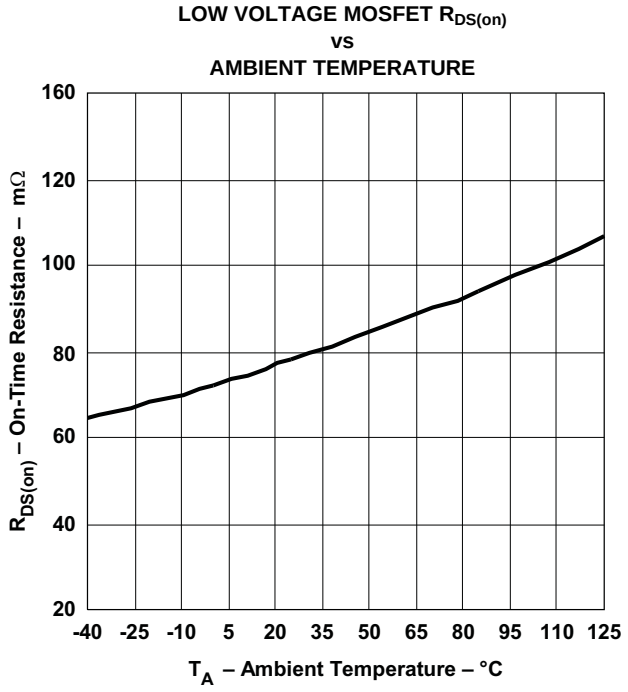


Figure 13.

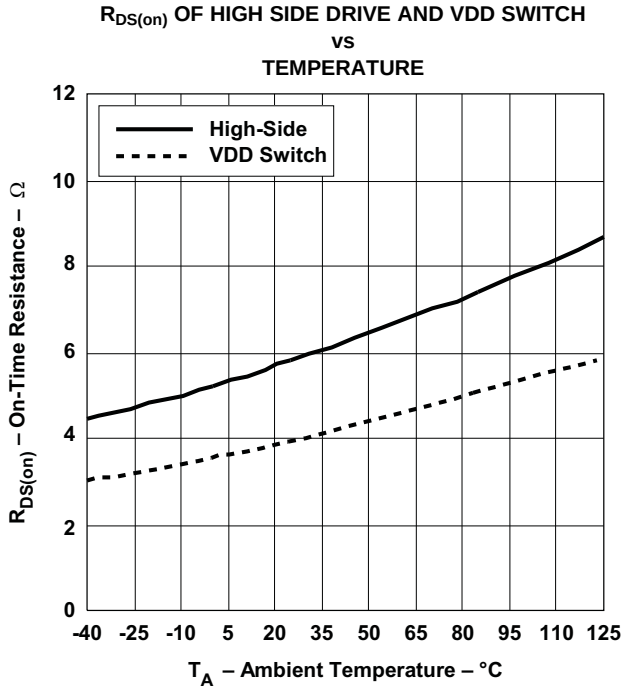


Figure 14.

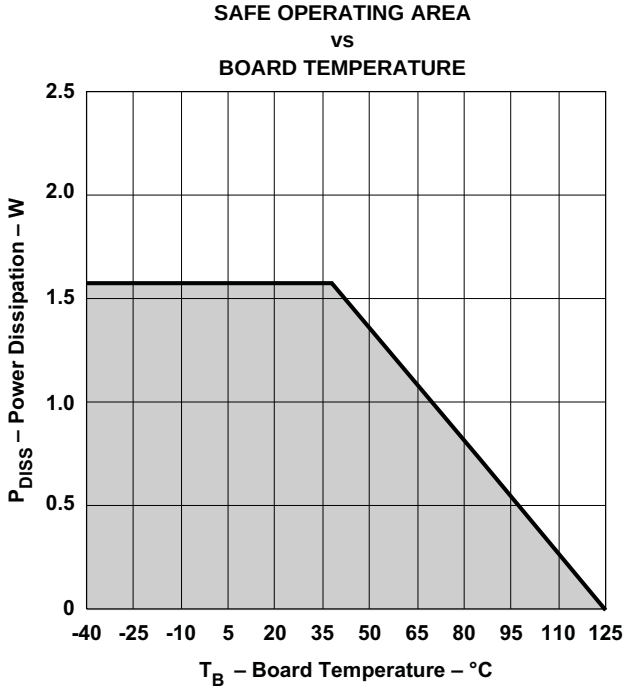


Figure 15.

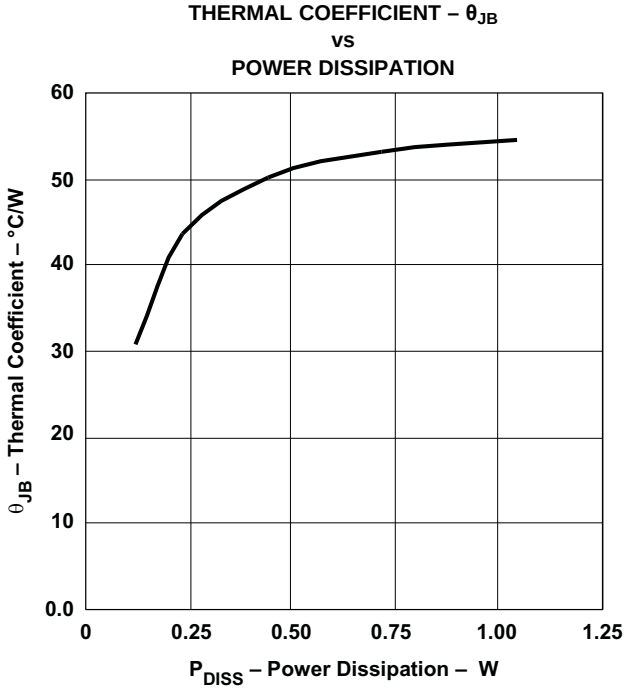


Figure 16.

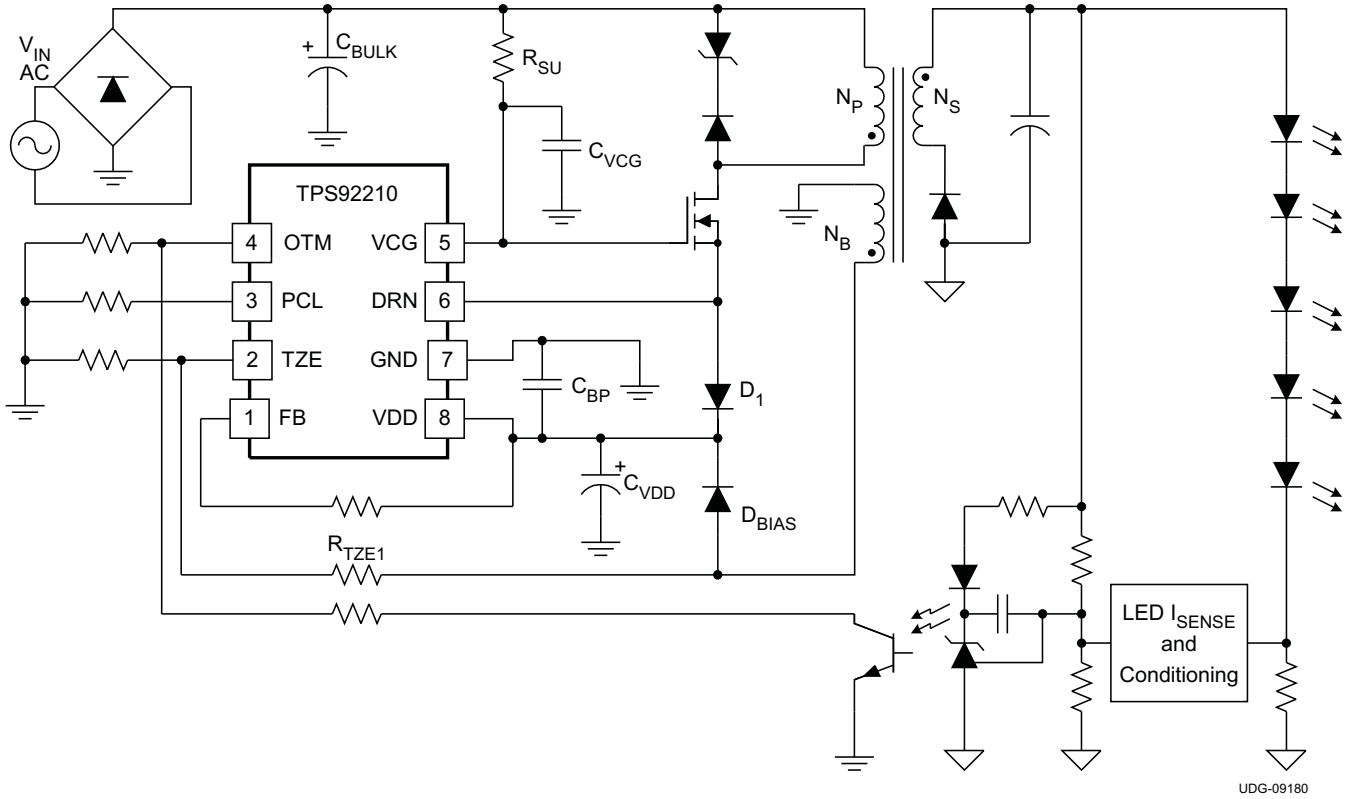


Figure 17. Typical Application

DETAILED DESCRIPTION

BIAS AND START-UP

The TPS92210 controls the turn-ON and turn-OFF of the flyback switch through its source by using the cascode configuration. The cascode configuration is also used to provide the initial bias during start-up. The cascode architecture utilizes a low voltage switch whose drain, namely the DRN pin, is connected to the source of the high voltage MOSFET (HV MOSFET). The gate of the HV MOSFET is held at a constant DC voltage using the VCG pin. The TPS92210 cascode based HVMOSFET drive architecture is shown in Figure 18.

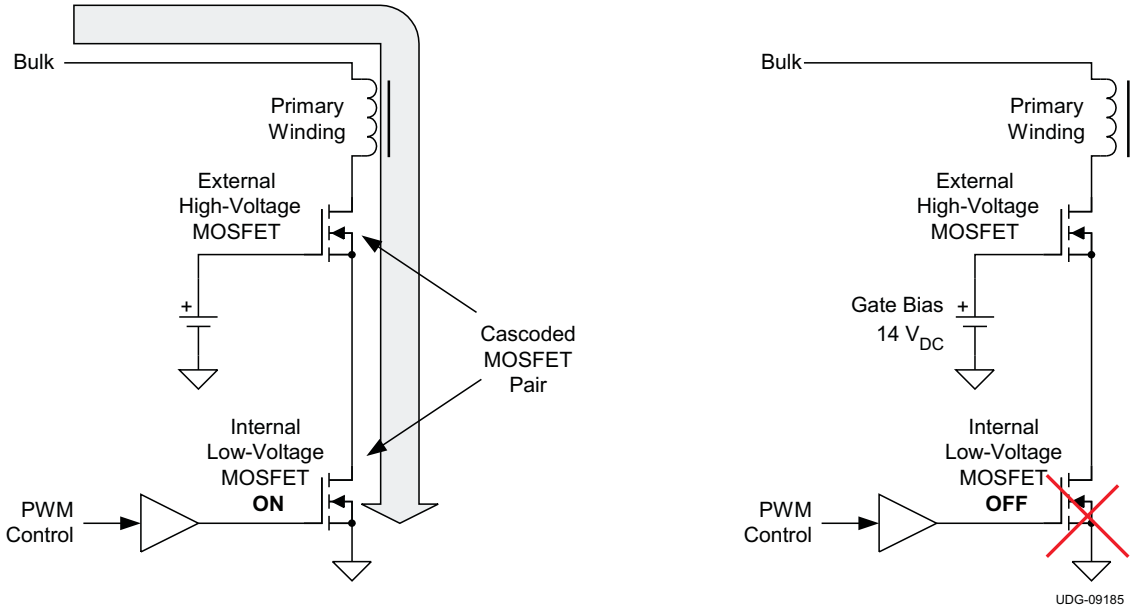


Figure 18. Cascoded Architecture

The start-up bias uses a low-level bleed current from either the AC line or the rectified and filtered AC line through the startup resistor (R_{SU}). The bleed current off the line (approximately 6 µA) charges a small VCG capacitor and raises the voltage at the HVMOSFET gate. The HVMOSFET acts as a source follower once the voltage at VCG pin reaches the threshold voltage of the HVMOSFET and raises the DRN pin voltage. During startup the TPS92210 is in undervoltage lockout (UVLO) state with the enable pulse-width modulation (PWM) signal low. This turns on the VDD switch connecting between the DRN pin and the VDD pin, thus allowing V_{VDD} to also rise with V_{VCG} minus a threshold voltage of HVMOSFET. An external schottky diode between DRN and VDD is used to steer away potentially high switching currents from flowing through the body diode of the internal VDD switch. The startup current and the operating current paths in the cascode architecture are shown in Figure 19. The VCG pin is shunt regulated at 14 V during normal operation and the regulation level is increased to 16 V during fault, UVLO and startup conditions.

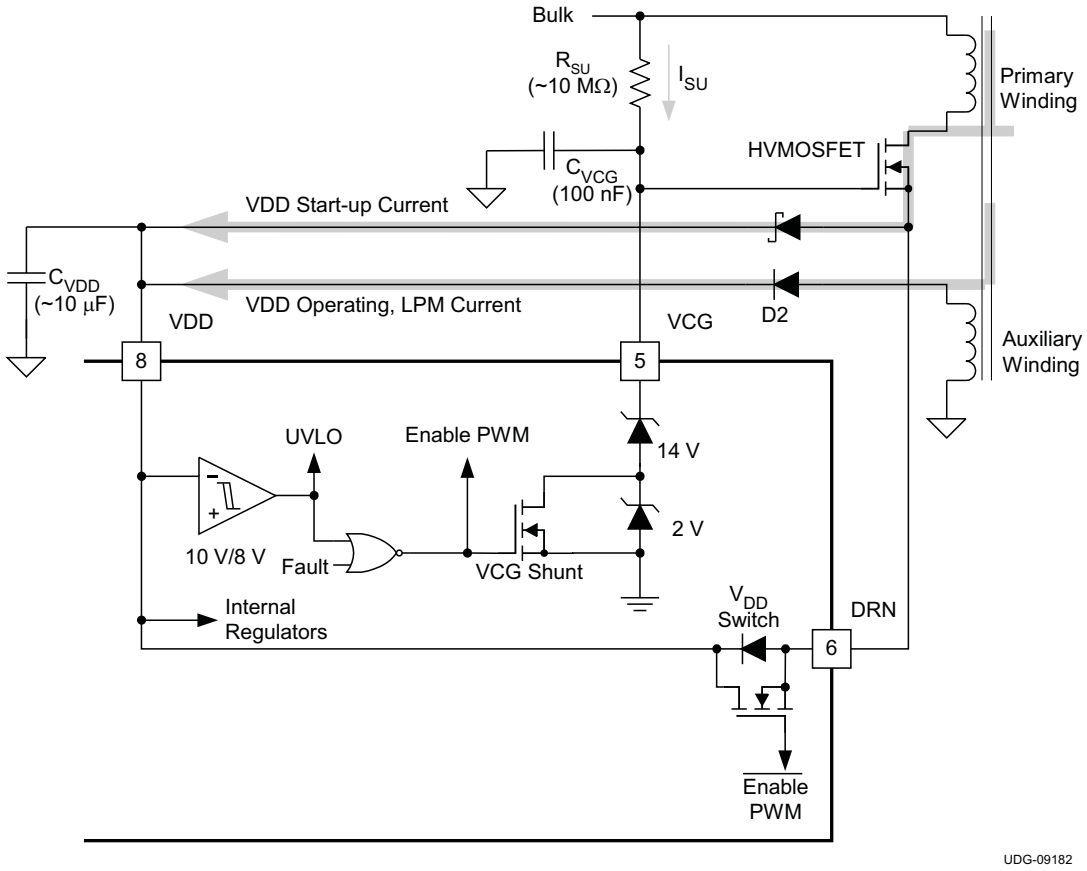


Figure 19. Start-Up and Operating Current in the Cascode Architecture for TPS92210

PRIMARY SIDE CURRENT SENSE

The TPS92210 integrates all of the current sensing and drive, thereby eliminating the need for a current sense resistor. The internal low-voltage switch with typical $R_{DS(on)}$ of 90 mΩ drives the HVMOSFET through its source and the entire primary current of the transformer flows through this switch and out of the GND pin. The TPS92210 utilizes a current mirror technique to sense and control the primary current. The primary current flowing through the low-voltage switch is scaled and reflected to the PWM comparator where it is compared with the PCL pin current. Thus the peak current reached at each switching cycle is sensed and limited by this comparison.

In peak current-mode control, based on the error signal input at the FB pin, the voltage at the PCL pin and hence the PCL pin current is modulated by TPS92210. The maximum peak primary current is programmed by connecting a low-power resistor from (R_{PCL}) from PCL pin to the quiet return of GND.

$$I_{DRN(pk)} = \left(\frac{100\,kV}{R_{PCL}} \right) \quad (1)$$

At the beginning of each switching cycle a blanking time of approximately 220 ns is applied to the internal current limiter. This allows the low-voltage switch to turn on without false limiting on the leading edge capacitive discharge currents. The drain-gate charge in the HVMOSFET does not affect the turn-off speed because the gate is connected to a low impedance DC source with the help of VCG pin. The cascode configuration enables very fast turn-off of the HVMOSFET and helps to keep switching losses low. Figure 20 illustrates the internal current sensing and control exhibited by programming the resistor at the PCL pin.

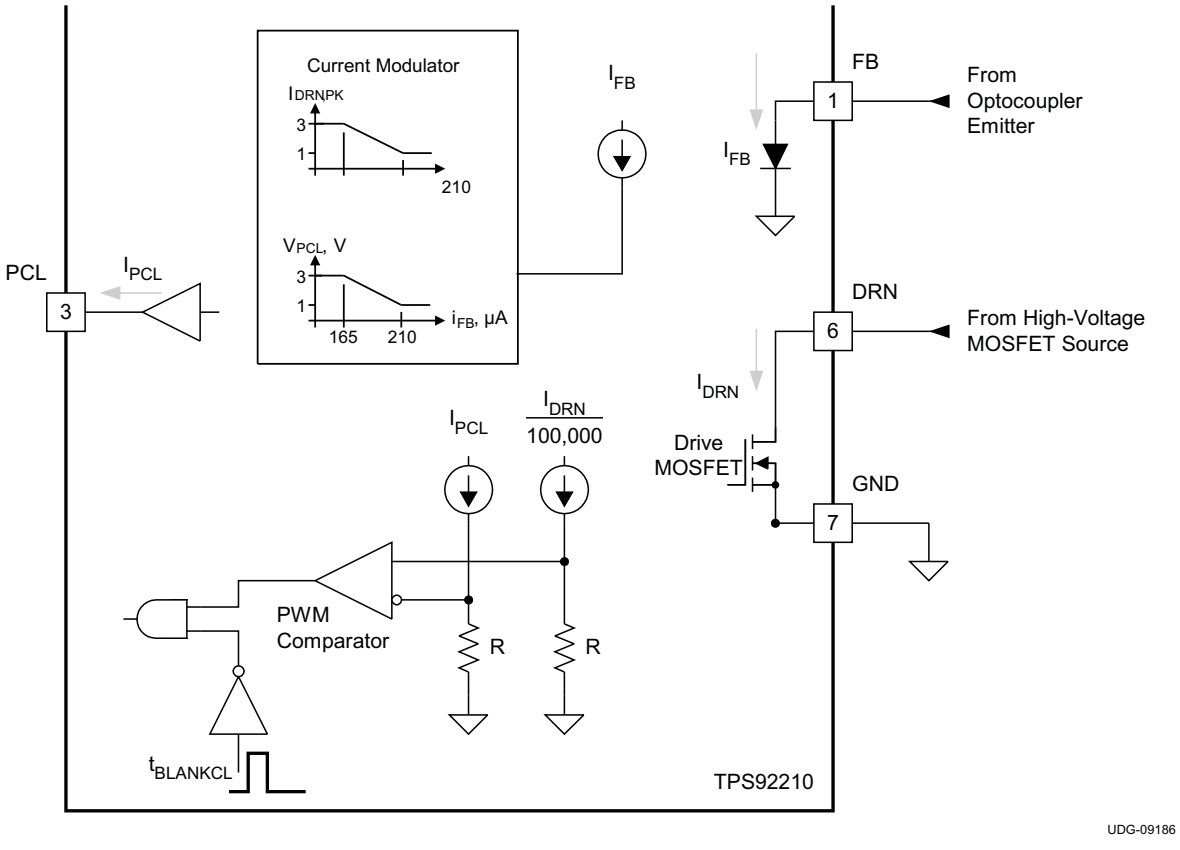


Figure 20. Peak Current Limit (PCL) Pin Details

FEEDBACK AND MODULATION

The TPS92210 can be programmed to operate in constant-on time control or in peak-current mode control based on how the error signal is fed back to its modulator.

Constant-On Time Control Using the OTM Pin

The *power factor* describes how well an AC load corresponds to a pure resistance. A flyback transformer operating in discontinuous conduction mode (DCM) creates a peak primary current described in Equation 2

$$I_{PEAK} = \left(\frac{V_{BULK} \times t_{ON}}{L_M} \right) = \left(\frac{V_{BULK}}{\left(\frac{L_M}{t_{ON}} \right)} \right) \quad (2)$$

where

- L_M is the magnetizing inductance of the flyback transformer
- t_{ON} is the on-time of the flyback switch
- (L_M/t_{ON}) is expressed in units of (µH/s)

thus,

$$I_{PEAK} = \frac{V_{BULK}}{\left(\frac{L_M}{t_{ON}} \right)} \left(V / \Omega \right) \quad (3)$$

If the on-time is limited to a fixed value, then the peak primary current in the transformer is directly proportional to the bulk supply voltage. Consequently, a flyback operating in DCM with a fixed inductance and fixed on-time behaves much like a pure resistance and exhibits a power factor close to unity when operating with a small bulk capacitance. The TPS92210 can easily be configured for constant on-time control, allowing fixed-frequency, single-stage power factor regulation.

In constant-on time control, the on-time of the primary switch can be programmed by connecting a resistor (R_{OTM}) between the OTM pin and the quiet return of GND. The on-time can be further modulated by connecting the collector of the opto-coupler to the OTM pin through a resistor as shown in Figure 21.

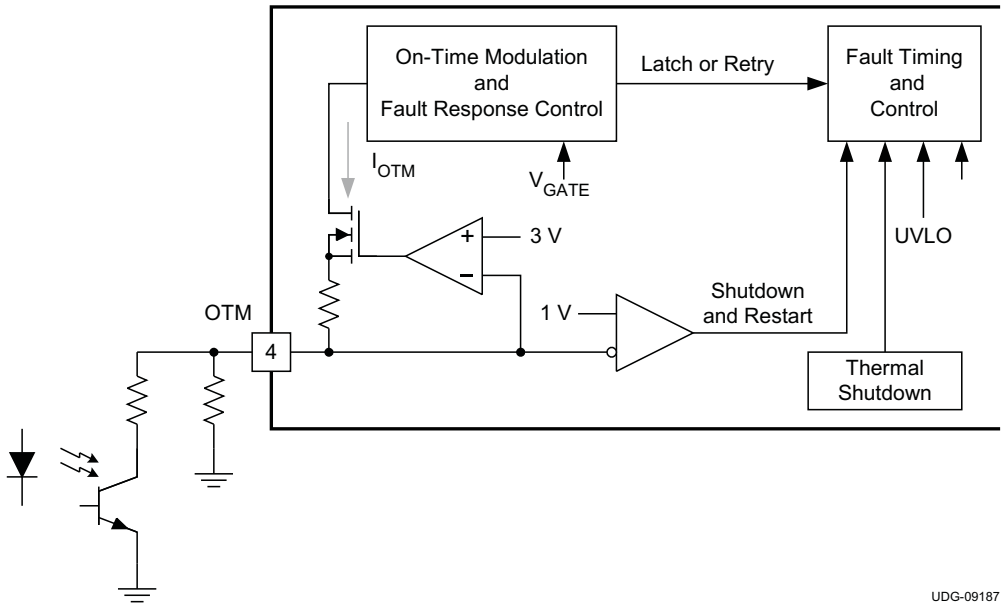


Figure 21. On-Time Modulation Detail

The OTM multi-function pin is also used to program the system response to overload and brownout conditions. Figure 22 shows how the on-time is programmed over the range of between 1.5 µs and 5 µs for either range of programming resistors. The resistor range determines the controller response to a sustained overload fault (to either latch-off or to shutdown/retry) which is the same response for a line-sag, or brown out, condition. The on-time is related to the programmed resistor based on the following equations.

The on-time for latch-off response to overcurrent faults is show in Equation 4.

$$R_{OTM} = t_{OTM} \times \left(1 \times 10^{11} \frac{\Omega}{s}\right) \quad (4)$$

The on-time for the shutdown/retry response to overcurrent faults is shown in Equation 5.

$$R_{OTM} = t_{OTM} \times \left(2 \times 10^{10} \frac{\Omega}{s}\right) \quad (5)$$

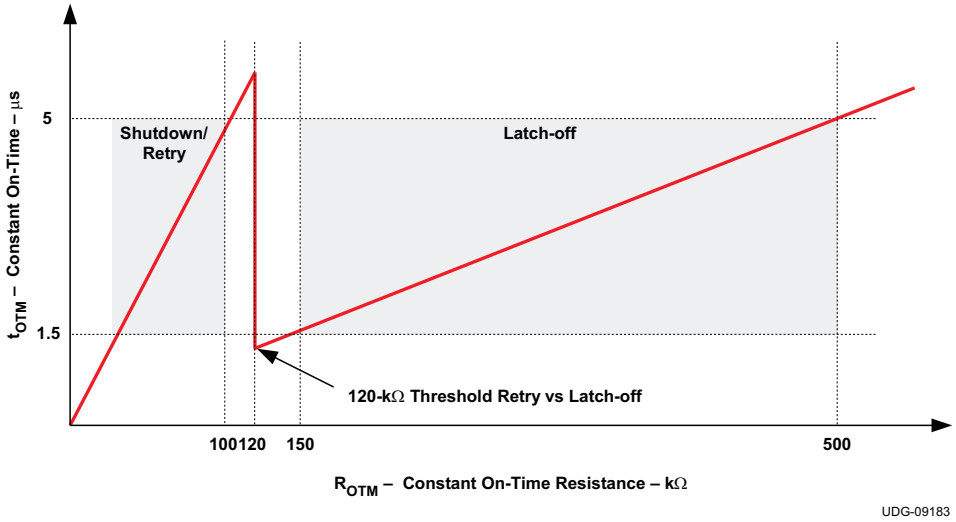


Figure 22. On-time Programming Range and Overload Fault Response Selection

The OTM pin can also be used to externally shutdown the converter by pulling the OTM pin low below $V_{OTM(SR)}$ threshold (typically 1 V). The PWM action is disabled and the controller retries after the shutdown/retry delay of 750 ms.

Peak-Current Mode Control Using the FB Pin

In peak-current mode control, the FB pin is used to feed back the output error signal to the internal modulator. In this mode of control, the emitter of the opto-coupler is connected to the FB pin and a resistor (R_{FB}) is connected from FB to the quiet return of GND to bleed off the dark current of the opto-coupler. The FB pin detects current input only, and the voltage at this pin is normally 0.7 V. The FB pin interface is outlined in Figure 23.

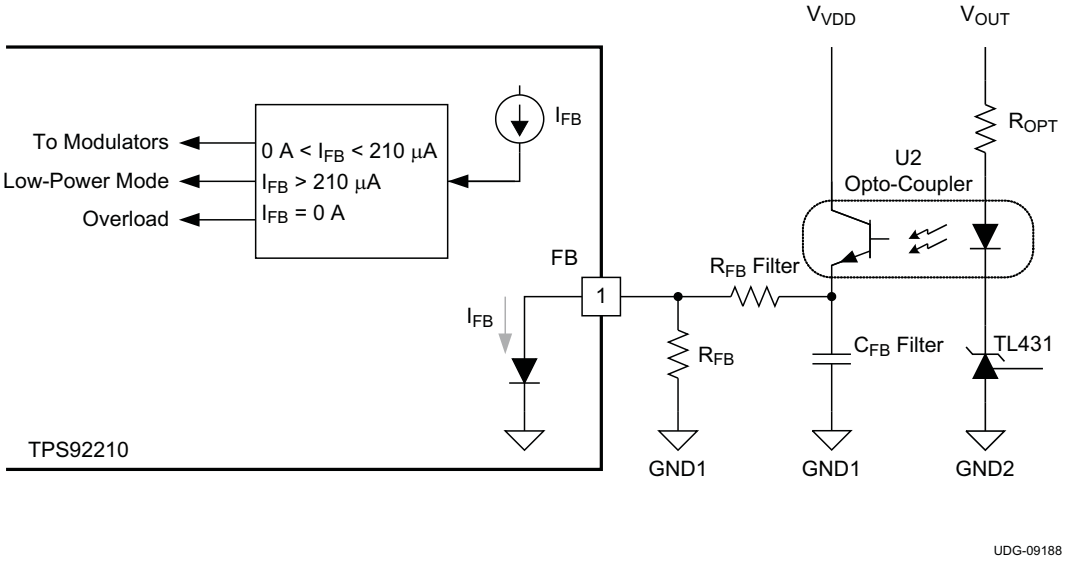


Figure 23. FB Pin Details for Peak-Current Mode Control

The FB current (I_{FB}) commands the TPS92210 to operate the flyback converter in one of the three modes

- Frequency Modulation (FM) mode
- Amplitude Modulation (AM) mode
- Low power mode (LPM)

The converter operates in FM mode with a large power load (23% to 100% the peak regulated power). The peak HVMOSFET current reaches its maximum programmed value and FB current regulates the output voltage by modulating the switching frequency, which is inversely proportional to t_{SW}. The switching frequency range is nominally from 30 kHz (23% peak power) to 133 kHz (100% peak power).

The maximum programmable HVMOSFET current, $I_{DRN,PK(max)}$, is set by the resistor on the PCL pin, as described in Equation 1. The converter operates in AM mode at moderate power levels (2.5% to 23% of the peak regulated power). The FB current regulates the output voltage by modulating the peak HVMOSFET current from 33% to 100% of the maximum programmed value while the switching frequency is fixed at approximately 30 kHz. The TPS92210 modulates the voltage on the PCL pin from 3 V to 1 V to vary the commanded peak current, as shown in Figure 24.

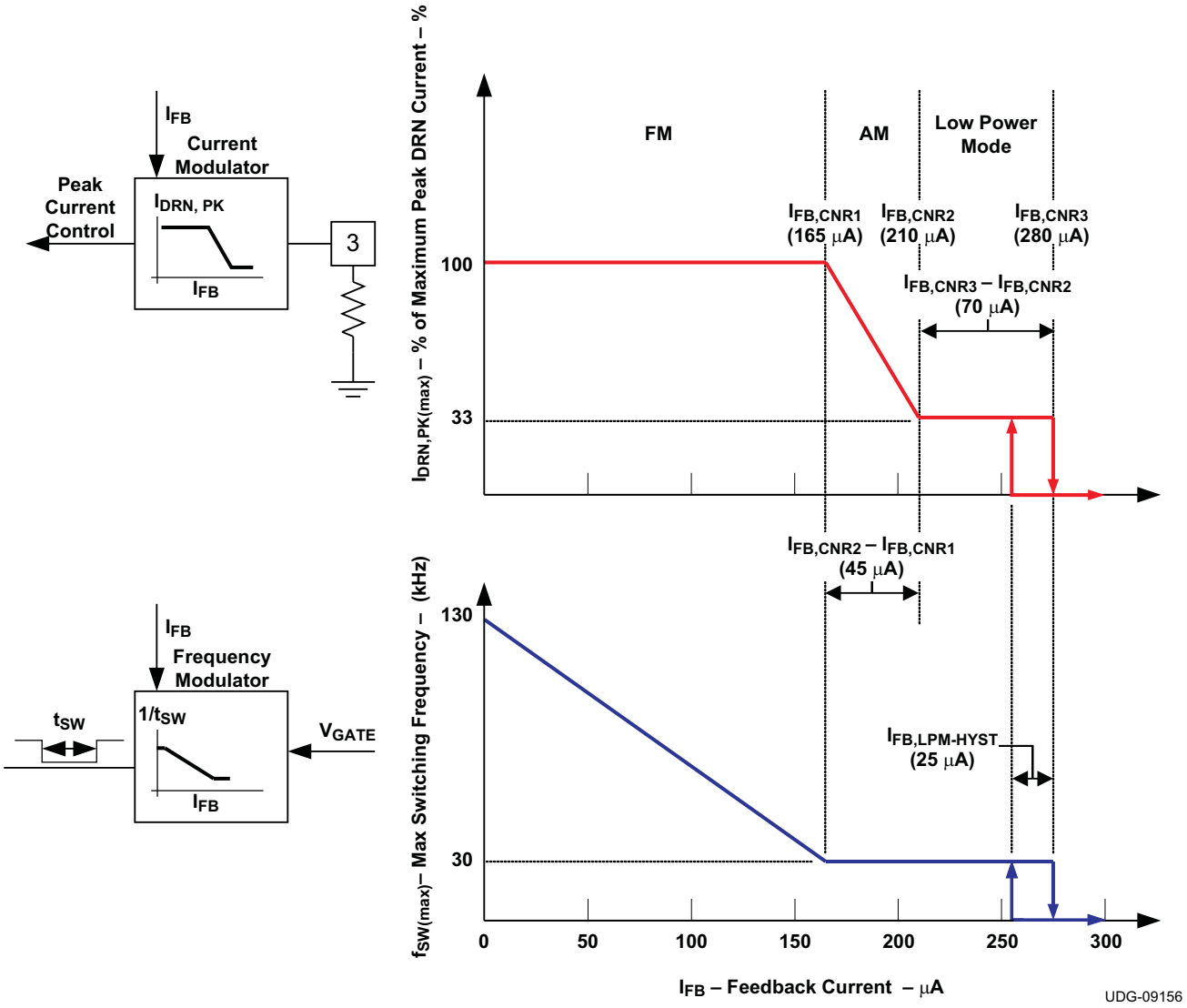


Figure 24. FB Pin Based Modulation Modes

The converter operates in LPM at light load (0% to 2.5% of the peak regulated power). The FB current regulates the output voltage in the Low Power Mode with hysteretic bursts of pulses using FB current thresholds. The peak HVMOSFET current is 33% of the maximum programmed value. The switching frequency within a burst of pulses is approximately 30 kHz. The duration between bursts is regulated by the power supply control dynamics and the FB hysteresis. The TPS92210 reduces internal bias power between bursts in order to conserve energy during light-load and no-load conditions.

TRANSFORMER ZERO ENERGY DETECTION

The TPS92210 ensures that the flyback converter always operates in DCM and initiates a new switching cycle only when the primary transformer has been completely reset or when its energy is zero. The TZE pin is connected through a resistive divider to the primary-side auxiliary winding for zero energy detection. The transformer zero energy is detected by monitoring the current sourced out of the TZE pin when the primary bias winding of the flyback converter is negative with respect to GND. The voltage at this pin is clamped at –160 mV during the negative excursions of the auxiliary winding. A small delay, between 50 ns and 200 ns, can be added with C_{TZE} to align the turn-on of the primary switch with the resonant valley of the primary winding waveform enabling valley switching. Figure 25 shows the waveform on the HVMOSFET drain, the voltage at the TZE pin and the primary current in the transformer. It also illustrates how C_{TZE} delays the voltage at the TZE pin to cause the TPS92210 to switch at the resonant valley.

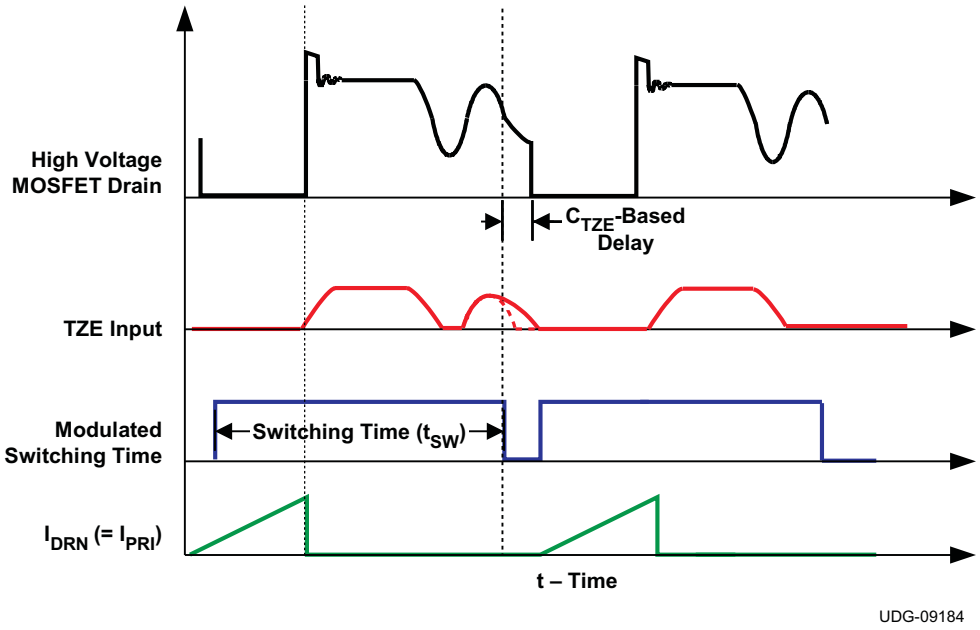


Figure 25. TZE and HVMOSFET Drain Voltages for Valley Switching

The TPS92210 requires that three conditions are satisfied before it can initiate a new switching cycle.

- The time since the last turn-on edge must be equal to or greater than the time that is requested by the feedback processor as determined by the feedback current, I_{FB}.
- The time since the last turn-on edge must be longer than the minimum period that is built into the device (nominally 7.5 µs which equals 133 kHz).
- Immediately following a high-to-low zero crossing of the TZE pin voltage. Or, it has been longer than $t_{WAIT,TZE}$ since the last zero crossing of the current has been detected

The TZE pin is also used to program the output overvoltage protection or open-LED detection feature. The output voltage is monitored by TPS92210 by sampling the voltage at the auxiliary winding. The voltage is sampled after a fixed delay of 1 µs after the internal low-voltage switch has turned off. This allows the auxiliary winding to be sampled after the bias winding voltage settles from the transient. The output over-voltage threshold is set using the turns ratio of the auxiliary winding to the output secondary and a resistive divider into the TZE pin. The controller latches-off on an open-LED fault and requires a power recycle to reset the fault latch (VDD recycling below fault reset threshold of 6 V). The interface to the TZE pin for zero energy detection and OVP feature is shown in Figure 26.

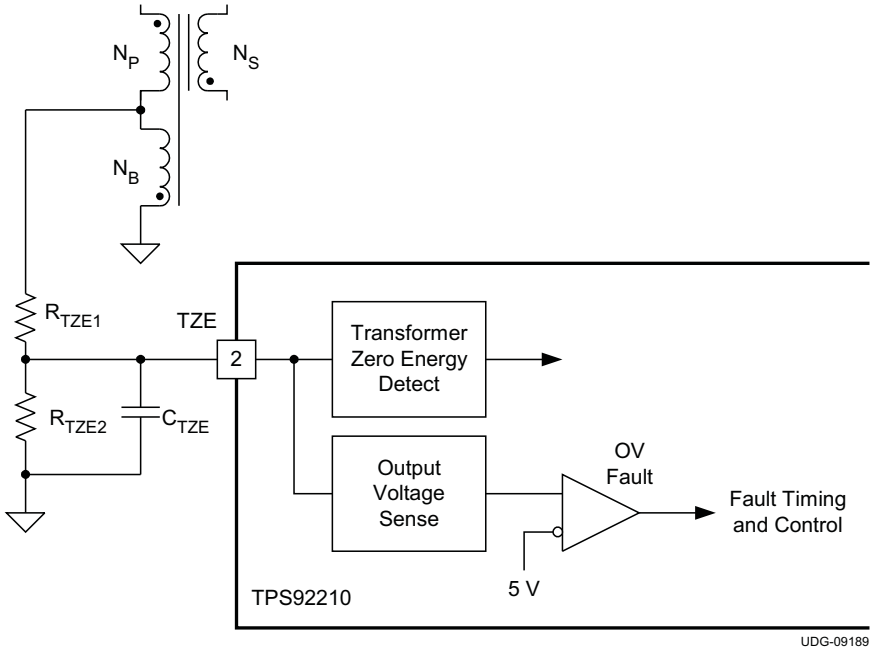


Figure 26. TZE and Output Overvoltage Detection

Terminal Components (1) (2)

NAME	TERMINAL	DESCRIPTION
PCL	3	$R_{PCL} = 33.2k\Omega \times \sqrt{\left(\frac{(K_P \times L_M)}{P_{IN}}\right)}$ $I_{DRN(pk)} = \left(\frac{100kV}{R_{PCL}}\right)$ where K_P = 0.54 W/µH L_M is the minimum value of primary inductance P_{IN} = POUT/η η = efficiency
DRN	6	M_1, power MOSFET with adequate voltage and current ratings, V_{GS} must have at least 20 V static rating. D1, Schottky diode, rated for at least 30 V, placed between DRN and VDD
FB	1	100 kΩ
GND	7	Bypass capacitor to VDD, C_{BP} = 0.1 µF, ceramic
OTM	4	For Latch-Off response to overcurrent faults: $R_{OTM} = t_{OTM} \times \left(1 \times 10^{11} \frac{\Omega}{s}\right)$ For shutdown/retry response to overcurrent faults: $R_{OTM} = t_{OTM} \times \left(2 \times 10^{10} \frac{\Omega}{s}\right)$
VDD	8	$C_{VDD} = \frac{I_{VDD(LPM)} \times t_{BURST}}{\Delta V_{DD(burst)}}$ where $\Delta VDD_{(BURST)}$ is the allowed VDD ripple during burst operation t_{BURST} is the estimated burst period The typical C_{VDD} value is approximately 48 µF. D_{BIAS} must have a voltage rating greater than: $V_{DBIAS} =\geq V_{OUT} \times \left(\frac{N_{PS}}{N_{PB}} + \frac{V_{BULK(max)}}{N_{PB}}\right)$ where V_{DBIAS} is the reverse voltage rating of diode D2 $V_{BULK(max)}$ is the maximum rectified voltage of C_{BULK} at the highest line voltage
VCG	5	C_{VCG} = at least 10xCGS of the HVMOSFET, usually C_{VCG} = 0.1 µF
TZE	2	$R_{TZE1} = \frac{(V_{OUT} + V_F)}{100\mu A} \times \frac{N_{PS}}{N_{PB}}$ $R_{TZE2} = \frac{TZE_{OVP} \times R_{TZE1}}{\left(V_{OUT(pk)} \times \frac{N_{PS}}{N_{PB}}\right) - TZE_{OVP}}$ where V_{OUT} is the average output voltage of the secondary V_F is the forward bias voltage of the secondary rectifier $V_{OUT(pk)}$ is the desired output overvoltage fault level

(1) Refer to the Electrical Characteristics Table for all constants and measured values, unless otherwise noted.
(2) Refer to Figure 17 for all component locations in the Terminal Components Table

REVISION HISTORY

Changes from Original (JANUARY 2010) to Revision A **Page**

- Changed Corrected Pin 2 name 1
- Changed Corrected Pin 2 name 12
- Changed location of Zener diode in Figure 19. 14

Changes from Revision A (DECEMBER 2010) to Revision B **Page**

- Added clarity to conditions in ELECTRICAL CHARACTERISTICS table 4
- Changed maximum PCL voltage specification from "1.05" to "1.1" in ELECTRICAL CHARACTERISTICS table 4
- Changed minimum I_{FM} range for low power mode(LPM) modulation from "50" to "45" in ELECTRICAL CHARACTERISTICS table 4
- Added clarity to conditions in ELECTRICAL CHARACTERISTICS table 5
- Changed minimum TZE low clamp voltage from "–200" to "–220" in ELECTRICAL CHARACTERISTICS table 5
- Added clarity to FUNCTIONAL BLOCK DIAGRAM 6
- Added clarity to "conditions" statement in TYPICAL CHARACTERISTICS 8
- Added clarity to Figure 23 18
- Added clarity to Figure 24 19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA01125DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92210	Samples
TPS92210D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92210	Samples
TPS92210DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92210	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

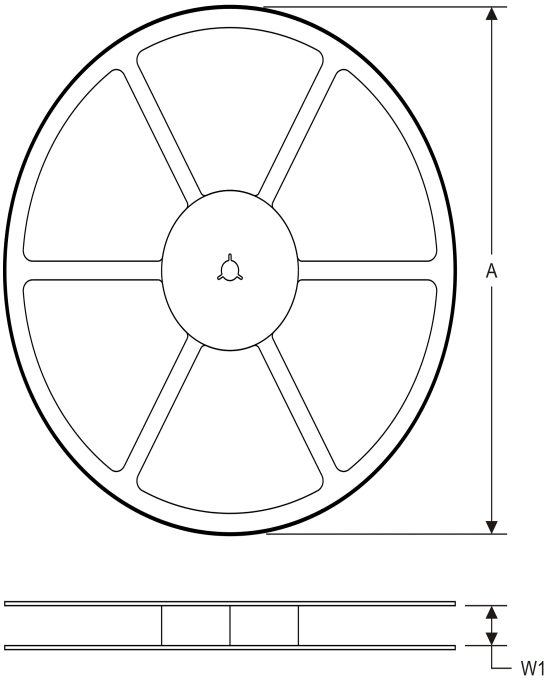
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

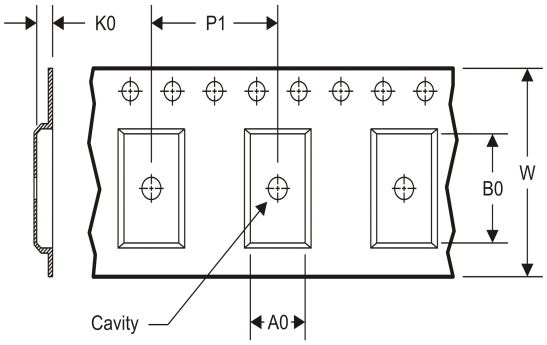
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



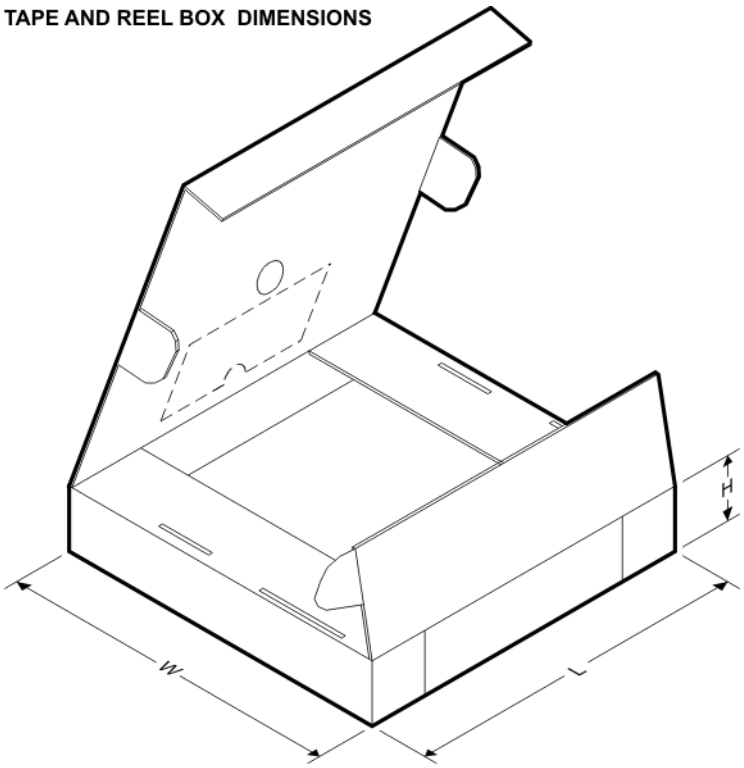
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

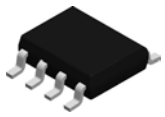
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92210DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92210DR	SOIC	D	8	2500	340.5	338.1	20.6

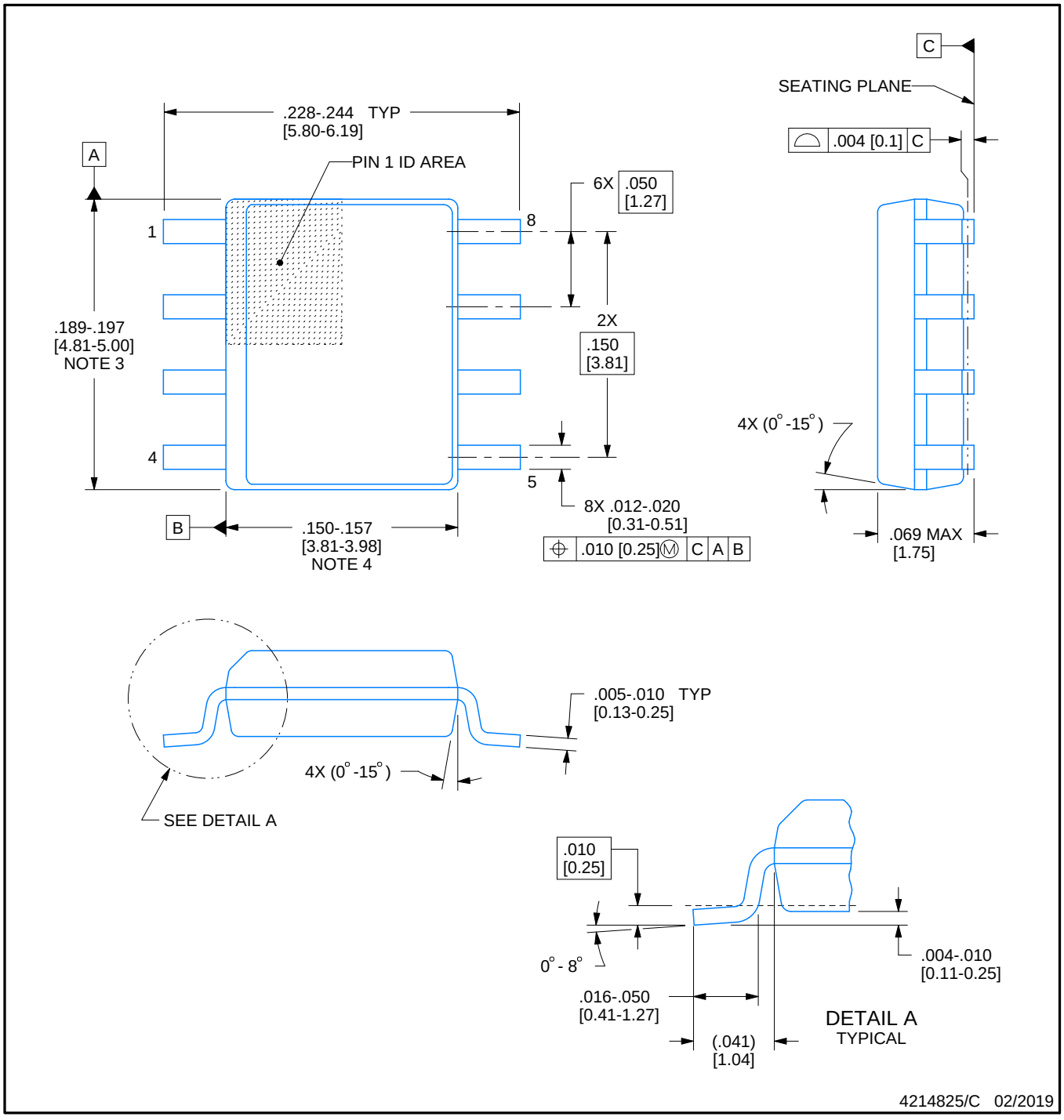


PACKAGE OUTLINE

D0008A

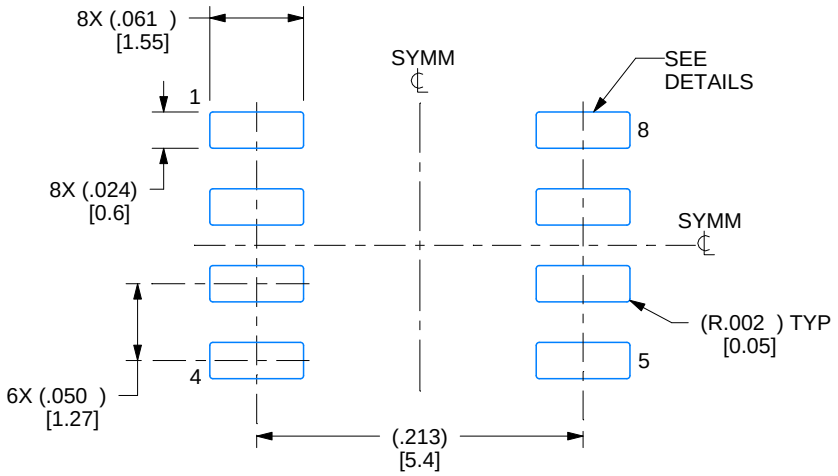
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

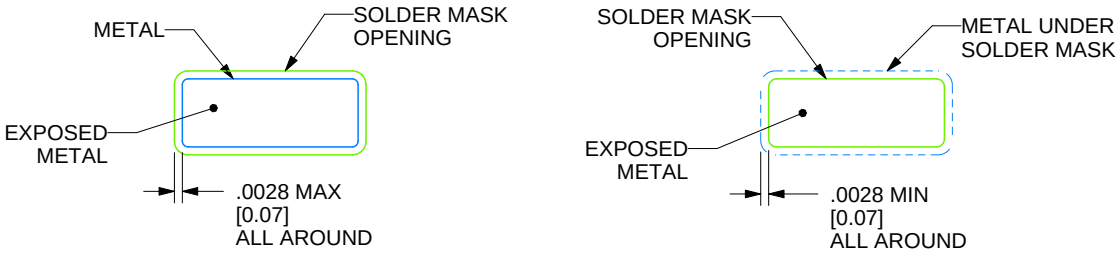


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

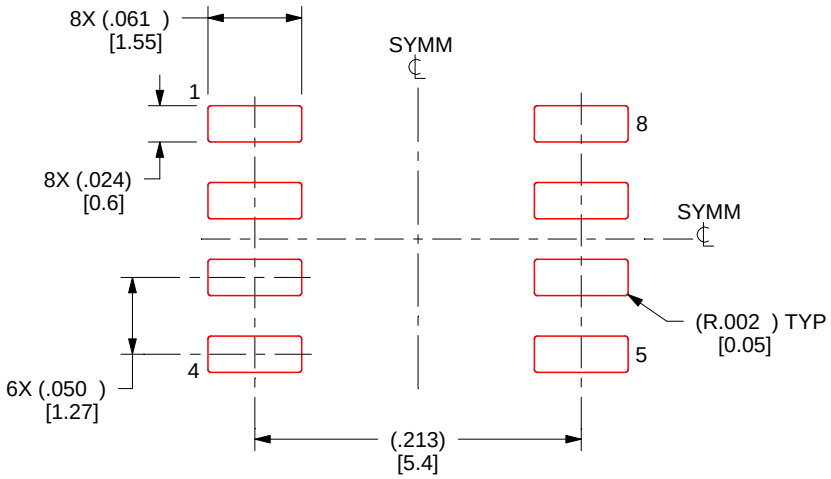
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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