

FS7140, FS7145

Programmable Phase-Locked Loop Clock Generator

Description

The FS7140 or FS7145 is a monolithic CMOS clock generator/regenerator IC designed to minimize cost and component count in a variety of electronic systems. Via the I²C-bus interface, the FS7140/45 can be adapted to many clock generation requirements.

The length of the reference and feedback dividers, their fine granularity and the flexibility of the post divider make the FS7140/45 the most flexible stand-alone PLL clock generator available.

Features

- Extremely Flexible and Low-jitter Phase Locked Loop (PLL) Frequency Synthesis
- No External Loop Filter Components Needed
- 150 MHz CMOS or 340 MHz PECL Outputs
- Completely Configurable via I²C-bus
- Up to Four FS714x can be Used on a Single I²C-bus
- 3.3 V Operation
- Independent On-chip Crystal Oscillator and External Reference Input
- Very Low “Cumulative” Jitter
- Pb-Free Packages are Available

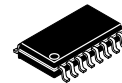
Applications

- Precision Frequency Synthesis
- Low-frequency Clock Multiplication
- Video Line-locked Clock Generation
- Laser Beam Printers (FS7145)

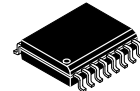


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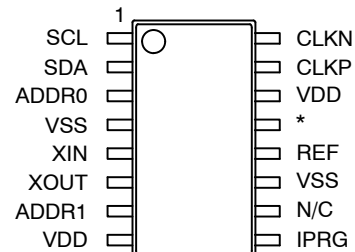


SOIC-16
01 SUFFIX
CASE 751BA



SSOP-16
02 SUFFIX
CASE 565AE

PIN CONNECTIONS



(Top View)

* FS7140 pin 13 = N/C
FS7145 pin 13 = SYNC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

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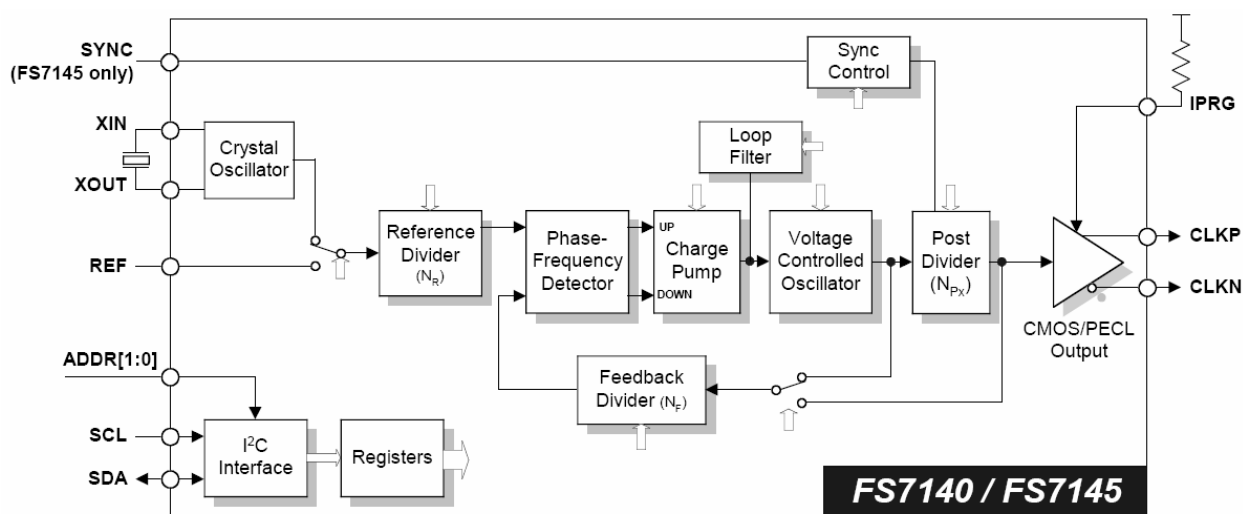


Figure 1. Device Block Diagram

Table 1. PIN DESCRIPTIONS*

| Pin | Type | Name | Description |
|-----|----------------------|-------------|---|
| 1 | DI | SCL | Serial interface clock (requires an external pull-up) |
| 2 | DIO | SDA | Serial interface data input/output (requires an external pull-up) |
| 3 | DI _D | ADDR0 | Address select bit "0" |
| 4 | P | VSS | Ground |
| 5 | AI | XIN | Crystal oscillator feedback |
| 6 | AO | XOUT | Crystal oscillator drive |
| 7 | DI _D | ADDR1 | Address select bit "1" |
| 8 | P | VDD | Power supply (+3.3 V nominal) |
| 9 | AI | IPRG | PECL current drive programming |
| 10 | - | n/c | No connection |
| 11 | P | VSS | Ground |
| 12 | DI ^U | REF | Reference frequency input |
| 13 | - DI ^U | n/c SYNC | FS7140 = No connection FS7145 = Synchronization input |
| 14 | P | VDD | Power supply (+3.3 V nominal) |
| 15 | DO | CLKP | Clock output |
| 16 | DO | CLKN | Inverted clock output |

*Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-up; DI_D = Input with Internal Pull-down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input; DO = Digital Output; P = Power/Ground; # = Active Low Pin

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ELECTRICAL SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Typ | Max | Units |
|----------|---|--------------------------|-----|----------------|-------|
| V_{DD} | Supply voltage, dc (V_{SS} = ground) | $V_{SS} - 0.5$ | | 4.5 | V |
| V_I | Input voltage, dc | $V_{SS} - 0.5$ | | $V_{DD} + 0.5$ | V |
| V_O | Output voltage, dc | $V_{SS} - 0.5$ | | $V_{DD} + 0.5$ | V |
| I_{IK} | Input clamp current, dc ($V_I < 0$ or $V_I > V_{DD}$) | -50 | | 50 | mA |
| I_{OK} | Output clamp current, dc ($V_I < 0$ or $V_I > V_{DD}$) | -50 | | 50 | mA |
| T_S | Storage temperature range (non-condensing) | -65 | | 150 | °C |
| T_A | Ambient temperature range, under bias | -55 | | 125 | °C |
| T_J | Junction temperature | | | 150 | °C |
| | Re-flow solder profile | Per IPC/JEDEC J-STD-020B | | | |
| | Input static discharge voltage protection (MIL-STD 883E, Method 3015.7) | | | 2 | kV |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

WARNING: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 3. OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Units |
|----------|-------------------------------------|-----|-----|-----|-------|
| V_{DD} | Supply voltage | 3.0 | 3.3 | 3.6 | V |
| T_A | Ambient operating temperature range | 0 | | 70 | °C |

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Table 4. DC ELECTRICAL SPECIFICATIONS (Note 1)

| Parameter | Symbol | Conditions/Description | Min | Typ | Max | Units |
|--|---------------|--|--------------------|---------------------|--------------------|---------------|
| OVERALL | | | | | | |
| Supply current, dynamic | I_{DD} | CMOS mode; $F_{XTAL} = 15 \text{ MHz}$; $F_{VCO} = 400 \text{ MHz}$; $F_{CLK} = 200 \text{ MHz}$; does not include load current | | 35 | | mA |
| Supply current, static | I_{DDL} | SHUT1, SHUT2 bit both "1" | | 400 | 700 | μA |
| SERIAL COMMUNICATION I/O (SDA, SCL) | | | | | | |
| High-level input voltage | V_{IH} | | $0.8 \cdot V_{DD}$ | | | V |
| Low-level input voltage | V_{IL} | | | | $0.2 \cdot V_{DD}$ | V |
| Hysteresis voltage | V_{hys} | | | $0.33 \cdot V_{DD}$ | | V |
| Input leakage current | I_I | SDA, SCL in read condition | -10 | | +10 | μA |
| Low-level output sink current (SDA) | I_{OL} | SDA in acknowledge condition; $V_{SDA} = 0.4 \text{ V}$ | 5 | 14 | | mA |
| ADDRESS SELECT INPUT (ADDR0, ADDR1) | | | | | | |
| High-level input voltage | V_{IH} | | $V_{DD}-1.0$ | | | V |
| Low-level input voltage | V_{IL} | | | | 0.8 | V |
| High-level input current (pull-down) | I_{IH} | $V_{ADDRx} = V_{DD}$ | | 30 | | μA |
| Low-level input current | I_{IL} | $V_{ADDRx} = 0 \text{ V}$ | -1 | | 1 | μA |
| REFERENCE FREQUENCY INPUT (REF) | | | | | | |
| High-level input voltage | V_{IH} | | $V_{DD}-1.0$ | | | V |
| Low-level input voltage | V_{IL} | | | | 0.8 | V |
| High-level input current | I_{IH} | $V_{REF} = V_{DD}$ | -1 | | 1 | μA |
| Low-level input current (pull-down) | I_{IL} | $V_{REF} = 0 \text{ V}$ | | -30 | | μA |
| SYNC CONTROL INPUT (SYNC) | | | | | | |
| High-level input voltage | V_{IH} | | $V_{DD}-1.0$ | | | V |
| Low-level input voltage | V_{IL} | | | | 0.8 | V |
| High-level input current | I_{IH} | $V_{REF} = V_{DD}$ | -1 | | 1 | μA |
| Low-level input current (pull-down) | I_{IL} | $V_{REF} = 0 \text{ V}$ | | -30 | | μA |
| CRYSTAL OSCILLATOR INPUT (XIN) | | | | | | |
| Threshold bias voltage | V_{TH} | | | $V_{DD}/2$ | | V |
| High-level input current | I_{IH} | $V_{XIN} = V_{DD}$ | | 40 | | μA |
| Low-level input current | I_{IL} | $V_{XIN} = \text{GND}$ | | -40 | | μA |
| Crystal frequency | F_X | Fundamental mode | | | 35 | MHz |
| Recommended crystal load capacitance* | $C_{L(XTAL)}$ | For best matching with internal crystal oscillator load | | 16-18 | | pF |
| CRYSTAL OSCILLATOR OUTPUT (XOUT) | | | | | | |
| High-level output source current | I_{OH} | $V_{XOUT} = 0$ | | -8.5 | | mA |
| Low-level output sink current | I_{OL} | $V_{XOUT} = V_{DD}$ | | 11 | | mA |
| PECL CURRENT PROGRAM I/O (IPRG) | | | | | | |
| Low-level input current | I_{IL} | $V_{IPRG} = 0 \text{ V}$; PECL mode | -10 | | 10 | μA |
| CLOCK OUTPUTS, CMOS MODE (CLKN, CLKP) | | | | | | |
| High-level output source current | I_{OH} | $V_O = 2.0 \text{ V}$ | | 19 | | mA |

1. Unless otherwise stated, $V_{DD} = 3.3 \text{ V} \pm 10\%$, no load on any output, and ambient temperature range $T_A = 0^\circ\text{C}$ to 70°C . Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical. Negative currents indicate flows out of the device.

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Table 4. DC ELECTRICAL SPECIFICATIONS (Note 1)

| Parameter | Symbol | Conditions/Description | Min | Typ | Max | Units |
|--|------------|--|-----|------------|-----|---------------|
| CLOCK OUTPUTS, CMOS MODE (CLKN, CLKP) | | | | | | |
| Low-level output sink current | I_{OL} | $V_O = 0.4\text{ V}$ | | -35 | | mA |
| CLOCK OUTPUTS, PECL MODE (CLKN, CLKP) | | | | | | |
| IPRG bias voltage | V_{IPRG} | V_{IPRG} will be clamped to this level when a resistor is connected from VDD to IPRG | | $V_{DD}/3$ | | V |
| IPRG bias current | I_{IPRG} | $I_{IPRG} - (V_{VDD} - V_{IPRG}) / R_{SET}$ | | | 3.5 | mA |
| Sink current to IPRG current ratio | | | | 13 | | |
| Tristate output current | I_Z | | -10 | | 10 | μA |

1. Unless otherwise stated, $V_{DD} = 3.3\text{ V} \pm 10\%$, no load on any output, and ambient temperature range $T_A = 0^\circ\text{C}$ to 70°C . Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical. Negative currents indicate flows out of the device.

Table 5. AC TIMING SPECIFICATIONS (Note 2)

| Parameter | Symbol | Conditions/Description | Min | Typ | Max | Units |
|---|-------------------|---|-----|-----|-----|-----------|
| OVERALL | | | | | | |
| Output frequency* | $f_{o(max)}$ | CMOS outputs | 0 | | 150 | MHz |
| | | PECL outputs | 0 | | 300 | |
| VCO frequency* | f_{VCO} | | 40 | | 400 | MHz |
| CMOS mode rise time* | t_r | $C_L = 7\text{ pF}$ | | 1 | | ns |
| CMOS mode fall time* | t_f | $C_L = 7\text{ pF}$ | | 1 | | ns |
| PECL mode rise time* | t_r | $C_L = 7\text{ pF}; R_L = 65\text{ ohm}$ | | 1 | | ns |
| PECL mode fall time* | t_f | $C_L = 7\text{ pF}; R_L = 65\text{ ohm}$ | | 1 | | ns |
| REFERENCE FREQUENCY INPUT (REF) | | | | | | |
| Input frequency | F_{REF} | | | | 80 | MHz |
| Reference high time | t_{REHF} | | 3 | | | ns |
| Reference low time | t_{REFL} | | 3 | | | ns |
| SYNC CONTROL INPUT (SYNC) | | | | | | |
| Sync high time | t_{SYNCH} | For orderly CLK stop/start | 3 | | | T_{CLK} |
| Sync low time | t_{SYNCL} | For orderly CLK stop/start | 3 | | | |
| CLOCK OUTPUT (CLKN, CLKP) | | | | | | |
| Duty cycle (CMOS mode)* | | Measured at 1.4 V | | 50 | | % |
| Duty cycle (PECL mode)* | | Measured at zero crossings of ($V_{CLKP} - V_{CLKN}$) | | 50 | | % |
| Jitter, long term ($\sigma_y(\tau)$)* | $t_{j(LT)}$ | For valid programming solutions. Long-term (or cumulative) jitter specified is RMS position error of any edge compared with an ideal clock generated from the same reference frequency. It is measured with a time interval analyzer using a 500 microsecond window, using statistics gathered over 1000 samples. | | | | ps |
| | | $F_{REF}/N_{REF} > 1000\text{ kHz}$ | | 25 | | ps |
| | | $F_{REF}/N_{REF} \cong 500\text{ kHz}$ | | 50 | | ps |
| | | $F_{REF}/N_{REF} \cong 250\text{ kHz}$ | | 100 | | ps |
| | | $F_{REF}/N_{REF} \cong 125\text{ kHz}$ | | 190 | | ps |
| | | $F_{REF}/N_{REF} \cong 62.5\text{ kHz}$ | | 240 | | ps |
| | | $F_{REF}/N_{REF} \cong 31.5\text{ kHz}$ | | 300 | | ps |
| Jitter, period (peak-peak)* | $t_{j(\Delta P)}$ | $40\text{ MHz} < \text{VCO frequency} < 100\text{ MHz}$ | | 75 | | ps |
| | | VCO frequency $> 100\text{ MHz}$ | | 50 | | ps |

2. Unless otherwise stated, $V_{DD} = 3.3\text{ V} \pm 10\%$, no load on any output, and ambient temperature range $T_A = 0^\circ\text{C}$ to 70°C . Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical.

Table 6. SERIAL INTERFACE TIMING SPECIFICATIONS (Note 3)

| Parameter | Symbol | Conditions/Description | Fast Mode | | Units |
|--------------------------------------|--------------|------------------------|-----------|-----|-------|
| | | | Min | Max | |
| Clock frequency | f_{SCL} | SCL | 0 | 400 | kHz |
| Bus free time between STOP and START | t_{BUF} | | 1300 | | ns |
| Set-up time, START (repeated) | $T_{su:STA}$ | | 600 | | ns |
| Hold time, START | $t_{hd:STA}$ | | 600 | | ns |
| Set-up time, data input | $T_{su:DAT}$ | SDA | 100 | | ns |
| Hold time, data input | $t_{hd:DAT}$ | SDA | 0 | | ns |
| Output data valid from clock | t_{AA} | | | 900 | ns |
| Rise time, data and clock | t_R | SDA, SCL | | 300 | ns |
| Fall time, data and clock | t_F | SDA, SCL | | 300 | ns |
| High time, clock | t_{HI} | SCL | 600 | | ns |
| Low time, clock | t_{LO} | SCL | 1300 | | ns |
| Set-up time, STOP | $t_{su:STO}$ | | 600 | | ns |

3. Unless otherwise stated, $V_{DD} = 3.3 V \pm 10\%$, no load on any output, and ambient temperature range $T_A = 0^\circ C$ to $70^\circ C$. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical.

FUNCTIONAL BLOCK DIAGRAM

Phase Locked Loop (PLL)

The PLL is a standard phase- and frequency-locked loop architecture. The PLL consists of a reference divider, a phase-frequency detector (PFD), a charge pump, an internal loop filter, a voltage-controlled oscillator (VCO), a feedback divider, and a post divider.

The reference frequency (generated by either the on-board crystal oscillator or an external frequency source), is first reduced by the reference divider. The integer value that the frequency is divided by is called the modulus and is denoted as NR for the reference divider. This divided reference is then fed into the PFD.

The VCO frequency is fed back to the PFD through the feedback divider (the modulus is denoted by NF).

The PFD will drive the VCO up or down in frequency until the divided reference frequency and the divided VCO frequency appearing at the inputs of the PFD are equal. The input/output relationship between the reference frequency and the VCO frequency is then:

$$\frac{f_{VCO}}{N_F} = \frac{f_{REF}}{N_R}$$

This basic PLL equation can be rewritten as

$$f_{VCO} = f_{REF} \left(\frac{N_F}{N_R} \right)$$

A post divider (actually a series combination of three post dividers) follows the PLL and the final equation for device output frequency is:

$$f_{CLK} = f_{REF} \left(\frac{N_F}{N_R} \right) \left(\frac{1}{N_{Px}} \right)$$

Reference Divider

The reference divider is designed for low phase jitter. The divider accepts the output of either the crystal oscillator circuit or an external reference frequency. The reference divider is a 12 bit divider, and can be programmed for any modulus from 1 to 4095 (divide by 1 not available on date codes prior to 0108).

Feedback Divider

The feedback divider is based on a dual-modulus divider (also called dual-modulus prescaler) technique. It permits division by any integer value between 12 and 16383. Simply program the FBKDIV register with the binary equivalent of the desired modulus. Selected moduli below 12 are also permitted. Moduli of: 4, 5, 8, 9, and 10 are also allowed (4 and 5 are not available on date codes prior to 0108).

Post Divider

The post divider consists of three individually programmable dividers, as shown in Figure 2.

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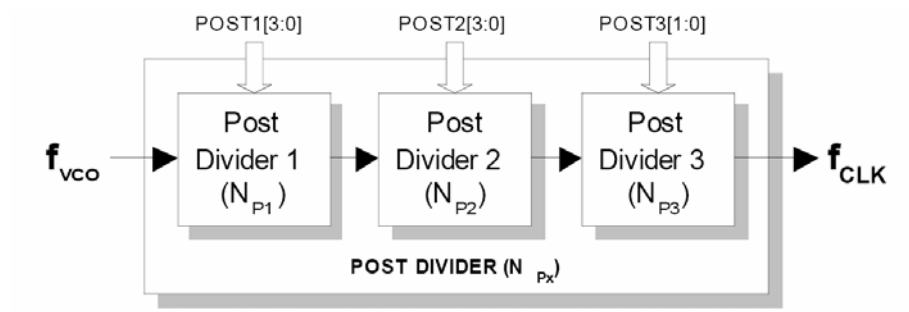


Figure 2. Post Divider

The moduli of the individual dividers are denoted as N_{P1} , N_{P2} and N_{P3} , and together they make up the array modulus N_{PX} .

$$N_{PX} = N_{P1} \times N_{P2} \times N_{P3}$$

The post divider performs several useful functions. First, it allows the VCO to be operated in a narrower range of speeds compared to the variety of output clock speeds that the device is required to generate. Second, the extra integer in the denominator permits more flexibility in the programming of the loop for many applications where frequencies must be achieved exactly.

Note that a nominal 50/50 duty factor is always preserved (even for selections which have an odd modulus).

See Table 12 for additional information.

Crystal Oscillator

The FS7140 is equipped with a Pierce-type crystal oscillator. The crystal is operated in parallel resonant mode. Internal load capacitance is provided for the crystal. While a recommended load capacitance for the crystal is specified, crystals for other standard load capacitances may be used if great precision of the reference frequency (100 ppm or less) is not required.

Reference Divider Source MUX

The source of frequency for the reference divider can be chosen to be the device crystal oscillator or the REF pin by the REFDSRC bit.

When not using the crystal oscillator, it is preferred to connect XIN to VSS. Do not connect to XOUT.

When not using the REF input, it is preferred to leave it floating or connected to V_{DD} .

Feedback Divider Source MUX

The source of frequency for the feedback divider may be selected to be either the output of the post divider or the output of the VCO by the FBKDSRC bit.

Ordinarily, for frequency synthesis, the output of the VCO is used. Use the output of the post divider only where a deterministic phase relationship between the output clock and reference clock are desired (line-locked mode, for example).

Device Shutdown

Two bits are provided to effect shutdown of the device if desired, when it is not active. SHUT1 disables most externally observable device functions. SHUT2 reduces device quiescent current to absolute minimum values. Normally, both bits should be set or cleared together.

Serial communications capability is not disabled by either SHUT1 or SHUT2.

Differential Output Stage

The differential output stage supports both CMOS and pseudo-ECL (PECL) signals. The desired output interface is chosen via the programming registers.

If a PECL interface is used, the transmission line is usually terminated using a Thévenin termination. The output stage can only sink current in the PECL mode, and the amount of sink current is set by a programming resistor on the LOCK/IPRG pin. The ratio of output sink current to IPRG current is 13:1. Source current for the CLKx pins is provided by the pull-up resistors that are part of the Thévenin termination.

Example

Assume that it is desired to connect a PECL-type fanout buffer right next to the FS7140.

Further assume:

- $V_{DD} = 3.3 \text{ V}$
- Desired $V_{HI} = 2.4 \text{ V}$
- Desired $V_{LO} = 1.6 \text{ V}$
- Equivalent $R_{LOAD} = 75 \text{ ohms}$

Then:

$$R1 \text{ (from CLKP and CLKN output to VDD)} =$$

$$\begin{aligned} & R_{LOAD} * V_{DD} / V_{HI} = \\ & 75 * 3.3 / 2.4 = \\ & 103 \text{ ohms} \end{aligned}$$

$$R2 \text{ (from CLKP and CLKN output to GND)} =$$

$$\begin{aligned} & R_{LOAD} * V_{DD} / (V_{DD} - V_{HI}) = \\ & 75 * 3.3 / (3.3 - 2.4) = \\ & 275 \text{ ohms} \end{aligned}$$

$$R_{prgm} \text{ (from VDD to IPRG pin)} =$$

$$\begin{aligned} & 26 * (V_{DD} * R_{LOAD}) / (V_{HI} - V_{LO}) / 3 = \\ & 26 * (3.3 * 75) / (2.4 - 1.6) / 3 = \\ & 2.68 \text{ Kohms} \end{aligned}$$

SYNC Circuitry

The FS7145 supports nearly instantaneous adjustment of the output CLK phase by the SYNC input. Either edge direction of SYNC (positive-going or negative-going) is supported.

Example (positive-going SYNC selected): Upon the negative edge of SYNC input, a sequence begins to stop the CLK output. Upon the positive edge, CLK resumes operation, synchronized to the phase of the SYNC input (plus a deterministic delay). This is performed by control of the device post-divider. Phase resolution equal to 1/2 of the VCO period can be achieved (approximately down to 2 ns).

I²C-bus Control Interface

This device is a read/write slave device meeting all Philips I²C-bus specifications except a "general call." The bus has to be controlled by a master device that generates the serial clock SCL, controls bus access and generates the START and STOP conditions while the device works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated. A device that sends data onto the bus is defined as the transmitter, and a device receiving data as the receiver.

I²C-bus logic levels noted herein are based on a percentage of the power supply (V_{DD}). A logic-one corresponds to a nominal voltage of V_{DD}, while a logic-zero corresponds to ground (V_{SS}).

Bus Conditions

Data transfer on the bus can only be initiated when the bus is not busy. During the data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is high. Changes in the data line while the clock line is high will be interpreted by the device as a START or STOP condition. The following bus conditions are defined by the I²C-bus protocol.

Not Busy

Both the data (SDA) and clock (SCL) lines remain high to indicate the bus is not busy.

START Data Transfer

A high to low transition of the SDA line while the SCL input is high indicates a START condition. All commands to the device must be preceded by a START condition.

STOP Data Transfer

A low to high transition of the SDA line while SCL input is high indicates a STOP condition. All commands to the device must be followed by a STOP condition.

Data Valid

The state of the SDA line represents valid data if the SDA line is stable for the duration of the high period of the SCL line after a START condition occurs. The data on the SDA line must be changed only during the low period of the SCL signal. There is one clock pulse per data bit.

Each data transfer is initiated by a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is determined by the master device, and can continue indefinitely. However, data that is overwritten to the device after the first eight bytes will overflow into the first register, then the second, and so on, in a first-in, first-overwritten fashion.

Acknowledge

When addressed, the receiving device is required to generate an acknowledge after each byte is received. The master device must generate an extra clock pulse to coincide with the acknowledge bit. The acknowledging device must pull the SDA line low during the high period of the master acknowledge clock pulse. Setup and hold times must be taken into account.

The master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been read (clocked) out of the slave. In this case, the slave must leave the SDA line high to enable the master to generate a STOP condition.

I²C-bus Operation

All programmable registers can be accessed randomly or sequentially via this bi-directional two wire digital interface. The crystal oscillator does not have to run for communication to occur.

The device accepts the following I²C-bus commands:

Slave Address

After generating a START condition, the bus master broadcasts a seven-bit slave address followed by a R/W bit. The address of the device is:

| | | | | | | |
|----|----|----|----|----|----|----|
| A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 1 | 0 | 1 | 1 | 0 | X | X |

where X is controlled by the logic level at the ADDR pins. The selectable ADDR bits allow four different FS7140 devices to exist on the same bus. Note that every device on an I²C-bus must have a unique address to avoid possible bus conflicts.

Random Register Write Procedure

Random write operations allow the master to directly write to any register. To initiate a write procedure, the R/W bit that is transmitted after the seven-bit device address is a logic-low. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is written into the slave's address pointer. Following an acknowledge by the slave, the master is allowed to write eight bits of data into the addressed register. A final acknowledge is returned by the device, and the master generates a STOP condition.

If either a STOP or a repeated START condition occurs during a register write, the data that has been transferred is ignored.

Random Register Read Procedure

Random read operations allow the master to directly read from any register. To perform a read procedure, the R/W bit that is transmitted after the seven-bit address is a logic-low, as in the register write procedure. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is then written into the slave's address pointer.

Following an acknowledge by the slave, the master generates a repeated START condition. The repeated START terminates the write procedure, but not until after the slave's address pointer is set. The slave address is then resent, with the R/W bit set this time to a logic-high, indicating to the slave that data will be read. The slave will acknowledge the device address, and then transmits the eight-bit word. The master does not acknowledge the transfer but does generate a STOP condition.

Sequential Register Write Procedure

Sequential write operations allow the master to write to each register in order. The register pointer is automatically incremented after each write. This procedure is more efficient than the random register write if several registers must be written.

To initiate a write procedure, the R/W bit that is transmitted after the seven-bit device address is a logic-low. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is written into the slave's address pointer. Following an acknowledge by the

slave, the master is allowed to write up to eight bytes of data into the addressed register before the register address pointer overflows back to the beginning address.

An acknowledge by the device between each byte of data must occur before the next data byte is sent.

Registers are updated every time the device sends an acknowledge to the host. The register update does not wait for the STOP condition to occur. Registers are therefore updated at different times during a sequential register write.

Sequential Register Read Procedure

Sequential read operations allow the master to read from each register in order. The register pointer is automatically incremented by one after each read. This procedure is more efficient than the random register read if several registers must be read.

To perform a read procedure, the R/W bit that is transmitted after the seven-bit address is a logic-low, as in the register write procedure. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is then written into the slave's address pointer.

Following an acknowledge by the slave, the master generates a repeated START condition. The repeated START terminates the write procedure, but not until after the slave's address pointer is set. The slave address is then resent, with the R/W bit set this time to a logic-high, indicating to the slave that data will be read. The slave will acknowledge the device address, and then transmits all eight bytes of data starting with the initial addressed register. The register address pointer will overflow if the initial register address is larger than zero. After the last byte of data, the master does not acknowledge the transfer but does generate a STOP condition.

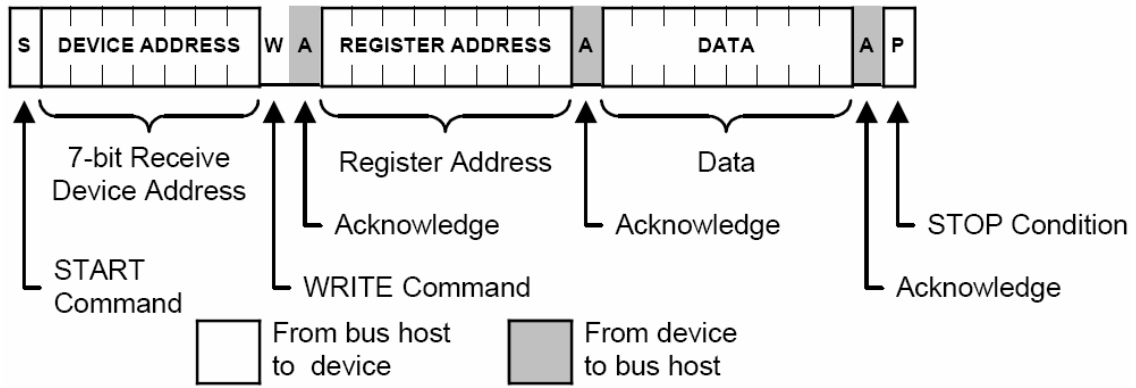


Figure 3. Random Register Write Procedure

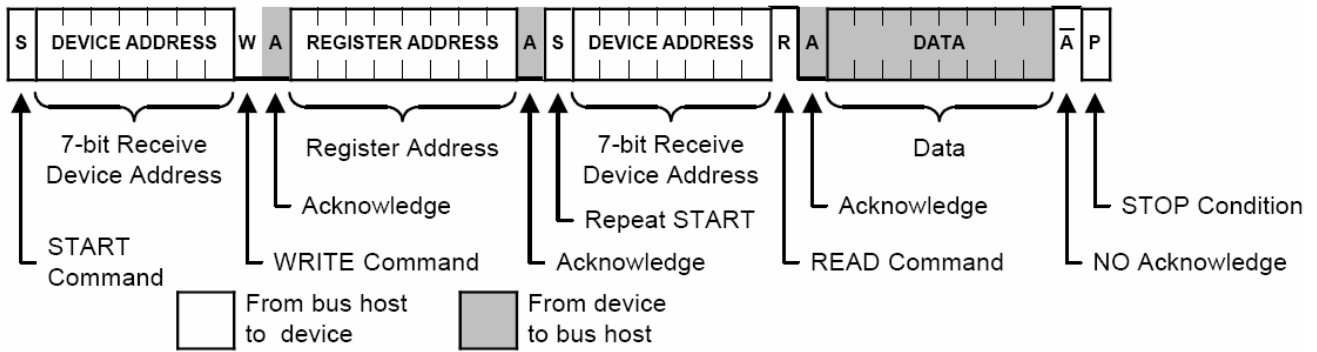


Figure 4. Random Register Read Procedure

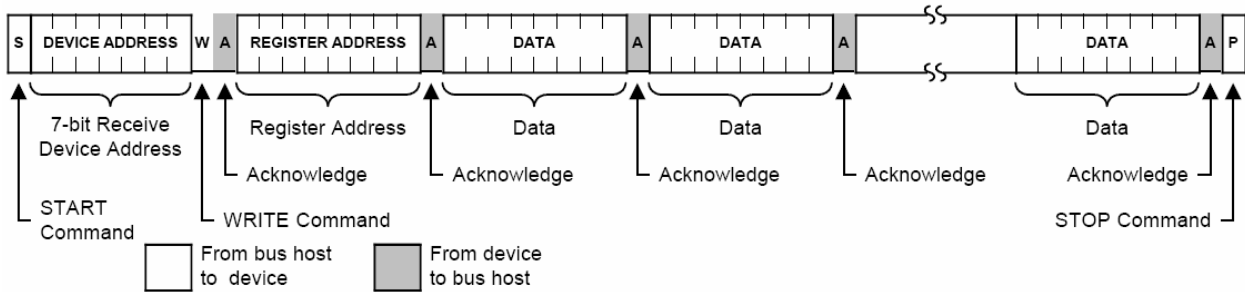


Figure 5. Sequential Register Write Procedure

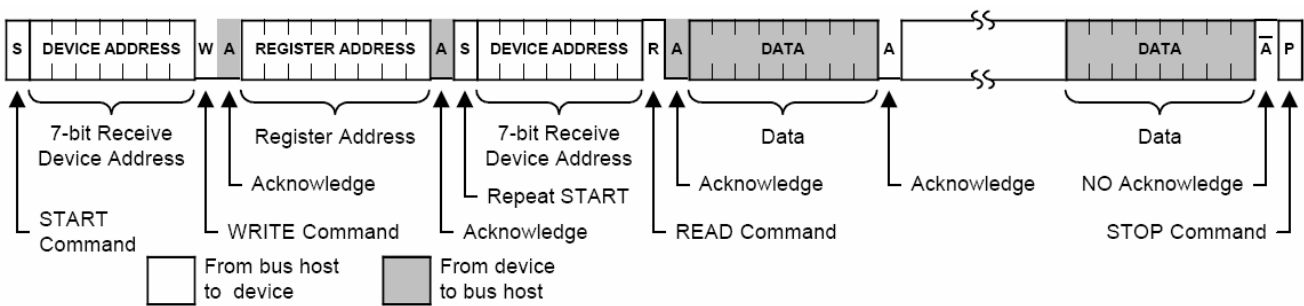


Figure 6. Sequential Register Read Procedure

FS7140, FS7145

Programming Information

All register bits are cleared to zero on power-up. All register bits may be read back as written.

Table 7. FS7140 REGISTER MAP

| Address | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------|---|--|---|--|---|--|--|--|
| Byte 7 | Reserved (Bit 63) Must be set to "0" | Reserved (Bit 62) Must be set to "0" | Reserved (Bit 61) Must be set to "0" | Reserved (Bit 60) Must be set to "0" | Reserved (Bit 59) Must be set to "0" | Reserved (Bit 58) Must be set to "0" | Reserved (Bit 57) Must be set to "0" | Reserved (Bit 56) Must be set to "0" |
| Byte 6 | Reserved (Bit 55) Must be set to "0" | Reserved (Bit 54) Must be set to "0" | SHUT2 (Bit 53) 0 = Normal 1 = Powered down | Reserved (Bit 52) Must be set to "0" | Reserved (Bit 51) Must be set to "0" | Reserved (Bit 50) Must be set to "0" | Reserved (Bit 49) Must be set to "0" | Reserved (Bit 48) Must be set to "0" |
| Byte 5 | Reserved (Bit 47) Must be set to "0" | LC (Bit 46) Loop filter cap select | LR[1] (Bit 45) | LR[0] (Bit 44) | Reserved (Bit 43) Must be set to "0" | Reserved (Bit 42) Must be set to "0" | CP[1] (Bit 41) | CP[0] (Bit 40) |
| | | | Loop filter resistor select | | | | Charge pump current select | |
| Byte 4 | CMOS (Bit 39) 0 = PECL 1 = CMOS | FBKDSRC (Bit 38) 0 = VCO output 1 = Post divider output | FBKDIV[13] (Bit 37) 8192 | FBKDIV[12] (Bit 36) 4096 | FBKDIV[11] (Bit 35) 2048 | FBKDIV[10] (Bit 34) 1024 | FBKDIV[9] (Bit 33) 512 | FBKDIV[8] (Bit 32) 256 |
| | | | See the Feedback Divider section for disallowed FBKDIV values | | | | | |
| Byte 3 | FBKDIV[7] (Bit 31) 128 | FBKDIV[6] (Bit 30) 64 | FBKDIV[5] (Bit 29) 32 | FBKDIV[4] (Bit 28) 16 | FBKDIV[3] (Bit 27) 8 | FBKDIV[2] (Bit 26) 4 | FBKDIV[1] (Bit 25) 2 | FBKDIV[0] (Bit 24) 1 |
| | See the Feedback Divider section for disallowed FBKDIV values | | | | | | | |
| Byte 2 | POST2[3] (Bit 23) | POST2[2] (Bit 22) | POST2[1] (Bit 21) | POST2[0] (Bit 20) | POST1[3] (Bit 19) | POST1[2] (Bit 18) | POST1[1] (Bit 17) | POST1[0] (Bit 16) |
| | Modulus = N + 1 (N = 0 to 11); See Table 12 | | | | Modulus = N + 1 (N = 0 to 11); See Table 12 | | | |
| Byte 1 | POST3[1] (Bit 15) | POST3[0] (Bit 14) | SHUT1 (Bit 13) 0 = Normal 1 = Powered down | REFDSRC (Bit 12) 0 = Crystal oscillator 1 = REF pin | REFDIV[11] (Bit 11) 2048 | REFDIV[10] (Bit 10) 1024 | REFDIV[9] (Bit 9) 512 | REFDIV[8] (Bit 8) 256 |
| | Modulus = 1, 2, 4 or 8; See Table 12 | | | | | | | |
| Byte 0 | REFDIV[7] (Bit 7) 128 | REFDIV[6] (Bit 6) 64 | REFDIV[5] (Bit 5) 32 | REFDIV[4] (Bit 4) 16 | REFDIV[3] (Bit 3) 8 | REFDIV[2] (Bit 2) 4 | REFDIV[1] (Bit 1) 2 | REFDIV[0] (Bit 0) 1 |

FS7140, FS7145

Table 8. FS7145 REGISTER MAP

| Address | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------|---|--|---|--|---|--|---|--|
| Byte 7 | Reserved (Bit 63) Must be set to "0" | Reserved (Bit 62) Must be set to "0" | Reserved (Bit 61) Must be set to "0" | Reserved (Bit 60) Must be set to "0" | Reserved (Bit 59) Must be set to "0" | Reserved (Bit 58) Must be set to "0" | Reserved (Bit 57) Must be set to "0" | Reserved (Bit 56) Must be set to "0" |
| Byte 6 | Reserved (Bit 55) Must be set to "0" | Reserved (Bit 54) Must be set to "0" | SHUT2 (Bit 53) 0 = Normal 1 = Powered down | Reserved (Bit 52) Must be set to "0" | Reserved (Bit 51) Must be set to "0" | Reserved (Bit 50) Must be set to "0" | SYNCPOL (Bit 49) "0" = negative "1" = positive | SYNCEN (Bit 48) "0" = negative "1" = positive |
| Byte 5 | Reserved (Bit 47) Must be set to "0" | LC (Bit 46) Loop filter cap select | LR[1] (Bit 45) | LR[0] (Bit 44) | Reserved (Bit 43) Must be set to "0" | Reserved (Bit 42) Must be set to "0" | CP[1] (Bit 41) | CP[0] (Bit 40) |
| | | | Loop filter resistor select | | | | Charge pump current select | |
| Byte 4 | CMOS (Bit 39) 0 = PECL 1 = CMOS | FBKDSRC (Bit 38) 0 = VCO output 1 = Post divider output | FBKDIV[13] (Bit 37) 8192 | FBKDIV[12] (Bit 36) 4096 | FBKDIV[11] (Bit 35) 2048 | FBKDIV[10] (Bit 34) 1024 | FBKDIV[9] (Bit 33) 512 | FBKDIV[8] (Bit 32) 256 |
| | | | See the Feedback Divider section for disallowed FBKDIV values | | | | | |
| Byte 3 | FBKDIV[7] (Bit 31) 128 | FBKDIV[6] (Bit 30) 64 | FBKDIV[5] (Bit 29) 32 | FBKDIV[4] (Bit 28) 16 | FBKDIV[3] (Bit 27) 8 | FBKDIV[2] (Bit 26) 4 | FBKDIV[1] (Bit 25) 2 | FBKDIV[0] (Bit 24) 1 |
| | See the Feedback Divider section for disallowed FBKDIV values | | | | | | | |
| Byte 2 | POST2[3] (Bit 23) | POST2[2] (Bit 22) | POST2[1] (Bit 21) | POST2[0] (Bit 20) | POST1[3] (Bit 19) | POST1[2] (Bit 18) | POST1[1] (Bit 17) | POST1[0] (Bit 16) |
| | Modulus = N + 1 (N = 0 to 11); See Table 12 | | | | Modulus = N + 1 (N = 0 to 11); See Table 12 | | | |
| Byte 1 | POST3[1] (Bit 15) | POST3[0] (Bit 14) | SHUT1 (Bit 13) 0 = Normal 1 = Powered down | REFDSRC (Bit 12) 0 = Crystal oscillator 1 = REF pin | REFDIV[11] (Bit 11) 2048 | REFDIV[10] (Bit 10) 1024 | REFDIV[9] (Bit 9) 512 | REFDIV[8] (Bit 8) 256 |
| | Modulus = 1, 2, 4 or 8; See Table 12 | | | | | | | |
| Byte 0 | REFDIV[7] (Bit 7) 128 | REFDIV[6] (Bit 6) 64 | REFDIV[5] (Bit 5) 32 | REFDIV[4] (Bit 4) 16 | REFDIV[3] (Bit 3) 8 | REFDIV[2] (Bit 2) 4 | REFDIV[1] (Bit 1) 2 | REFDIV[0] (Bit 0) 1 |

Table 9. DEVICE CONFIGURATION BITS

| Name | Description |
|---------|--|
| REFDSRC | Reference divider source |
| | [0] = crystal oscillator / [1] = REF pin |
| FBKDSRC | Feedback divider source |
| | [0] = VCO output / [1] = post divider output |
| SHUT1 | Shutdown1 |
| | [0] = normal / [1] = powered down |
| SHUT2 | Shutdown2 |
| | [0] = normal / [1] = powered down |
| CMOS | CLKP/CLKN output mode |
| | [0] = PECL output / [1] CMOS output |

Table 10. MAIN LOOP TUNING BITS

| Name | Description | |
|---------|------------------------------|----------------|
| CP[1:0] | Charge pump current | |
| | [00] | 2.0 μ A |
| | [01] | 4.5 μ A |
| | [10] | 11.0 μ A |
| | [11] | 22.5 μ A |
| LR[1:0] | Loop filter resistor select | |
| | [00] | 400 K Ω |
| | [01] | 133 K Ω |
| | [10] | 30 K Ω |
| | [11] | 12 K Ω |
| LC | Loop filter capacitor select | |
| | [0] | 185 pF |
| | [1] | 500 pF |

Table 11. PLL DIVIDER CONTROL BITS

| Name | Description |
|--------------|-----------------------------|
| REFDIV[11:0] | Reference divider (N_R) |
| FBKDIV[13:0] | Feedback divider (N_F) |

Table 12. SYNC CONTROL BITS (FS7145 only)

| Name | Description |
|---------|---|
| SYNCEN | Sync enable |
| | [0] = disabled / [1] = enabled |
| SYNCPOL | Sync polarity |
| | [0] = negative edge / [1] = positive edge |

Table 13. POST DIVIDER CONTROL BITS

| Name | Description | |
|------------|--------------------------------------|------------|
| POST1[3:0] | Post divider #1 (N_{P1}) modulus | |
| | [0000] | 1 |
| | [0001] | 2 |
| | [0010] | 3 |
| | [0011] | 4 |
| | [0100] | 5 |
| | [0101] | 6 |
| | [0110] | 7 |
| | [0111] | 8 |
| | [1000] | 9 |
| | [1001] | 10 |
| | [1010] | 11 |
| | [1011] | 12 |
| POST2[3:0] | Post divider #2 (N_{P2}) modulus | |
| | [0000] | 1 |
| | [0001] | 2 |
| | [0010] | 3 |
| | [0011] | 4 |
| | [0100] | 5 |
| | [0101] | 6 |
| | [0110] | 7 |
| | [0111] | 8 |
| | [1000] | 9 |
| | [1001] | 10 |
| | [1010] | 11 |
| | [1011] | 12 |
| POST3[1:0] | Post divider #3 (N_{P3}) modulus | |
| | [00] | 1 |
| | [01] | 2 |
| | [10] | 4 |
| | [11] | 8 |
| | [1100] | Do not use |
| | [1101] | |
| [1110] | | |
| [1111] | | |

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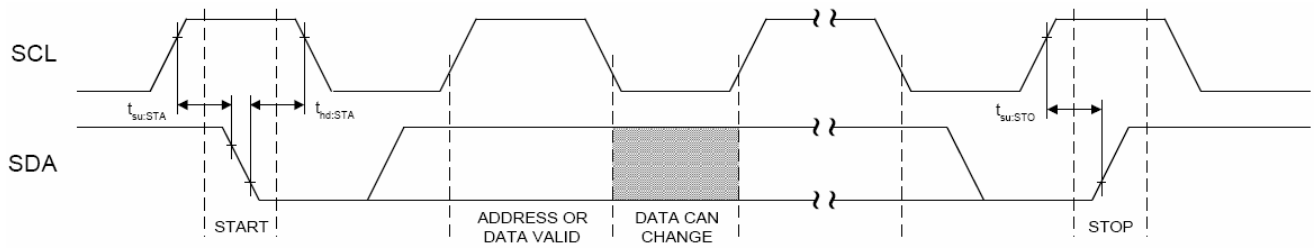


Figure 7. Bus Timing Data

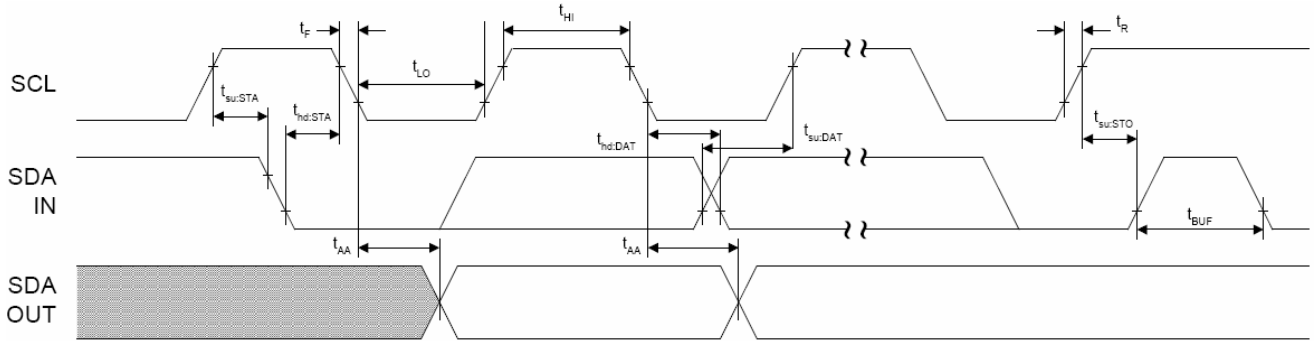


Figure 8. Data Transfer Sequence

FS7140, FS7145

PACKAGE DIMENSIONS

SSOP 16
CASE 565AE-01
ISSUE O

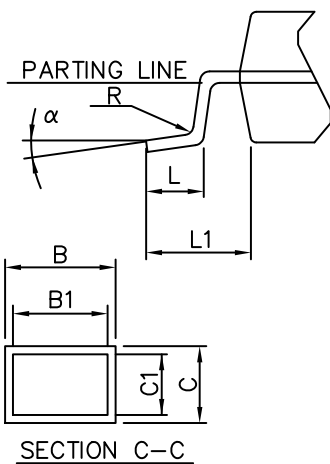
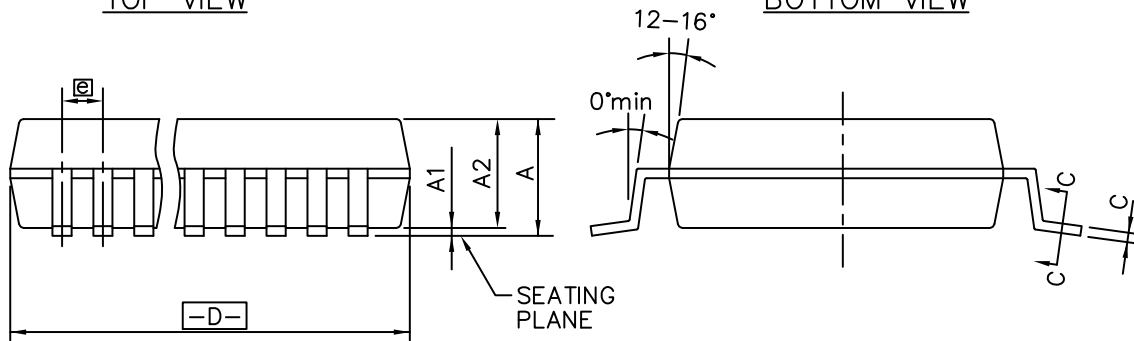
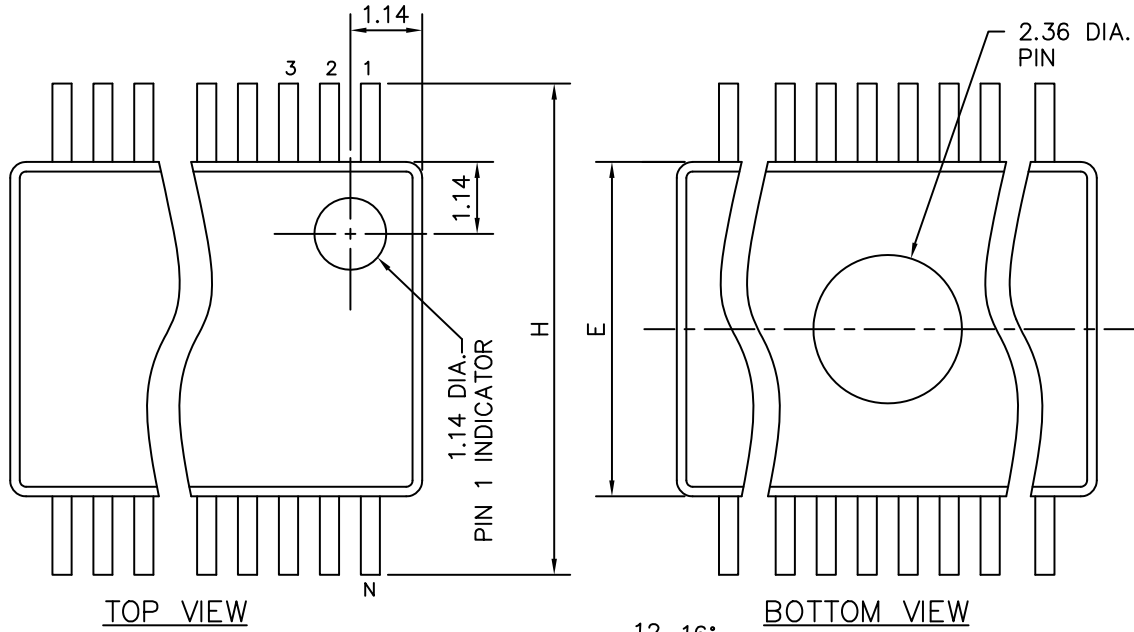


TABLE IN MILLIMETERS

| SYMBOL | COMMON DIMENSIONS | | | NOTE VARIATIONS | 1 | | | 2 |
|----------------|-------------------|------|------|-----------------|-------|-------|-------|----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | N |
| A | 1.73 | 1.86 | 1.99 | | 2.87 | 3.00 | 3.13 | 8 |
| A ₁ | 0.05 | 0.13 | 0.21 | AA | 6.07 | 6.20 | 6.33 | 14 |
| A ₂ | 1.68 | 1.73 | 1.78 | AB | 6.07 | 6.20 | 6.33 | 16 |
| B | 0.25 | - | 0.38 | AC | 7.07 | 7.20 | 7.33 | 20 |
| B1 | 0.25 | 0.30 | 0.33 | AD | 8.07 | 8.20 | 8.33 | 24 |
| C | 0.09 | - | 0.20 | AE | 10.07 | 10.20 | 10.33 | 28 |
| C1 | 0.09 | 0.15 | 0.16 | AF | 10.07 | 10.20 | 10.33 | 30 |
| D | SEE VARIATIONS | | | 1 | | | | |
| E | 5.20 | 5.30 | 5.38 | | | | | |
| e | 0.65 BSC | | | | | | | |
| H | 7.65 | 7.80 | 7.90 | | | | | |
| L | 0.63 | 0.75 | 0.95 | | | | | |
| L1 | 1.25 REF. | | | | | | | |
| N | SEE VARIATIONS | | | 2 | | | | |
| α | 0° | 4° | 8° | | | | | |
| R | 0.09 | 0.15 | - | | | | | |

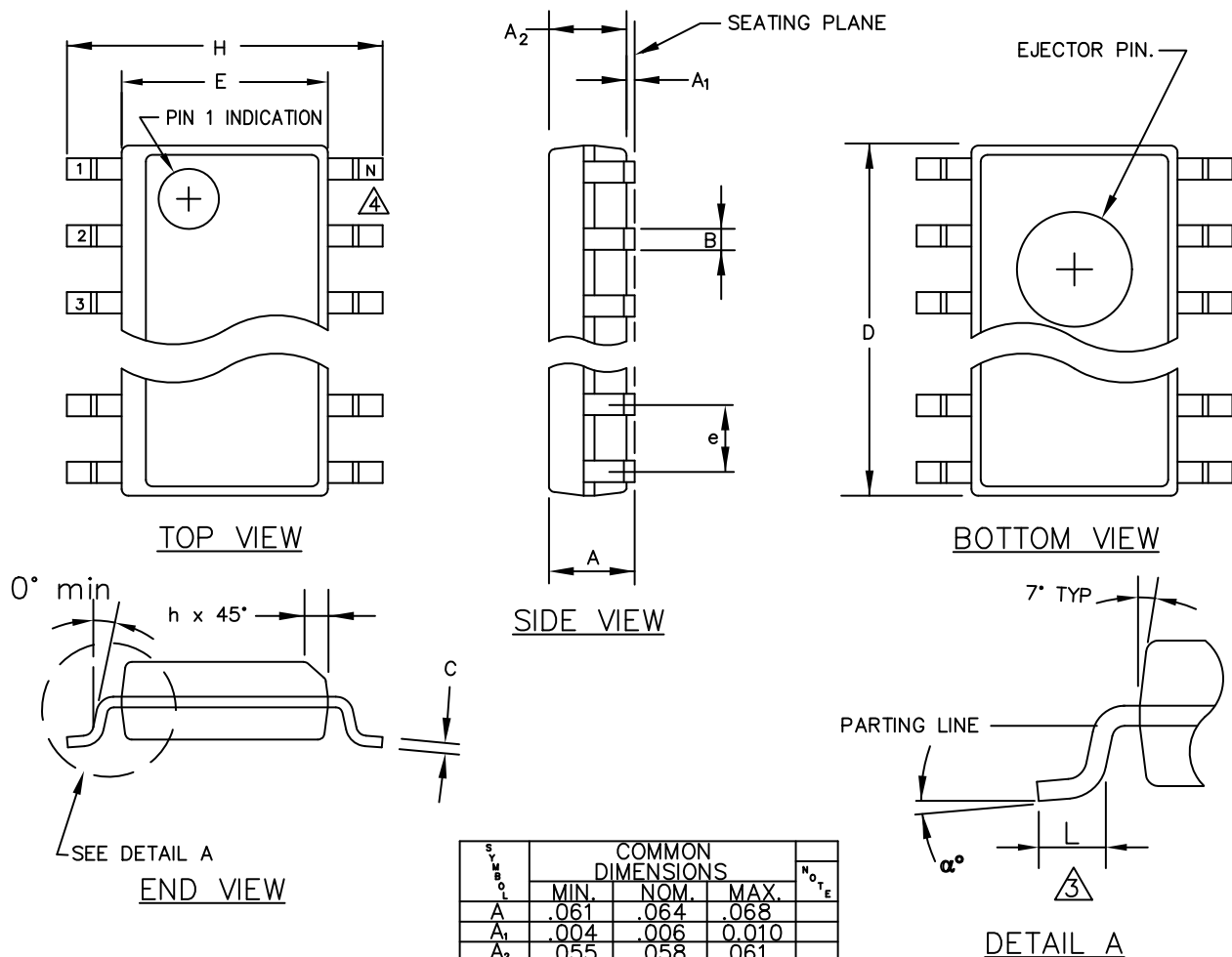
NOTE:

MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.20mm on D PER SIDE.

FS7140, FS7145

PACKAGE DIMENSIONS

SOIC 16
CASE 751BA-01
ISSUE O



| SYMBOL | COMMON DIMENSIONS | | | NOTE |
|----------------|-------------------|------|-------|------|
| | MIN. | NOM. | MAX. | |
| A | .061 | .064 | .068 | |
| A ₁ | .004 | .006 | 0.010 | |
| A ₂ | .055 | .058 | .061 | |
| B | .0138 | .016 | .020 | |
| C | .0075 | .008 | .0098 | |
| D | SEE VARIATIONS | | | 1 |
| E | .150 | .155 | .157 | |
| e | .050 BSC | | | |
| H | .230 | .236 | .244 | |
| h | .010 | .013 | .016 | |
| L | .016 | .025 | .035 | |
| N | SEE VARIATIONS | | | 2 |
| α° | 0° | 5° | 8° | |


| VARIATIONS | | | | |
|------------|------|------|------|----|
| | 1 | | | 2 |
| | D | | | N |
| NOTE | MIN. | NOM. | MAX. | |
| AA | .189 | .194 | .196 | 8 |
| AB | .337 | .342 | .344 | 14 |
| AC | .386 | .391 | .393 | 16 |

FS7140, FS7145

Table 14. ORDERING INFORMATION

| Part Number | Package | Shipping Configuration | Temperature Range |
|----------------|--|------------------------|--------------------------|
| FS7145-01-XTD | 16-pin (0.150") SOIC | Tube/Tray | 0°C to 70°C (commercial) |
| FS7145-01-XTP | 16-pin (0.150") SOIC | Tape & Reel | 0°C to 70°C (commercial) |
| FS7140-02G-XTD | 16-pin (5.3 mm) SSOP 'Green' or lead-free packaging | Tube/Tray | 0°C to 70°C (commercial) |
| FS7140-02G-XTP | 16-pin (5.3 mm) SSOP 'Green' or lead-free packaging | Tape & Reel | 0°C to 70°C (commercial) |
| FS7140-01G-XTD | 16-pin (0.150") SOIC 'Green' or lead-free packaging | Tube/Tray | 0°C to 70°C (commercial) |
| FS7140-01G-XTP | 16-pin (0.150") SOIC 'Green' or lead-free packaging | Tape & Reel | 0°C to 70°C (commercial) |
| FS7145-02G-XTD | 16-pin (5.3 mm) SSOP 'Green' or lead-free packaging | Tube/Tray | 0°C to 70°C (commercial) |
| FS7145-02G-XTP | 16-pin (5.3 mm) SSOP 'Green' or lead-free packaging | Tape & Reel | 0°C to 70°C (commercial) |

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