BURR - BROWN®



SDM862
SDM863
SDM872
SDM873

16 Single Ended/8 Differential Input 12-BIT DATA ACQUISITION SYSTEMS

FEATURES

- COMPLETE 12-BIT DATA ACQUISITION SYSTEM IN A MINIATURE PACKAGE
- INPUT RANGES SELECTABLE FOR UNIPOLAR OR BIPOLAR OPERATION
- THROUGHPUT RATES:

	862/3	872/3
8-BIT ACCURACY:	45kHz	67kHz
12-BIT ACCURACY:	33kHz	50kHz

- SELECTABLE GAINS OF 1, 10, AND 100
- FULL MICROPROCESSOR COMPATIBLE INTERFACE
- GUARANTEED NO MISSING CODES OVER TEMPERATURE
- SURFACE-MOUNT OR PIN GRID ARRAY PACKAGE OPTIONS
- HIGH RELIABILITY SCREENED VERSIONS AVAILABLE
- FULL SPECIFICATION OVER THREE TEMPERATURE RANGES: 0 to +70°C, –25 to +85°C, –55 to +125°C
- EVERY UNIT SUPPLIED WITH ELECTRICAL TEST DATA

APPLICATIONS

- INDUSTRIAL PROCESS MONITORING
- AIRBORNE SYSTEMS MONITORING
- ENGINE MONITORING
- POWER PLANT MONITORING
- SECURITY SYSTEMS MONITORING
- AUTOMATIC TEST EQUIPMENT

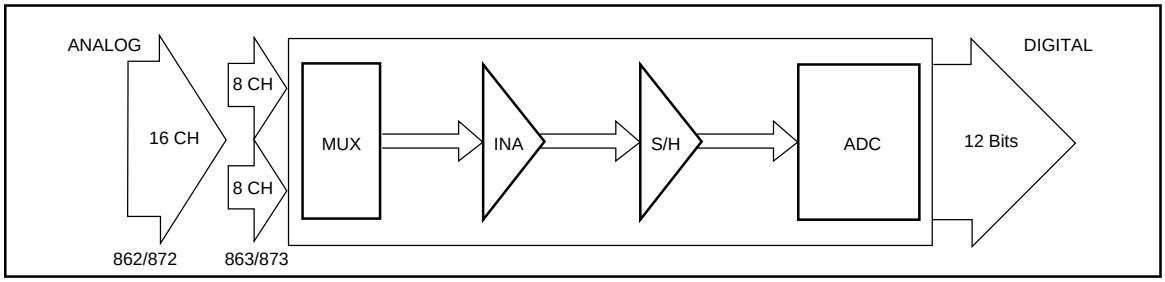
DESCRIPTION

16 Single-Ended Inputs:	SDM862	SDM872
8 Differential Inputs:	SDM863	SDM873
33kHz Throughput Rate:	SDM862	SDM863
50kHz Throughput Rate:	SDM872	SDM873

The SDM components are complete, pin-compatible, data acquisition systems housed in a hermetically sealed 1"-square leadless chip carrier or a 1.1"-square pin grid array. The small package outlines and low power consumption provide an ideal data acquisition solution when space is at a premium.

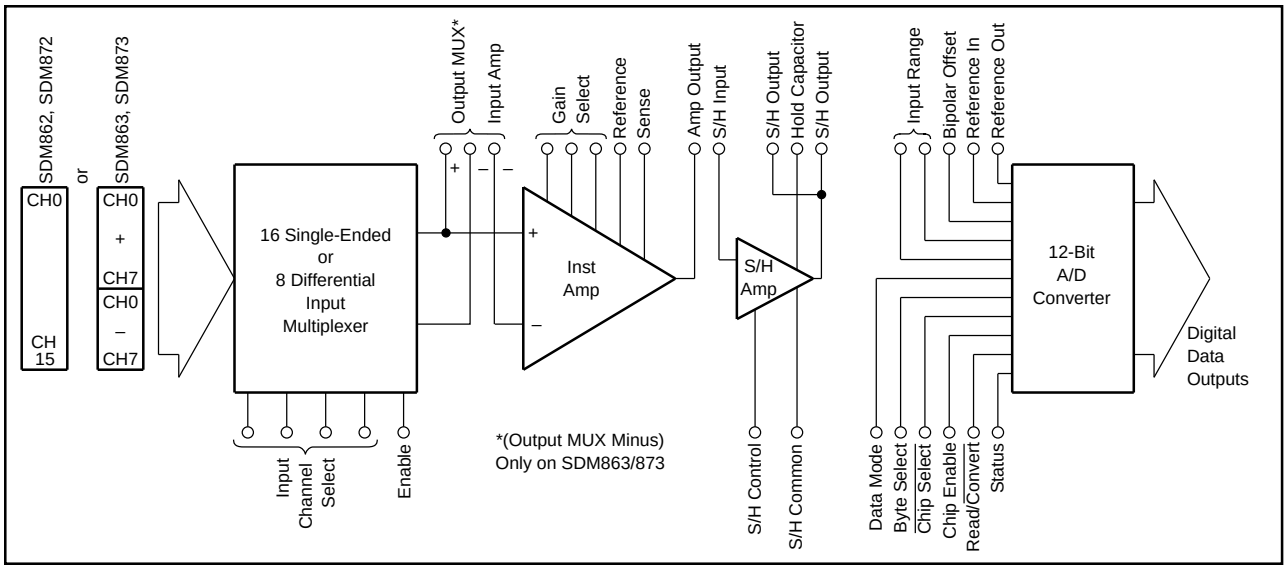
The devices comprise of an input multiplexer, instrumentation amplifier with selectable gains, sample/hold amplifier and A/D converter with microprocessor interface and three-state buffers.

The SDM family will accept unipolar or bipolar voltage inputs in the range 0 to +10V, ±5V and ±10V. For low-level signals, jumper-selectable gains of 10 or 100 can be applied. The number of input channels can be expanded by the addition of multiplexers. System integration is simplified by the microprocessor interface and the facility of the sample/hold amplifier being controlled directly by the A/D converter.



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SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V, V_{DD} = 5V, external sample/hold capacitor of 4700pF. **All grades are burned-in at +125°C for 48 hours min.**

PARAMETER	SDM862/863/872/873 J, A, R			SDM862/863/872/873 K, B, S			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			*	Bits
INPUT							
ANALOG							
Voltage Ranges: Bipolar			±5, ±10				V
Unipolar			0-10				V
Input Impedance: On Channel		10^{10}			*		Ω
Off Channel		10^{10}			*		Ω
Input Capacitance: On Channel		20			*		pF
Off Channel		20			*		pF
CMRR (20VDC to 1kHz)	80	85		*	*		dB
Crosstalk (20Vp-p, 1kHz) (1)		–85	–80		*	*	dB
Feedthrough (at 1kHz) (1)		–85	–80		*	*	dB
Offset (channel to channel) G = 1 (2)		30	100		*	*	µV
Input Bias Current/Channel		1	5		*	*	nA
Input Voltage Range (3)	+10	+11		*	*		V
	–10	–15		*	*		V
DIGITAL (7, 8)							
MUX Input Channel Select: Logic '1'		5	30		*	*	µA
Logic '0'		5	30		*	*	µA
MUX Input: Logic High	4.0			*			V
Logic Low			0.8			*	V
S/H Command: Logic '1'		0.2			*		nA
Logic '0'		5	30		*	*	µA
ADC Section: Logic '1'			10			*	µA
Logic '0'			10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Integral Linearity (4)			±0.024			±0.012	%FSR
Differential Linearity (4)			±0.024			*	%FSR
No Missing Codes		Over Operating Temperature Range					
Gain Error (5): G = 1			0.5			*	%
G = 100		0.9			*		%
Unipolar Offset Error (5)		16			*		mV
Bipolar Offset Error (5)			50			*	mV
Noise Error							
(Measured at S/H Output) G = 1		0.5	1		*	*	mVp-p
Droop Rate		50	500		*	*	µV/ms
Temperature Coefficients:							
Unipolar Offset			20			15	ppm of FSR/°C
Bipolar Offset			30			25	ppm of FSR/°C
Full-Scale Calibration			60			35	ppm of FSR/°C

SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V, V_{DD} = 5V, external sample/hold capacitor of 4700pF.

PARAMETERS	SDM862/863/872/873 J, A, R			SDM862/863/872/873 K, B, S			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM TIMINGS							
ADC Conversion Time: SDM862/SDM863	9	20	25	*	*	*	µs
SDM872/SDM873	9	12	15	*	*	*	µs
S/H Aperture Delay		50			*		ns
S/H Aperture Uncertainty		2			*		ns
TIMING							
Throughput (Serial Mode)							
SDM862/SDM863			22			*	kHz
SDM872/SDM873			28			*	kHz
(Overlap Mode):							
SDM862/SDM863			33			*	kHz
SDM872/SDM873			50			*	kHz
MULTIPLEXER [6]							
Switching Time (between channels)		+1.5			*		µs
Settling Time (10V step to 0.02%)		2.5			*		µs
Enable Time 'ON'		1	2		*	*	µs
'OFF'		0.25	0.5		*	*	µs
INSTRUMENTATION AMPLIFIER [6]							
Settling Time (20V step to 0.01%)							
G = 1		5	12.5		*	*	µs
G = 10		3	7.5		*	*	µs
G = 100		4	7.5		*	*	µs
Slew Rate	12	17		*	*		V/µs
S/H AMPLIFIER [6]							
Acquisition (10V step to 0.01%)		5			*		µs
Aperture Delay		50			*		ns
Hold Mode Settling Time		1.5			*		µs
Slew Rate		10			*		V/µs
OUTPUT							
DIGITAL DATA							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (Sink = 1.6mA)			+0.4			*	V
Logic 1 (Source = 500µA)	+2.4			*			V
Leakage (Data Bits Only), High-Z State	–5	0.1	+5	*	*	*	µA
POWER SUPPLY REQUIREMENTS							
Rated Voltage: Analog (±V_{CC})	14.25	15	15.75	*	*	*	VDC
Digital (V_{DD})	4.5	5	5.5	*	*	*	VDC
Supply Drain: +15V		13	22		*	*	mA
–15V		22	30		*	*	mA
+5V		11	15		*	*	mA
Power Dissipation		580	855		*	*	mW
TEMPERATURE RANGE							
Operating Temperature Range							
JH, KH/JL, KL	0		70	*		*	°C
AH, BH/AL, BL	–25		+85	*		*	°C
RH, SH/RL, SL	–55		+125	*		*	°C
Storage Temperature Range	–65		+150	*		*	°C

* Specification same as SDM862/863/872/873J, A, R grades.

NOTES: (1) Measured at the same and hold output. (2) Measured with all input channels grounded. (3) The range of voltage on any input with respect to common over which accuracy and leakage current is guaranteed. (4) Applicable over full operating temperature range. NO MISSING CODES GUARANTEED OVER TEMPERATURE RANGE. (5) Adjustable to zero using external potentiometer or select-on-test resistor. (6) Specifications are at +25°C and measured at 50% level of transition. (7) When using TTL drivers a 1kΩ pull-up resistor should be used. (8) Muxes operate in a break-before-make manner.

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DIGITAL TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
tdsc	Status Delay from CE		100	200	ns
thec	CE Pulse Width	50	30		ns
tssc	$\overline{CS}$ to CE Setup	50	20		ns
thsc	$\overline{CS}$ Low During CE High	50	20		ns
tsrc	R/$\overline{C}$ to CE Setup	50	0		ns
thrc	R/$\overline{C}$ Low During CE High	50	20		ns
tsac	Byte Select to CE Setup	0	0		ns
thac	Byte Selected Valid During CE High	50	20		ns
tc 86X	Conversion Time: 12 Bit Cycle	9	20	25	µs
	8 Bit Cycle	6	13	17	µs
tc 87X	Conversion Time: 12 Bit Cycle	9	12	15	µs
	8 Bit Cycle	6	8	10	µs
READ MODE					
tdd	Access Time from CE		75	150	ns
thd	Data Valid after CE Low	25	35		ns
thl	Output Float Delay		100	150	ns
tssr	$\overline{CS}$ to CE Setup	50	0		ns
tsrr	R/$\overline{C}$ to CE Setup	0	0		ns
tsar	Byte Select to CE Setup	50	25		ns
thsr	$\overline{CS}$ Valid after CE Low	0	0		ns
thrr	R/$\overline{C}$ High after CE Low	0	0		ns
thar	Byte Select Valid after CE Low	50	25		ns
ths 86X	Status Delay after Data Valid	100	500	1000	ns
ths 87X	Status Delay after Data Valid	100	300	600	ns

ABSOLUTE MAXIMUM RATINGS(1)

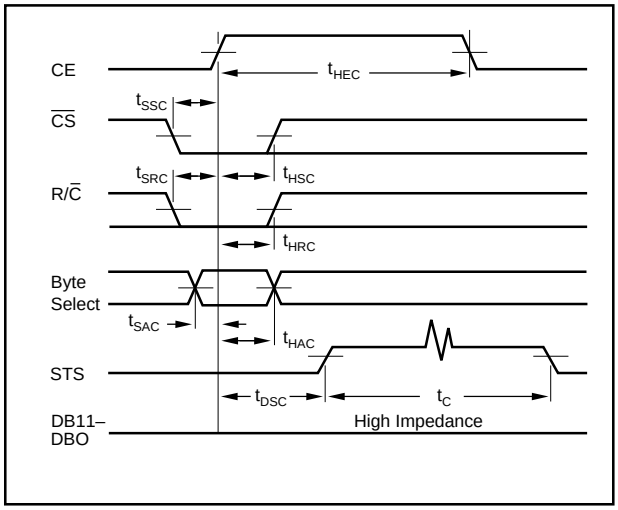
$+V_{CC}$ to ACOM	–0.5V to +16V
$-V_{CC}$ to ACOM	+0.5 to –16V
$+V_{DD}$ to DCOM	–0.5V to +7.0V
Analog Input Signal Range	$+V_{CC}$ +20V to $-V_{CC}$ –20V
Digital Input Signal	–0.5V to $+V_{DD}$
ACOM to DCOM	±1V

NOTE: (1) Absolute maximum ratings are limiting values applied individually, beyond which the serviceability of the circuit may be impaired. Functions operation under any of these conditions is not necessarily implied.

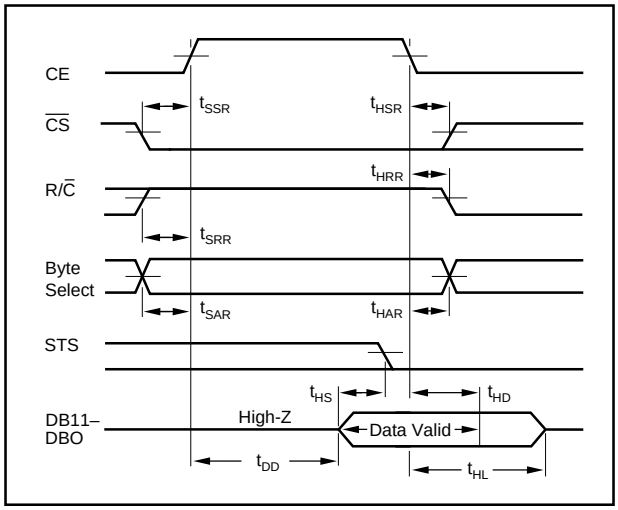
/QM HIGH RELIABILITY SCREENING

High Power Internal	
Visual Inspection	Burr-Brown Spec. QC2010
Stabilization Bake	24Hr at +150°C
Temperature Cycling	10 Cycles –65°C to +150°C
Constant Acceleration	30kG, Y1 axis
Hermeticity Fine Leak	Helium 5 x 10^{-8}cc/s
Hermeticity Gross Leak	Fluorocarbon
Burn-In	160Hr at +125°C

CONVERSION CYCLE TIMING



READ CYCLE TIMING



ORDERING INFORMATION[1]

Product	Input	LCC, PGA Package	Accuracy (% FSR)	Throughput	Temperature Range (°C)	Product	Input	LCC, PGA Package	Accuracy (% FSR)	Throughput	Temperature Range (°C)
SDM862J	16SE	L,H	±0.024	33kHz	0 to +70	SDM863J	8DIF	L, H	±0.024	33kHz	0 to +70
SDM862K	16SE	L,H	±0.012	33kHz	0 to +70	SDM863K	8DIF	L, H	±0.012	33kHz	0 to +70
SDM862A	16SE	L,H	±0.024	33kHz	–25 to +85	SDM863A	8DIF	L, H	±0.024	33kHz	–25 to +85
SDM862B	16SE	L,H	±0.012	33kHz	–25 to +85	SDM863B	8DIF	L, H	±0.012	33kHz	–25 to +85
SDM862R	16SE	L,H	±0.024	33kHz	–55 to +125	SDM863R	8DIF	L, H	±0.024	33kHz	–55 to +125
SDM862S	16SE	L,H	±0.012	33kHz	–55 to +125	SDM863S	8DIF	L, H	±0.012	33kHz	–55 to +125
SDM872J	16SE	L,H	±0.024	50kHz	0 to +70	SDM873J	8DIF	L,H	±0.024	50kHz	0 to +70
SDM872K	16SE	L,H	±0.012	50kHz	0 to +70	SDM873K	8DIF	L,H	±0.012	50kHz	0 to +70
SDM872A	16SE	L,H	±0.024	50kHz	–25 to +85	SDM873A	8DIF	L,H	±0.024	50kHz	–25 to +85
SDM872B	16SE	L,H	±0.012	50kHz	–25 to +85	SDM873B	8DIF	L,H	±0.012	50kHz	–25 to +85
SDM872R	16SE	L,H	±0.024	50kHz	–55 to +125	SDM873R	8DIF	L,H	±0.024	50kHz	–55 to +125
SDM872S	16SE	L,H	±0.012	50kHz	–55 to +125	SDM873S	8DIF	L,H	±0.012	50kHz	–55 to +125

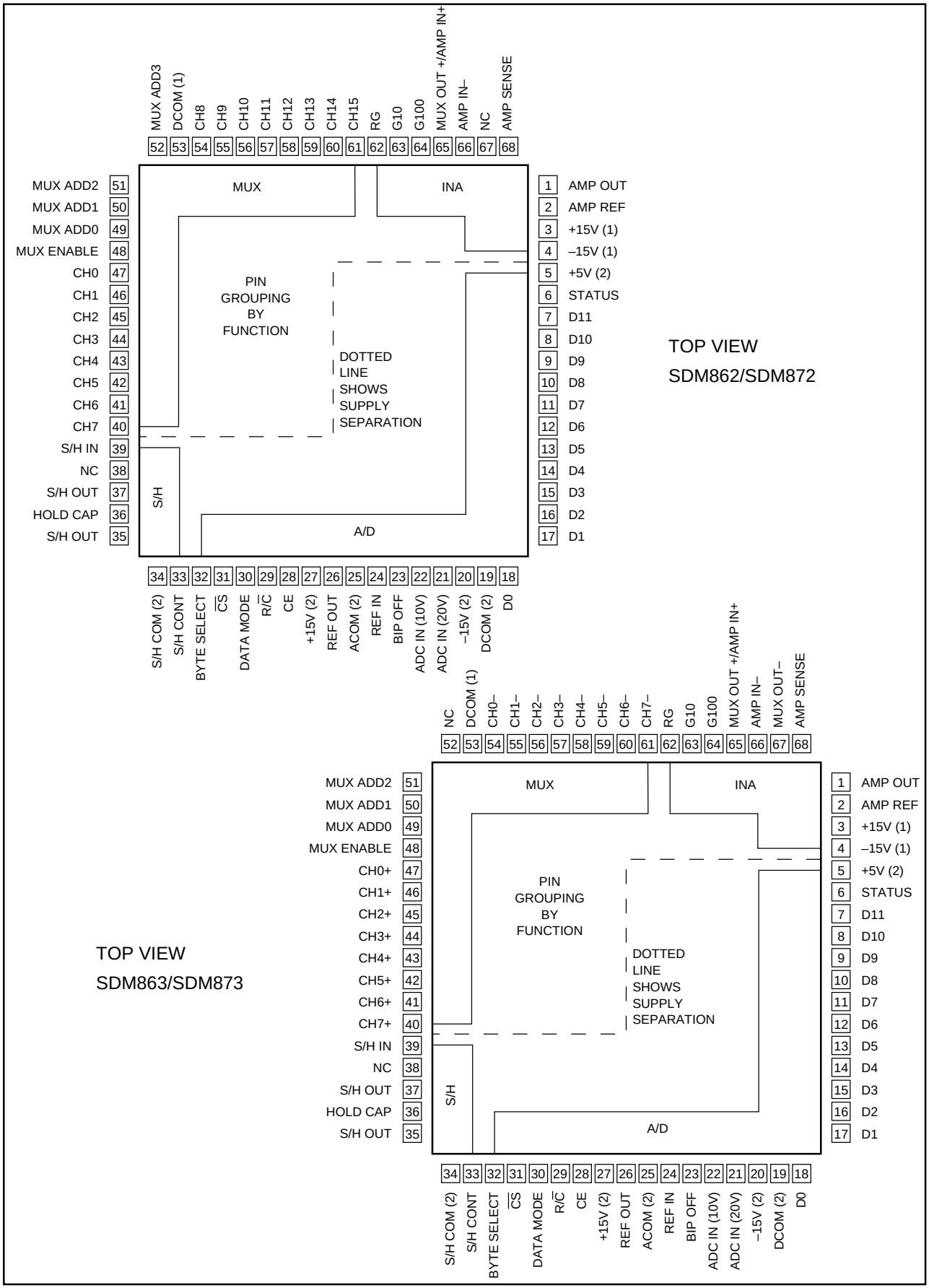
NOTE: (1) 16 single-ended inputs, LCC package, with accuracy of 0.24% FSR. Temp Range of 0°C to +70°C and throughput of 33kHz = SDM862JL.

PACKAGE INFORMATION

PRODUCT	DESCRIPTION	PACKAGE DRAWING NUMBER[1]
PC862/863-1	LCC (Socketed) Evaluation PCB[2]	907
PC862/863-2	PGA Evaluation PCB	906

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Socket is MC0068-1.

PIN CONFIGURATIONS



PIN DESIGNATION	DEFINITION	COMMENTS SDM8X2 = SDM862 OR SDM872
CH0 to CH15 CH0 to CH7 (+, –) (PINS 40 to 47, 54 to 61)	Channel Inputs	Analog Inputs (Total 16) for single-ended and differential operation. Unused inputs must be connected to analog common.
MUX OUT+/AMP IN+ (PIN 65)	MULTIPLEXER “HI” OUTPUT	On the SDM8X2 this is the multiplexer output. On the SDM8X3 it is the output of the positive selected inputs. It is connected internally to the positive input of the instrumentation amplifier.
MUXOUT (Pin 67)	MULTIPLEXER “LO” OUTPUT	This pin is used on the SDM8X3 only. It should be connected to the negative input of the instrumentation amplifier.
AMP IN (Pin 66)	Negative input of instrumentation amplifier	On the SDM8X2 this should be connected to analog common. On the SDM8X3 it should be connected to Muxout—(Pin 67).
AMP OUT (Pin 1)	Output of instrumentation amplifier	This pin should be connected to the input of the S/H amplifier (Pin 39).
AMP SENSE (Pin 68)	Output sense line of instrumentation amplifier	This pin will normally be connected direct to AMP OUT (Pin 1).
AMP REF (Pin 2)	Reference for amplifier output	This pin will normally be connected to analog common. Care should be taken to minimize tracking and contact resistance to analog common to optimize system accuracy.
S/H OUT (Pins 35/37)	Output of sample/hold amplifier	Two pins are provided to facilitate a guard ring around the hold capacitor pin. These pins should be connected to either ADC in (20V) or ADC in (10V) depending on the desired range.
HOLD CAP (Pin 36)	Connection for hold capacitor on S/H amplifier	The tracking to the hold capacitor should be as short as possible and a guard ring employed using Pins 35 and 37.
ADC IN (20V); ADC IN (10V) (Pins 21, 22)	Inputs to A/D converter	Connect to S/H amplifier output. Use appropriate pin for desired range.
RG, G10, G100 (Pins 62, 63, 64)	Gain settling pins on instrumentation amplifier	For Gain = 1, no connections. For Gain = 10, connect G10 to RG. For Gain = 100, connect G100 to RG.
REF OUT (PIN 26)	10V Reference voltage	This is the reference voltage for the A/D converter.
REF IN, BIP OFF (Pins 24, 23)	Reference input and offset input to A/D converter	Connect trim potentiometers (or select-on-test resistors) to these pins for unipolar or bipolar operation as shown in Figures 12, 13.
S/H IN (Pin 39)	Input to sample/hold amplifier	Connect to amp out (Pin 1).
MUX ENABLE (Pin 48)	Multiplex enable/disable	Logic ‘1’ on this pin will enable a selected channel on the internal multiplexer. Logic ‘0’ de-selects all channels.
MUX ADD0 to MUX ADD3 (Pins 49 to 52)	Address inputs for channel selection	These address lines select a particular channel as specified in Figure 24.
S/H CONT (Pin 33)	Track/Hold control on S/H amplifier	Logic ‘1’ holds an analog value for conversion by the A/D converter. This line may be controlled by the status (Pin 6) of the converter to simplify external timing control.
S/H COM (Pin 34)	Reference for S/H logic control	Connect to digital common.
D0 to D11 (Pins 7 to 18)	3-state digital outputs	The 12- or 8-bit result of a conversion is available as output on these pins (D0-LSB, D11-MSB).
STATUS (Pin 6)	Status of A/D conversion	This output is at logic ‘1’ while the internal A/D converter is carrying out a conversion. This pin may be used to directly control the S/H amplifier.
CE (Pin 28)	Chip enable	This input must be at logic ‘1’ to either initiate a conversion or read output data (see Figures 10, 17, 18, 19, 20).
$\overline{CS}$ (Pin 31)	Chip select	This input must be at logic ‘0’ to either initiate a conversion or read output data (see Figures 10, 17, 18, 19, 20).
R/$\overline{C}$ (Pin 29)	Read/convert	Data can be read when this pin is logic ‘1’ or a conversion can be initiated when this pin is logic ‘0’. This pin is typically connected to the R/$\overline{W}$ control line of a microprocessor-based system (see Figures 10, 17, 18, 19, 20).
DATA MODE (Pin 30)	Select 12- or 8-Bit Data	When data mode is at logic ‘1’ all 12 output data bits are enabled simultaneously. When data mode is at logic ‘0’ MSBs and LSBs are controlled by byte select (Pin 32).
BYTE SELECT (Pin 32)	Byte address, short cycle	When reading output data, byte select at logic ‘0’ enables the 8 MSBs. Byte select at logic ‘1’ enables the 4 LSBs. The 4 LSBs can therefore be connected to four of the MSB lines for inter-connection to an 8-bit bus. In start convert mode, logic ‘0’ enables a 12-bit conversion while logic ‘1’ will short cycle the conversion to 8 bits (see Figure 10).
+15V(1), +15V(2)(Pins 3, 27)	Power Supply	Connect to +15V supply using decoupling as indicated in Figures 15, 16.
–15V(1), –15V(2)(Pins 4, 20)	Power Supply	Connect to –15V supply using decoupling as indicated in Figures 15, 16.
ACOM(2) (Pin 25)	Analog Common	Analog common connection. Note that a common (including digital common) should be connected together at one point close to the device.
DCOM (1) (Pin 53)	Reference for MUX logic control.	Connect to digital common.
+5V (Pin 5)	Logic power supply	Connect to +5V digital supply line with decoupling as in Figures 15, 16.
DCOM(2) (Pin 19)	Reference for A/D converter control lines	Connect to S/H common at one point close to device.
NC (Pin 38)	No internal connection	

SYSTEM DESCRIPTION

The SDM comprises four circuit elements—an input-protected multiplexer, an instrumentation amplifier, a sample/hold amplifier, and an analog-to-digital converter.

INSTALLATION

MULTIPLEXER

The SDM family has a choice of input multiplexers (MUX).

SDM862 and SDM872: 16 single-ended inputs
SDM863 and SDM873: 8 differential inputs

On all models, the analog inputs may be expanded using the enable control. See Figure 1. When the enable is at a logic "0," the internal MUX is disabled, allowing additional multiplexers to be connected in parallel. The limiting factor for the number of additional multiplexers is the cumulative effect of leakage current flowing in the signal source impedance, causing offset errors.

Differential inputs will generally eliminate the noise associated with common system grounds, but care must be taken to ensure that neither of the differential inputs exceed the maximum input range. Otherwise, signal distortion will result. A return path for the input bias currents must always be provided. This prevents the charging of stray capacitances in applications using floating sources, such as transformers and thermocouples. Multiplexer inputs are protected from overvoltage, as indicated in the electrical specifications, and should be current limited to 20mA.

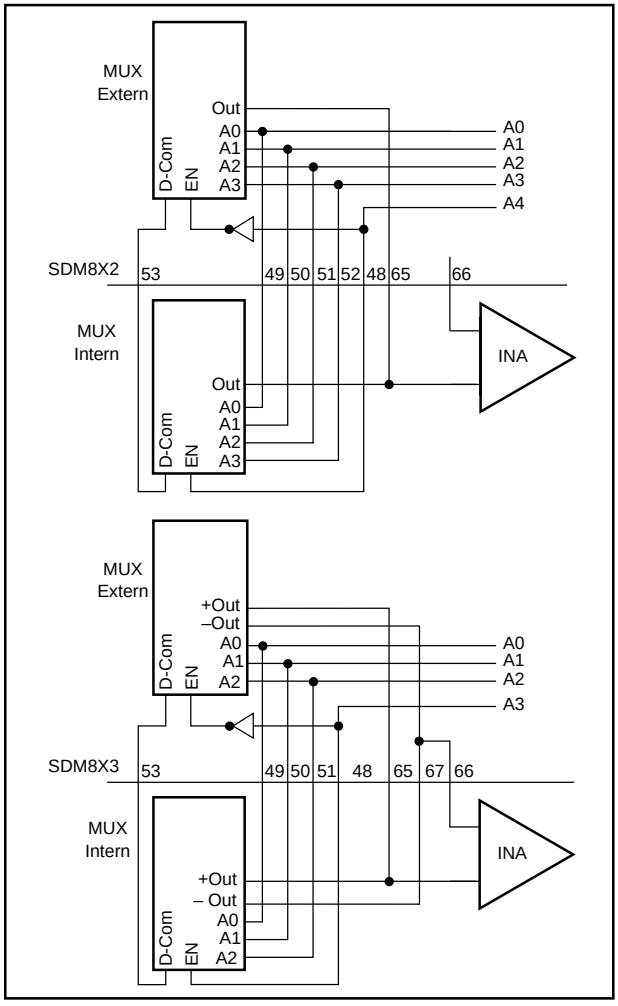


FIGURE 1. External Multiplexer Connections for Differential and Single-Ended Operation.

Where high-speed operation is required and channels require rapid sampling, then it is important to buffer the inputs against the effect of current sharing between the MUX output capacitance and the input filter capacitance. See Figure 2.

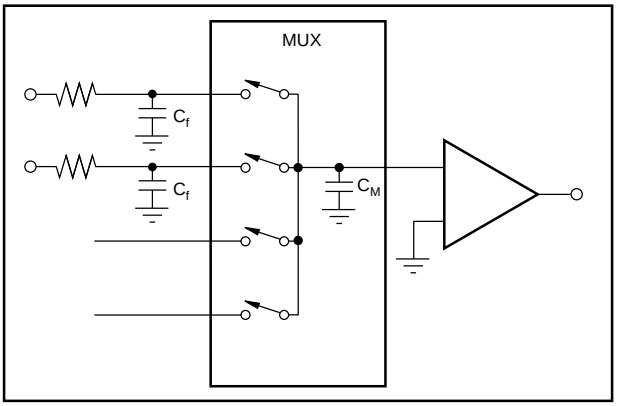


FIGURE 2. Filter and MUX Capacitance.

All data acquisition systems using a MUX require consideration of the errors that may be introduced by MUX output capacitance. The applications information explains this more fully in the input filtering section.

Shown in Figure 3 is an application that demonstrates the flexibility of signal conditioning and gives the opportunity to use a higher bandwidth filter. Diodes shown are low leakage types (1na). The low output impedance of the amplifiers reduces the time taken to charge MUX capacitance C_M.

INSTRUMENT AMPLIFIER

The instrument amplifier (INA) presents a very high input impedance to the signal source, eliminating gain errors introduced by voltage divider action between the source output impedance and SDM input impedance. Where the differential models are used, the INA performs the differential to single-ended conversion required to drive the sample/hold amplifier. Gains may be set by using external jumpers, to values of 1 (no jumper), 10 and 100. For gains other than these presets, the following formula may be used to find an external resistor value to add in series with the G = 10 or G = 100 jumpers.

$$R_{ext} = \frac{40k\Omega}{G - 1} - Ri$$

Where Ri = 4444Ω, G = 10 input.
404Ω, G = 100 input.

It should be noted that the internal gain set resistors have a ±20% tolerance and ±20ppm/°C drift.

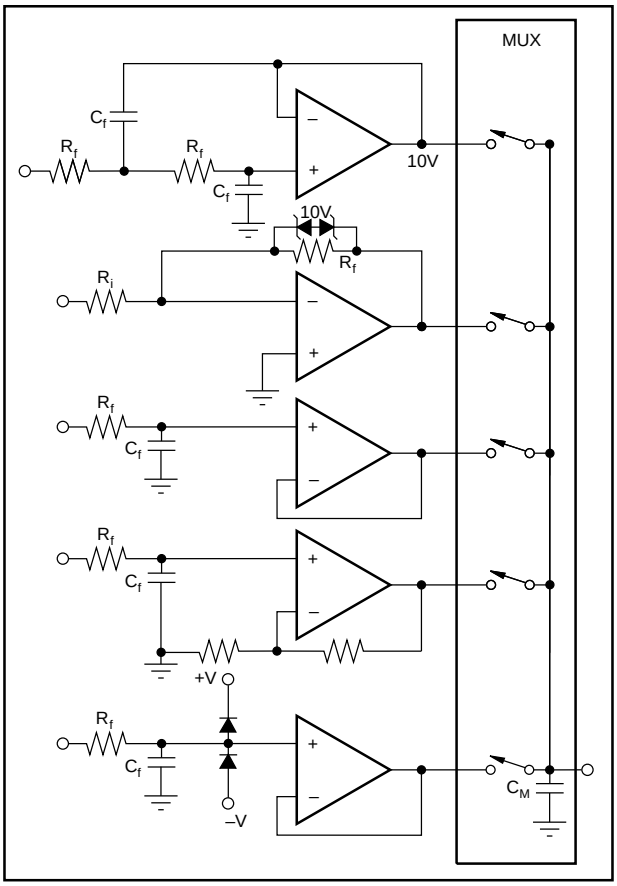


FIGURE 3. Example Application Illustrating Flexible Signal Conditioning.

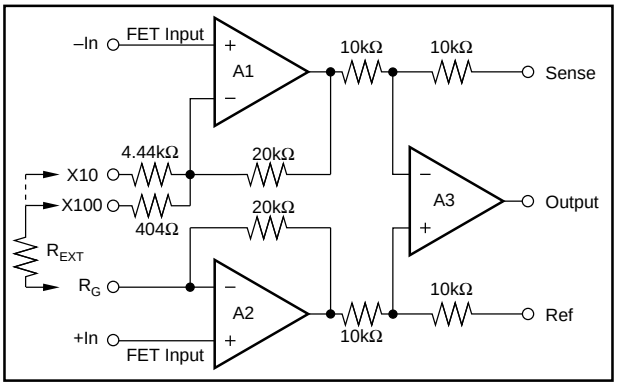


FIGURE 4. Use External Gain Set Resistor.

Where it is necessary to keep the input amplifiers from saturating or increasing the overall gain, then the gain of the output amplifier can be increased from unity by using the circuit in Figure 5.

The values of the resistors in Figure 5 are in the following table.

O/P GAIN	R_1 and R_3 Ω	R_2 Ω
2	1200	2740
5	1000	511
10	1500	340

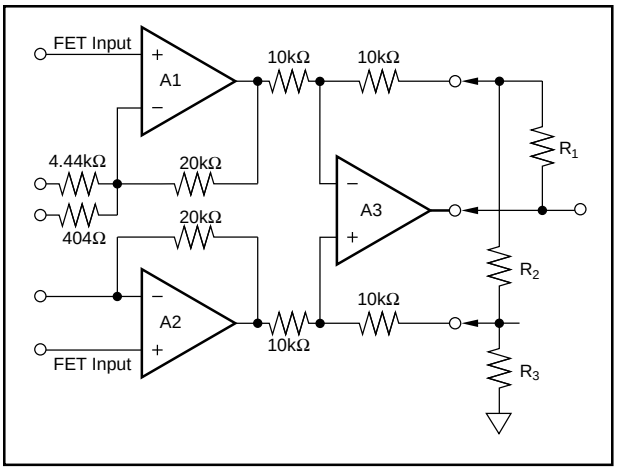


FIGURE 5. Increasing Output Amplifier Gain.

Matching of R_1 and R_3 is required to maintain high common-mode rejection (CMR), R_2 sets the gain and may be varied without effect on CMR.

To ensure that the effects of temperature are minimized when altering the gain with external components, it is very important to use low tempco resistors. When connecting the output sense, ensure that series resistance is minimized because resistance present will degrade CMR.

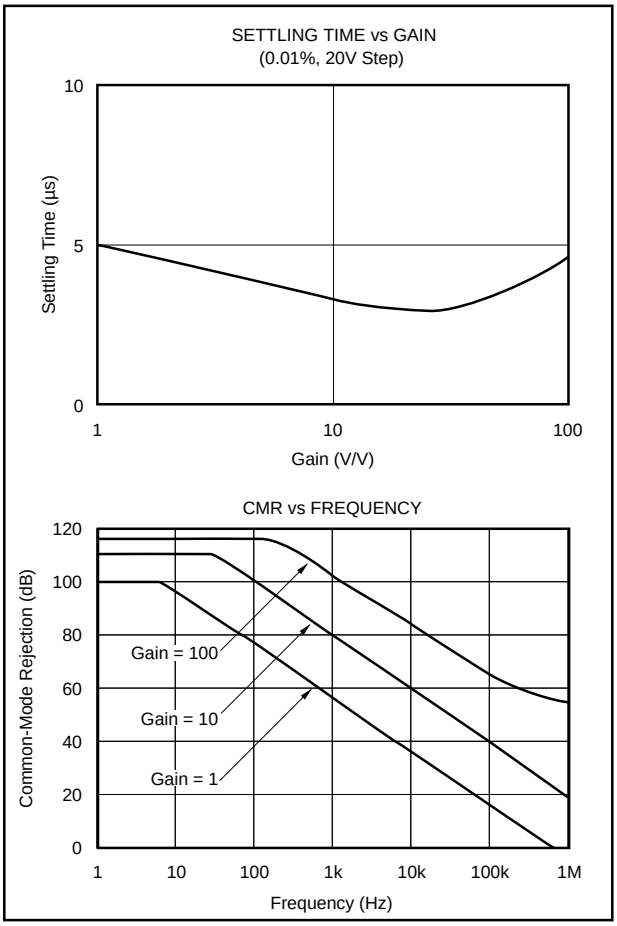


FIGURE 6. Typical INA Settling Time and CMR.

Some applications may require programmable gains. This may be realized with Figure 7.

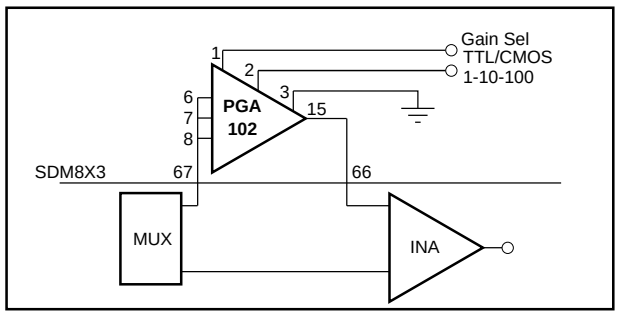


FIGURE 7. Setting Programmable Gains.

SAMPLE/HOLD AMPLIFIER

The Sample/Hold amplifier (S/H) is used to track the incoming signal and "hold" the required instantaneous value so that it does not change while the ADC is carrying out its conversion. Timing for the S/H may be derived from the STATUS output of the ADC, with care being taken to comply with the SDM timing considerations.

Capacitors with high insulation resistance and low dielectric absorption such as Teflon™, polystyrene or polypropylene should be used as storage elements. (Polystyrene should not be used above +80°C.) Teflon™ is recommended for high temperature operation. Care should be taken in the printed circuit layout to minimize stray capacitance and leakage currents from the capacitor to minimize charge offset and droop errors. The use of a guard ring driven by the S/H output around the pin connecting to the hold capacitor is recommended. (Refer to the application board layout for an example of this.)

The value of the external hold capacitor determines the droop rate, charge offset and acquisition time of the S/H, Figure 8. Droop rate for the SDM is specified with a hold capacitor value of 4700pf. There is a trade-off between acquisition time and droop rate, as the hold capacitor is increased in value it takes longer to charge, and hence there is a corresponding increase in acquisition time and reduction in droop rate. The droop rate is determined by the amount of leakage present in the SDM, board leakage and the dielectric absorption of the hold capacitance. The hold capacitor is also a compensation element for the S/H and should not be reduced below 2nf for good stability. The offset error in sample mode is not affected by the hold capacitor. However, during the transition to hold mode there is approximately 5pC of charge injected into the hold capacitor, causing an offset error that has been nulled for use with a 5nf hold capacitor. Any other value for the hold capacitor will cause a minor but fixed hold mode offset to be introduced, and is proportional to the change in value from 5nf. Therefore, the SDM should be offset nulled with the S/H in hold mode.

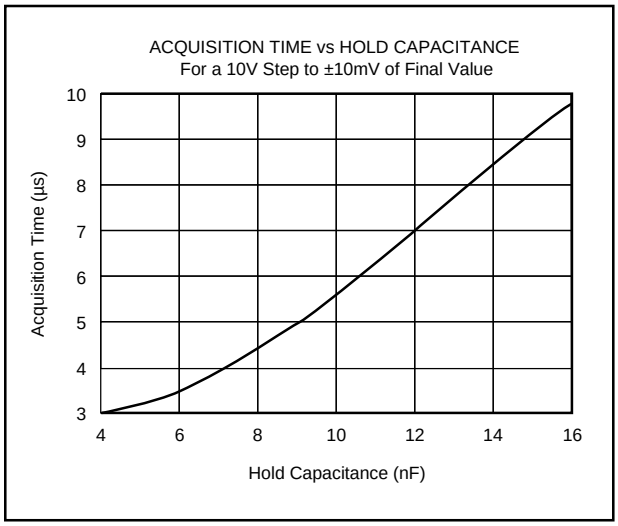


FIGURE 8. Acquisition Time vs Hold Capacitance for a 10V Step Settling to ±10mV of Final Value.

ANALOG-TO-DIGITAL CONVERTER

This circuit element converts the analog voltage presented by the sample/hold amplifier to a digital number in binary format under control of the digital signals detailed in Figure 9. The converter can convert unipolar and bipolar signals in the range 10V and 20V. It can be calibrated to remove gain and offset errors from the entire system. The converter contains its own clock, voltage reference, and microprocessor interface with 3-state outputs. The converter will normally be used to digitize signals to 12-bit resolution, but it can be short-cycled to provide 8-bit resolution at higher speed. The digital output is compatible with 8- or 16-bit data buses, the data format being selected by control signals as detailed in Figure 9.

CE	$\overline{CS}$	R/$\overline{C}$	DATA MODE	BYTE SELECT	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
^	0	0	X	0	Initiate 12-bit conversion
^	0	0	X	1	Initiate 8-bit conversion
1	v	0	X	0	Initiate 12-bit conversion
1	v	0	X	1	Initiate 8-bit conversion
1	0	v	X	0	Initiate 12-bit conversion
1	0	v	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

FIGURE 9. Control Input Truth Table.

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure). Thus, with the SDM connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of –10V is 2.44mV

below the first code transition (000_H to 001_H at –9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Figure 13).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of –1LSB), a missing code will occur.

The SDM is guaranteed to have no missing codes to 12-bit resolution over it's respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An SDM connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The SDM specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition 7FFH to 800H.

Bipolar offset error for the SDM is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full-scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

OPERATING INSTRUCTIONS

OPERATING MODES

The SDM can operate in one of two modes, namely serial and overlap, as shown in Figure 10. In serial mode, control of the device is such that a multiplexer channel X is first selected, time is then allowed for the instrumentation amplifier to settle, the sample/hold amplifier is set to HOLD mode and finally a conversion is carried out. This procedure is then repeated for channel Y. Faster throughput can be obtained using overlap mode. While a conversion is being

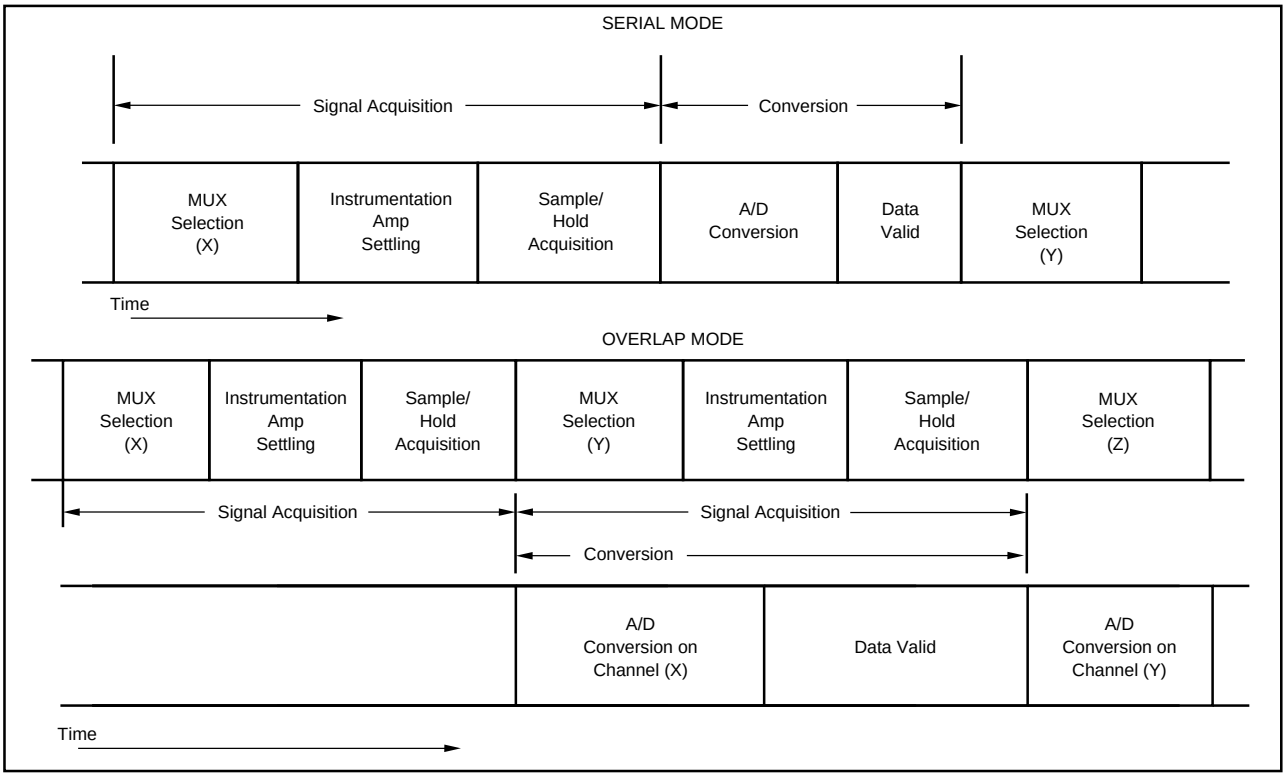


FIGURE 10. Serial and Overlap Modes of Operation.

carried out by the ADC on a voltage from channel X held on the sample/hold, channel Y is selected and the multiplexer and instrumentation amplifier allowed to settle. In this way, the total throughput time is limited only by the sum of the sample/hold acquisition time and the ADC conversion time.

CALIBRATION – UNIPOLAR

If adjustment of unipolar offset and gain are not required, then the gain set potentiometer in Figure 11 (Unipolar operation) may be replaced with a 50Ω, 1% metal film resistor, and the offset network replaced with a connection from pin 23 to ground.

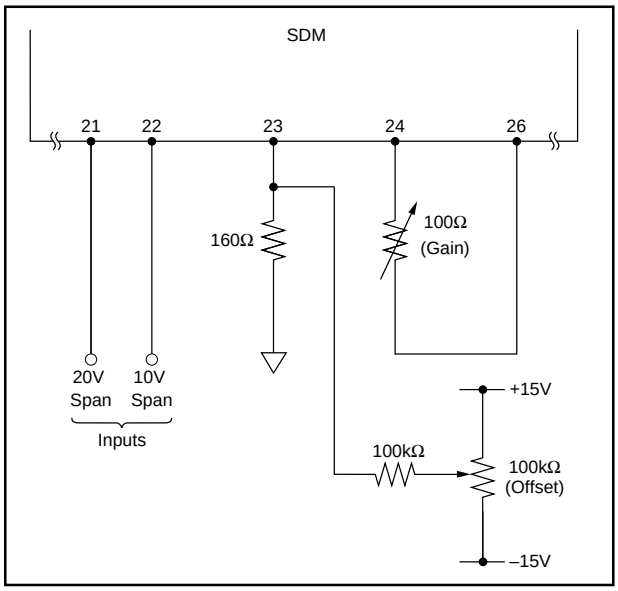


FIGURE 11. Unipolar Calibration.

CALIBRATION - BIPOLAR

If adjustment of bipolar offset and gain are not required then the gain set and offset potentiometers in Figure 12 (Bipolar operation) may both be replaced with 50Ω, 1% metal film resistors.

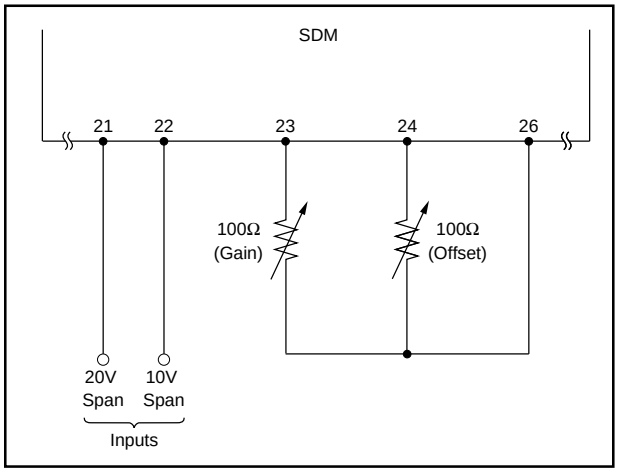


FIGURE 12. Bipolar Calibration.

CALIBRATION - GENERAL

The input voltage ranges of the ADC are 0-10V, ±5V and ±10V. Calibration in all ranges is achieved by adjusting the offset and gain potentiometers (indicated in Figures 11 and 12) such that the 000 to 001 code transition takes place at +1/2LSB from full-scale negative (–FS) and the FFE to FFF transition takes place at –3/2LSB from full-scale positive (+FS). The procedure is therefore to select the required range from Figure 13, apply the specified (–FS+1/2LSB) voltage to any selected input channel and adjust the offset potentiometer for the 000 to 001 transition. The (+FS–3/2LSB) voltage should then be applied to the same channel and the gain potentiometer adjusted for the FFE to FFF transition. The offset should always be made before the gain adjustment.

FULL-SCALE RANGE	000 TO 001 TRANSITION VOLT.	FFE TO FFF TRANSITION VOLT.	1LSB EQUALS
0–10V	+0.0012V	+9.9963V	2.44mV
±5V	–4.9988V	+4.9963V	2.44mV
±10V	–9.9976V	+9.9927V	4.88mV

FIGURE 13. Code Transition Ranges.

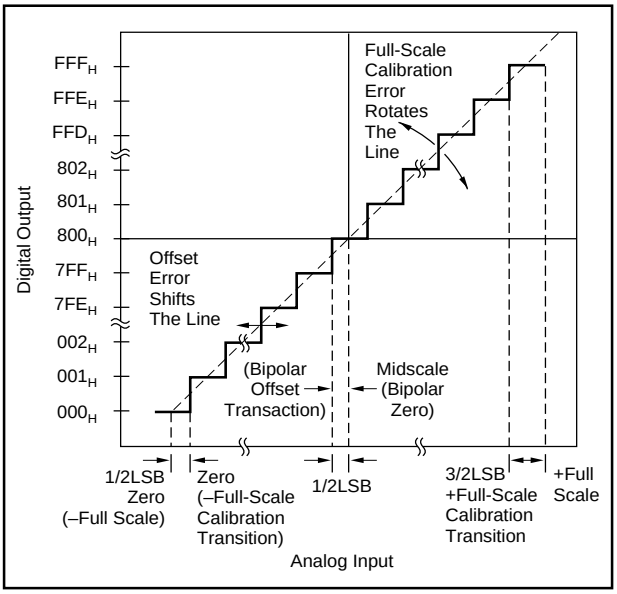


FIGURE 14. SDM Transfer Characteristic Terminology.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

It should be noted that the multiplexer/instrumentation amplifier section and sample/hold plus ADC section of the SDM have separate power connections. This is to enable more flexible grounding techniques to be implemented, Figures 15, 16. It also facilitates the use of independent decoupling of the analog front-end power supply, and the ADC plus associated digital circuitry power supply if desired. In this way, a separately decoupled analog front-end can be made to be substantially more immune to power supply noise generated by the ADC circuitry than if the

power supplies to the two sections were directly connected. This feature is important where low-level signals are in use or high input signal noise immunity is desired.

The output section has three grounds:

Pin 25 Analog Common, A/D Converter
Pin 34 S/H Amp Digital Input Reference
Pin 19 Digital Common, A/D Converter

The input section has one ground:

Pin 53 Common for digital MUX-inputs and power supply decoupling.

All grounds have to be interconnected externally to the SDM, and it is recommended that all grounds are connected via one track to a single point as close as possible to the SDM. To check that the grounding structure is correct, the ground tracking should be sketched and a grounding "tree" should result whereby all grounds route to a central point.

In general, layout should be such that analog and digital tracks are separated as much as possible with coupling between analog and digital lines minimized by careful lay-out. For instance, if the lines must cross they should do so at right angles to each other. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

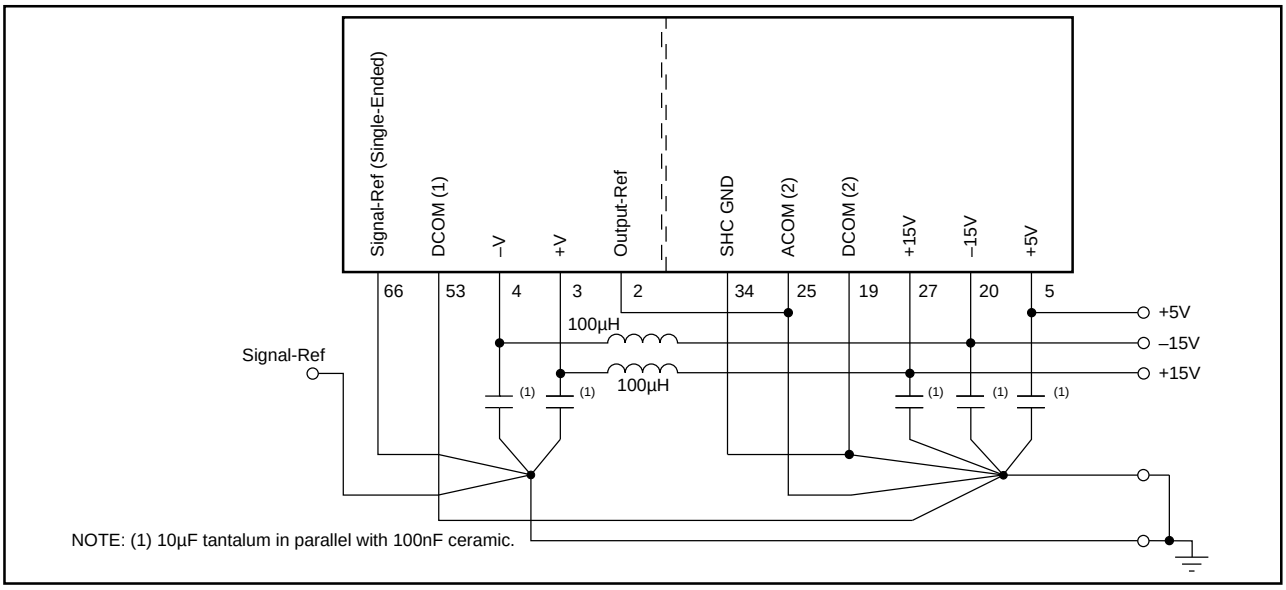


FIGURE 15. Recommended Decoupling of Power Supplies.

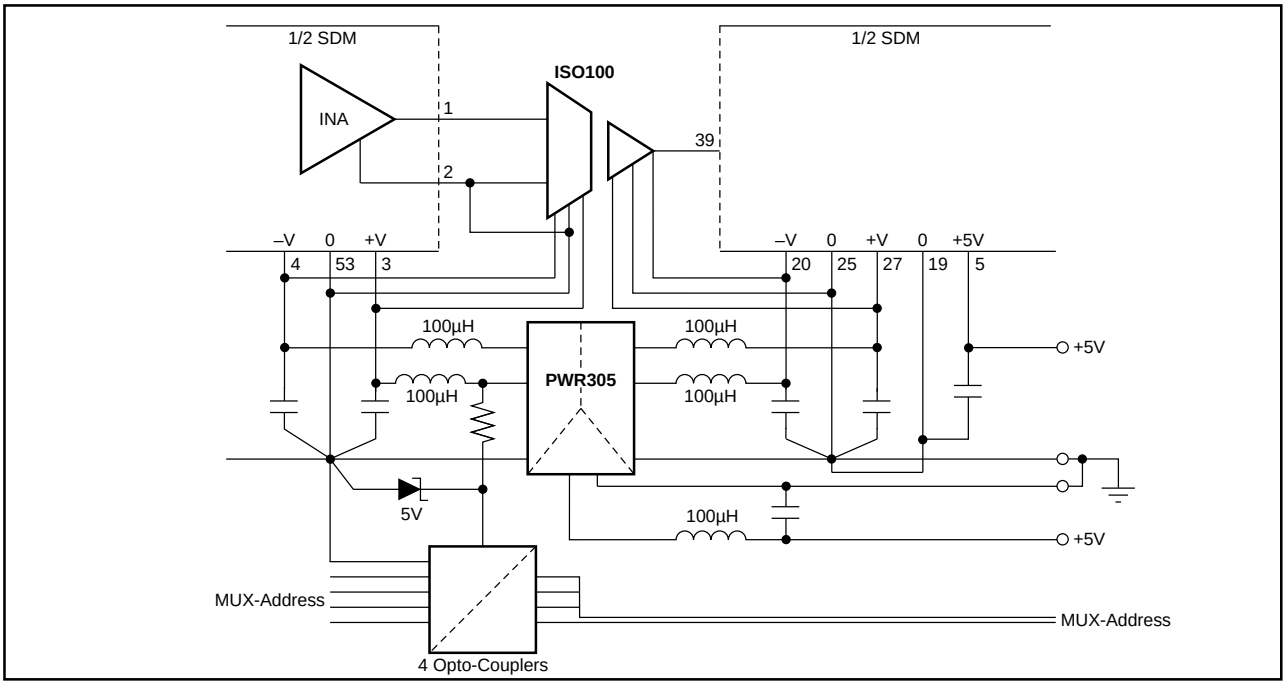


FIGURE 16. Galvanic Isolation Between Analog and Digital Signals.

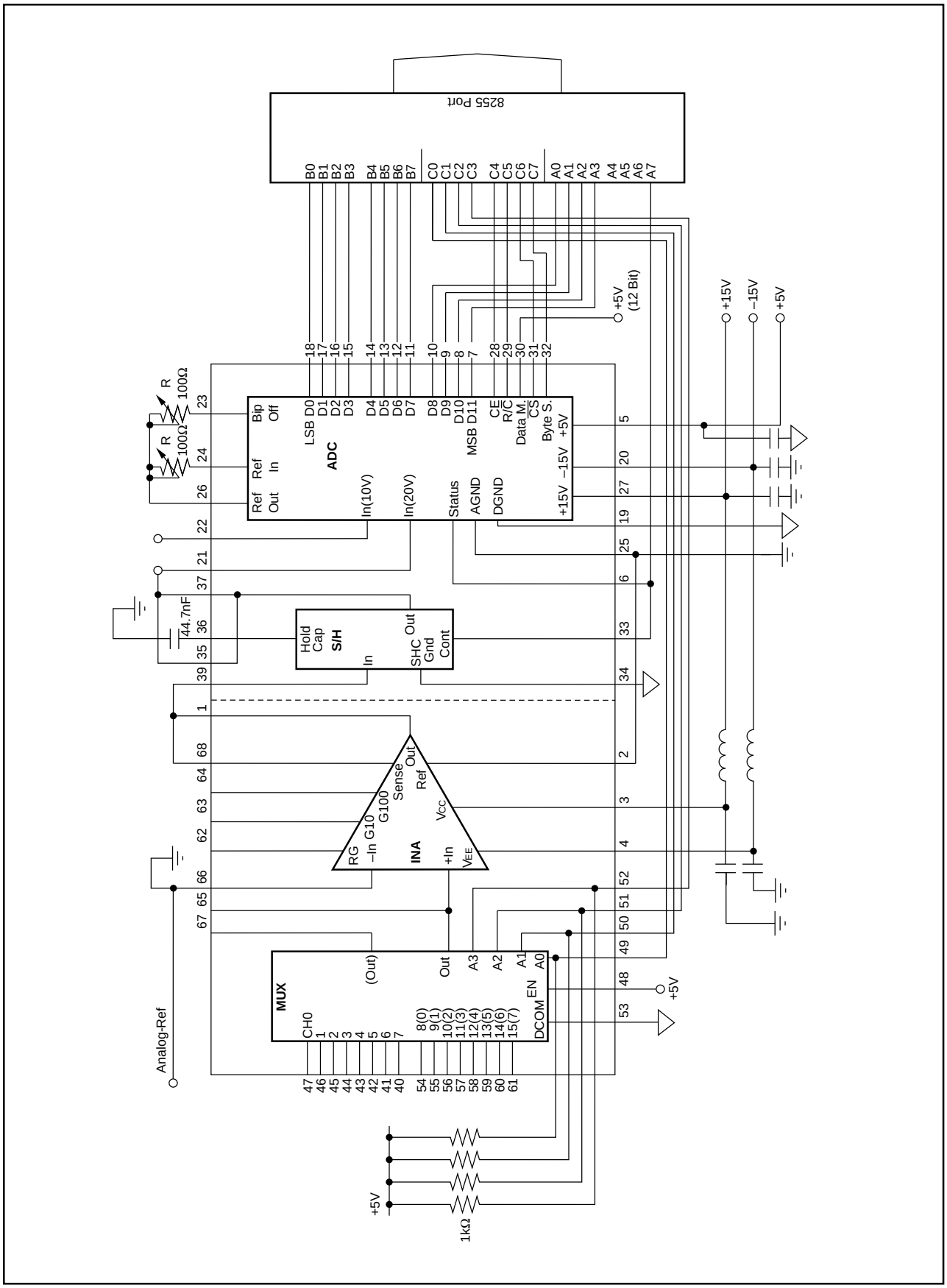


FIGURE 17. The SDM Connected to an Input/Output Port.

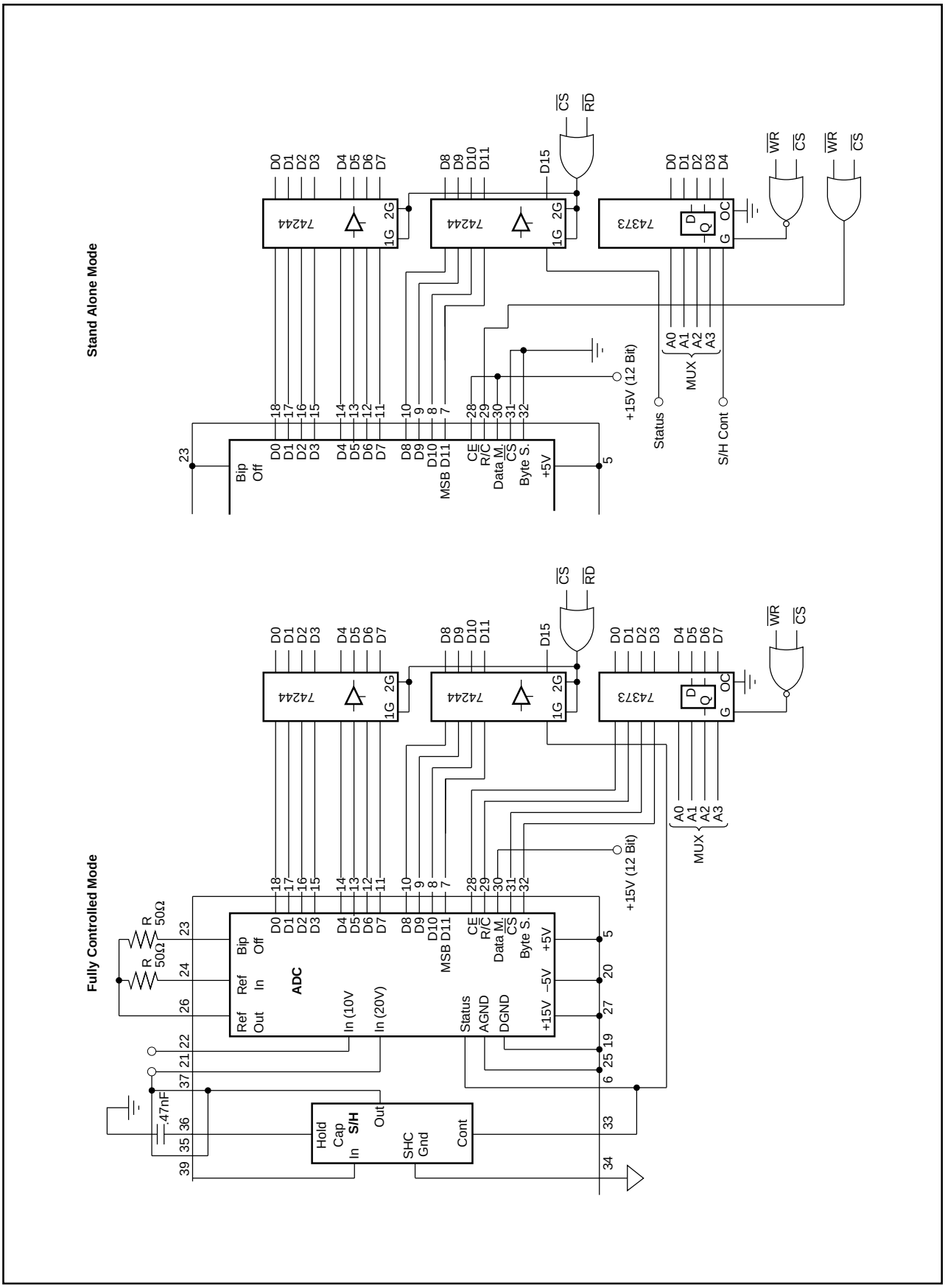


FIGURE 18. The SDM Connected to a 16-Bit-BUS.

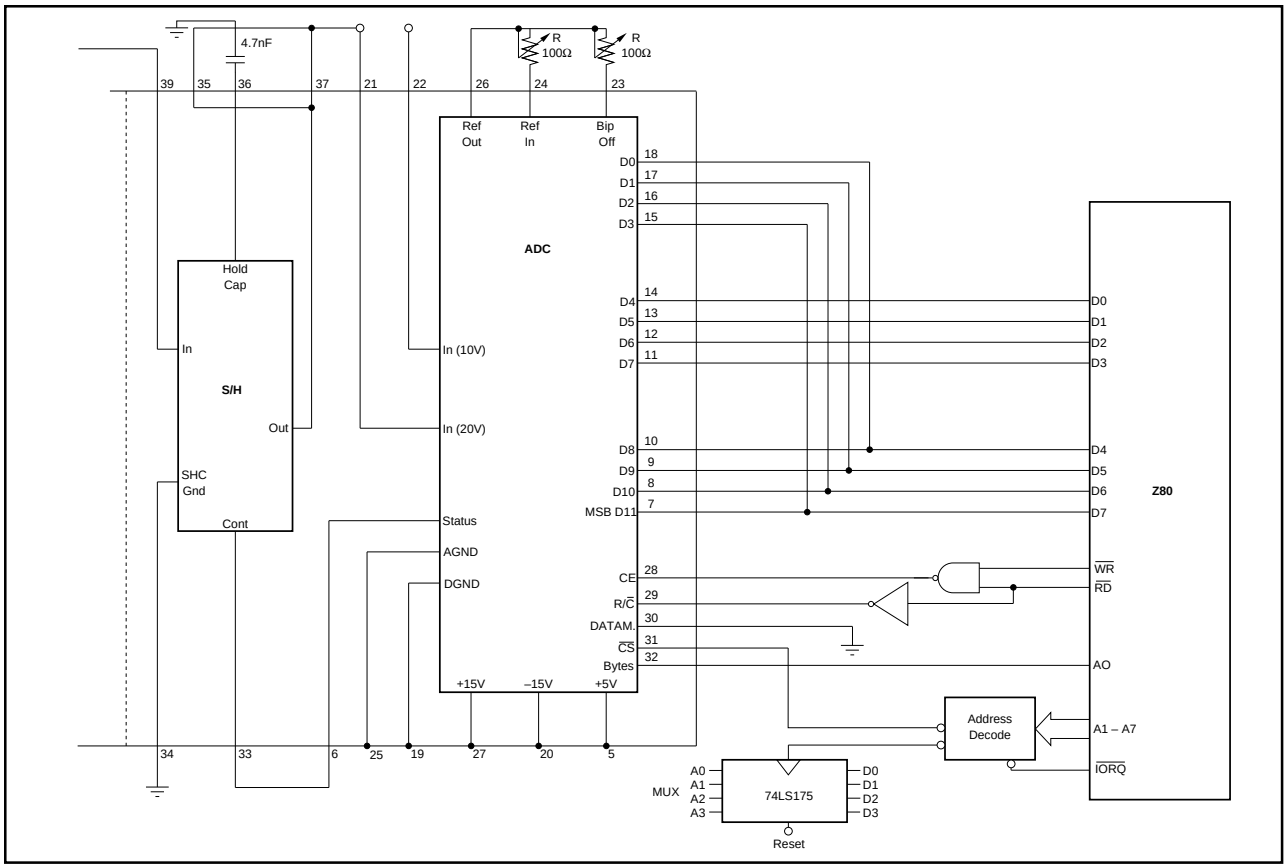


FIGURE 19a. SDM on the Z80 Interface.

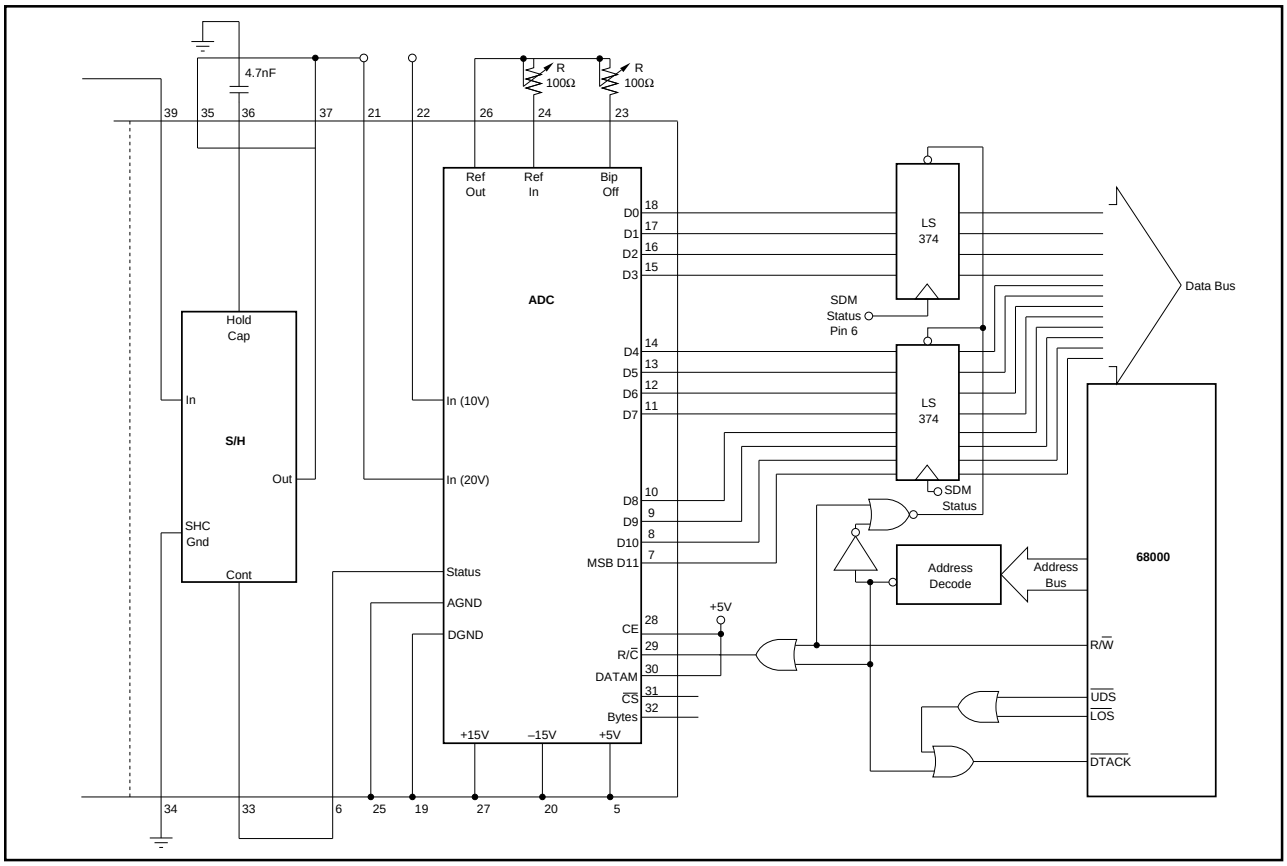


FIGURE 19b. 68000/SDM Interface.

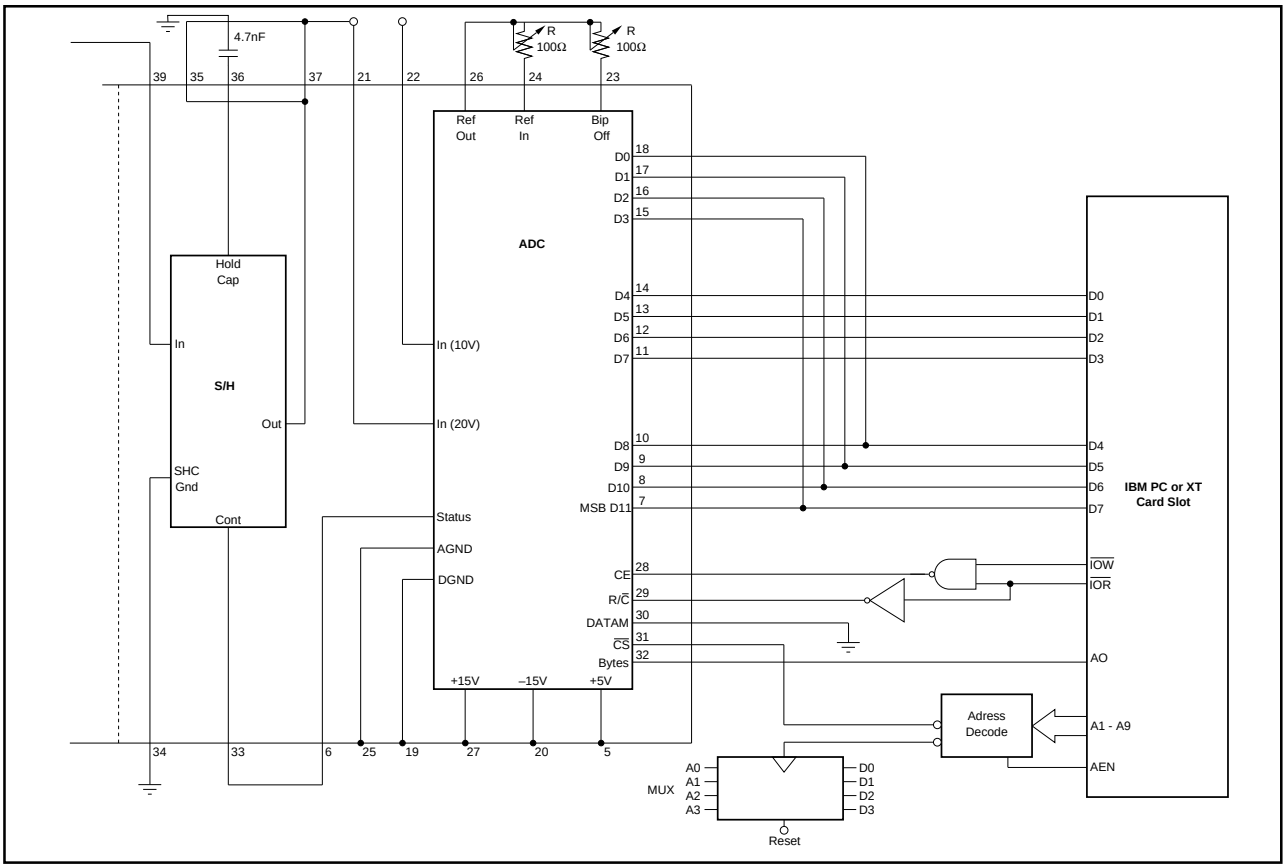


FIGURE 19c. IBM PC SDM Interface.

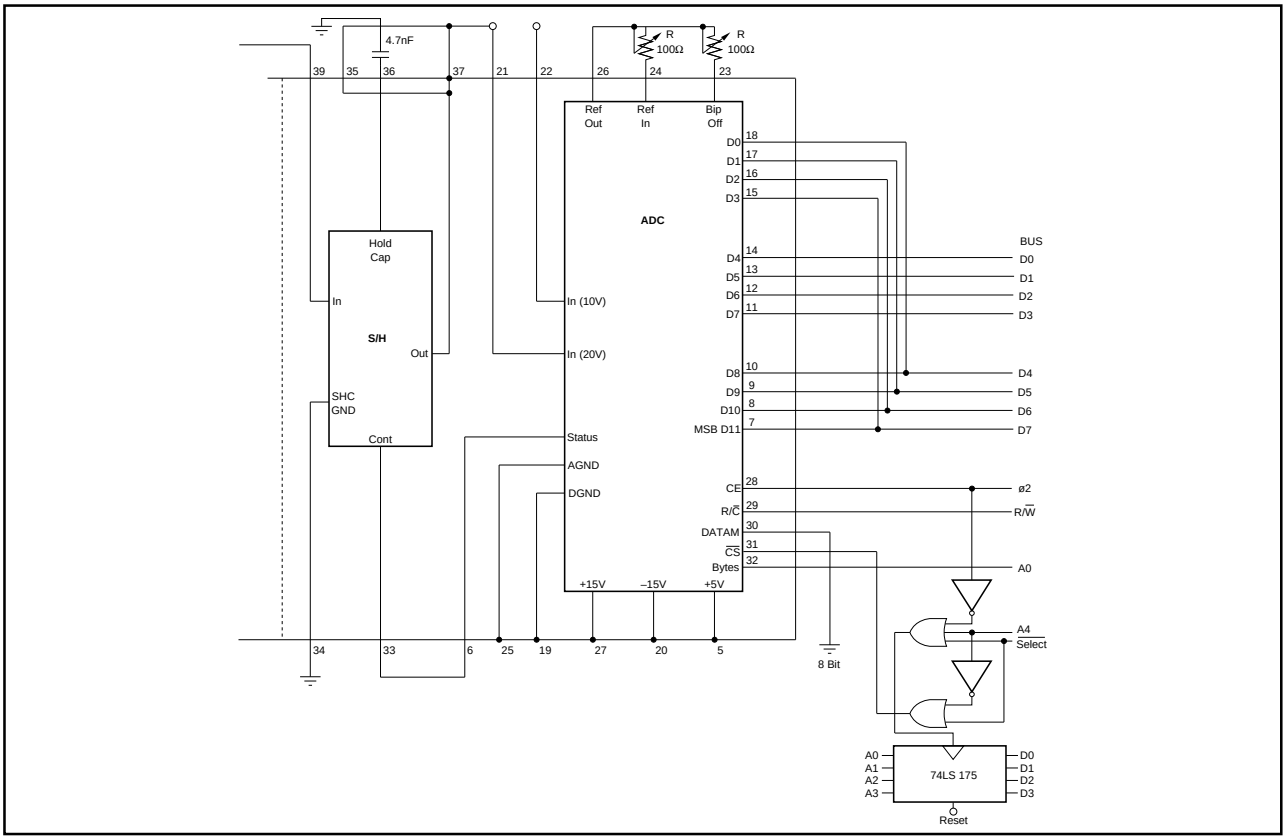


FIGURE 20. SDM on the 6502 BUS.

CONTROLLING THE SDM

The Burr-Brown SDM family can be easily interfaced to most microprocessor systems, as shown in Figures 17-20. The microprocessor may control each conversion, or the converter may operate in a stand-alone mode controlled only by the R/$\overline{C}$ input.

STAND-ALONE OPERATION

The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and BYTE SELECT are connected to LOW and CE and DATA MODE are connected to HIGH. The output data are presented as 12-bit words.

Conversion is initiated by a High-to-Low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In each case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 21 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 22 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Table I lists timing specifications for stand-alone operation.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS} 86X	STS Delay After Data Valid	300	500	1000	ns
t_{HS} 87X		100	300	600	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE I. Stand-Alone Mode Timing.

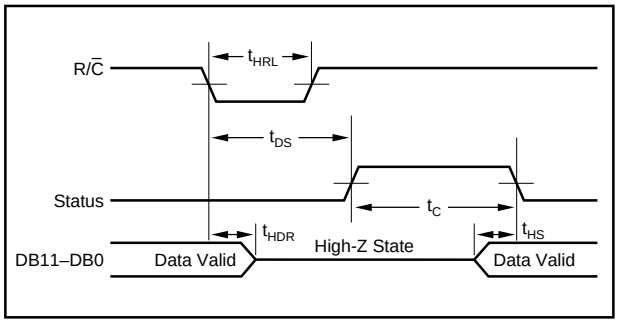


FIGURE 21. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

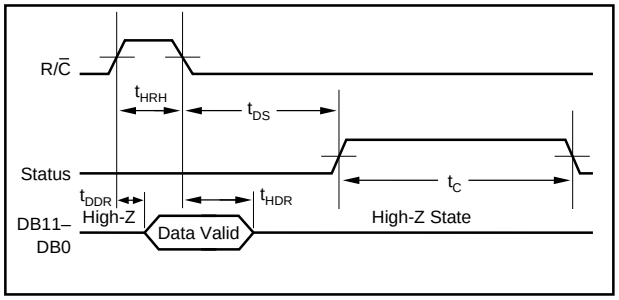


FIGURE 22. R/$\overline{C}$ Pulse High—Outputs Enabled Only Where R/$\overline{C}$ is High.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the BYTE SELECT input, which is latched upon receipt of a conversion start transition. BYTE SELECT is latched because it is also involved in enabling the output buffers. No other control inputs are latched. If BYTE SELECT is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if BYTE SELECT is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0-DB2) will be low (logic 0) and DB3 will be high (logic 1).

Conversion Start

A conversion is initiated by a transition on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$)—refer to Figure 9. The last of the three to reach the required state start the conversion and thus all three may be dynamically controlled. If necessary, they may change state simultaneously, and the nominal delay time is independent of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Conversion Cycle Timing of the Digital Specifications.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SDM	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 23. 12-Bit Data Format for 8-Bit Systems (connected as Figures 18 and 19).

The STATUS output indicates the state of the converter by being high only during a conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore, data is not valid. During this period additional transitions of the three control inputs will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if BYTE SELECT changes state after the beginning of conversion, any additional start conversion transition will latch the new state of BYTE SELECT, possibly resulting in an incorrect conversion length (8 bit versus 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four conditions are met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. In this condition the data lines are enabled according to the state of the inputs DATA MODE and BYTE SELECT. See Read Cycle Timing for timing relationships and specification.

In most applications the DATA MODE input will be hardwired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When DATA MODE is high, all 12 outputs lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus and the state of the BYTE SELECT is ignored.

When DATA MODE is low, the data is presented in the form of two 8-bit bytes, with selection of each byte by the state of BYTE SELECT during the read cycle.

The BYTE SELECT input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When BYTE SELECT is low, the byte addressed contains the 8MSBs. When BYTE SELECT is high, the byte addressed contains the 4LSBs from the conversion followed by four zeros that have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 23. The design of the SDM guarantees that the BYTE SELECT input may be toggled at any time without damage to the output buffers occurring.

In the majority of applications, the read operation will be attempted only after the conversion is complete and the status output has gone low. In those situations requiring the fastest possible access to the data, the read may be started as much as (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Read Cycle Timing for these timing relationships.

APPLICATIONS INFORMATION

ASSEMBLY OF SURFACE MOUNT PACKAGES

There are several assembly methods for the LCC versions of the SDM8XX. The associated advantages and disadvantages of three methods are outlined below.

1. DIRECT SURFACE MOUNT ONTO PCB

ADVANTAGES	DISADVANTAGES
Ease of assembly Low cost Low weight Small footprint size	Difficult to inspect solder joints Difficult to clean Choice of board material important in wide temperature range applications

In wide temperature applications it is important to match the coefficients of thermal expansion of the board and the SDM8XXL. Below is a list of materials and their approximate coefficients of linear thermal expansion.

MATERIAL	(ppm/°C)
Alumina (96%) - SDM Package	6-7
Copper-clad-Invar (50% Cu)	9
(30% Cu)	6
(10% Cu)	3
Epoxy-Kevlar (60% Kevlar)	6
Polyimide-Kevlar (40% Kevlar)	6
Beryllia	5
Polyimide-glass (x-axis)	12
(y-axis)	14

Kevlar™ E.I. du Pont de Nemours & Co.

2. ATTACHMENT OF SURFACE MOUNT EDGE CLIPS

ADVANTAGES	DISADVANTAGES
Ease of Inspection Easy cleaning Thermal expansion taken up by the flexing of the edge clips	Extra cost Extra assembly

ASSEMBLY

The edge clips are attached to the edges of the SDM8XXL as in Figure 24 before the device is mounted on to the board.

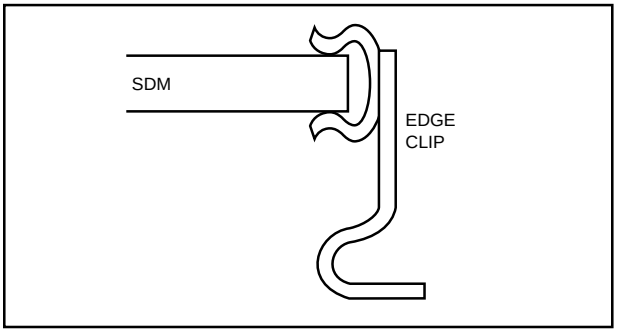


FIGURE 24. Edge Clip Assembly.

SUPPLIERS OF EDGE CLIPS

USA	USA
DIE-TECH INC., R.D. 1, Sipe Road, York Haven, PA 17370 USA PHONE: (717) 938-6771	NAS Electronics, 381 Park St., Hackensack, NJ 07602 USA PHONE: (201) 343-3156
EUROPE	**EUROPE**
SEMI-DICE (UK) Ltd, Buckingham House, Mineral Lane, Chesham, Bucks. HP5 2AU UK PHONE: 0494 771275	NASBRIT Ltd, Wester Goudi Ind. Est. Dundee DD2 4UX UK PHONE: 0382 622222

3. SURFACE MOUNT SOCKET

ADVANTAGES	DISADVANTAGES
Board thermal expansion not so critical Ease of component replacement	Cost Extra height (if critical)

Below is the name and address of a supplier of a 68-pin surface mountable socket.

The part number is: Socket 212-068-012
Spring cover CCS-004

USA	EUROPE
Methode Electronics INC, Interconnect Products Div. 1700 Hick Road, Rolling Meadows, TX 75050 USA PHONE: (312) 392-3500	Lucas Methode Connectors Ltd, Halifax Road Ingrow Bridge, Keighley, Yorkshire BD21 5HR UK PHONE: 0535 603282

General Comments

The advantages and disadvantages of all the methods mentioned above are for general use of surface mount components. Every user will find that the importance of these factors will depend on his application and situation.

EVALUATION BOARD

For the engineer who wishes to evaluate the SDM family, Burr-Brown has designed printed circuit boards on a single 'Eurocard' (shown here for LCC only). These boards enable the design engineer to experiment with various accuracy improvement techniques which are described below. Special consideration has been given to the grounding and circuit layout techniques required when dealing with 12-bit analog signals.

The printed circuit board has been designed so that the solutions to several of the problems likely to be encountered by the user can be examined.

It should not be thought that every user is required to adopt all of the techniques used on the circuit board. In many applications very few external components will be required. However, in following the application guidelines illustrated by the circuitry and accompanying notes, the designer will be able to select and adapt the solutions most suited to their won particular application or problem area.

Provisions for the following are made on the LCC PC board:

—68 pin LCC socket (Burr-Brown Part No. MC0068).
—8 differential or 16 single-ended inputs.
—Input filtering with overvoltage protection for each channel.
—Socket for quad D-type flip-flop 74175 (MUX address latches).
—7 additional I.C. sockets for easy interfacing to various BUS systems (connection by wire wrap techniques).
—2 voltage regulators (15V).
—LC power supply decoupling.

The layout pays particular attention to the requirements when operating with precision analog signals. This requires strict separation of the analog and digital areas. Analog and digital commons are totally separated and connected together only at the commons of the supply voltage. All common lines are low resistance and low inductance.

SUPPLY VOLTAGES

In order to avoid coupling between the external supply voltage 15V supplies, 2 voltage regulators (78M15, 79L15) are provided on the PC board. The unregulated supply voltage may vary from ±17V to ±25V.

The MUX/INA section and SHC/ADC section of the SDM have separate supply lines which can be inductively decoupled. This is recommended in order to suppress the high frequency noise which comes from the ADC during conversion.

The power supply rejection of the instrumentation amplifier reduces with increasing frequency. If high frequency noise on the supplies is not decoupled it will be injected into the signal path and cause errors. This effect can be particularly pronounced when using the 'overlap' mode since the instru-

SDM862/872						SDM863/873				
MUX ADD3	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Selected	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Pair Selected
X	X	X	X	L	NONE	X	X	X	L	NONE
L	L	L	L	H	0	L	L	L	H	0
L	L	L	H	H	1	L	L	H	H	1
L	L	H	L	H	2	L	H	L	H	2
L	L	H	H	H	3	L	H	H	H	3
L	H	L	L	H	4	H	L	L	H	4
L	H	L	H	H	5	H	L	H	H	5
L	H	H	L	H	6	H	H	L	H	6
L	H	H	H	H	7	H	H	H	H	7
H	L	L	L	H	8			–		
H	L	L	H	H	9			–		
H	L	H	L	H	10			–		
H	L	H	H	H	11			–		
H	H	L	L	H	12			–		
H	H	L	H	H	13			–		
H	H	H	L	H	14			–		
H	H	H	H	H	15			–		

FIGURE 25. Channel Select Truth Table.

mentation amplifier is settling to a new analog value while the ADC is still carrying out the previous conversion.

The digital supply voltage is +5V and is also LC-filtered.

All supply lines are bypassed with a 10µF tantalum and a 100nF ceramic capacitor situated **as close as possible** to the package.

If the voltage regulators for the ±15V are not used, small inductors for decoupling of the supply voltages are recommended. If inductors are not fitted a dynamic ground loop will be created from supply lines via bypass capacitors to analog common.

INPUT PROTECTION

The multiplexer is protected up to an input voltage which can exceed the supply voltage by a maximum of 20V. This means, that with ±15V supply voltage, the input voltage can be ±35V without damage. This is also the case when the supply voltages are switched off (0V). The maximum input voltage can then be ±20V. For higher overvoltage protection a series resistor has to be used. The current via the multiplexer should be limited to 20mA absolute maximum, 1mA is preferred. For example, a 10kΩ series resistor would give an additional 10V overprotection.

For much higher overvoltages (e.g. 100V), high value series resistors cannot be used as offset errors would result. In practice, a combination of series resistors and diodes is used. The diodes are connected to ±15V and will conduct whenever the input voltage exceeds the ±15V supply voltage. The diodes are selected by signal source impedance, as well as filter resistance, as the diode leakage current across the series resistor can cause offset and linearity errors. In this circuit, IN4148 together with 10kΩ are used.

INPUT FILTER

Processor noise can be induced in the analog ground. Input filtering is therefore recommended for analog data acquisition. Such high frequency noise signals can cause dynamic overload of the instrumentation amplifier resulting in nonlinear behavior. This leads directly to digitizing errors.

The design of the filter takes into account the characteristics of the SDM and of the signal source.

The following points have to be considered:

—The stray capacitance, output capacitance of the multiplexer and input capacitance of the instrument amplifier (up to 80pf in some cases) has to be discharged in order to minimize errors caused by ‘charge sharing.’

—The series resistor limits the current in the protection diodes, but it also has to be selected for the required filter time constant.

—The noise rejection of the filter has to be >80db in order to satisfy a 12-bit A/D conversion.

As well as considering the above, different calculations have to be carried out for single and differential input signals.

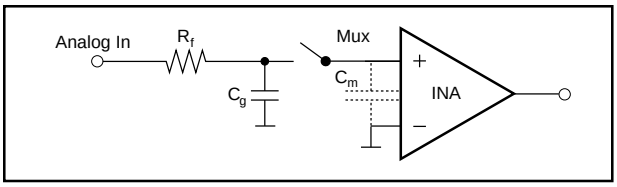


FIGURE 26.

Single-Ended Measurement

R_f limits the maximum input current through the protection diodes. In this case, R_f has been chosen as 10kΩ and together with the capacitor C_g, forms the input filter time constant (C_g = 0.47µF). The time constant must be chosen according to the requirements of the input signal bandwidth and noise rejection. The multiplexer capacitance (C_m) is discharged mainly by C_g. This means C_g has to be sufficiently large compared with C_m or charged via R_f prior to resampling of the signal.

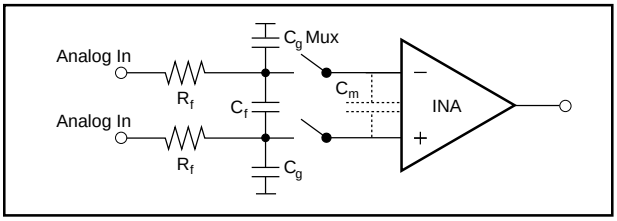


FIGURE 27.

Differential Measurement

Capacitor C_f, is used for limiting the input signal frequency. The bandwidth is calculated as follows:

$$F_f = \frac{1}{4\pi R_f C_f} \quad \text{IF } C_f >> C_g$$

When selecting the value of C_f, it should be noted that C_m has to be discharged when switching the multiplexer channels. This means that the voltage error of C_f (induced by ‘charge sharing’ with C_m) has to be smaller than 1LSB. Therefore, C_f should have a minimum value of a 0.47µF. The resistors R_f, together with the source impedance, have to be sufficiently small in order to recharge C_f prior to signal sampling. This prevents errors in the signal value caused by the charge stored on C_m by the previously selected channel.

The 2 capacitors C_g form together with R_f a common-mode filter. This filter greatly improves accuracy in a noisy environment (decrease of common-mode rejection of instrumentation amplifier with increasing frequency).

For good common-mode filter operation, both time constants R_f and C_g should match each other within 2%. Additional errors will be induced by a mismatch.

Selected values are: C_f = 0.47µF, C_g = 10nF, R_f = 10kΩ. The filter reduces the signal slew rate so that the instrumentation amplifier can follow the voltage variation of the signal with the noise component eliminated.

In general, all measurements which require more than a gain of 10 should be done in differential mode. Single ended

measurements should be limited to applications where current sources are measured via shunts or where signal voltages in the range of some volts are available.

Bus-Interface

As the outputs of the SDM are BUS compatible, only a few ICs are necessary to interface to various BUS systems. For such interfacing, 20-pin IC sockets are provided. Wiring is by wire wrap to the BUS connector.

Setting of Various Modes

Circuit Board positions are provided for the connection of 'jumpers' as follows:

J1, J2—ADC analog input volt age settings.
J3—Set for differential (SDM8X3) or single ended (SMD8X2) operation.
J4—Instrumentation amplifier gain settings.

(a) 16 input channels, single ended:
—Use SDM8X2
—Consider single-ended filtering
—Connect J3 (pin 66) to common

(b) Differential inputs
—Use SDM8X3
—Consider differential filtering
—Connect J3 (pin 66) to pin 67

(c) Analog input

±10V	Connect J1 to pin 21
	Connect J2 to pot P2 (100Ω)
±5V	Connect J1 to pin 22
	Connect J2 to pot P2 (100Ω)
0 to +10V:	Connect J1 to pin 22
	Connect J2 to junction of R_1/R_2

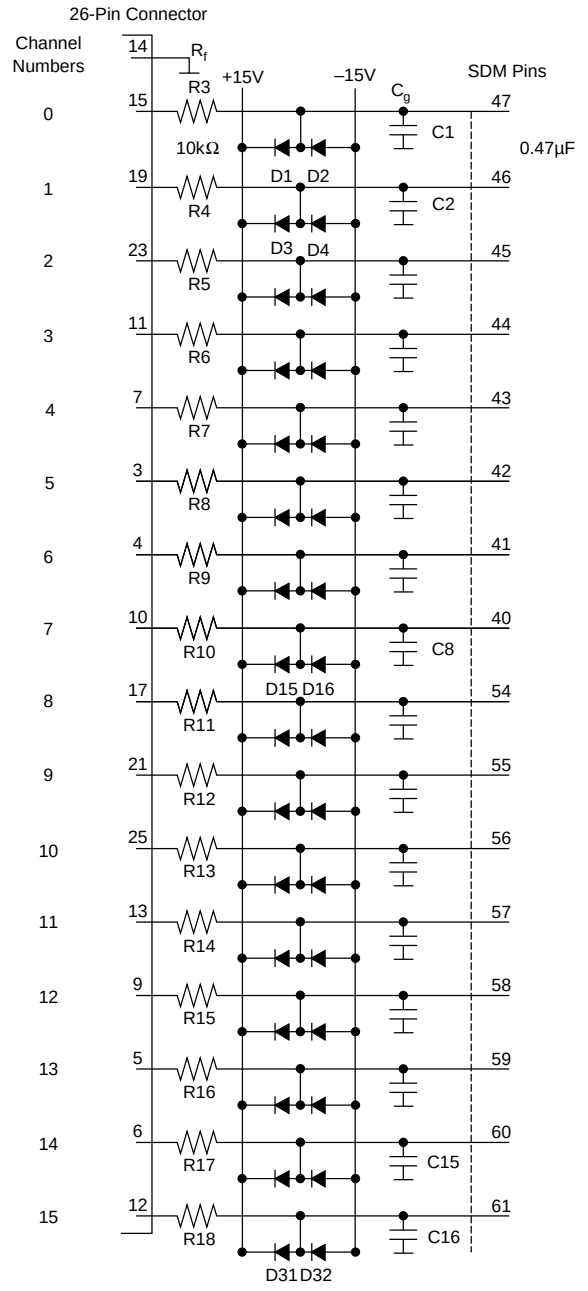
(d) Gain of instrumentation amplifier

G = 1	Jumper J4 open
G = 10	Jumper J4 to pin 63
G = 100	Jumper J4 to pin 64

Other gains: use additional resistor between pin 62 and pin 63 (see section on Instrumentation Amplifier) as low tempco resistor is recommended in order to minimize gain drift.

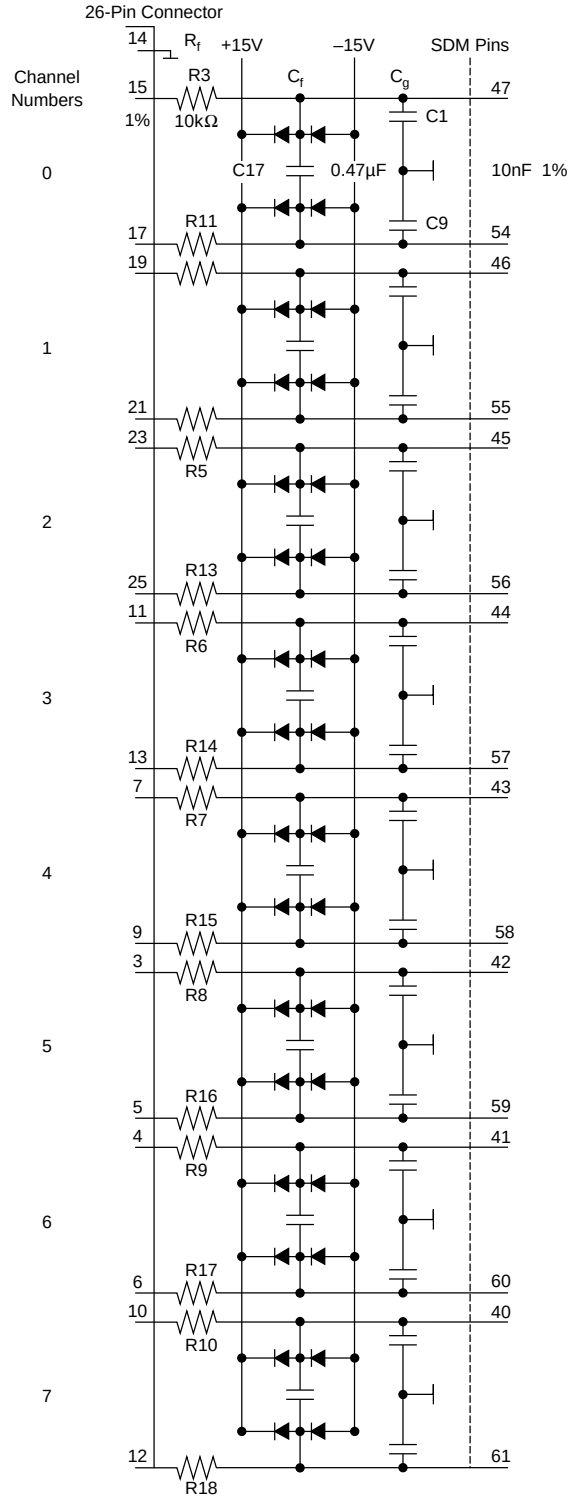
INPUT FILTER AND PROTECTION CIRCUITRY

SINGLE-ENDED



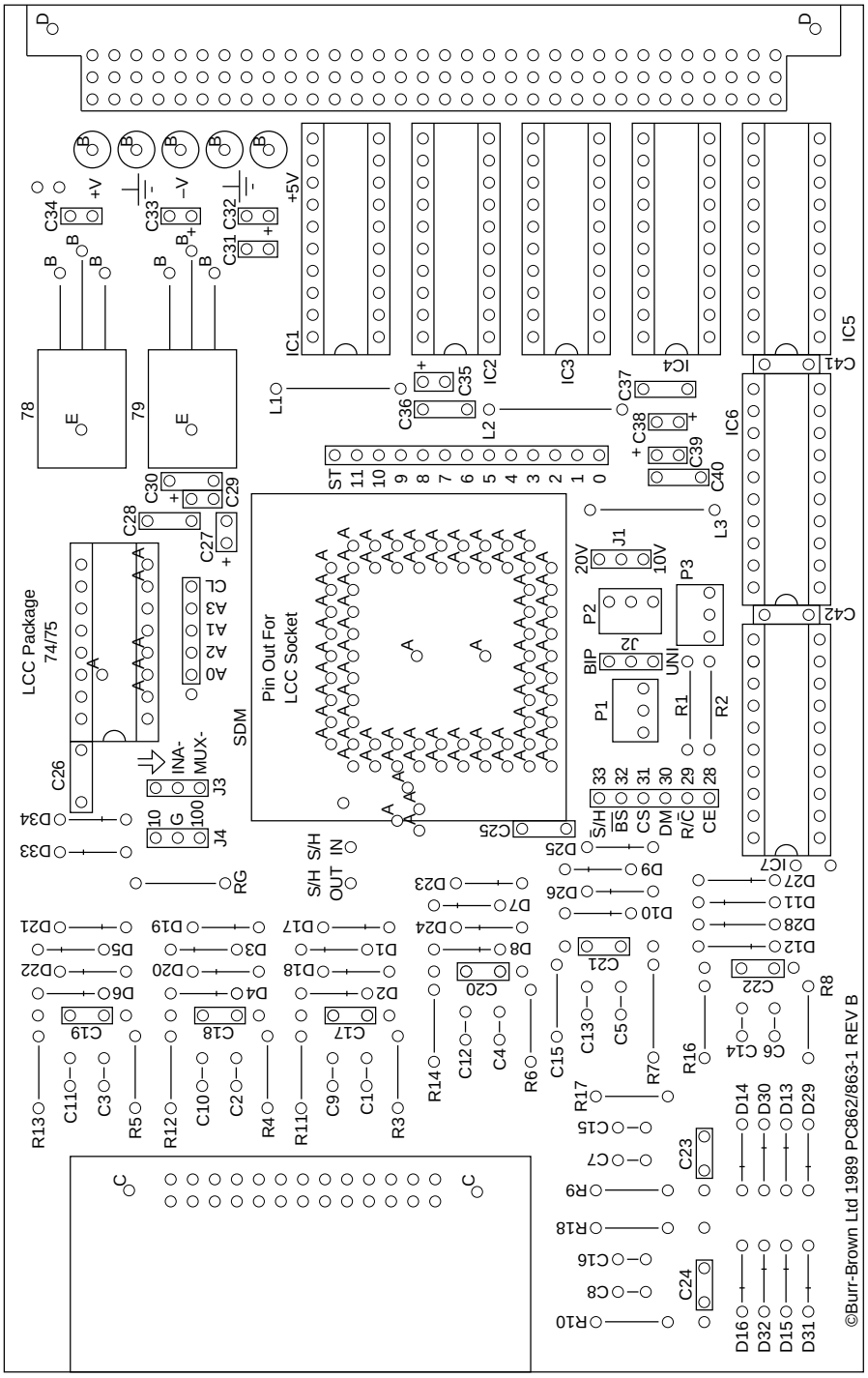
Pins 1, 2, 8, 14, 16, 18, 20, 22, 24 and 26 are Connected to Common

DIFFERENTIAL



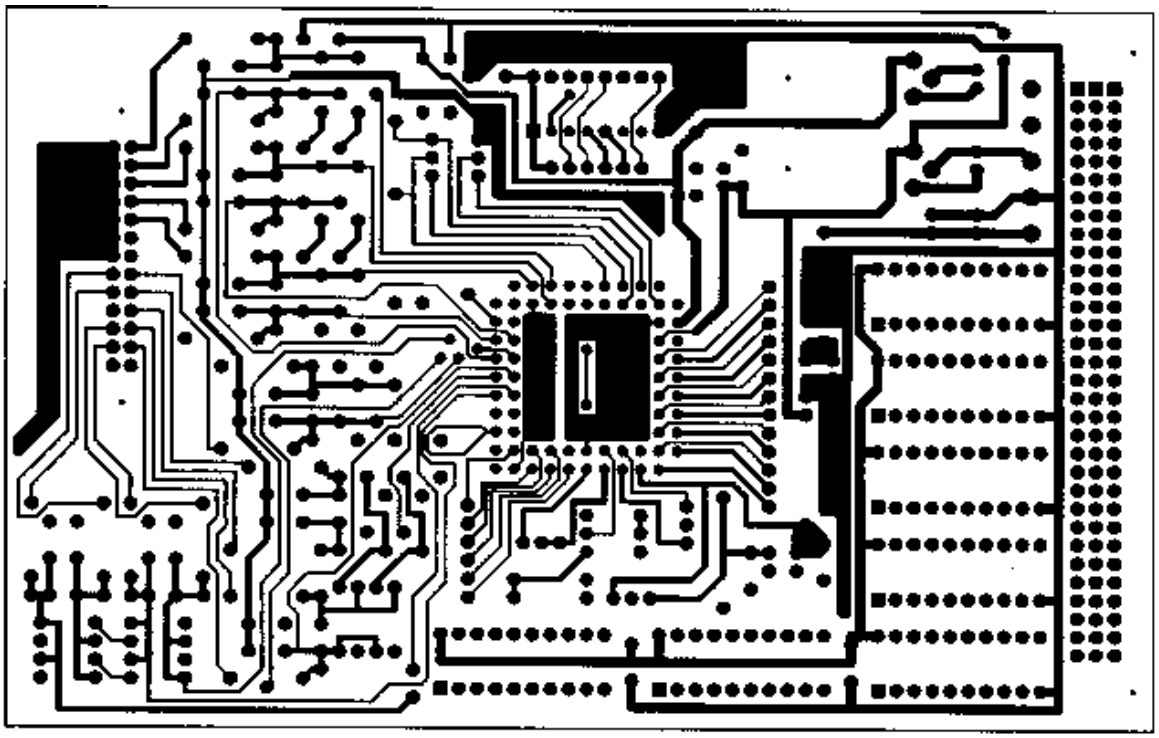
Pins 1, 2, 8, 14, 16, 18, 20, 22, 24 and 26 are Connected to Common

PCB COMPONENT LAYOUT

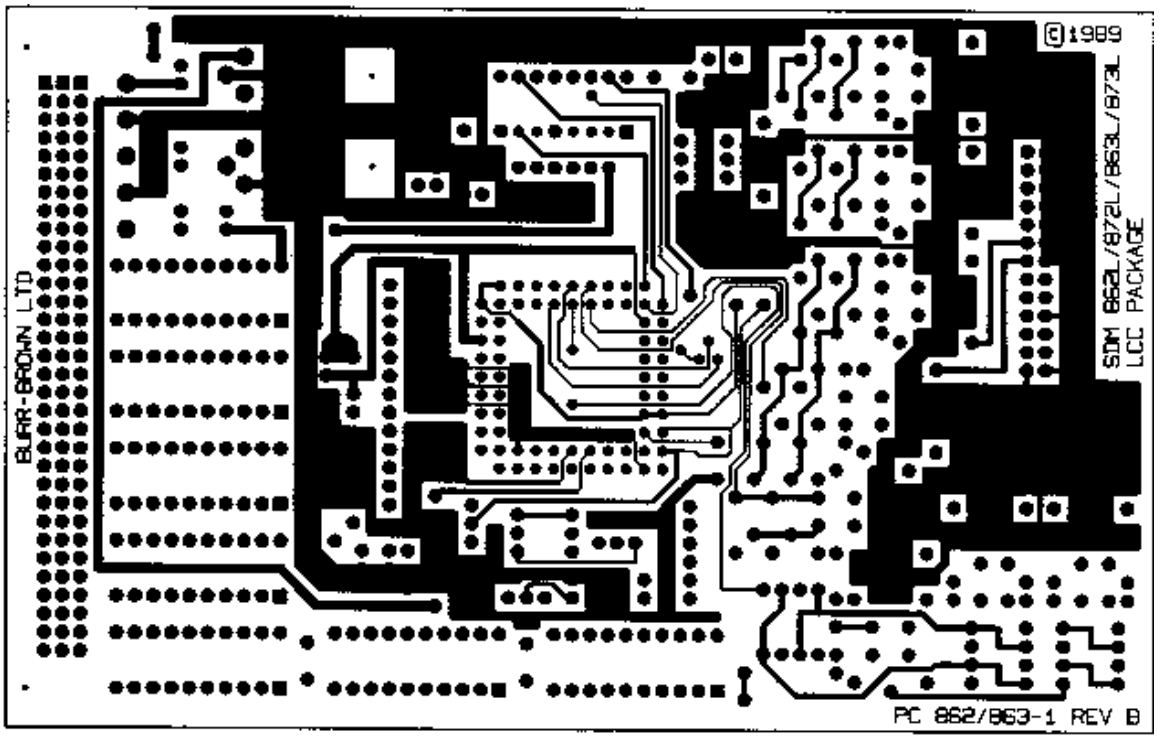


NOTE: (1) NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2
(2) NOT DRAWN TO SCALE

P.C.B. LAYOUT

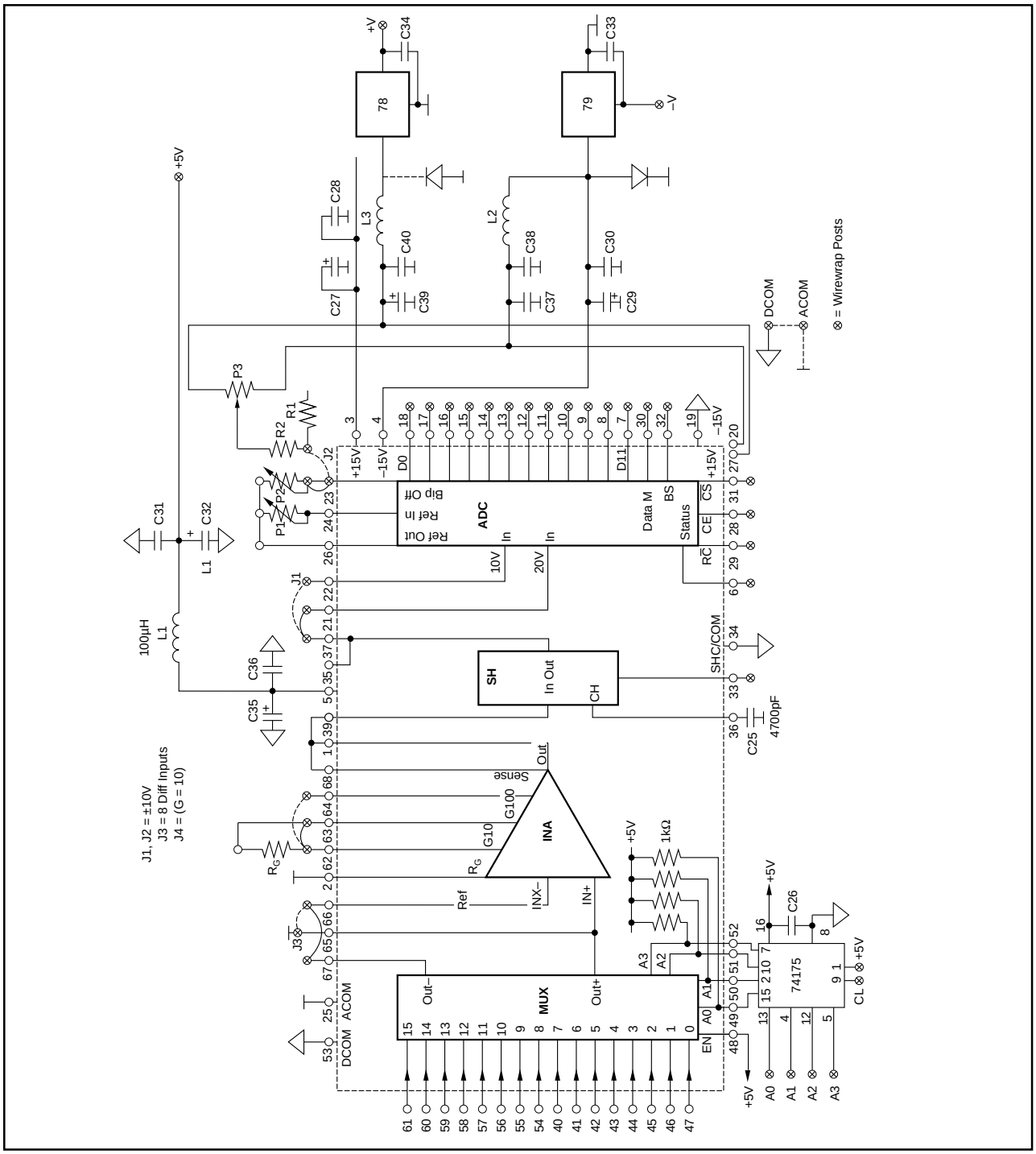


NOTE: NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2



NOTE: NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2

CIRCUIT DIAGRAM—SDM PC BOARD



P.C.B. COMPONENTS PARTS LIST

R1	100Ω } For 0–10V Settling	C26	10nF Ceramic	P3	100kΩ **0–10V Range Only**
R2	100kΩ } For 0–10V Settling	C27, C29, C35 }	10µF Tantalum (Decoupling)	L1...L3	100µH (Decoupling)
R3...R18	10kΩ 1%	C32, C38, C39 }	10µF Tantalum (Decoupling)	D1...D32	1N4148 (Input Protection Diodes)
C1...C16	0.47µF—Single Ended Input Mode	C28, C30, C31 }	100nF Ceramic (Decoupling)	D33, D34	1N4007
	10nF 1%—Differential Input Mode	C36, C37, C40 }	100nF Ceramic (Decoupling)	78	MC78M15CG
C17...C24	0.47µF—Differential Input Mode	C33, C34	0.33µF Tantalum	79	MC79L15CG
C25	4.700pF (Polypropylene, Polystyrene or Teflon™)	P1	100Ω	**74175**	74LS175
		P2	100Ω **±5V, ±10V Range Only**	LCC Socket	MC0068

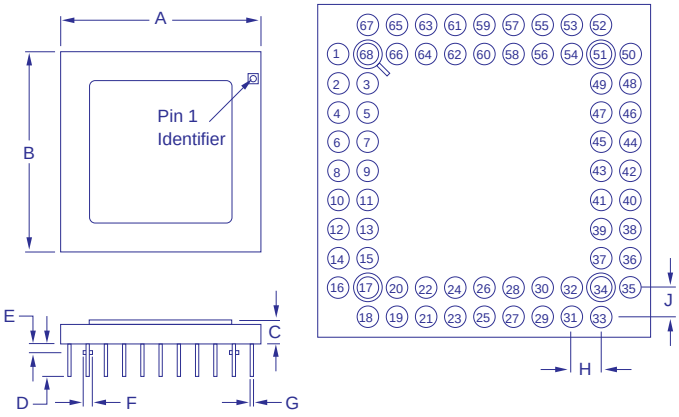
UNLESS OTHERWISE MARKED—RESISTORS ARE 1/4W, 5%, CAPACITORS ARE 10%

Teflon™ E.I. du Pont de Nemours & Co.

MECHANICAL (P.G.A.)

Package Number 906

TOP VIEW **Bottom VIEW**

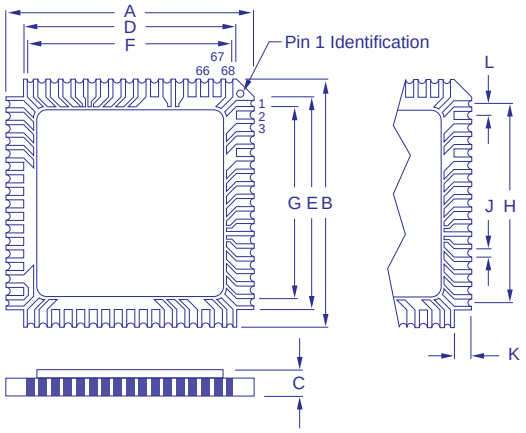


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.087	1.109	27.610	28.169
B	1.087	1.109	27.610	28.169
C	.095	.120	2.413	3.048
D	.162	.198	4.115	5.029
E	.045	.055	1.143	1.397
F	.045	.055	1.143	1.397
G	.016	.020	.406	.508
H	.100 BASIC		2.540 BASIC	
J	.100 BASIC		2.540 BASIC	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.
TERMINATION: Gold plated KOVAR.
CASE: Ceramic with gold plated nickel lid.
HERMETICITY: Gross leak test.
WEIGHT: 9 grms (0.32 oz)

MECHANICAL (L.C.C.)

Package Number 907 — TOP VIEW



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.945	.965	24.003	24.511
B	.945	.965	24.003	24.511
C	.076	.094	1.934	2.388
D	.841	.859	21.361	21.819
E	.841	.859	21.361	21.819
F	.755	.785	19.177	19.939
G	.755	.785	19.177	19.939
H	.800 BASIC		20.320 BASIC	
J	.027	.033	.686	.838
K	.045 BASIC		1.143 BASIC	
L	.050 BASIC		1.270 BASIC	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.
TERMINATION: Gold plated nickel on refractory metallization.
CASE: Ceramic with gold plated nickel lid.
HERMETICITY: Gross leak test.
WEIGHT: 4.37 grms (0.124 oz)