1.5A, Rad Hard, Positive, High Voltage LDO

ISL75052SEH

The ISL75052SEH is a radiation hardened, single output LDO specified for an output current of 1.5A. The device operates from an input voltage range of 4.0V to 13.2V and provides for output voltages of 0.6V to 12.7V. The output is adjustable based on a resistor divider setting. Dropout voltages as low as 75mV (at 0.5A) typical can be realized using the device. This allows the user to improve the system efficiency by lowering V_{IN} to nearly V_{OUT}.

The ENABLE feature allows the part to be placed into a low shutdown current mode of 165µA (typ). When enabled the device operates with a low ground current of 11mA (typ), which provides for operation with Low Quiescent Power consumption.

The device has superior transient response and is designed keeping Single Event Effects in mind. This results in reduction of the magnitude of SET seen on the output. There is no need for additional protection diodes and filters.

COMP pin is provided to enable the use of external compensation. This is achieved by connecting a resistor and capacitor from COMP to ground. The device is stable with Tantalum capacitors as low as 47µF (KEMET T525 series) and provides excellent regulation all the way from no Load to full Load. The programmable soft-start allows one to program the inrush current by means of the decoupling capacitor used on the BYP pin. The OCP pin allows the short circuit output current limit threshold to be programmed by means of a resistor from OCP pin to GND. The OCP setting range is from a 0.16A min to 3.2A max. The resistor sets the constant current threshold for the output under fault conditions. The thermal shutdown disables the output if the device temperature exceeds the specified value, it will subsequently enter a ON/OFF cycle till the fault is removed.

Applications

- LDO regulator for Space Power Systems
- DSP, FPGA and µP Core Power Supplies
- Post Regulation of SMPS and Down Hole Drilling

Features

- **DLA SMD 5962-13220**
- **Input supply range 4.0V to 13.2V.**
- **Output Current up to 1.5A at a T_J = +150°C**
- **Best in class Accuracy ±1.5%**
  - Over line, load and temperature
- **Ultra Low Dropout:**
  - **75mV Dropout (typ) @ 0.5A**
  - **225mV Dropout (typ) @ 1.5A**
- **Noise of 100µV_{RMS} (typ) between 300Hz to 300kHz**
- **SET mitigation with no added filtering/diodes**
- Shutdown Current of 165µA (typ)
- Externally adjustable Output Voltage
- PSRR 65dB (typ) @ 1kHz
- **EN**able and **PG**ood Feature
- Programmable Soft-Start/In-rush Current Limiting
- Adjustable Overcurrent Protection
- Over-Temperature Shutdown
- Stable with 47µF Min Tantalum Capacitor
- Package 16 Ld Flat Pack
- **Radiation Environment**
  - **High Dose Rate (50-300rad(Si)/s) . . . . . 100krad(Si)**
  - **Low Dose Rate (0.01rad(Si)/s). . . . . 100krad(Si)***
  - SET/SEL/SEB 86 MeV.cm2/mg

*Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate.

Related Literature

See AN1850, "ISL75052SEH Evaluation Board User's Guide"

See AN1851, "SEE Testing of the ISL75052SEH"

See AN1852, "Radiation Report of the ISL75052SEH"

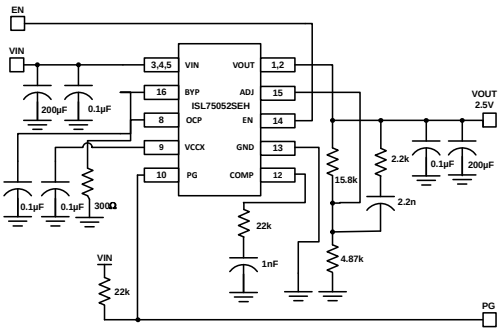

FIGURE 1. TYPICAL APPLICATION

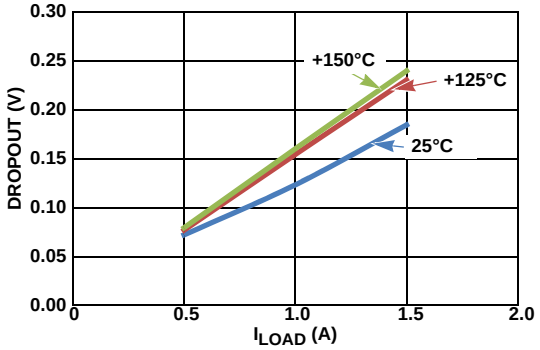

FIGURE 2. DROPOUT vs I_{OUT}

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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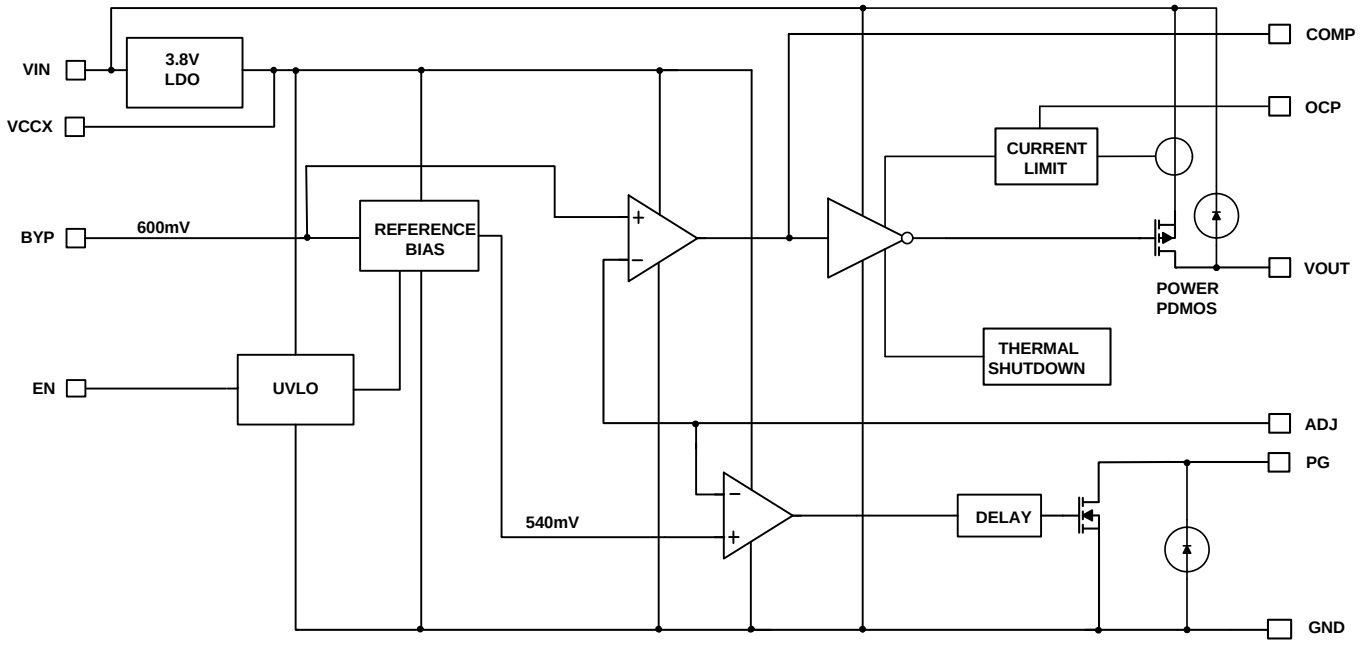
Block Diagram



Typical Applications

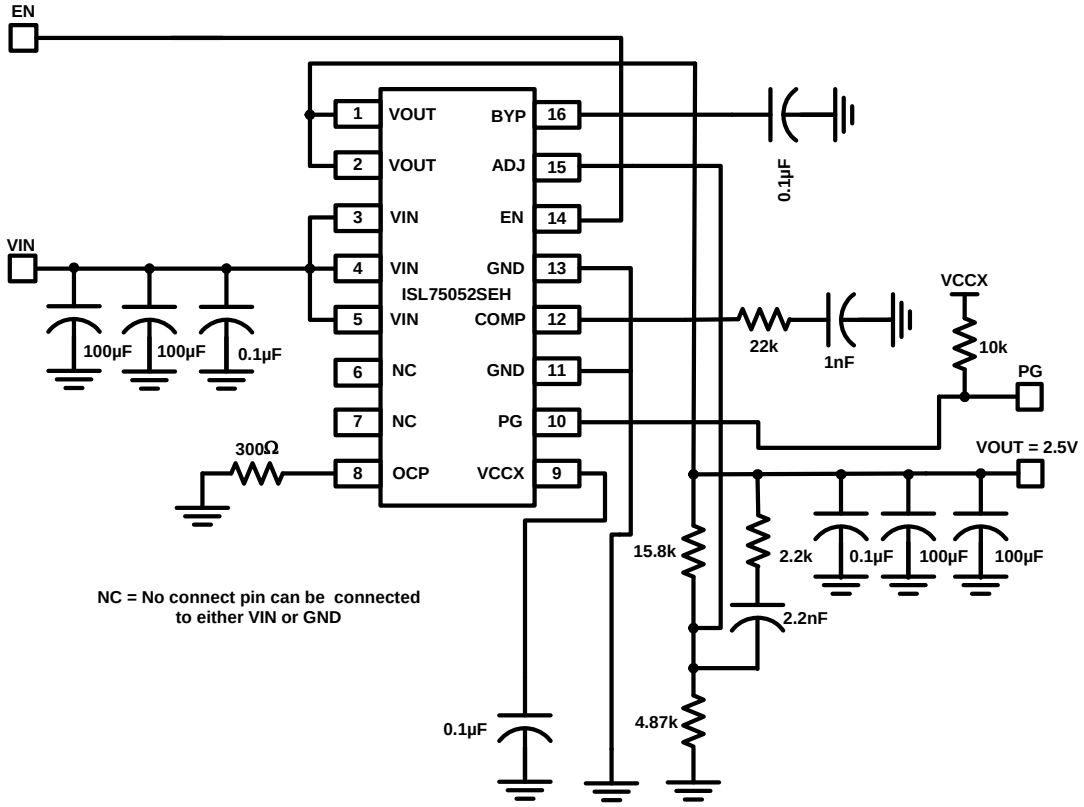
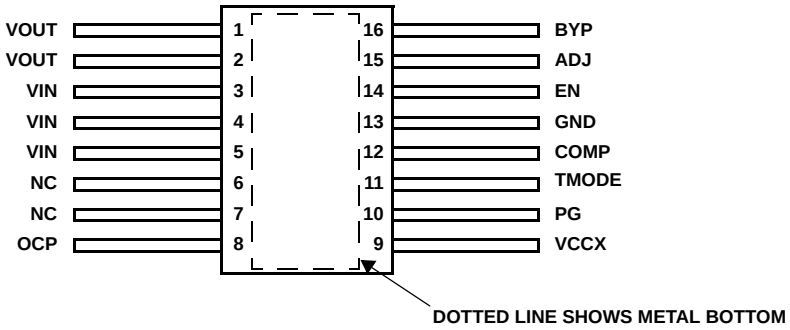


FIGURE 3.

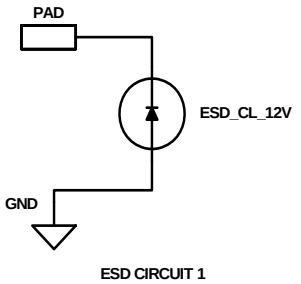
Pin Configuration

ISL75052SEH
(16 Ld CDFP)
TOP VIEW

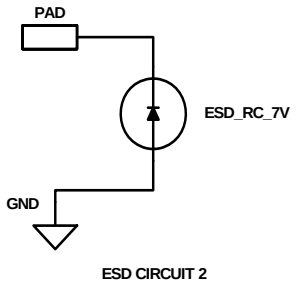


Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION	ESD CIRCUIT
3, 4, 5	VIN	Input supply pins.	Circuit 1
10	PG	This pin is logic high when V_{OUT} is in regulation signal. A logic low defines when V_{OUT} is not in regulation.	Circuit 2
13	GND	GND pin. Pin 13 is also connected to the metal lid of the package.	Circuit 2
9	VCCX	The 3.8V internal bus is pinned out to accept a decoupling capacitor. Connect a 0.1µF ceramic capacitor from VCCX pin to GND.	Circuit 2
1, 2	VOUT	Output voltage pins.	Circuit 1
12	COMP	Add compensation capacitor & resistor between COMP and GND.	Circuit 2
15	ADJ	ADJ pin allows V_{OUT} to be programmed with an external resistor divider.	Circuit 2
6, 7	NC	No connect. May be grounded if needed.	Circuit 2
16	BYP	Connect a 0.1µF capacitor from BYP pin to GND, to filter the internal VREF.	Circuit 2
8	OCP	OCP pin allows the Current limit to be programmed with an external resistor.	Circuit 2
14	EN	V_{IN} independent chip enable. TTL and CMOS compatible.	Circuit 2
11	TMODE	Test Mode pin, must be connected to GND.	Circuit 2
	Bottom Metallization	The metal surface on the bottom surface of the package is floating. For mounting instructions see “Bottom Metal Mounting Guidelines” on page 8.	Circuit 2



ESD CIRCUIT 1



ESD CIRCUIT 2

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG DWG. #
5962R1322001VXC	ISL75052SEHVFE	Q 5962R13 22001VXC	-55 to +125	16 Ld CDFP	K16.E
5962R1322001V9A	ISL75052SEHVX		-55 to +125	Die	
ISL75052SEHF/SAMPLE	ISL75052SEHX/SAMPLE		-55 to +125	Die Sample	
ISL75052SEHFE/PROTO	ISL75052SEHFE/PROTO	ISL75052 SEHFE /PROTO	-55 to +125	16 Ld CDFP	K16.E
ISL75052SEHEV1ZB	Evaluation Board				

NOTE:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Absolute Maximum Ratings

V_{IN} Relative to GND without ion beam (Note 2) . . . . . -0.3 to +16.0V
V_{IN} Relative to GND under ion beam (Note 2) . . . . . -0.3 to +14.7V
V_{OUT} Relative to GND (Note 2) . . . . . -0.3 to +14.7V
PG,EN,OCP/ADJ,COMP,REFIN,REFOUT relative to GND (Note 2) . . . -0.3 to +6.5VDC

Recommended Operating Conditions (Notes 3)

Ambient Temperature Range (T_A) . . . . . -55°C to +125°C
Junction Temperature (T_J) (Note 2). . . . . +150°C
V_{IN} Relative to GND . . . . . 4.0V to 13.2V
V_{OUT} Range . . . . . 2.5V to 12.7V
PG, EN, OCP/ADJ relative to GND . . . . . 0V to +5.5V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld CDFP Package (Notes 5, 6)	26	4.5

Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Radiation Information

Maximum Total Dose
High Dose(Dose Rate = 50 - 300radSi/s) . . . . . 100 krads (Si)
Low Dose(Dose Rate = 10milliradSi/s) (Note 4) . . . . . 100 krads (Si)
SET (V_{OUT} within ±5% During Events . . . . . 86MeV/mg/cm^2
SEL/B (No Latchup/Burnout . . . . . 86MeV/mg/cm^2
The output capacitance used for SEE testing is 2x100µF for C_{IN} and C_{OUT}, 100nF for BYPASS

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.
3. Refer to “Bottom Metal Mounting Guidelines” on page 8.
4. Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer by wafer basis to 50 krad(Si) at low dose rate.
5. θJA is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See TechBrief TB379
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
7. Electromigration specification defined as lifetime average junction temperature of +150°C where max rated DC current = lifetime average current.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the following specified conditions: $V_{IN} = V_{OUT} + 0.5V$, $V_{OUT} = 4.0V$, $C_{IN} = C_{OUT} = 2x100µF$ 60mΩ, KEMET type T541X107N025AH or equivalent, $T_J = +25°C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to “Applications Information” on page 7 of the data sheet and Tech Brief TB379. Boldface limits apply over the operating temperature range, -55°C to +125°C. Pulse load techniques used by ATE to ensure $T_J = T_A$ defines guaranteed limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DC CHARACTERISTICS						
DC Output Voltage Accuracy	V_{OUT}	V_{OUT} Resistor adjust to: 2.5V and 5.0V				
		V_{OUT} = 2.5V, 4.0V < V_{IN} < 5.0V; 0A < I_{LOAD} < 1.5A, T_J = -55°C to +125°C	**-1.5**	0.2	**1.5**	%
		V_{OUT} = 2.5V, 4.0V < V_{IN} < 5.0V; 0A < I_{LOAD} < 1.5A, T_J = +25°C, Post Rad.	**-2.0**	0.2	**2.0**	%
		V_{OUT} = 5.0V, 5.5V < V_{IN} < 6.9V; 0A < I_{LOAD} < 1.5A, T_J = -55°C to +125°C	**-1.5**	0.2	**1.5**	%
		V_{OUT} = 5.0V, 5.5V < V_{IN} < 6.9V, 0A < I_{LOAD} < 1.5A, T_J = +25°C, Post Rad.	**-2.0**	0.2	**2.0**	%
		V_{OUT} Resistor adjust to: 10.0V				
		V_{OUT} = 10.0V, 10.5V < V_{IN} < 13.2V, I_{LOAD} = 0A, T_J =-55°C to +125°C	**-1.5**	0.2	**1.5**	%
		V_{OUT} = 10.0V, 10.5V < V_{IN} < 13.2V, I_{LOAD} = 0A, T_J = +25°C, Post Rad.	**-2.0**	0.2	**2.0**	%
		V_{OUT} = 10.0V, V_{IN} = 10.5V, I_{LOAD} = 1.5A, V_{IN} =13.2V, I_{LOAD} = 1.0A, T_J = -55°C to +125°C	**-1.5**	0.2	**1.5**	%
		V_{OUT} = 10.0V, V_{IN} = 10.5V; I_{LOAD} =1.5A, V_{IN} =13.2V, I_{LOAD} = 1.0A, T_J = +25°C, Post Rad.	**-2.0**	0.2	**2.0**	%

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the following specified conditions: $V_{IN} = V_{OUT} + 0.5V$, $V_{OUT} = 4.0V$, $C_{IN} = C_{OUT} = 2x100\mu F$ 60mΩ, KEMET type T541X107N025AH or equivalent, $T_J = +25°C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 7 of the data sheet and Tech Brief TB379. Boldface limits apply over the operating temperature range, -55°C to +125°C. Pulse load techniques used by ATE to ensure $T_J = T_A$ defines guaranteed limits. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
VCCX Pin	V_{VCCX}	T_J = -55°C to +125°C; 4V < V_{IN} < 13.2V; I_{LOAD} = 0A;	**3.7**	3.9	**4.1**	V
ADJ Pin	V_{ADJ}	T_J = -55°C to +125°C	**591**	600	**609**	mV
ADJ Pin	V_{ADJ}	T_J = 25°C, Post Rad	**588**	600	**612**	mV
BYP Pin	V_{BYP}	4.0V < V_{IN} < 13.2V; I_{LOAD}=0A, T_J = -55°C to +125°C	**588**	600	**612**	mV
DC Input Line Regulation		4.0V < V_{IN} < 13.2V, V_{OUT} = 2.5V		1	**8**	mV
DC Input Line Regulation		5.5V < V_{IN} < 13.2V, V_{OUT} = 5.0V		1	**20**	mV
DC Input Line Regulation		10.5V < V_{IN} < 13.2V, V_{OUT} = 10.0V		1	**10**	mV
DC Output Load Regulation		V_{OUT} = 2.5V; 0A < I_{LOAD} < 1.5A, V_{IN} = 4.0V		0.3	**9**	mV
DC Output Load Regulation		V_{OUT} = 5.0V; 0A < I_{LOAD} < 1.5A, V_{IN} = 5.5V		1.3	**18**	mV
DC Output Load Regulation		V_{OUT} = 10.0V; 0A < I_{LOAD} < 1.5A, V_{IN} = 10.5V		0.1	**36**	mV
ADJ Input Current		V_{ADJ} = 0.6V			1	µA
Ground Pin Current	I_Q	V_{OUT} = 2.5V; I_{LOAD} = 0A, 4.0V < V_{IN} < 13.2V		6	**10**	mA
Ground Pin Current	I_Q	V_{OUT} = 2.5V; I_{LOAD} = 1.5A, 4.0V < V_{IN} < 13.2V		8	**12**	mA
Ground Pin Current	I_Q	V_{OUT} = 10.0V, I_{LOAD} = 0A, 11.0V < V_{IN} < 13.2V		15	**20**	mA
Ground Pin Current	I_Q	V_{OUT} = 10.0V, I_{LOAD} = 1.5A, 11.0V < V_{IN} < 13.2V		20	**25**	mA
Ground Pin Current in Shutdown	I_{SHDNL}	ENABLE Pin = 0V, V_{IN} = 4.0V		70	**120**	µA
Ground Pin Current in Shutdown	I_{SHDNH}	ENABLE Pin = 0V, V_{IN} = 13.2V		165	**300**	µA
Dropout Voltage (Note 10)	V_{DO}	I_{LOAD} = 0.5A, V_{OUT} = 3.6V and 12.7V		75	**160**	mV
Dropout Voltage (Note 10)	V_{DO}	I_{LOAD} = 1.0A, V_{OUT} = 3.6V and 12.7V		150	**300**	mV
Dropout Voltage (Note 10)	V_{DO}	I_{LOAD} = 1.5A, V_{OUT} = 3.6V and 12.7V		225	**400**	mV
Output Short Circuit Current for 16 Ld FP	ISCL	V_{OUT} SET = 4.0V, V_{OUT} + 0.5V < V_{IN} < 13.2V, R_{SET} = 3k, Note 12)	0.16	0.24	0.32	A
Output Short Circuit Current for 16 Ld FP	ISCH	V_{OUT} SET = 4.0V, V_{OUT} + 0.5V < V_{IN} < 13.2V, R_{SET} = 300Ω, Note 12)	1.6	2.4	3.2	A
Thermal Shutdown Temperature (Note 9)	TSD	V_{OUT} + 0.5V < V_{IN} < 13.2V	154	175	**196**	°C
Thermal Shutdown Hysteresis (Rising Threshold) (Note 9)	TSDn	V_{OUT} + 0.5V < V_{IN} < 13.2V			**25**	°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection (Note 9)	PSRR	V_{P-P} = 300mV, f = 1kHz, I_{LOAD} = 1.5A; V_{IN} = 4.9V, V_{OUT} = 4.0V	**55**	65		dB
Input Supply Ripple Rejection (Note 9)	PSRR	V_{P-P} = 300mV, f = 120Hz, I_{LOAD} = 5mA; V_{IN} = 4.9V, V_{OUT} = 2.5V	**60**	70		dB
Input Supply Ripple Rejection (Note 9)	PSRR	V_{P-P} = 300mV, f = 100kHz, I_{LOAD} = 1.5A; V_{IN} = 4.9V, V_{OUT} = 4.0V	40	50		dB
Phase Margin, (Note 9)	PM	V_{OUT} = 2.5V, 4.0V and 10V, C_{OUT} = 2x100µF, R_{COMP}=22k, C_{COMP} = 1nF	**50**			°
Gain Margin, (Note 9)	GM	V_{OUT} = 2.5V, 4.0V and 10V C_{OUT} = 2x100µF, R_{COMP} = 22k, C_{COMP} = 1nF	**10**			dB
Output Noise Voltage, (Note 9)		I_{LOAD} = 10mA, BW = 300Hz < f < 300kHz, BYPASS to GND capacitor = 0.2µF		100		μV_{RMS}

Electrical Specifications Unless otherwise noted, all parameters are guaranteed over the following specified conditions: $V_{IN} = V_{OUT} + 0.5V$, $V_{OUT} = 4.0V$, $C_{IN} = C_{OUT} = 2x100\mu F$ 60mΩ, KEMET type T541X107N025AH or equivalent, $T_J = +25°C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 7 of the data sheet and Tech Brief TB379. Boldface limits apply over the operating temperature range, -55°C to +125°C. Pulse load techniques used by ATE to ensure $T_J = T_A$ defines guaranteed limits. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DEVICE START-UP CHARACTERISTICS						
Enable Pin Characteristics						
Turn-on Threshold		4.0V < V_{IN} < 13.2V	**0.5**	0.8	**1.2**	V
Enable Pin Leakage Current		V_{IN} = 13.2V, EN = 5.5V			**1**	µA
Enable Pin Propagation Delay (EN step 1.2V to V_{OUT} = 100mV)		V_{IN} = 4.5V, V_{OUT} = 4.0V, I_{LOAD} = 1.5A, C_{OUT} = 22µF, C_{BYP} = 0.2µF		0.5	1.0	ms
Enable Pin Turn-on Delay (EN step 1.2V to PGOOD)		V_{IN} = 4.5V, V_{OUT} = 4.0V, I_{LOAD} = 1.5A, C_{OUT} = 2x100µF, C_{BYP} = 0.2µF		1.4	3.0	ms
Enable Pin Turn-on Delay (EN step 1.2V to PGOOD)		V_{IN} = 4.5V, V_{OUT} = 4.0V, I_{LOAD} = 1.5A, C_{OUT} = 22µF, C_{BYP} = 0.2µF		1.1	2.5	ms
Hysteresis (Falling Threshold)		4.0V < V_{IN} < 13.2V	**75**	170		mV
PG Pin Characteristics						
V_{OUT} Error Flag Rising Threshold			**83**	88	**94**	%V_{OUT}
V_{OUT} Error Flag Falling Threshold			**80**	86	**91**	%V_{OUT}
V_{OUT} Error Flag Hysteresis			**1.75**	2.5		%V_{OUT}
Error Flag Low Voltage		I_{SINK} = 1mA		5	**100**	mV
Error Flag Low Voltage		I_{SINK} = 10mA		5	**400**	mV
Error Flag Leakage Current		V_{IN} = 13.2V, PG = 5.5V			**1**	µA

8. Parameters with bold face MIN and/or MAX limits are 100% tested at -55°C, 25°C and 125°C.
9. Limits established by characterization and are not production tested.
10. Dropout is defined by the difference in supply V_{IN} and V_{OUT} when the supply produces a 2% drop in V_{OUT} from its nominal value.
11. Refer to thermal package guidelines in "Bottom Metal Mounting Guidelines" on page 8..
12. OCP recovery overshoot should be within ±4% of the nominal VOUT setpoint.
13. SET performance of <±5% at LET = 86MeV.cm2/mg has been evaluated at V_{OUT} = >2.5V with $C_{IN} = C_{OUT} = 2x100\mu F$ 10V 60mΩ in parallel with 0.1µF CDR04 X7R capacitor. Capacitor on BYP = 0.1µF CDR04 X7R.

Applications Information

Input Voltage Requirements

This RH LDO will work from a V_{IN} in the range of 4.0V to 13.2V. The input supply can have a tolerance of as much as ±10% for conditions noted in the specification table. The minimum guaranteed input voltage is 4.0V. However, due to the nature of an LDO, V_{IN} must be some margin higher than the output voltage plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The Dropout spec of this family of LDOs has been generously specified in order to allow design for efficient operation.

External Capacitor Requirements

GENERAL GUIDELINE

External capacitors are required for proper operation. Careful attention must be paid to layout guidelines and selection of capacitor type and value to ensure optimal performance.

OUTPUT CAPACITOR

It is recommended to use a combination of Tantalum and Ceramic capacitors to achieve a good volume to capacitance ratio. The recommended combination is a 2x100µF 60mΩ rated, KEMET T541 series tantalum capacitor, in parallel with a 0.1µF MIL-PRF-49470 ceramic capacitor to be connected to V_{OUT} and Ground pins of the LDO with PCB traces no longer than 0.5cm.

INPUT CAPACITOR

It is recommended to use a combination of Tantalum and Ceramic capacitors to achieve a good capacitance to volume ratio. The recommended combination is a 2x100µF 60mΩ rated, KEMET T541 series tantalum capacitor in parallel with a 0.1µF MIL-PRF-49470 ceramic capacitor to be connected to V_{IN} and Ground pins of the LDO with PCB traces no longer than 0.5cm.

Current Limit Protection

The RH LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The current limit circuit performs as a constant current source when the output current exceeds the current limit threshold which can be adjusted by means of a resistor connected between the OCP

pin and GND. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage mode regulation. In the event of an overload condition the LDO will begin to cycle on and off due to the die temperature exceeding thermal fault condition. However, one may never witness thermal cycling if the heatsink used for the package can keep the die temperature below the limits specified for thermal shutdown. The ROCP can be calculated using the equation:

$$R_{OCP} = 893/I_{OCP} \quad \text{(EQ. 1)}$$

Where:

R_{OCP} = The OCP resistor value in ohms.

I_{OCP} = The required OCP threshold in amps.

ESD Clamps

The ESD_CL_12V ESD clamps break down at nominally 17V. The ESD_RC_7V clamps break down at nominally 7.5V with a tolerance of ±10%. The PG pin has a diode to GND. The VOUT pin has a diode to VIN (see “Pin Descriptions” on page 3).

COMP Pin

This pin helps compensate the device for various load conditions. For 4.0V < VIN < 6.0V use RCOMP = 40k and CCOMP = 1nF. For 6V < VIN < 13.2V use RCOMP = 40k and CCOMP = 4.7nF. The max current of the COMP pin when shorted to GND is 160µA.

Undervoltage Lockout

The undervoltage lockout function detects when VCCX exceeds 3.2V. When that level is reached, the LDO feedback loop is closed and the LDO can begin regulating. This is achieved by freeing the BYP net to charge up and act as a reference voltage to the EA. Prior to that happening, the LDO Power PMOS device is clamped off.

Bottom Metal Electrical Potential

The package bottom metal is electrically isolated and unbiased. The bottom metal may be electrically connected to any potential which offers the best thermal path through conductive mounting materials (conductive epoxy, solder, etc.) or may be left unbiased through the use of electrically non-conductive mounting materials (non-conductive epoxy, Sil-pad, kapton film, etc.).

Bottom Metal Mounting Guidelines

The package bottom is a solderable metal surface. The following JESD51-5 guidelines may be used to mount the package:

- Place a thermal land on the PCB under the bottom metal.
- The land should be approximately the same size to 1mm larger than the 0.19x0.41inch bottom metal.
- Place an array of thermal vias below the thermal land.
- Via array size: ~4 x 9 = 36 thermal vias
- Via diameter: ~0.3mm drill diameter with plated copper on the inside of each via.
- Via pitch: ~1.2mm.

Vias should drop to and contact as much buried metal area as feasible to provide the best thermal path.

Thermal Fault Protection

In the event the die temperature exceeds +170°C (typ.) the output of the LDO will shut down until the die temperature can cool down to +150°C (typ.). The level of power combined with the thermal impedance of the package (θ_{JC} of 5°C/W for the 16 Ld CDFP package) will determine if the junction temperature exceeds the thermal shutdown temperature specified in the specification table (see “Bottom Metal Mounting Guidelines” on page 8).

Typical Operating Performance

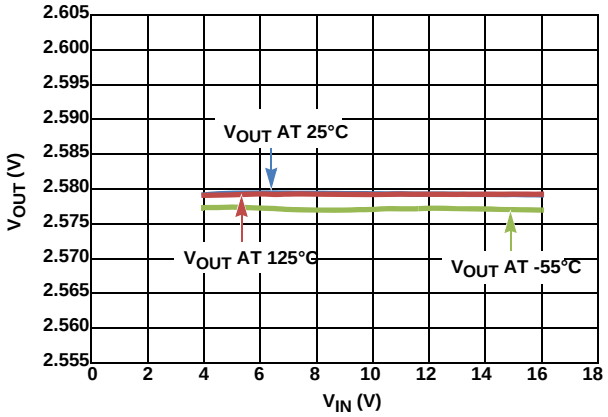


FIGURE 4. LINE REGULATION vs TEMPERATURE (°C), V_{OUT} = 2.579V, I_{OUT} = 0mA

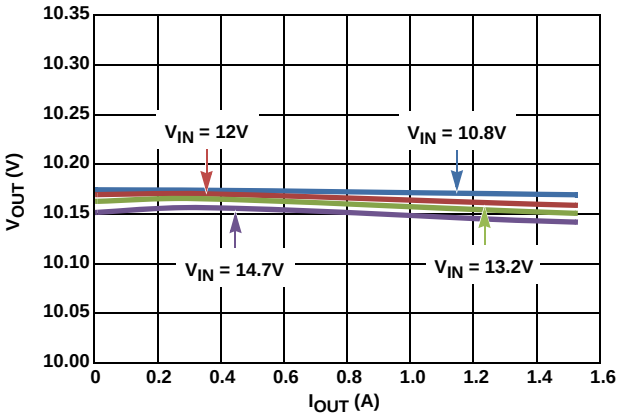


FIGURE 5A. LOAD REGULATION V_{OUT} = 10.17V AT 25°C

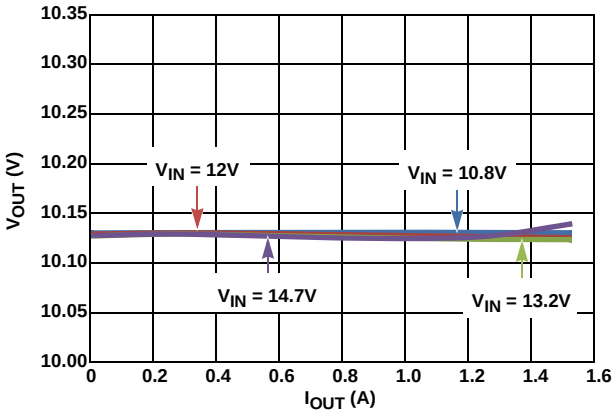


FIGURE 5B. LOAD REGULATION V_{OUT} = 10.13V AT 125°C

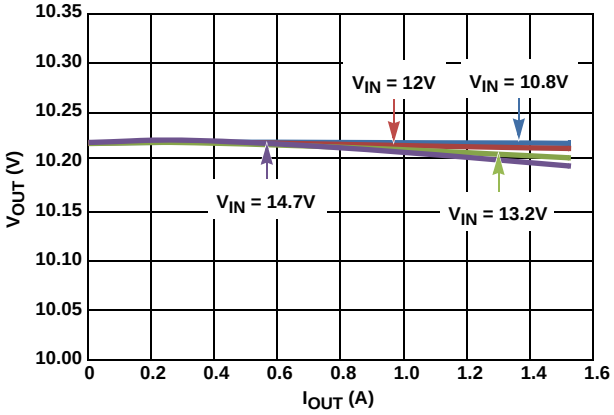


FIGURE 5C. LOAD REGULATION V_{OUT} = 10.22V AT -55°C

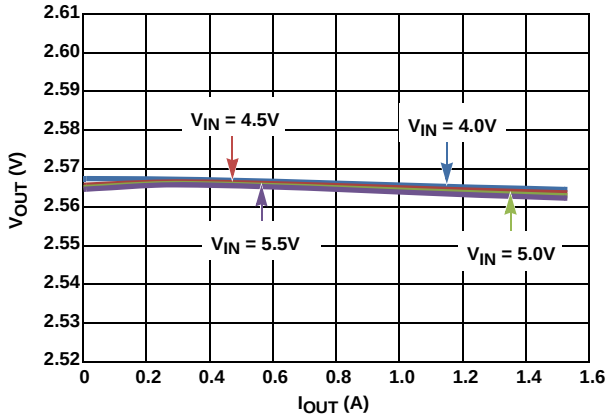


FIGURE 6A. LOAD REGULATION V_{OUT} = 2.567V AT 25°C

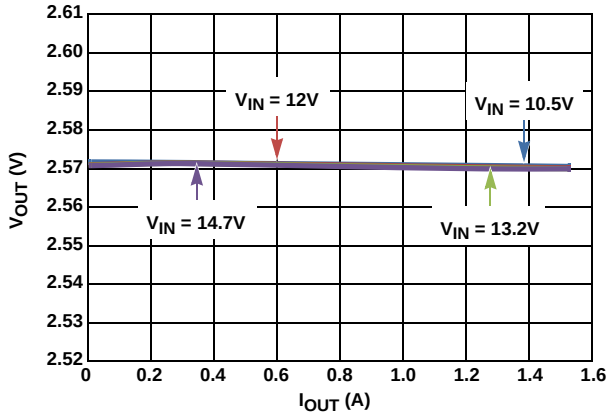


FIGURE 6B. LOAD REGULATION V_{OUT} = 2.571V AT 125°C

Typical Operating Performance (Continued)

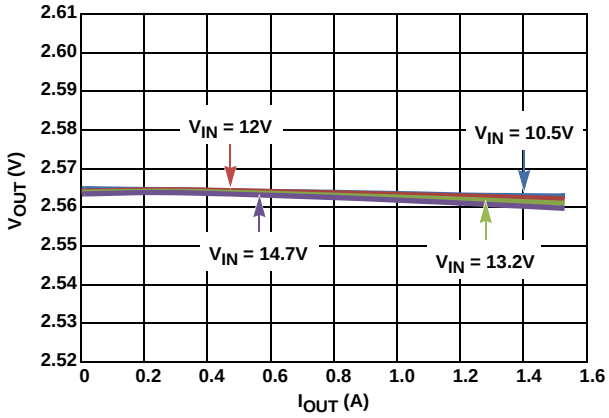


FIGURE 6C. LOAD REGULATION V_{OUT} = 2.564V AT -55°C

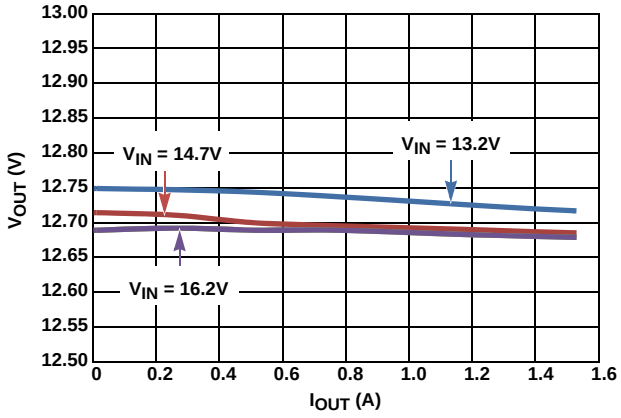


FIGURE 7A. LOAD REGULATION V_{OUT} = 12.75V AT 25°C

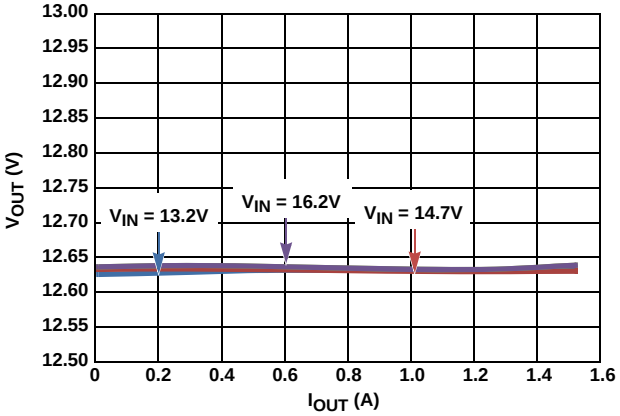


FIGURE 7B. LOAD REGULATION V_{OUT} = 12.63V AT 125°C

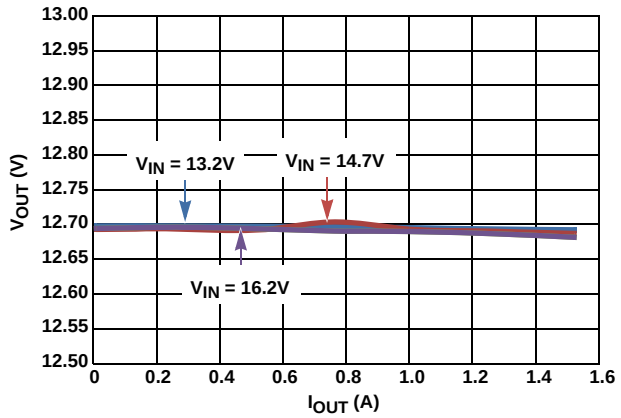


FIGURE 7C. LOAD REGULATION V_{OUT} = 12.7V AT -55°C

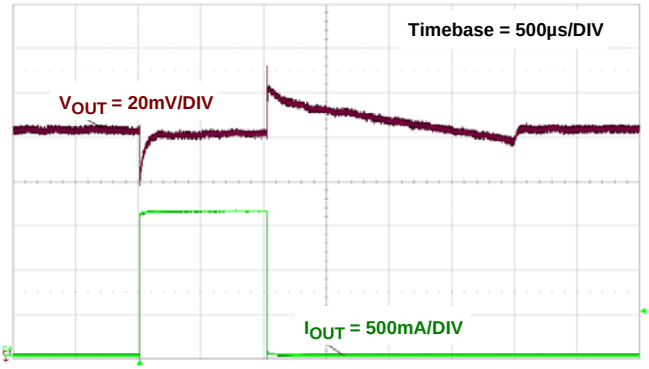


FIGURE 8. LOAD STEP RESPONSE, 25°C, V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 0A to 1.6A, C_{OUT} = 200µF, 30mΩ

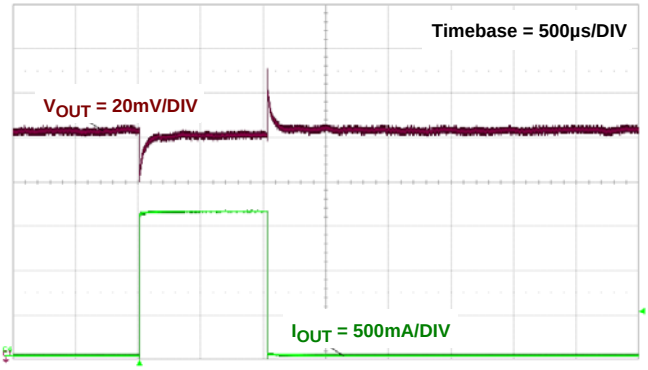


FIGURE 9. LOAD STEP RESPONSE, 25°C, V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 0.15A to 1.6A, C_{OUT} = 200µF, 30mΩ

Typical Operating Performance (Continued)

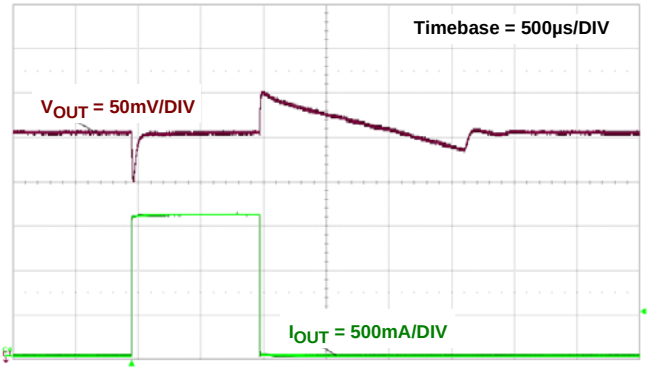


FIGURE 9A. LOAD STEP RESPONSE, 25°C, V_{IN} = 13.2V, V_{OUT} = 10V, I_{OUT} = 0A to 1.5A, C_{OUT} = 200µF, 30mΩ

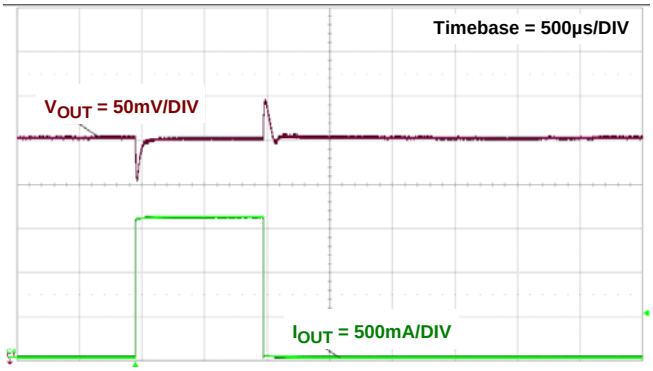


FIGURE 9B. LOAD STEP RESPONSE, 25°C, V_{IN} = 13.2V, V_{OUT} = 10V, I_{OUT} = 0.15A to 1.5A, C_{OUT} = 200µF, 30mΩ

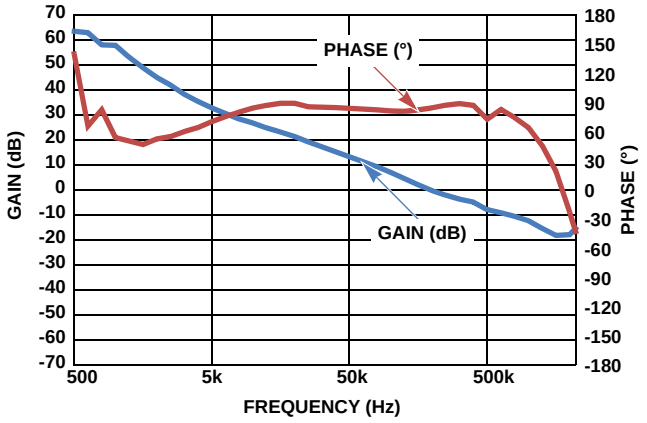


FIGURE 10. GAIN PHASE PLOTS, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 0.2A, R_{COMP} = 22k, C_{COMP} = 1nF, C_{OUT} = 200µF, 30mΩ, PHASE MARGIN = 98.68°, GAIN MARGIN = 23.01dB

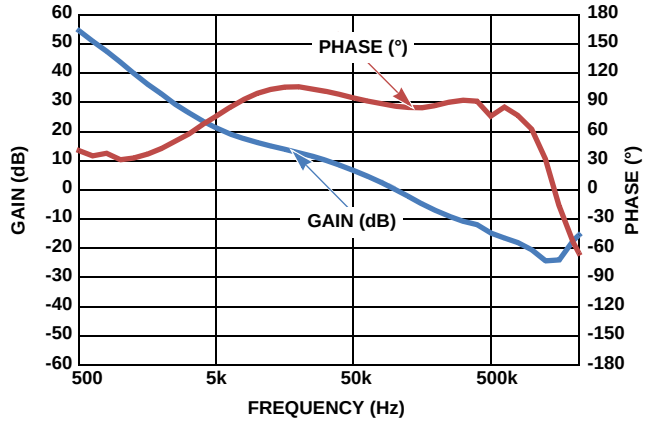


FIGURE 11. GAIN PHASE PLOTS, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 1.5A, R_{COMP} = 22k, C_{COMP} = 1nF, C_{OUT} = 200µF, 30mΩ, PHASE MARGIN = 84.56°, GAIN MARGIN = 18.06dB

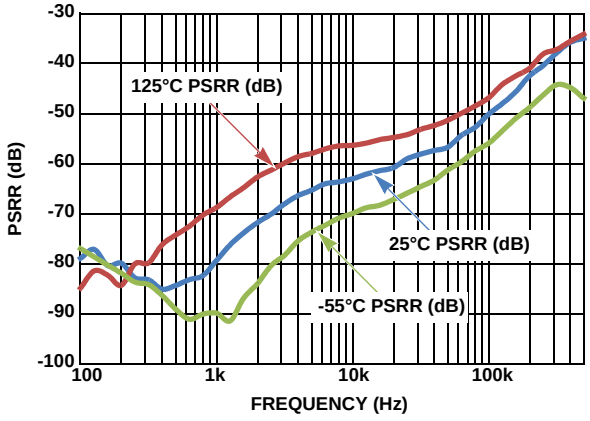


FIGURE 12. PSRR, V_{IN} = 4.9V, V_{OUT} = 4.0V, I_{OUT} = 1.5A, R_{COMP} = 22k, C_{COMP} = 1nF, C_{OUT} = 200µF, 30mΩ

Typical Operating Performance (Continued)

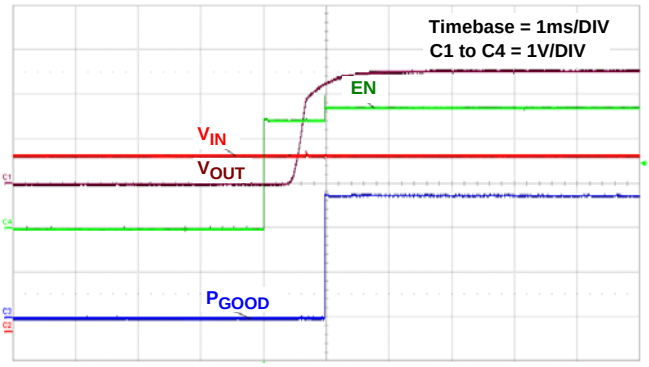


FIGURE 13. 25°C START-UP WITH ENABLE, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 0.1A

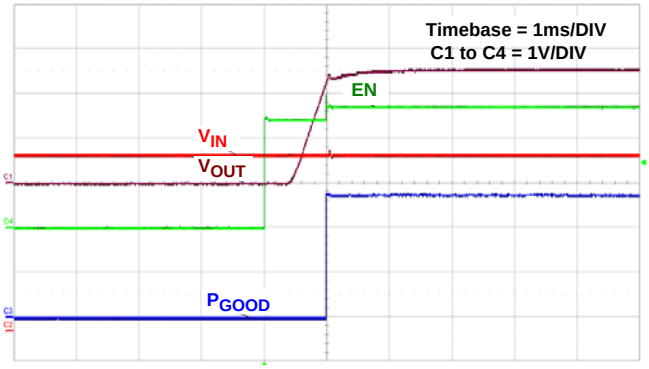


FIGURE 14. 25°C START-UP WITH ENABLE, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 1.5A

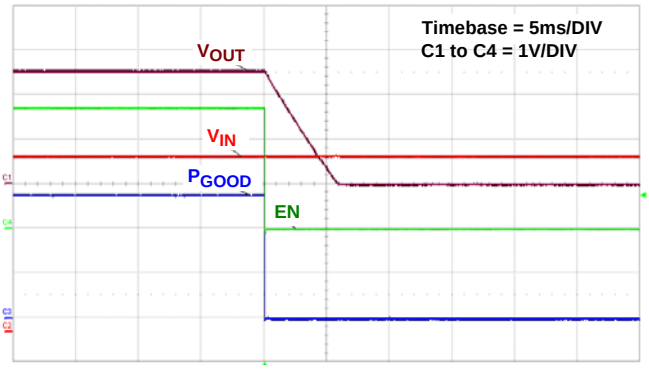


FIGURE 15. 25°C SHUTDOWN WITH ENABLE, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 0.1A

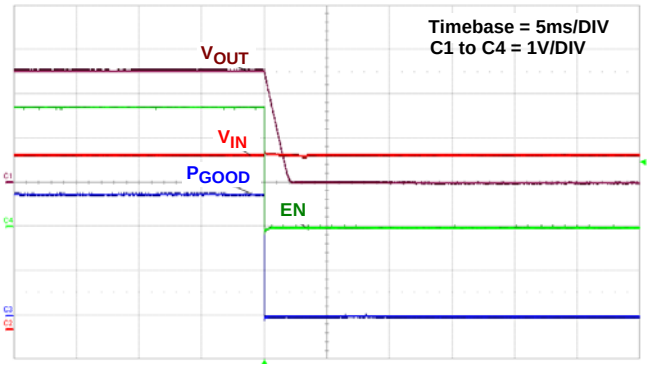


FIGURE 16. 25°C SHUTDOWN WITH ENABLE, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 1.5A

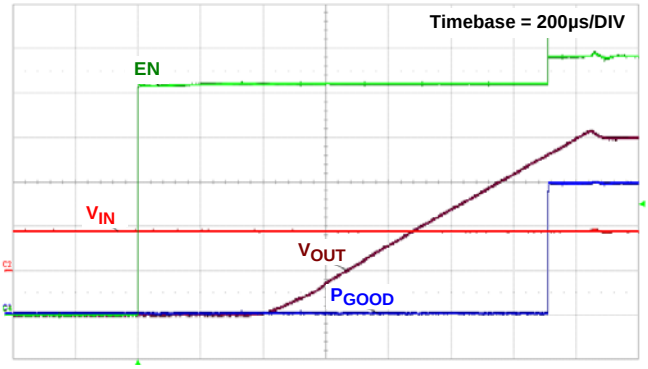


FIGURE 17. 25°C PROPAGATION DELAY, V_{IN} = 4.5V, V_{OUT} = 4V, I_{OUT} = 1.5A, EN 50% TO V_{OUT} 5%

Package Characteristics

Weight of Packaged Device

0.59 Grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Connected to Pin 13 (GND)
Case Isolation to Any Lead: $20 \times 10^9\ \Omega$ (min)

Die Characteristics

Die Dimensions

2819µm x 5638µm (111 mils x 222 mils).
Thickness: 304.8µm ± 25.4µm (12.0 mils ± 1 mil).

Interface Materials

GLASSIVATION

Type: Silicon Oxide and Silicon Nitride
Thickness: 0.3µm ± 0.03µm to 1.2µm ± 0.12µm

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 2.7µm ± 0.4µm

SUSTRATE

Type: Silicon

BACKSIDE FINISH

Silicon

ASSEMBLY RELATED INFORMATION

SUBSTRATE POTENTIAL

Ground

ADDITIONAL INFORMATION

WORST CASE CURRENT DENSITY

$< 2 \times 10^5\ A/cm^2$

TRANSISTOR COUNT

1074

PROCESS

0.6µm BiCMOS Junction Isolated

Metallization Mask Layout

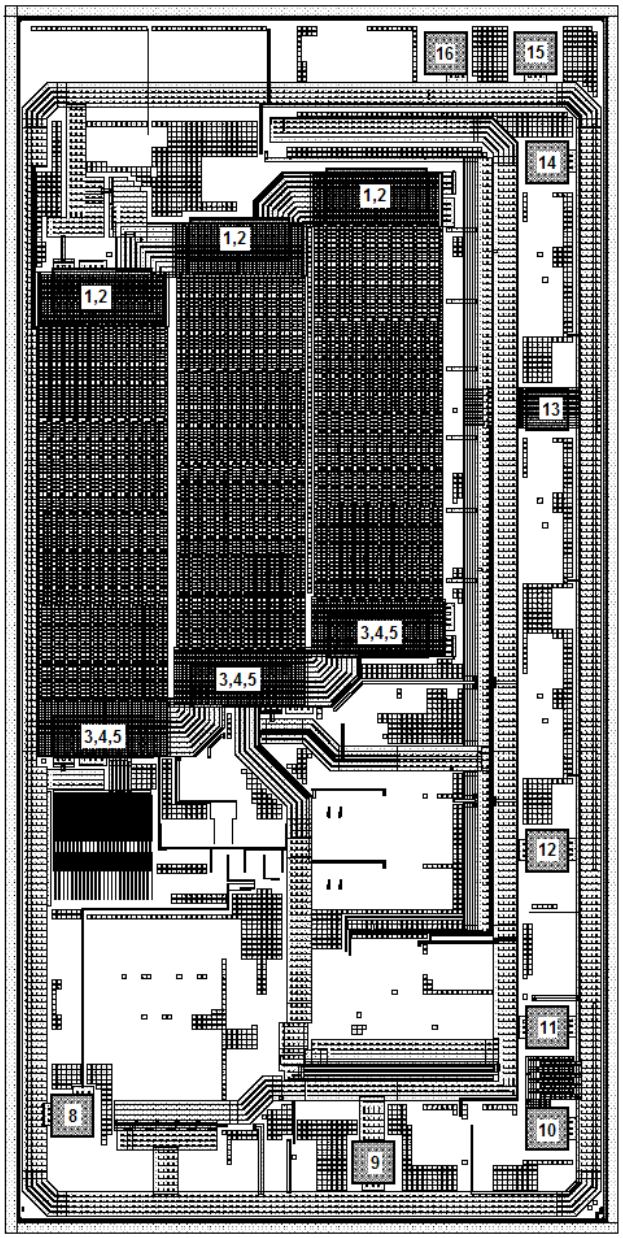


TABLE 1. DIE LAYOUT X-Y COORDINATES

PAD	X	Y	DX	DY	PIN NAME	PIN#
1	1019	1021	185	450	VOUT	1,2
2	1249	390	185	449	VOUT	1,2
3	2764	1354	5508	2689	VIN	3,4,5
4	3070	1030	185	450	VIN	3,4,5
5	3300	399	185	450	VIN	3,4,5
6	5037	256	185	185	OCP	8
7	5253	1635	185	185	VCCX	9
8	5099	2436	185	185	PG	10
9	4635	2436	185	185	TMODE	11
10	3824	2436	185	185	COMP	12
11	2840	1660	185	450	VIN	3,4,5
12	1799	2436	185	185	GND	13
13	668	2436	185	185	EN	14
14	168	2381	185	185	ADJ	15
15	168	1972	185	184	BYP	16
16	789	1652	185	450	VOUT	1,2

For additional products, see www.intersil.com/en/products.html

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
May 29, 2013	FN8456.0	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

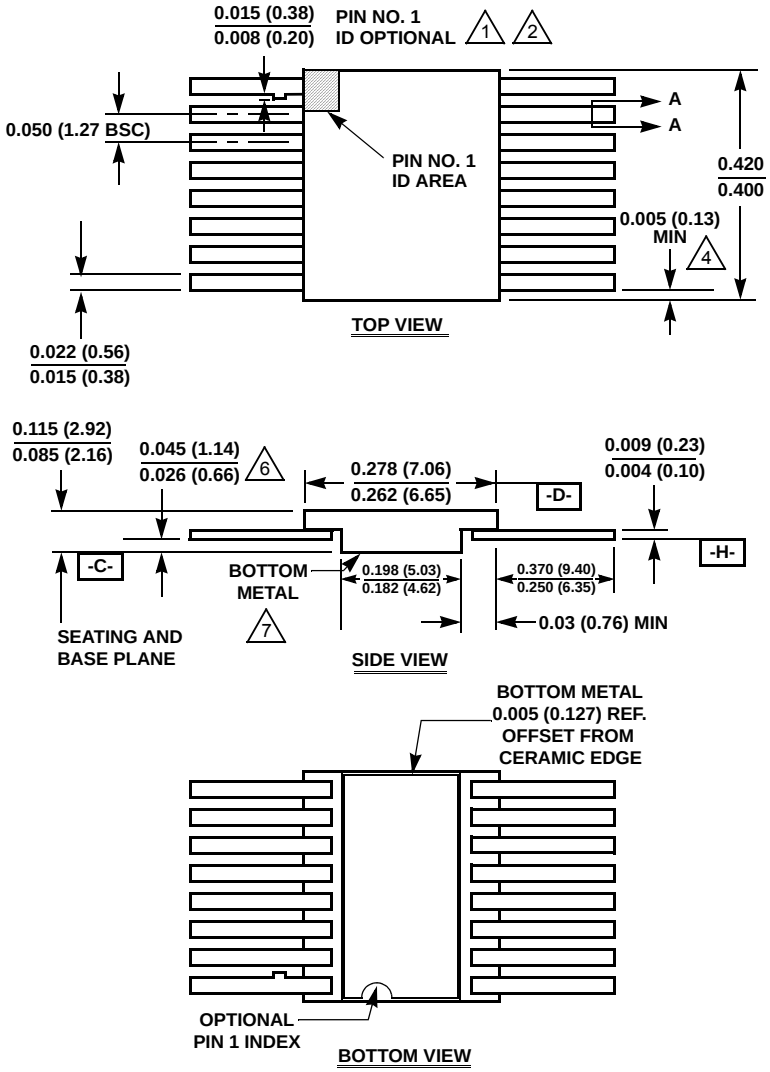
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

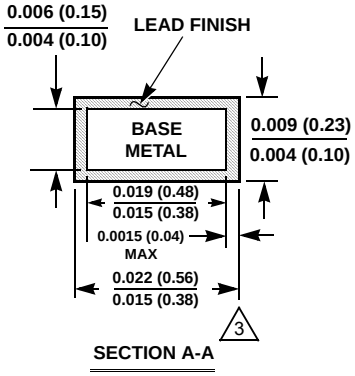
Package Outline Drawing

K16.E

16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 1, 1/12





NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. The bottom of the package is a solderable metal surface.
8. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
9. Dimensions: INCH (mm). Controlling dimension: INCH.