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MAX16956

36V, 300mA, Mini Buck Converter with 1.1µA IQ

General Description

The MAX16956 is a small, synchronous buck converter with integrated high-side and low-side switches. The device is designed to deliver up to 300mA with input voltages from 3.5V to 36V, while using only 1.1µA quiescent current at no load (fixed-output versions). Voltage quality can be monitored by observing the $\overline{\text{RESET}}$ signal. The device can operate near dropout by running at 97% duty cycle, making it ideal for automotive applications under cold-crank.

The device offers fixed-output voltages of 5V and 3.3V, as well as an adjustable version. The adjustable version allows the user to program the output voltage between 1V and 15V by using a resistor-divider. Frequency is fixed at 2.1MHz, which allows for small external components, reduced output ripple, and minimized AM radio interference. The device offers both forced-PWM and skip modes of operation, with ultra-low quiescent current of 1.1µA in skip mode. The device can be ordered with spread- spectrum frequency modulation designed to minimize EMI-radiated emissions due to the switching frequency.

The MAX16956 is available in a small (3mm x 3mm) 10-pin µMAX® package and operates across the full automotive temperature range of -40°C to +125°C. The device is AEC-Q100 qualified.

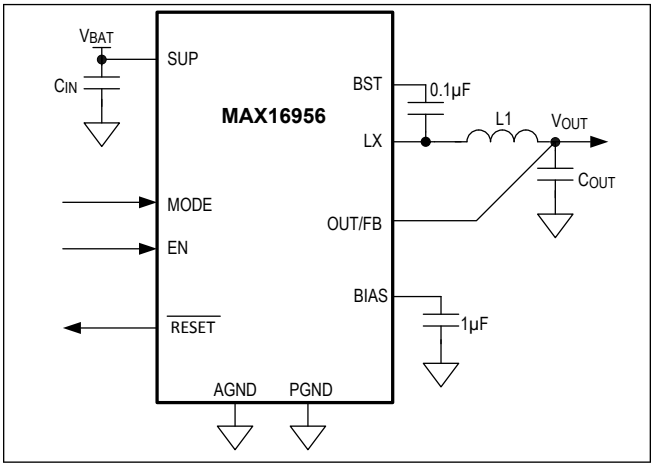
Applications

- Automotive Body ECUs
- Point-of-Load Applications
- Distributed DC Power Systems

Benefits and Features

- Integration and High-Switching Frequency Saves Space
  - DC-DC Converter Up to 300mA Capability
  - Fixed 5V/3.3V or Programmable Output-Voltage Options (1V to 15V)
  - Current-Mode-Control Architecture
  - 2.1MHz Operating Frequency
  - Fixed 5.4ms Internal Soft-Start
- Spread-Spectrum Frequency Modulation Reduces EMI Emissions
- Low I_Q Enables Designers to Meet Stringent OEM Module Power-Consumption Requirements
  - 1.1µA Quiescent Current in Standby Mode (Fixed-Output-Voltage Versions Only)
- Wide Input Voltage Range Supports Automotive Applications
  - Operating VIN Range: 3.5V to 36V (42V Tolerant)
  - 97% (Max) Duty-Cycle Operation with Low Dropout
- Robust Performance Supports Wide Range of Automotive Applications
  - Short-Circuit, Thermal Protections
  - -40°C to +125°C Automotive Temperature Range
  - AEC-Q100 Qualified

Simplified Block Diagram



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***Ordering Information** appears at end of data sheet.*

19-6737; Rev 6; 2/21

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Absolute Maximum Ratings

(Voltages Referenced to PGND) .....
SUP ..... -0.3V to +42V
EN..... -0.3V to V_{SUP} + 0.3V
BST to LX ..... +6V
BST..... -0.3V to +47V
MODE, OUT/FB, $\overline{RESET}$.....-0.3V to V_{BIAS} + 0.3V
AGND ..... -0.3V to +0.3V
BIAS ..... -0.3V to +6.0V
OUT/FB Short-Circuit Duration .....Continuous
Continuous Power Dissipation (T_A = +70°C)
(derate 12.9mW/ºC above +70°C).....1031mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s).....300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

10 µMAX

Package Code	U10E+3
Outline Number	21-0109
Land Pattern Number	90-0148
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction to Ambient (θ_{JA})	77.6°C/W
Junction to Case (θ_{JC})	5°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, V_{MODE} = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{SUP}		3.5		36	V
		T < 500ms (Note 3)			42	
Supply Current	I_{SUP}	V_{EN} = 0V		0.75	3.0	µA
		No load, fixed 3.3V V_{OUT}		1.1	3.0	
		No load, fixed 5V V_{OUT}		1.8	5.0	
		No load, adjustable V_{OUT}		32	70	
		V_{MODE} = V_{BIAS} , no load, FPWM, no switching	0.5	1	1.5	mA
UV Lockout		V_{BIAS} rising	3.0	3.2	3.4	V
		Hysteresis		0.4		

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, V_{MODE} = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BIAS Regulator Voltage	V_{BIAS}	V_{SUP} = 5.5V to 36V (MAX16956C/F only)			5		V
BIAS Current Limit				10			mA
BUCK CONVERTER							
Voltage Accuracy	V_{OUT},5V	V_{OUT} = 5V	6V ≤ V_{SUP} ≤ 36V, I_{LOAD} = 0 to 300mA	4.9	5.0	5.2	V
	V_{OUT},3.3V	V_{OUT} = 3.3V	6V ≤ V_{SUP} ≤ 36V, I_{LOAD} = 0 to 300mA	3.2	3.3	3.4	
FB Voltage Accuracy	V_{FB}	Adjustable output versions, 6V ≤ V_{SUP} ≤ 36V		0.98	1.0	1.03	V
FB Input Current	I_{FB}	V_{FB} = 1V			0.02		µA
FB Load Regulation	ΔV_{LOAD}	I_{LOAD} = 0.3mA to 300mA			1		%
FB Line Regulation	ΔV_{LINE}	6V ≤ V_{SUP} ≤ 36V			0.02		%/V
High-Side DMOS RDSON	$R_{ON,HS}$	V_{BIAS} = 5V, I_{LX} = 200mA			1000	2200	mΩ
Low-Side DMOS RDSON	$R_{ON,LS}$	V_{BIAS} = 5V, I_{LX} = 200mA			500	1200	mΩ
DMOS High-Side Current-Limit Threshold	I_{MAX}			0.425	0.5	0.575	A
DMOS High-Side Skip-Mode Peak-Current Threshold	I_{SKIP}			70	100	130	mA
DMOS Low-Side Zero-Crossing Threshold	I_{ZX}				40		mA
DMOS Low-Side Negative Current-Limit Threshold	I_{NEG}	FPWM mode			-0.320		A
Soft-Start Ramp Time	t_{SS}				5.4		ms
LX Rise Time	$t_{RISE,LX}$	(Note 3)			6		ns
Minimum On-Time	t_{ON_MIN}				60		ns
Maximum Duty Cycle	DC_{MAX}				97		%
PWM Switching Frequency	f_{SW}			1.95	2.1	2.25	MHz
Spread-Spectrum Range	SS	Spread-spectrum option only		±6			%
RESET OUTPUT ($\overline{RESET}$)							
$\overline{RESET}$ Threshold	V_{THR_RES}	V_{OUT} rising		90	92	94	$\%V_{OUT}$
	V_{THF_RES}	V_{OUT} falling		88	90	92	
$\overline{RESET}$ Debounce	t_{DEB}				12		µs
$\overline{RESET}$ High Leakage Current	$I_{LEAK,RES}$	T_A = +25°C				1	µA
$\overline{RESET}$ Low Level	$V_{OUT,RES}$	Sinking 1mA				0.4	V

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, V_{MODE} = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVELS						
EN Input High Threshold	$V_{IH,EN}$		2.4			V
EN Input Low Threshold	$V_{IL,EN}$				0.4	V
EN Input Current	$I_{IN,EN}$			0.1		µA
MODE Input High Threshold	$V_{IH,MODE}$		1.4			V
MODE Input Low Threshold	$V_{IL,MODE}$				0.4	V
MODE Internal Pulldown	$R_{PD,MODE}$			1000		kΩ
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}	(Note 3)		+175		°C
Thermal-Shutdown Hysteresis	$T_{SHDN,HYS}$	(Note 3)		+15		°C

Note 2: Limits are 100% tested at T_A = +25°C (and/or T_A = +125°C). Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

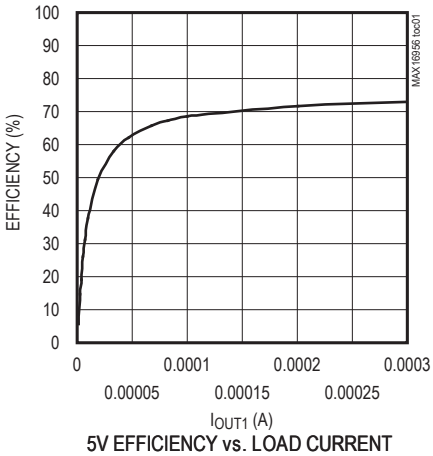
Note 3: Guaranteed by design; not production tested.

Note 4: When the typical minimum on-time of 80ns is violated, the device skips pulses.

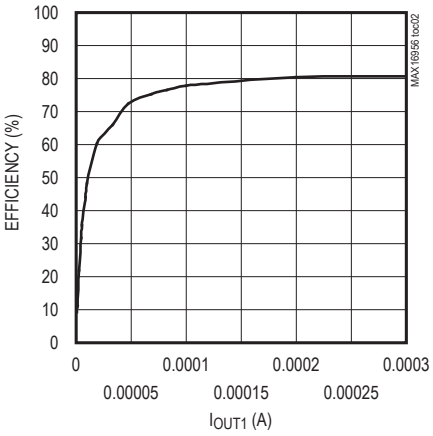
Typical Operating Characteristics

(V_{CC} = +3.5V, R_{SEN} = 6.8Ω, T_A = +25°C unless otherwise noted.)

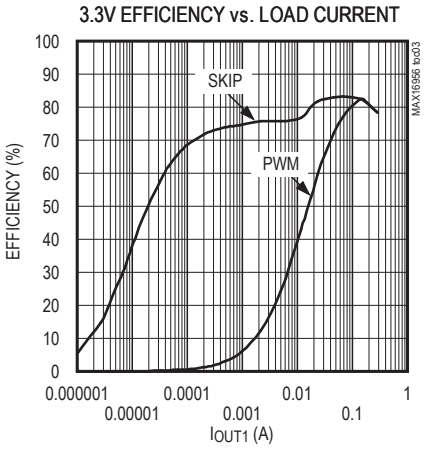
3.3V EFFICIENCY vs. LOAD CURRENT—SKIP MODE (1µA to 300µA)



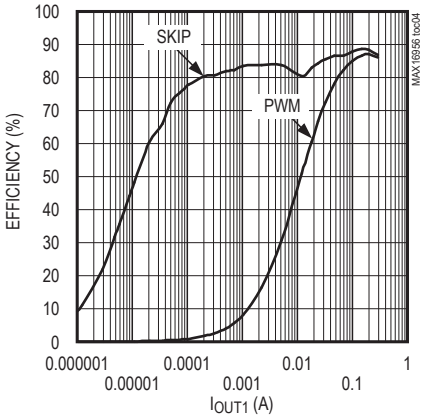
5V EFFICIENCY vs. LOAD CURRENT—SKIP MODE (1µA to 300µA)



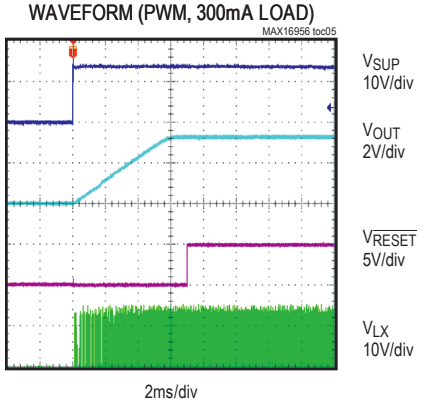
3.3V EFFICIENCY vs. LOAD CURRENT



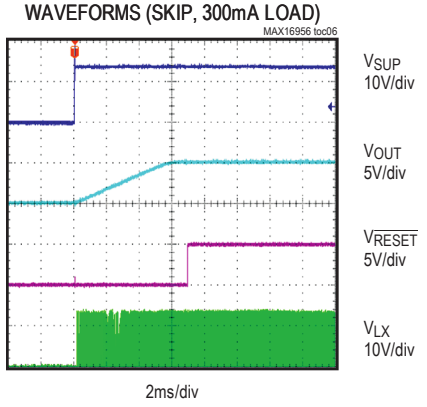
5V EFFICIENCY vs. LOAD CURRENT



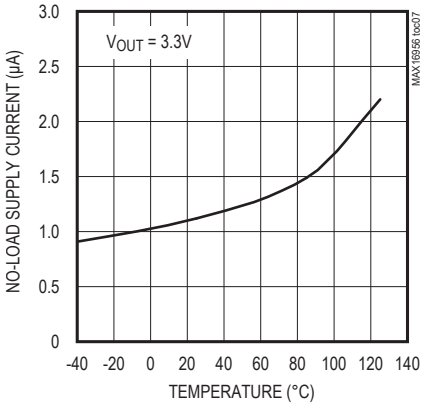
3.3V FIXED-OUTPUT STARTUP WAVEFORM (PWM, 300mA LOAD)



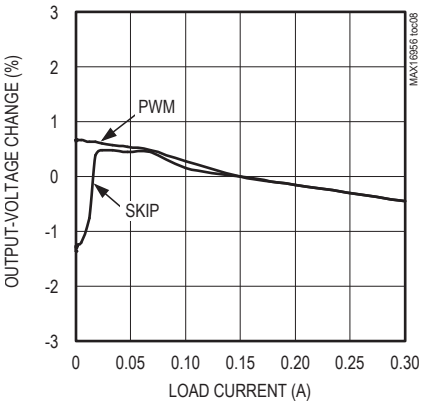
5V FIXED-OUTPUT STARTUP WAVEFORMS (SKIP, 300mA LOAD)



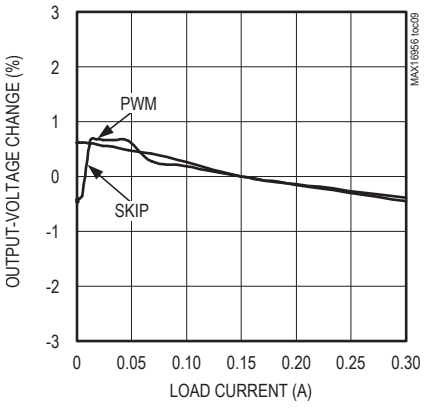
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE (SKIP MODE)



LOAD REGULATION (3.3V OUTPUT)



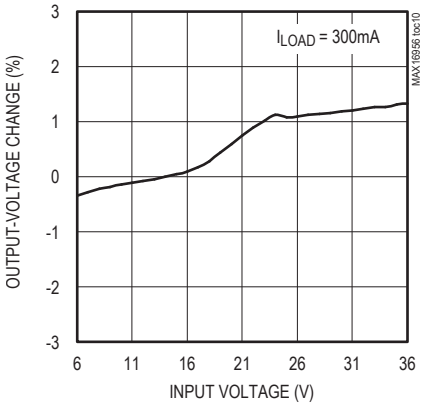
LOAD REGULATION (5V OUTPUT)



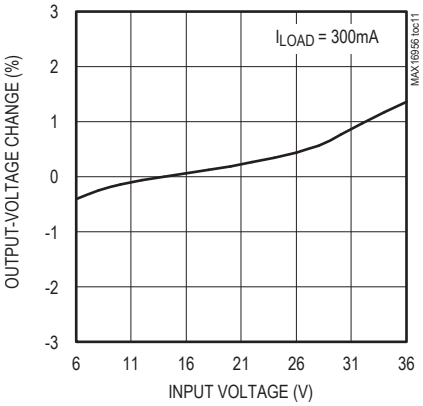
Typical Operating Characteristics (continued)

(V_{CC} = +3.5V, R_{SEN} = 6.8Ω, T_A = +25°C unless otherwise noted.)

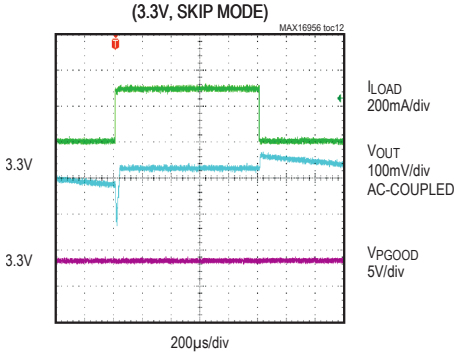
LINE REGULATION (3.3V OUTPUT)



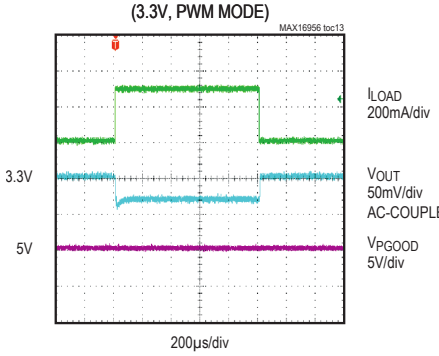
LINE REGULATION (5V OUTPUT)



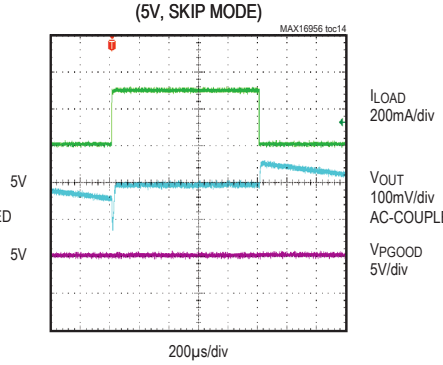
LOAD-TRANSIENT RESPONSE (3.3V, SKIP MODE)



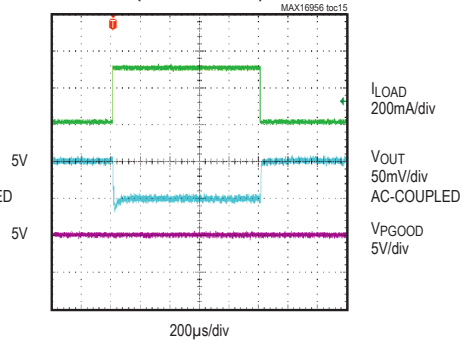
LOAD-TRANSIENT RESPONSE (3.3V, PWM MODE)



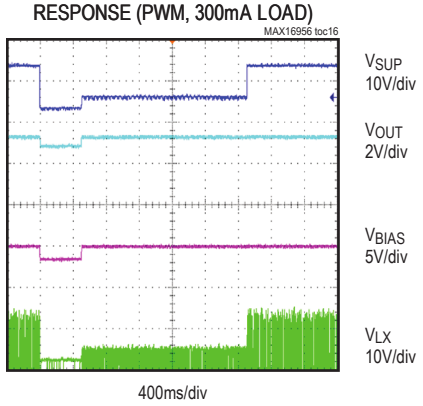
LOAD-TRANSIENT RESPONSE (5V, SKIP MODE)



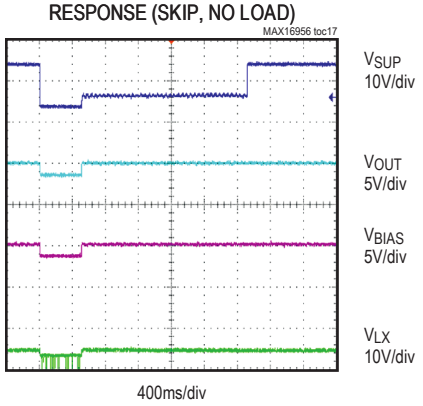
LOAD-TRANSIENT RESPONSE (5V, PWM MODE)



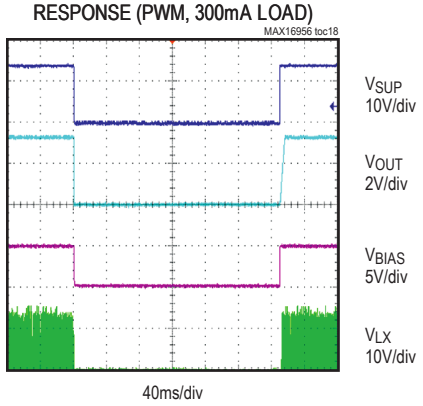
3.3V FIXED-OUTPUT COLD-CRANK RESPONSE (PWM, 300mA LOAD)



5V FIXED-OUTPUT COLD-CRANK RESPONSE (SKIP, NO LOAD)



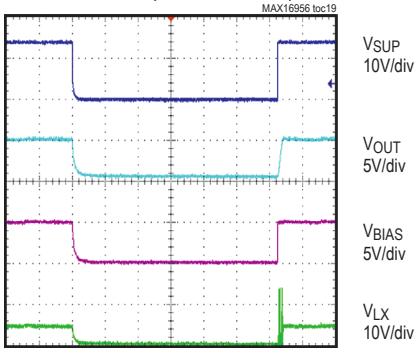
3.3V FIXED-OUTPUT DIPS AND DROPS RESPONSE (PWM, 300mA LOAD)



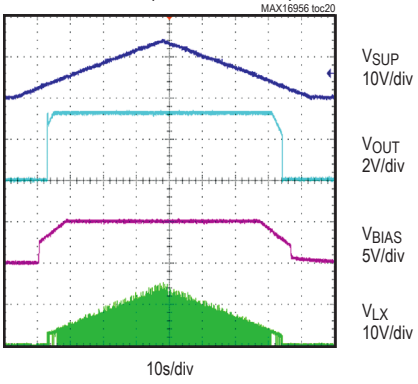
Typical Operating Characteristics (continued)

(V_{CC} = +3.5V, R_{SEN} = 6.8Ω, T_A = +25°C unless otherwise noted.)

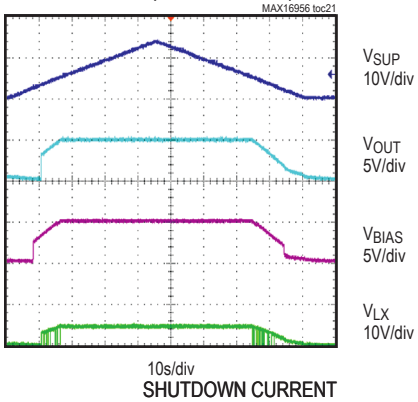
5V FIXED DIPS AND DROPS RESPONSE (SKIP, NO LOAD)



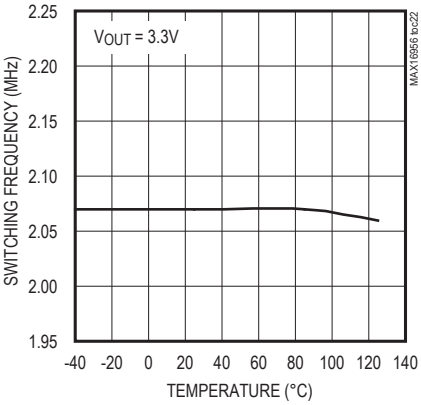
3.3V FIXED-OUTPUT SLOW V_{SUP} RESPONSE (PWM, NO LOAD)



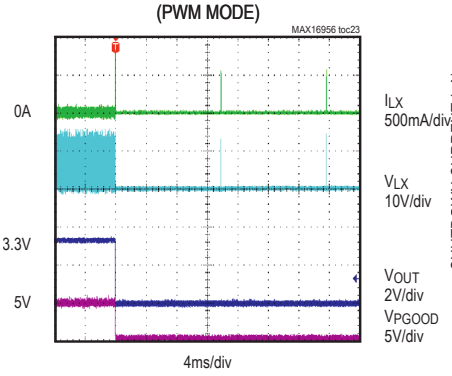
5V FIXED-OUTPUT SLOW V_{SUP} RESPONSE (SKIP, NO LOAD)



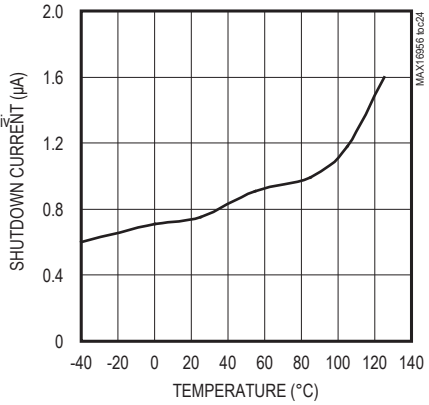
SWITCHING FREQUENCY vs. TEMPERATURE



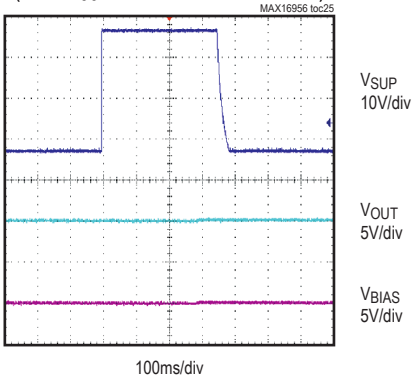
SHORT-CIRCUIT RESPONSE (PWM MODE)



SHUTDOWN CURRENT vs. TEMPERATURE

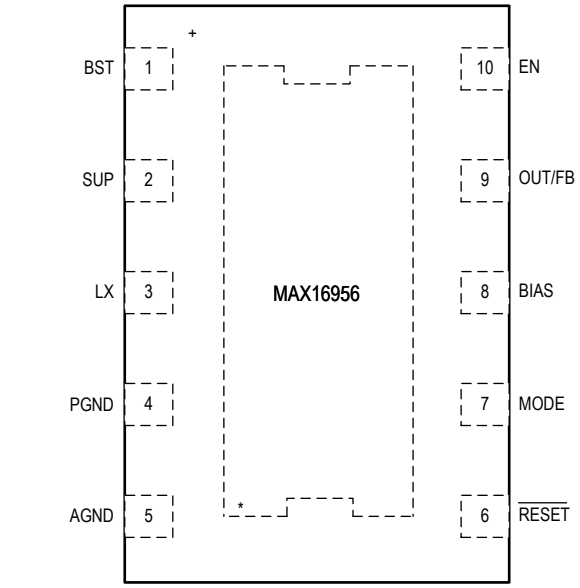


5V FIXED-OUTPUT LOAD-DUMP RESPONSE (SKIP, V_{SUP} = 13.5V TO 42V, NO LOAD)



Pin Configuration

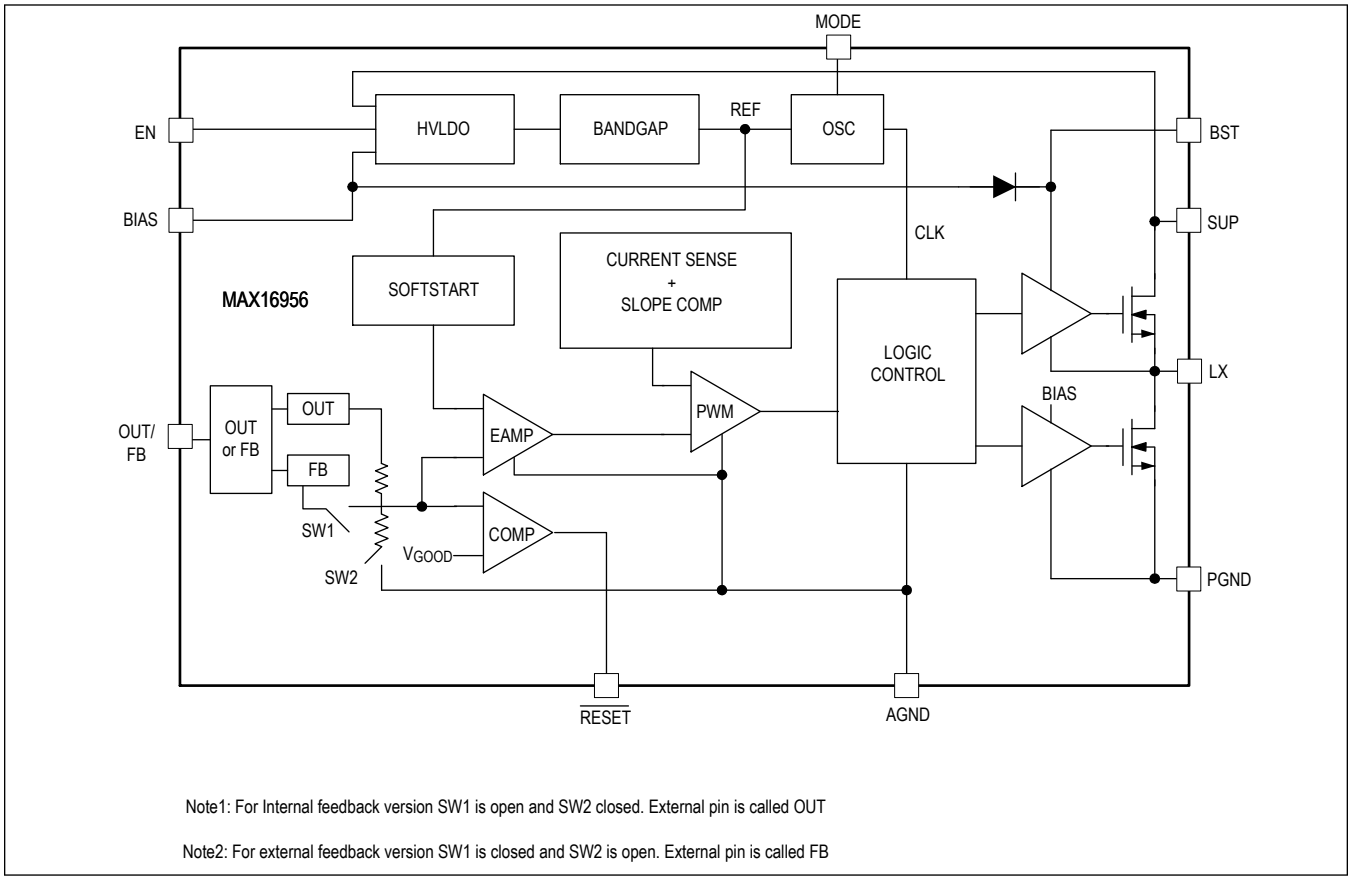
MAX16956



Pin Description

PIN	NAME	FUNCTION
1	BST	High-Side Driver Supply. Connect a 0.1µF bootstrap capacitor between LX and BST.
2	SUP	IC Supply Input. Connect a minimum of 4.7µF ceramic capacitor from SUP to PGND.
3	LX	Buck Switching Node. LX is high impedance when the device is off.
4	PGND	Power Ground. Connect to AGND under the device in a star configuration.
5	AGND	Analog Ground. Connect to PGND under the device in a star configuration.
6	$\overline{\text{RESET}}$	Open-Drain Reset Output. An external pullup resistor is required.
7	MODE	Mode Switch-Control Input. Connect to ground or leave open to enable skip-mode operation under light loads. Connect to BIAS to enable forced-PWM mode. MODE has a 1MΩ internal pulldown.
8	BIAS	5V Internal Logic Supply. Connect a 1µF ceramic capacitor to AGND.
9	OUT/FB	MAX16956A/B/D/E (Fixed Output): Buck Regulator Voltage-Sense Input. Bypass OUT to PGND with a minimum 22µF X7R ceramic capacitor. MAX16956C/F (Adjustable Output): Feedback Input. Connect FB to a resistive divider between the buck output and AGND to set the output voltage.
10	EN	SUP Voltage-Compatible Enable Input. Drive EN low to disable the device. Drive EN high to enable the device.
—	EP	Exposed Pad. Connect EP to a large copper ground plane for effective power dissipation. Do not use EP as the only IC ground connection. EP must be connected to PGND.

Block Diagram



Note1: For Internal feedback version SW1 is open and SW2 closed. External pin is called OUT

Note2: For external feedback version SW1 is closed and SW2 is open. External pin is called FB

Detailed Description

The MAX16956 is a small, current-mode buck converter that features synchronous rectification and requires no external compensation network. The device operates from a 3.5V to 36V supply voltage and can deliver up to 300mA output current. Frequency is fixed at 2.1MHz, which allows for small external components, reduced output ripple, and guarantees no AM-band interference.

The device offers fixed output voltages of 5V and 3.3V. The device also offers adjustable output-voltage versions that can be set by using an external resistive divider. Voltage quality can be monitored by observing the $\overline{\text{RESET}}$ signal. The device offers both forced-PWM and skip mode, with ultra-low-quiescent cur- rent of 1.1µA in skip mode.

DC-DC Converter Control Architecture

The device step-down converter uses a PWM peak current- mode control scheme, with a load-line architecture. Peak current-mode control provides several advantages over voltage-mode control, including precise control of the induc- tor current on a cycle-by-cycle basis, simpler compensa- tion, and inherent compensation for line voltage variation.

An internal transconductance amplifier establishes an integrated error voltage. The heart of the PWM control- ler is an open-loop comparator: one input is the inte- grated voltage-feedback signal; the other consists of the amplified current-sense signal plus slope-compensation ramp. Integrated high-side current sensing is used, which reduces component count and layout risk by eliminating the need to carefully route sensitive external signals. Error-amplifier compensation is also integrated, once again simplifying the power-supply designer's task while eliminating external components.

At each rising edge of the internal clock, the high-side MOSFET turns on until the PWM comparator trips, the maximum duty cycle is reached, or the peak current limit is reached (see the Current Limit /Short-Circuit Protection section). During this on-time, current ramps up through the inductor, storing energy in a magnetic field and sourcing current to the output. The current-mode feed- back system regulates the peak inductor current as a function of the output-voltage error signal. During the second-half of the cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as the current ramps down, providing current to the output. The output capacitor stores charge when the inductor current exceeds the required load current and discharges when the inductor current is lower, smoothing the voltage across the load.

The device features load-line architecture to reduce the output capacitance needed, potentially saving system cost and size. The output voltage is positioned slightly positive at no load, still within the tolerance window, to take advantage of the fact that any load disturbance is a load step only. This increases the amount of margin available to the undershoot that occurs on a load step, allowing a reduction in the required output capacitance. As the load increases, a small but controlled amount of load regulation ("load-line") error occurs, so that at heavier loads the voltage is positioned slightly below nominal. This takes advantage of the fact that any load disturbance is load released, increasing the amount of margin available to the overshoot that occurs.

The device can operate in either forced-PWM or skip mode. In forced-PWM mode, the converter maintains a constant switching frequency, regardless of load, to allow for easier filtering of the switching noise. The device includes proprietary circuitry that dramatically reduces quiescent current consumption in skip mode, improving light-load efficiency. See the Forced PWM/Skip Modes section for further details.

System Enable (EN)

An enable control input (EN) activates the device from its low-power shutdown mode. EN is compatible with inputs from automotive battery level down to 3.5V. The high-voltage compatibility allows EN to be connected to SUP, KEY/KL30, or the inhibit pin (INH) of a CAN transceiver.

Linear Regulator Output (BIAS)

The device includes a 5V linear regulator output (BIAS) that provides power to the internal circuit blocks. Connect a 1µF ceramic capacitor from BIAS to AGND. Do not load this pin externally.

Undervoltage Lockout

When V_{BIAS} drops below the undervoltage-lockout (UVLO) level of V_{UVLO} = 2.8V (typ), the device assumes that the supply voltage is too low for proper operation, so the UVLO circuitry inhibits switching. When V_{BIAS} rises above the

UVLO rising threshold, the controller enters the startup sequence and then resumes normal operation.

Startup and Soft-Start

The device features an internal soft-start timer. The output-voltage soft-start ramp time is 5.4ms (typ). If a short circuit or undervoltage is encountered after the soft- start timer has expired, the device is disabled for 13.4ms (typ) and then reattempts soft-start again. This pattern repeats until the short circuit has been removed.

$\overline{\text{RESET}}$ Output

The device features an open-drain $\overline{\text{RESET}}$ output to monitor the output voltage. The $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) after the regulator output increases above 92% of the nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output drops to below 90% of the nominal regulated voltage.

Forced PWM/Skip Modes

The device features a logic-level input (MODE) to switch between forced-PWM and skip modes. Connecting MODE to BIAS enables the forced-PWM operation. Connecting MODE to ground, or leaving unconnected, enables skip-mode operation with ultra-low-quiescent current of 1.1µA. In skip-mode operation, the converter's switching frequency is load dependent until the output load reaches the skip threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the forced-PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch the MOSFETs on and off as often as is the case in the forced-PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Current Limit /Short-Circuit Protection

The device has fault protection designed to protect itself from abnormal conditions. If the output is soft shorted (meaning the output is overloaded but over 50% of regulation), cycle-by-cycle current limit limits how high the inductor current goes for any cycle. If the output is hard shorted to ground and the output falls to less than 50% of regulation, the part goes into a mode where it switches until 15 cycles are ended by current limit, then waits for 13.4ms before trying to soft-start again. This mode of operation limits the amount of power dissipated by the device under these conditions. The device also has overtemperature protection. If the die temperature exceeds approximately 175°C, the device stops switching until the die temperature drops by approximately 15°C and then resumes operation, including going through soft-start again.

Spread-Spectrum Option

The device has an internal spread-spectrum option to optimize EMI performance. This is factory set on the D, E, and F variants of the device. For spread-spectrum-enabled variants of the device, the operating frequency is varied ±6% centered on 2.1MHz. The modulation signal is a triangular wave with a period of 230µs at 2.1MHz. Therefore, f_{SW} ramps down 6% and back to 2.1MHz in 115µs and also ramps up 6% and back to 2.1MHz in 115µs. The cycle repeats.

Applications Information

Setting the Output Voltage

The device's adjustable output-voltage version (see the Selector Guide for more details) allows the user to set the output to any voltage between 1V and 15V. Connect a resistive divider from output (V_{OUT}) to FB to AGND to set the output voltage (Figure 1). Select R2 (FB to AGND resistor) less than or equal to 100kΩ. Calculate R1 (V_{OUT} to FB resistor) with the following equation

$$R1 = R2 \times [(\frac{V_{OUT}}{V_{FB}}) - 1]$$

where V_{FB} = 1V (see the *Electrical Characteristics*).

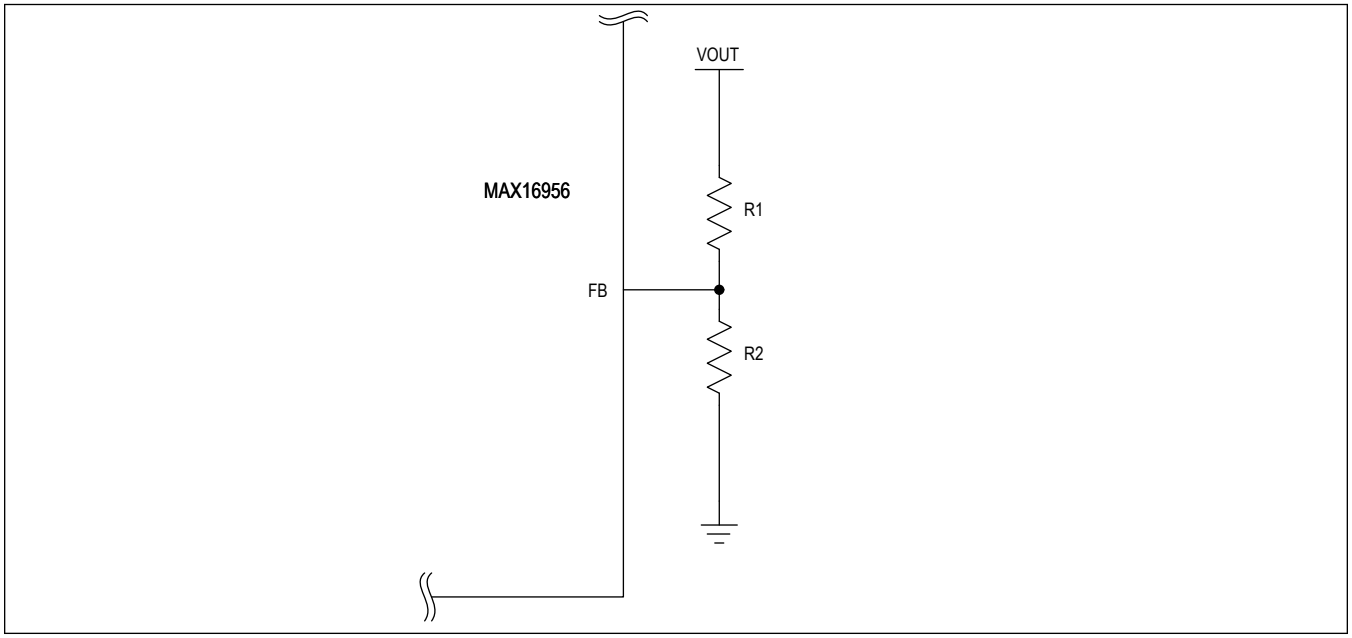


Figure 1. Adjustable Output-Voltage Setting

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determines the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{SUP} - V_{OUT})}{V_{SUP} \times f_{SW} \times I_{OUT} \times LIR}$$

where V_{SUP}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is 2.1MHz. Table 1 lists some of the inductor values for 300mA output current and several output voltages.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}}$$

IRMS has a maximum value when the input voltage equals twice the output voltage ($V_{SUP} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$. Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

Table 1. Inductor Values for 300mA Output Current

V_{SUP}/V_{OUT} (V)	14V/5V	14V/3.3V
INDUCTOR (µH) I_{LOAD} = 300mA	10µH (typ) 22µH (max)	10µH (typ) 22µH (max)

The input voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\triangle V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{OUT}}{V_{SUP}}$$

where I_{OUT} is the maximum output current and D is the duty cycle.

Output Capacitor

The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to noload conditions. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output voltage ripple. Therefore, the size of the output capacitor depends on the maximum ESR required to meet the output voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Therefore, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value. When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent voltage droop and voltage rise from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising-load edge is no longer a problem.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low-switching power losses and clean, stable operation. Use a multi- layer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1. The input capacitor (4.7µF, see Figures 3 and 4) should be placed immediately next to the SUP pin of the device. Since the device operates at 2.1MHz switching frequency, this placement is critical for effective decoupling of high-frequency noise from the SUP pin.
2. Solder the exposed pad to a large copper plane area under the device. To effectively use this copper area as heat exchanger between the PCB and ambient, expose the copper area on the top and bottom sides. Add a few small vias or one large via on the copper pad for efficient heat transfer. Connect the exposed pad to PGND, ideally at the return terminal of the output capacitor.
3. Isolate the power components and high-current path from the sensitive analog circuitry. Doing so is essential to

prevent any noise coupling into the analog signals.

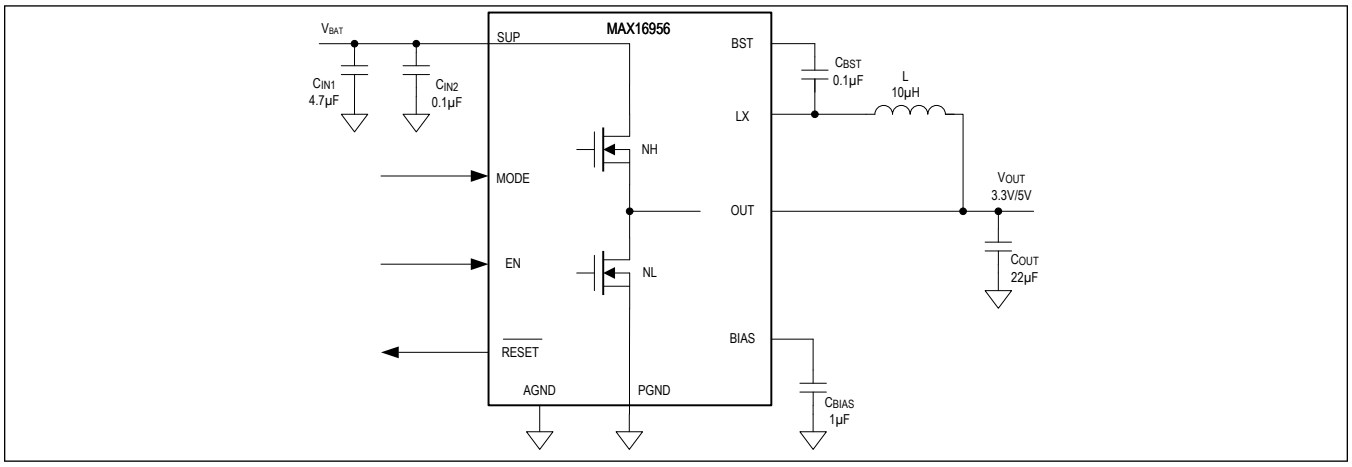
4. Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
5. Connect PGND and AGND together at the return terminal of the output capacitor. Do not connect them anywhere else.
6. Keep the power traces and load connections short. This practice is essential for high efficiency.
7. Place the BIAS capacitor ground next to the AGND pin and connect with a short and wide trace.

Table 2. SELECTOR GUIDE

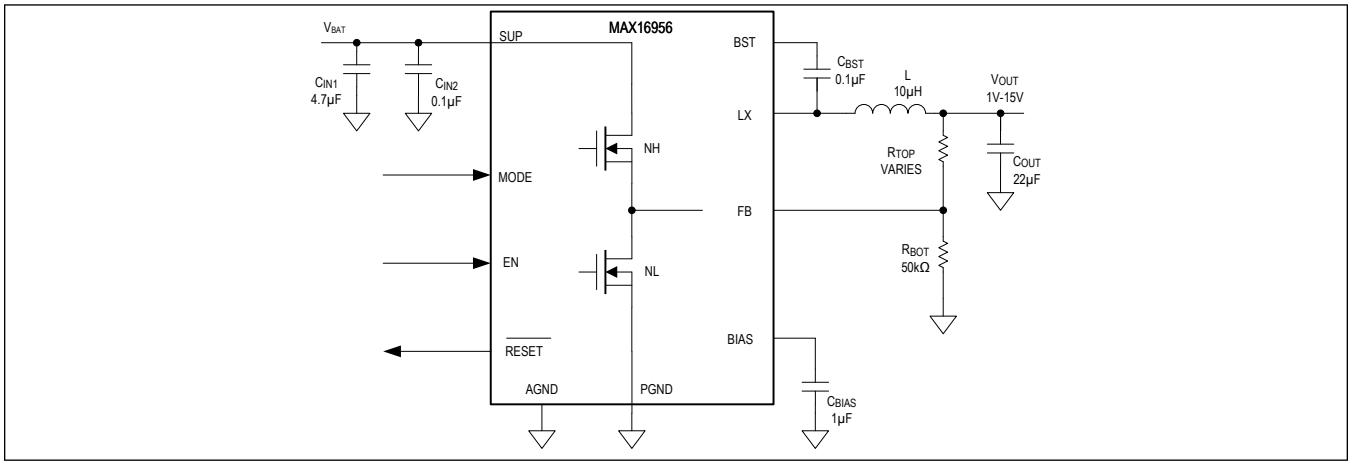
PART	V_{OUT}	$\overline{RESET}$ TIME (µs)	SPREAD SPECTRUM	PIN-PACKAGE	TOP MARK
MAX16956AUBA+	Fixed 5V	10	Off	10 µMAX-EP	+AABX
MAX16956AUBA/ V+	Fixed 5V	10	Off	10 µMAX-EP	+AABH
MAX16956AUBB+	Fixed 3.3V	10	Off	10 µMAX-EP	+AABY
MAX16956AUBB/ V+	Fixed 3.3V	10	Off	10 µMAX-EP	+AABI
MAX16956AUBC +	Adjustable	10	Off	10 µMAX-EP	+AABZ
MAX16956AUBC / V+	Adjustable	10	Off	10 µMAX-EP	+AABJ
MAX16956AUBD / V+	Fixed 5V	10	On	10 µMAX-EP	+AABK
MAX16956AUBE/ V+	Fixed 3.3V	10	On	10 µMAX-EP	+AABL
MAX16956AUBF/ V+	Adjustable	10	On	10 µMAX-EP	+AABM

Typical Application Circuits

MAX16956AUBA/V+ (5.0V Fixed) and MAX16956AUBB/V+ (3.3V Fixed), 10-Pin µMAX



MAX16956AUBC/V+, Variable Output Voltage, 10-Pin µMAX



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16956AUB_ +	-40°C to +125°C	10 µMAX-EP*
MAX16956AUB_ / V+	-40°C to +125°C	10 µMAX-EP*

Note: *Insert the desired suffix letter (from the Selector Guide) into the blank to indicate the output voltage and spread-spectrum option.*

/ V denotes an automotive qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/13	Initial release	—
1	2/14	Changed PGND to AGND for pin 8 in the Pin Description section, removed C1 from Figure 1, and added nonautomotive OPNs for MAX16956A, MAX16956B, and MAX16956C versions	8, 11, 15
2	3/14	Removed future product references	15
3	2/15	Updated the Benefits and Features section	1
4	8/15	Updated Block Diagram	9
5	10/15	Added top marks to Selector Guide	15
6	2/21	Increasing the output voltage range to 15V.	1,2,10,11,14

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