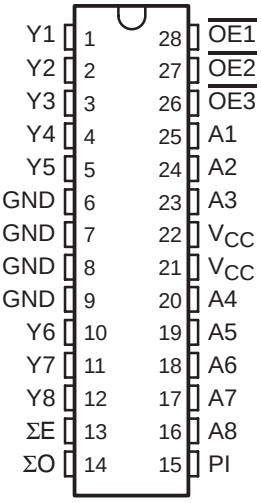
- **Inputs Are TTL-Voltage Compatible**
- **Combines '244 and '280 Functions In One Package**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

The 74ACT11656 contains eight noninverting buffers with 3-state outputs and a 9-bit parity generator/checker. The device is intended for bus-oriented applications.

When data is transmitted, the parity input (PI) terminal is configured as an input and combined with the A-input data to generate a flag on either parity output (ΣE or ΣO) terminal, depending on the number of inputs that are high.

The output-enable ($\overline{OE1}$, $\overline{OE2}$, and $\overline{OE3}$) inputs can be used to disable the device so that the buses are effectively isolated.

The 74ACT11656 is characterized for operation from −40°C to 85°C.

FUNCTION TABLES

INPUTS				OUTPUT
$\overline{OE1}$	$\overline{OE2}$	$\overline{OE3}$	A	Y
L	L	L	L	L
L	L	L	H	H
H	X	X	X	Z
X	H	X	X	Z
X	X	H	X	Z

NO. OF INPUTS HIGH (PI, A1−A8)	PARITY OUTPUTS	
	ΣE	ΣO
EVEN 0, 2, 4, 6, 8	H	L
ODD 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = high	Z	Z

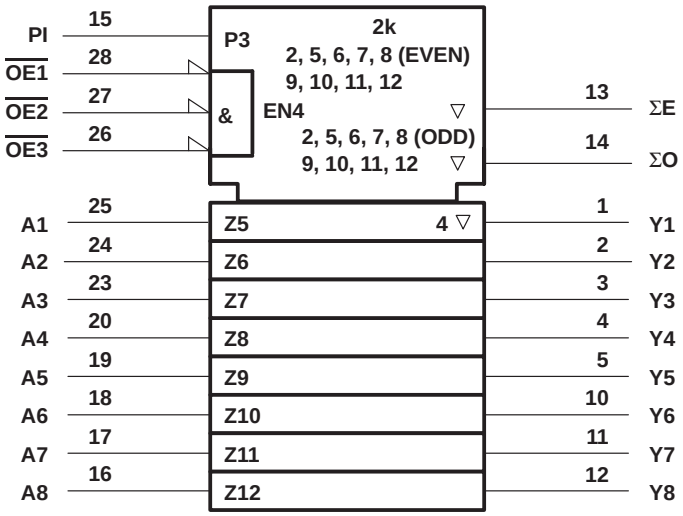
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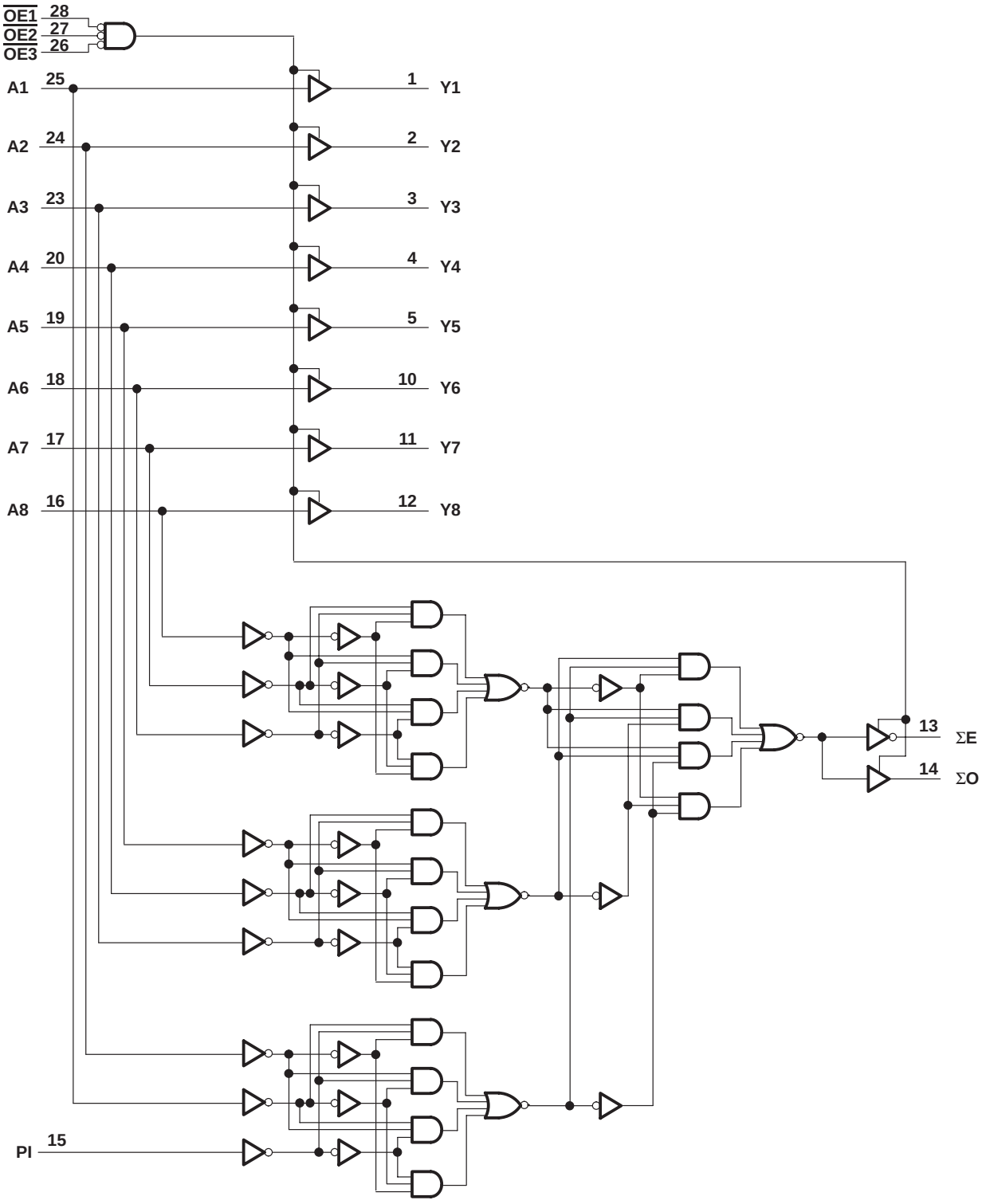
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±225 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 1.7 W
Operating free-air temperature range, T_A . . . . . −40° C to 85°C
Storage temperature range, T_{stg} . . . . . −65° C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta V$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 µA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
VOL	I_{OL} = 50 µA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND		5.5 V			±0.5		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			8		80	µA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		4.5				pF
C_o	$V_O = V_{CC}$ or GND		5 V		10				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

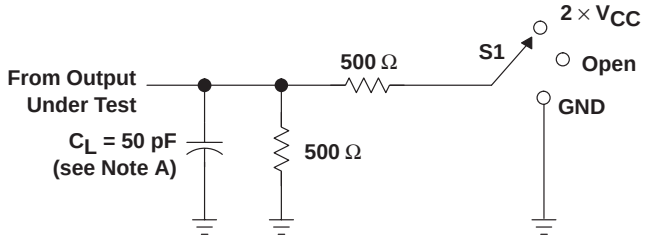
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	3.2	5.9	7.5	3.2	8.4	ns
t_{PHL}			2.5	5.9	8.3	2.5	9.5	
t_{PLH}	A	ΣE, ΣO	3.5	8.1	10.7	3.5	12	ns
t_{PHL}			3.9	8.7	11.4	3.9	13.2	
t_{PZH}	$\overline{OE}$	Y	2.5	6.6	9.6	2.5	11.2	ns
t_{PZL}			3.8	8.3	12.1	3.8	14.6	
t_{PHZ}	$\overline{OE}$	Y	4.9	7.8	10	4.9	10.9	ns
t_{PLZ}			5.1	7.6	9.2	5.1	9.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

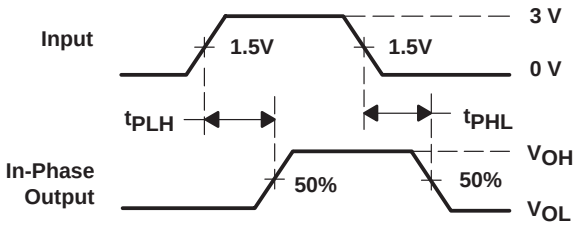
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF,	f = 1 MHz	70	pF
		Outputs disabled			22	

PARAMETER MEASUREMENT INFORMATION

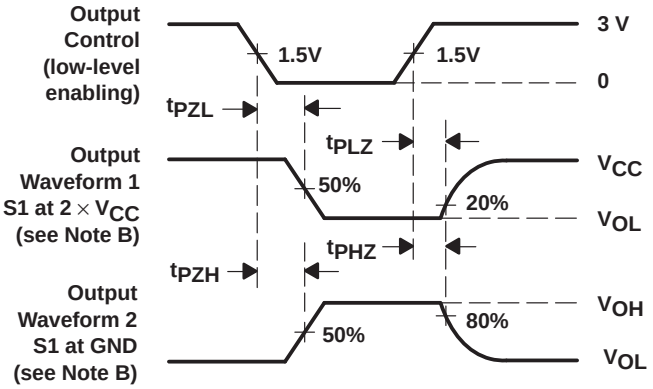


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74ACT11656DW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
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OBSOLETE: TI has discontinued the production of the device.

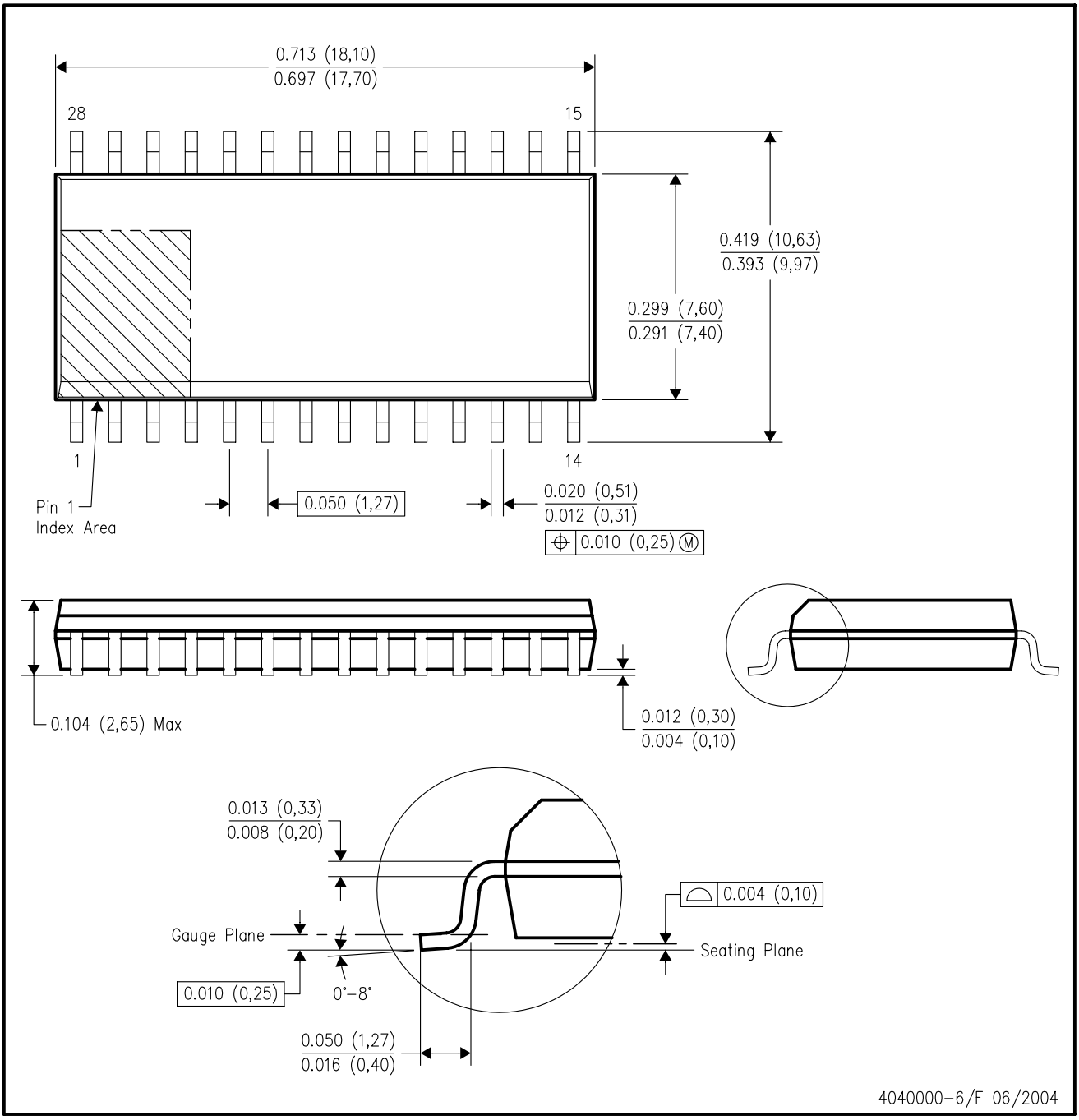
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R–PDSO–G28) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74ACT11656DW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI

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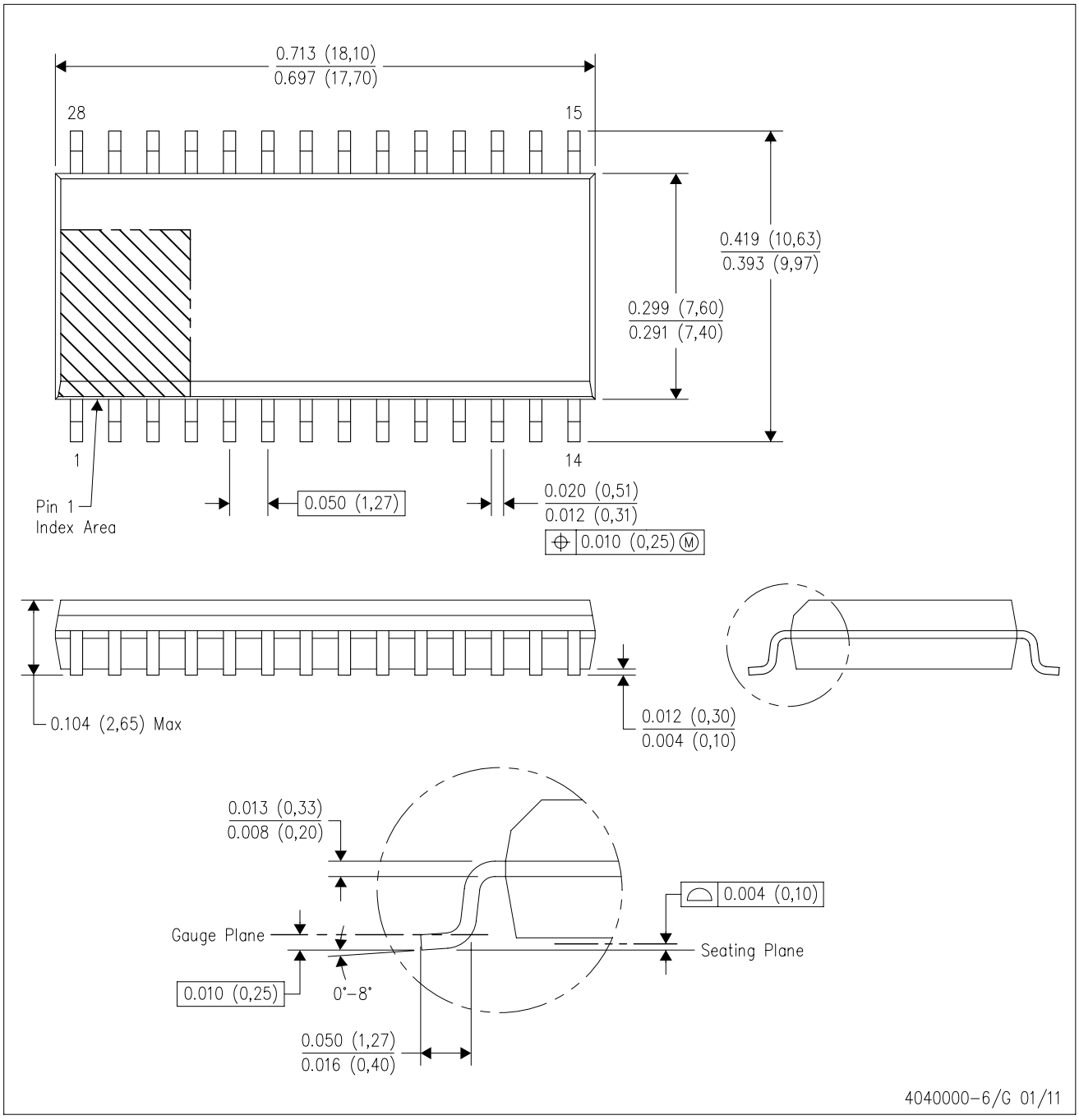
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



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D. Falls within JEDEC MS–013 variation AE.

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