Document Title

512K x16 bit Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History		Draft Date	Remark
0.0	Initial Draft		Sep. 28 , 2007	Preliminary
0.1	0.1 Revision	Fix typo error	Nov. 12, 2007	

Emerging Memory & Logic Solutions Inc.
4F Korea Construction Financial Cooperative B/D, 301-1 Yeon-Dong, Jeju-Si, Jeju-Do, Rep.of Korea Zip Code : 690-719
Tel : +82-64-740-1712 Fax : +82-64-740-1749~1750 / Homepage : www.emlsi.com

The attached data sheets are provided by EMLSI reserve the right to change the specifications and products. EMLSI will answer to your questions about device. If you have any questions, please contact the EMLSI office.

EM680FU16A Series
Low Power, 512Kx16 SRAM

FEATURES

- Process Technology : 0.15μm Full CMOS
- Organization : 512K x 16 bit
- Power Supply Voltage : 2.7V ~ 3.3V
- Low Data Retention Voltage : 1.5V(Min.)
- Three state output and TTL Compatible
- Package Type : 48-FPBGA 8.0x10.0

GENERAL DESCRIPTION

The EM680FU16A families are fabricated by EMLSI's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Typ.)	Operating (I_{CC1}.Max)	
EM680FU16A-45LF	Industrial (-40 ~ 85°C)	2.7V~3.3V	45ns	2 μA	3mA	48-FPBGA
EM680FU16A-55LF	Industrial (-40 ~ 85°C)	2.7V~3.3V	55ns	2 μA	3mA	48-FPBGA
EM680FU16A-70LF	Industrial (-40 ~ 85°C)	2.7V~3.3V	70ns	2 μA	3mA	48-FPBGA

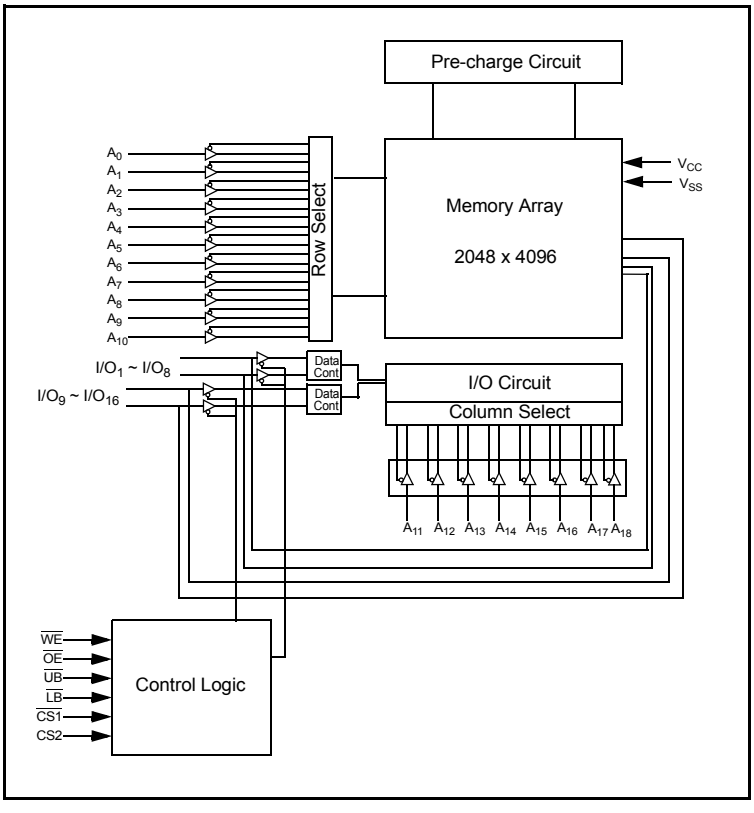
PIN DESCRIPTION

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	CS2
B	I/O_9	$\overline{UB}$	A_3	A_4	$\overline{CS1}$	I/O_1
C	I/O_{10}	I/O_{11}	A_5	A_6	I/O_2	I/O_3
D	V_{SS}	I/O_{12}	A_{17}	A_7	I/O_4	V_{CC}
E	V_{CC}	I/O_{13}	DNU	A_{16}	I/O_5	V_{SS}
F	I/O_{15}	I/O_{14}	A_{14}	A_{15}	I/O_6	I/O_7
G	I/O_{16}	DNU	A_{12}	A_{13}	$\overline{WE}$	I/O_8
H	A_{18}	A_8	A_9	A_{10}	A_{11}	DNU

48-FPBGA : Top view (ball down)

Name	Function	Name	Function
$\overline{CS1}$,CS2	Chip select inputs	Vcc	Power Supply
$\overline{OE}$	Output Enable input	Vss	Ground
$\overline{WE}$	Write Enable input	$\overline{UB}$	Upper Byte ($I/O_{9\sim16}$)
A_0~A_{18}	Address Inputs	$\overline{LB}$	Lower Byte ($I/O_{1\sim8}$)
I/O_1~I/O_{16}	Data Inputs/outputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Minimum	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.2 to 4.0V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	^oC

* Stresses greater than those listed above “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O_{1-8}	I/O_{9-16}	Mode	Power
H	X	X	X	X	X	High-Z	High-Z	Deselected	Stand by
X	L	X	X	X	X	High-Z	High-Z	Deselected	Stand by
X	X	X	X	H	H	High-Z	High-Z	Deselected	Stand by
L	H	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	H	L	H	L	L	Data Out	Data Out	Word Read	Active
L	H	X	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	H	X	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	H	X	L	L	L	Data In	Data In	Word Write	Active

NOTE: X means don’t care. (Must be low or high state)

RECOMMENDED DC OPERATING CONDITIONS [1)]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	-	V_{CC} + 0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

1. T_A= -40 to 85°C, otherwise specified.
2. Overshoot: V_{CC} +2.0 V in case of pulse width ≤ 20ns
3. Undershoot: -2.0 V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f =1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Ouput capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

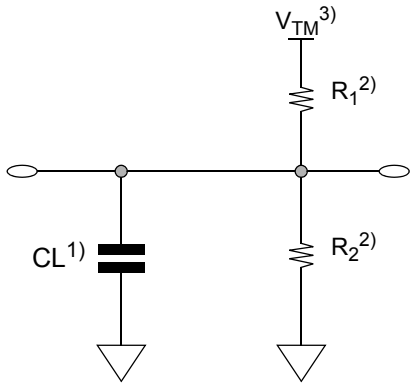
DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1	-	1	uA
Output leakage current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{LB}$=$\overline{UB}$=V_{IH} V_{IO}=V_{SS} to V_{CC}		-1	-	1	uA
Operating power supply	I_{CC}	I_{IO}=0mA, $\overline{CS1}$=V_{IL}, CS2=$\overline{WE}$=V_{IH}, V_{IN}=V_{IH} or V_{IL}		-	-	3	mA
Average operating current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, $\overline{CS1}$≤0.2V, $\overline{LB}$≤0.2V or/and $\overline{UB}$≤0.2V, CS2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V		-	-	3	mA
	I_{CC2}	Cycle time = Min, I_{IO}=0mA, 100% duty, $\overline{CS1}$=V_{IL}, CS2=V_{IH}, $\overline{LB}$=V_{IL} or/and $\overline{UB}$=V_{IL} , V_{IN}=V_{IL} or V_{IH}	45ns	-	-	40	mA
			55ns	-	-	30	
			70ns	-	-	20	
Output low voltage	V_{OL}	I_{OL} = 2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0mA		2.2	-	-	V
Standby Current (TTL)	I_{SB}	$\overline{CS1}$=V_{IH}, CS2=V_{IL}, Other inputs=V_{IH} or V_{IL}		-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS1}$≥V_{CC}-0.2V, CS2≥V_{CC}-0.2V ($\overline{CS1}$ controlled) or 0V≤CS2≤0.2V (CS2 controlled), Other inputs = 0~V_{CC} (Typ. condition : V_{CC}=3.0V @ 25°C) (Max. condition : V_{CC}=3.3V @ 85°C)	LF	-	2	15	uA

AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.4 to 2.2V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : 1.5V
Output Load (See right) : CL = 100pF+ 1 TTL (70ns)
CL[1)] = 30pF + 1 TTL (45ns/55ns)



1. Including scope and Jig capacitance
2. R_1=3070 ohm, R_2=3150 ohm
3. V_{TM}=2.8V
4. CL = 5pF + 1 TTL (measurement with $t_{LZ1,2}$, t_{HZ12}, t_{OLZ}, t_{OHZ}, t_{WHZ})

READ CYCLE (V_{CC} =2.7 to 3.3V, Gnd = 0V, T_A = -40°C to +85°C)

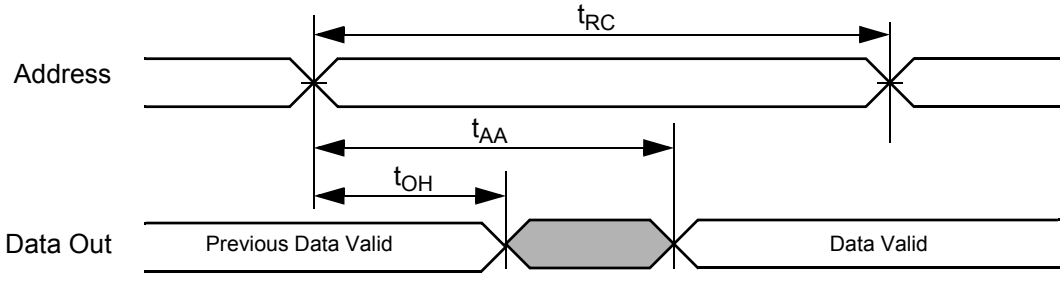
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	45	-	55	-	70	-	ns
Address access time	t_{AA}	-	45	-	55	-	70	ns
Chip select to output	t_{CO1}, t_{CO2}	-	45	-	55	-	70	ns
Output enable to valid output	t_{OE}	-	30	-	35	-	35	ns
$\overline{UB}$, $\overline{LB}$ Access time	t_{BA}	-	45	-	55	-	70	ns
Chip select to low-Z output	t_{LZ1}, t_{LZ2}	5	-	5	-	5	-	ns
$\overline{UB}$, $\overline{LB}$ enable to low-Z output	t_{BLZ}	5	-	5	-	5	-	ns
Output enable to low-Z output	t_{OLZ}	5	-	5	-	5	-	ns
Chip disable to high-Z output	t_{HZ1}, t_{HZ2}	0	20	0	20	0	25	ns
$\overline{UB}$, $\overline{LB}$ disable to high-Z output	t_{BHZ}	0	20	0	20	0	25	ns
Output disable to high-Z output	t_{OHZ}	0	20	0	20	0	25	ns
Output hold from address change	t_{OH}	10	-	10	-	10	-	ns

WRITE CYCLE (V_{CC} =2.7 to 3.3V, Gnd = 0V, T_A = -40°C to +85°C)

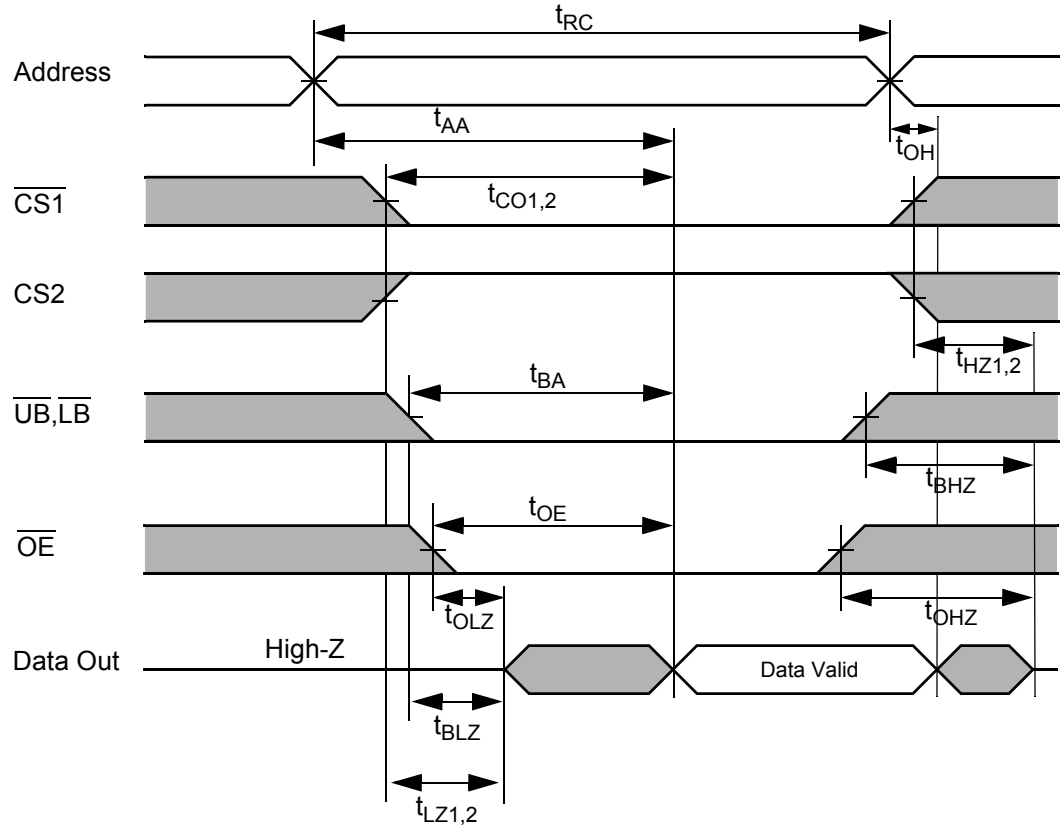
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	45	-	55	-	70	-	ns
Chip select to end of write	t_{CW1}, t_{CW2}	45	-	45	-	60	-	ns
Address setup time	t_{AS}	0	-	0	-	0	-	ns
Address valid to end of write	t_{AW}	45	-	45	-	60	-	ns
$\overline{UB}$, $\overline{LB}$ valid to end of write	t_{BW}	45	-	45	-	60	-	ns
Write pulse width	t_{WP}	45	-	45	-	55	-	ns
Write recovery time	t_{WR}	0	-	0	-	0	-	ns
Write to ouput high-Z	t_{WHZ}	0	20	0	20	0	25	ns
Data to write time overlap	t_{DW}	25	-	30	-	30	-	ns
Data hold from write time	t_{DH}	0	-	0	-	0	-	ns
End write to output low-Z	t_{OW}	5	-	5		5	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1). (Address Controlled, $\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=$\overline{WE}$=V_{IL})



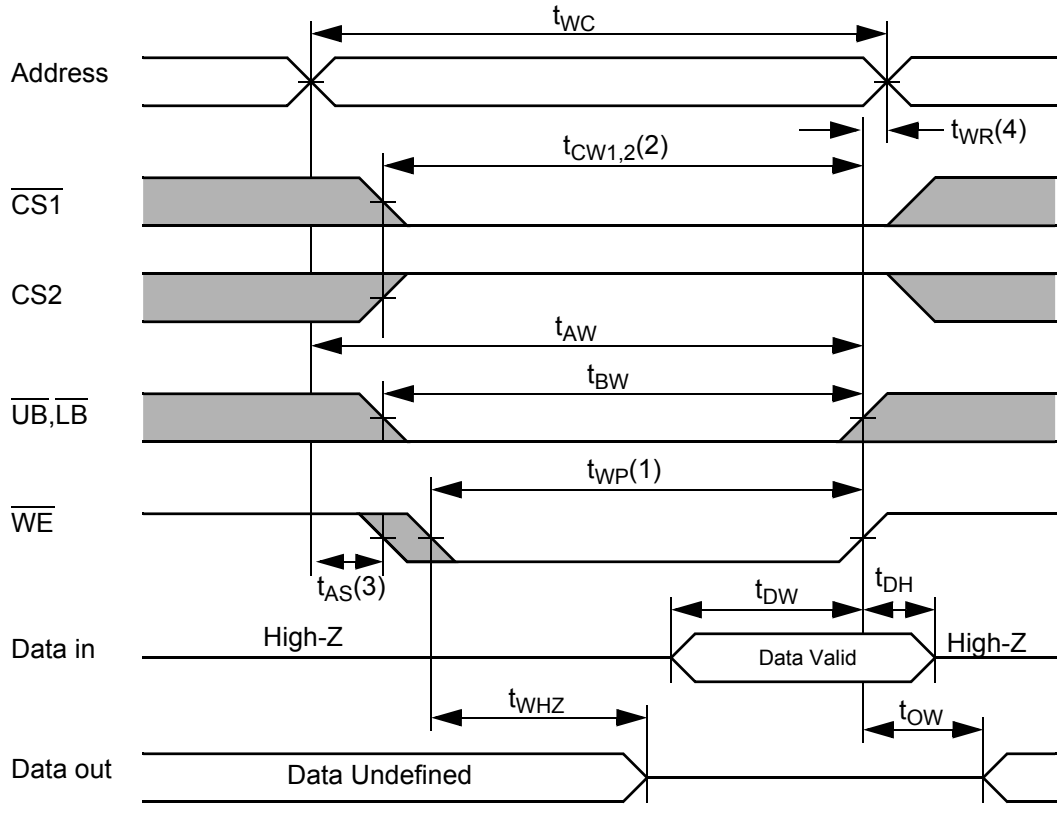
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$ = V_{IH})



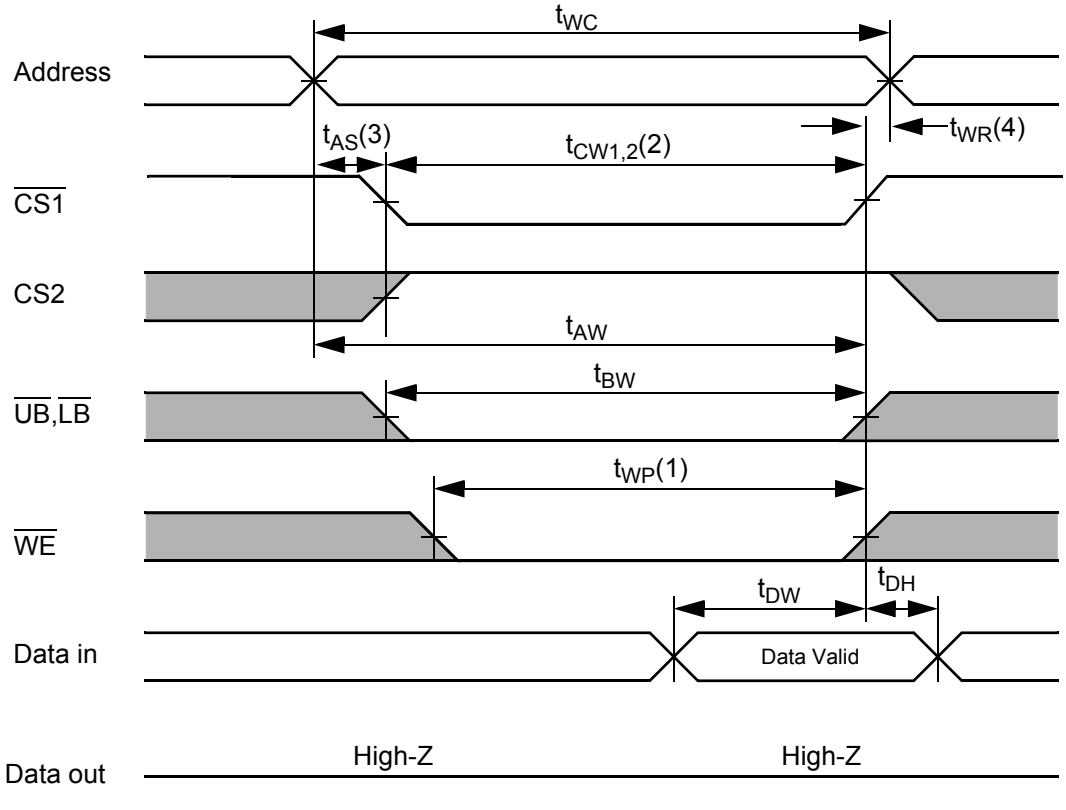
NOTES (READ CYCLE)

1. $t_{HZ1,2}$ and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referanced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ1,2}$(Max.) is less than $t_{LZ1,2}$(Min.) both for a given device and from device to device interconnection.

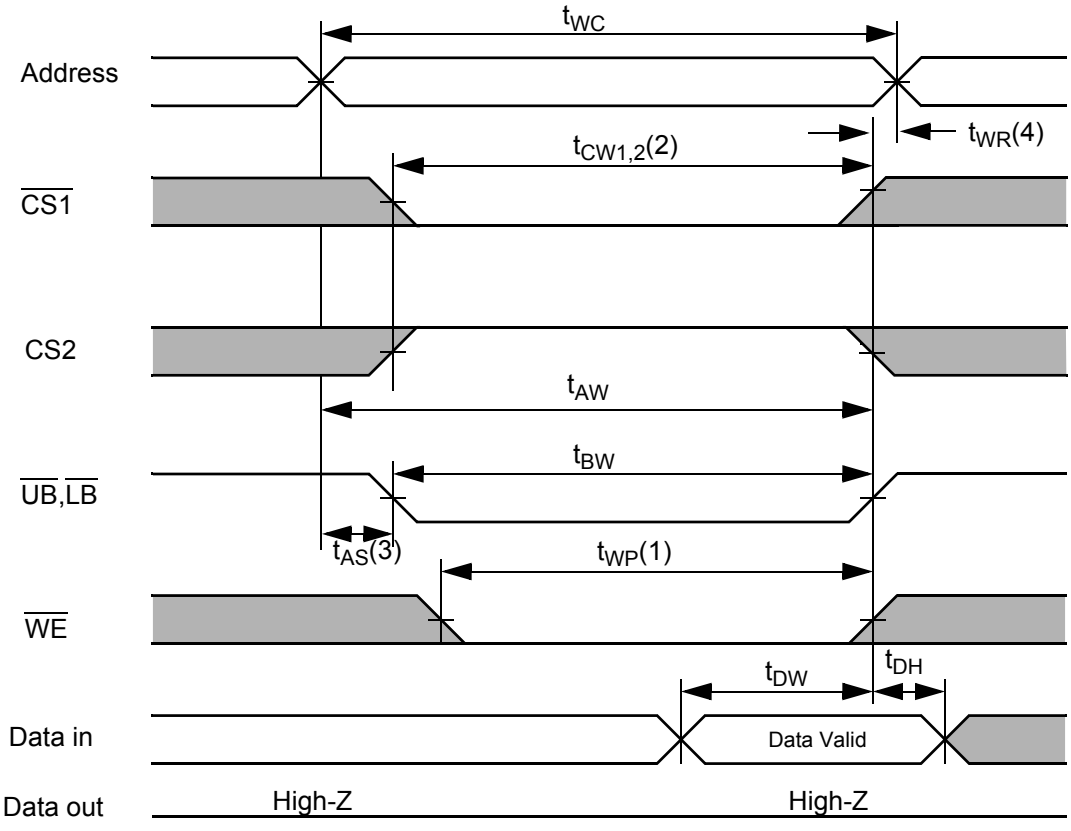
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ CONTROLLED)



NOTES (WRITE CYCLE)

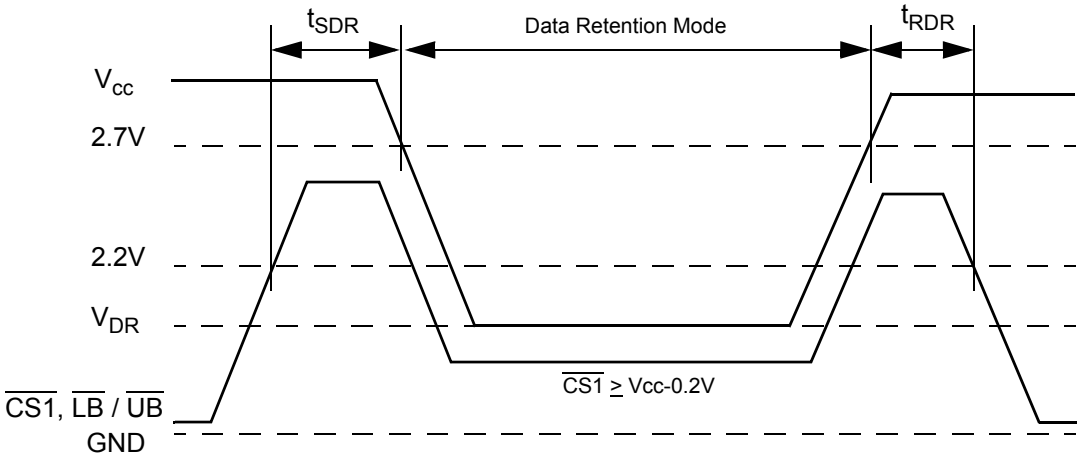
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$, a high CS2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ goes low, CS2 goes high and $\overline{WE}$ goes low. A write ends at the earliest transition among $\overline{CS1}$ goes high, CS2 goes low and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW1} is measured from the $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low.

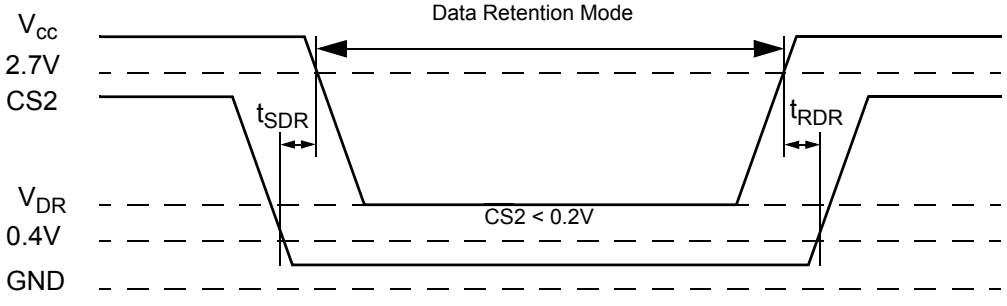
DATA RETENTION CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS}_1 \geq$ Vcc-0.2V [1)]	1.5	-	3.3	V
Data Retention Current	I_{DR}	V_{CC}=1.5V, $\overline{CS}_1 \geq$ Vcc-0.2V [1)]	-	-	4	uA
Chip Deselect to Data Retention Time	t_{SDR}	See data retention wave form	0	-	-	ns
Operation Recovery Time	t_{RDR}		t_{RC}	-	-	

1. $\overline{CS1} \geq$ Vcc-0.2V , CS2 $\geq$ Vcc-0.2V ($\overline{CS1}$ controlled) or CS2 $\leq$ 0.2V (CS2 controlled)

DATA RETENTION WAVE FORM



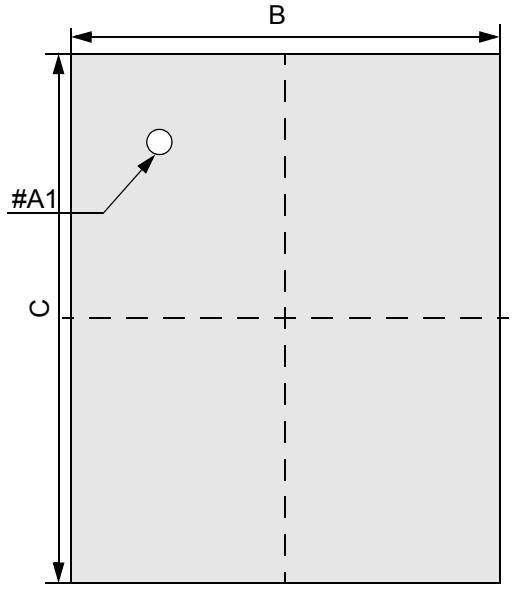


Unit: millimeters

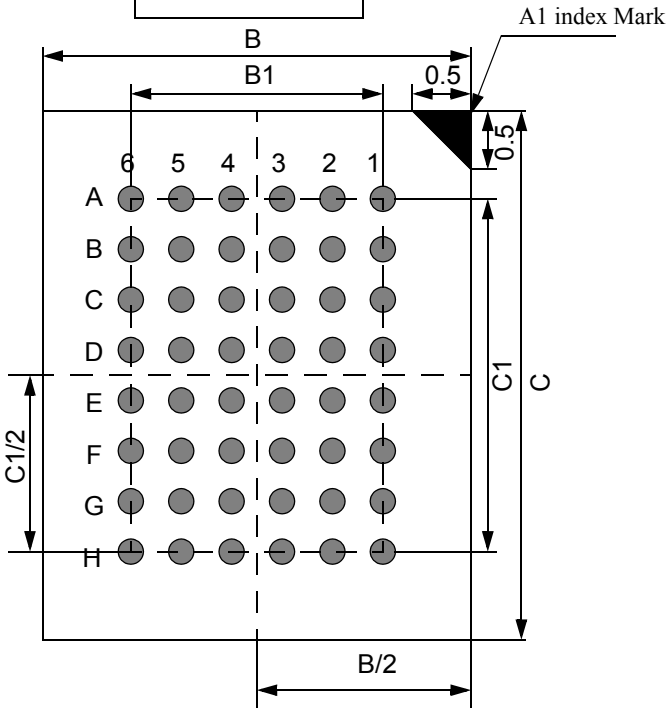
PACKAGE DIMENSION

48 Ball Fine Pitch BGA (0.75mm ball pitch)

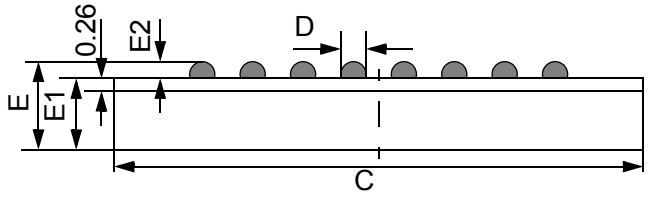
Top View



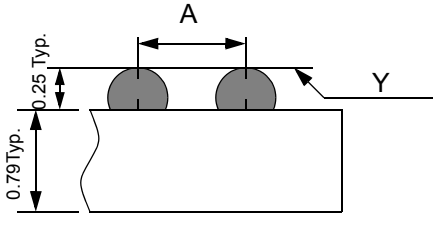
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.75	-
B	7.90	8.00	8.10
B1	-	3.75	-
C	9.90	10.00	10.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.04	1.10
E1	-	0.79	-
E2	-	0.25	-
Y	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)

SRAM PART CODING SYSTEM

EM X XX X X X XX X X - XX XX

1. EMLSI Memory
2. Product Type
3. Density
4. Function
5. Technology
6. Operating Voltage
7. Organization
8. Generation
9. Package
10. Speed
11. Power

1. Memory Component
EM ---------- Memory

2. Product Type
6 ---------- SRAM

3. Density
1 ---------- 1M
2 ---------- 2M
4 ---------- 4M
8 ---------- 8M

4. Function
0 ---------- Dual CS
1 ---------- Single CS
2 ---------- Multiplexed
3 ---------- Single CS / LBB, UBB(tBA=tOE)
4 ---------- Single CS / LBB, UBB(tBA=tCO)
5 ---------- Dual CS / LBB, UBB(tBA=tOE)
6 ---------- Dual CS / LBB, UBB(tBA=tCO)

5. Technology
F ---------- Full CMOS

6. Operating Voltage
T ---------- 5.0V
V ---------- 3.3V
U ---------- 3.0V
S ---------- 2.5V
R ---------- 2.0V
P ---------- 1.8V

7. Organization
8 ---------- x8 bit
16 ---------- x16 bit

8. Generation
Blank ---------- 1st generation
A ---------- 2nd generation
B ---------- 3rd generation
C ---------- 4th generation
D ---------- 5th generation
E ---------- 6th generation
F ---------- 7th generation
G ---------- 8th generation

9. Package
Blank ---------- KGD, 48&36FpBGA
S ---------- 32 sTSOP1
T ---------- 32 TSOP1
U ---------- 44 TSOP2
V ---------- 32 SOP

10. Speed
45 ---------- 45ns
55 ---------- 55ns
70 ---------- 70ns
85 ---------- 85ns
10 ---------- 100ns
12 ---------- 120ns

11. Power
LL ---------- Low Low Power
LF ---------- Low Low Power(Pb-Free & Green)
L ---------- Low Power
S ---------- Standard Power