Document Title

128K X 8 BIT 3.3V HIGH SPEED LOW VCC CMOS SRAM

Revision History

Rev. No.	History	Issue Date	Remark
2.0	Add product family and 32-pin TSSOP package	May 9, 2002	Final
2.1	Add 36 ball BGA package type	August 22, 2002	

AMIC

LP61L1024

128K X 8 BIT 3.3V HIGH SPEED LOW VCC CMOS SRAM

Features

- Single +3.3V power supply
- Access times: 12/15 ns (max.)
- Current: Operating: 170mA (max.)
  Standby: 10mA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL compatible
- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 2.0V (min.)
- Available in 32-pin SOJ 300 mil, 32-pin TSOP and 32-pin TSSOP and 36-pin CSP packages

General Description

The LP61L1024 is a low operating current 1,048,576-bit static random access memory organized as 131,072 words by 8 bits and operates on a single 3.3V power supply.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.
Two chip enable inputs are provided for POWER-DOWN and device enable and an output enable input is included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 2.0V.

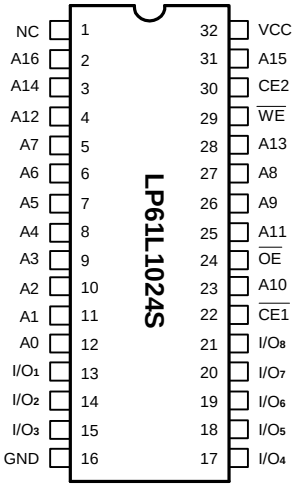
Product Family

Product Family	Operating Temperature	VCC Range	Speed	Power Dissipation			Package Type
				Data Retention (I_{CCDR}, Typ.)	Standby (I_{SB1}, Typ.)	Operating (I_{CC1}, Typ.)	
LP61L1024	0°C ~ 70°C	3V ~ 3.6V	12/15 ns	0.4mA	0.5mA	130mA	32L SOJ 32L TSOP 32L TSSOP 36B μBGA

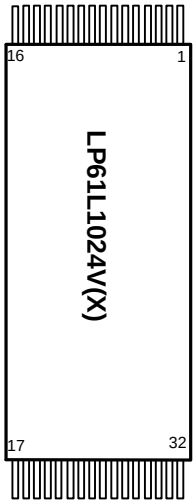
1. Typical values are measured at VCC = 3.0V, T_A = 25°C and not 100% tested.
2. Data retention current VCC = 2.0V.

Pin Configurations

■ **SOJ**



■ **TSOP / TSSOP**

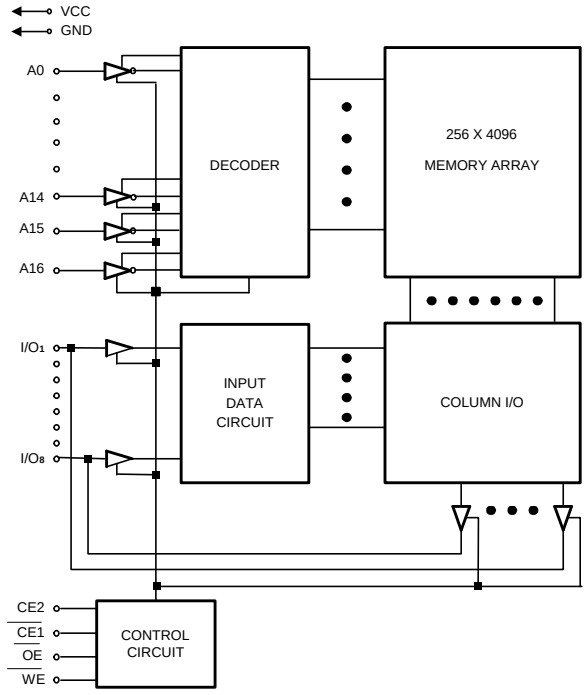


Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A11	A9	A8	A13	$\overline{WE}$	CE2	A15	VCC	NC	A16	A14	A12	A7	A6	A5	A4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A3	A2	A1	A0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A10	$\overline{OE}$

■ **CSP (Chip Size Package)**
36-pin Top View

	1	2	3	4	5	6
A	A0	A1	NC	A3	A6	A8
B	I/O4	A2	$\overline{WE}$	A4	A7	I/O6
C	I/O5		NC	A5		I/O1
D	GND					VCC
E	VCC					GND
F	I/O6		NC	NC		I/O2
G	I/O7	$\overline{OE}$	$\overline{CE1}$	A16	A15	I/O3
H	A9	A10	A11	A12	A13	A14

Block Diagram



Pin Description

Pin No.	Symbol	Description
2 - 12, 23, 25 - 28, 31	A0 - A16	Address Inputs
29	$\overline{WE}$	Write Enable
24	$\overline{OE}$	Output Enable
22	$\overline{CE1}$	Chip Enable
30	CE2	Chip Enable
1	NC	No Connection
13 - 15, 17 - 21	I/O1 - I/O8	Data Input/Outputs
32	VCC	Power Supply
16	GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	0	+0.8	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND ..... -0.5V to +7.0V
IN, IN/OUT Volt to GND .....-0.5V to VCC +0.5V
Operating Temperature, Topr ..... 0°C to +70°C
Storage Temperature, Tstg..... -55°C to +125°C
Temperature Under Bias, Tbias..... -10°C to +85°C
Power Dissipation, Pt.....1.0W
Soldering Temp. & Time .....260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C, VCC = 3.3V + 10%, GND = 0V)

Symbol	Parameter	LP61L1024-12/15		Unit	Conditions
		Min.	Max.		
$\lvert I_{LI} \rvert$	Input Leakage Current	-	2	µA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage Current	-	2	µA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to VCC
I_{CC1} (1)	Dynamic Operating Current	-	170	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} $I_{I/O}$ = 0 mA
I_{SB}	Standby Power Supply Current	-	30	mA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}
I_{SB1}		-	10	mA	$\overline{CE1}$ ≥ VCC - 0.2V, CE2 ≥ VCC - 0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ VCC - 0.2V
I_{SB2}		-	10	mA	$\overline{CE1}$ ≤ 0.2V, CE2 ≤ 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ VCC - 0.2V
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -4 mA

Note: 1. I_{CC1} is dependent on output loading, cycle rates, and Read/Write patterns

Truth Table

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB2}
Output Disable	L	H	H	H	High Z	I_{CC1}
Read	L	H	L	H	D_{OUT}	I_{CC1}
Write	L	H	X	L	D_{IN}	I_{CC1}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		8	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		10	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, VCC = 3.3V + 10, GND = 0V)

Symbol	Parameter		LP61L1024-12		LP61L1024-15		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
t_{RC}	Read Cycle Time		12	-	15	-	ns
t_{AA}	Address Access Time		-	12	-	15	ns
t_{ACE1}	Chip Enable Access Time	$\overline{CE1}$	-	12	-	15	ns
t_{ACE2}		CE2	-	12	-	15	ns
t_{OE}	Output Enable to Output Valid		-	7	-	9	ns
t_{CLZ1}	Chip Enable to Output in Low Z	$\overline{CE1}$	3	-	5	-	ns
t_{CLZ2}		CE2	3	-	5	-	ns
t_{OLZ}	Output Enable to Output in Low Z		2	-	2	-	ns
t_{CHZ1}	Chip Disable to Output in High Z	$\overline{CE1}$	-	7	-	10	ns
t_{CHZ2}		CE2	-	7	-	10	ns
t_{OHZ}	Output Disable to Output in High Z		2	7	2	9	ns
t_{OH}	Output Hold from Address Change		3	-	5	-	ns

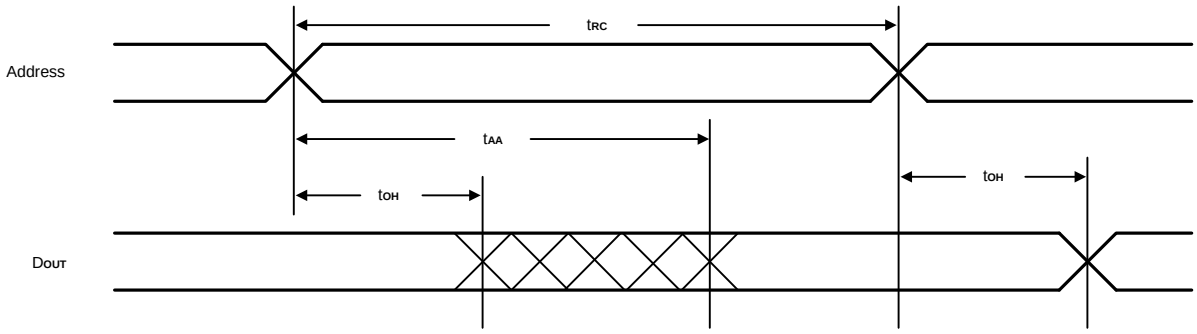
AC Characteristics (continued)

Symbol	Parameter	LP61L1024-12		LP61L1024-15		Unit
		Min.	Max.	Min.	Max.	
Write Cycle						
t_{WC}	Write Cycle Time	12	-	15	-	ns
t_{CW}	Chip Enable to End of Write	10	-	12	-	ns
t_{AS}	Address Setup Time of Write	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	10	-	12	-	ns
t_{WP}	Write Pulse Width	8	-	10	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{WHZ}	Write to Output in High Z	0	7	0	8	ns
t_{DW}	Data to Write Time Overlap	8	-	10	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	ns
t_{OW}	Output Active from End of Write	5	-	5	-	ns

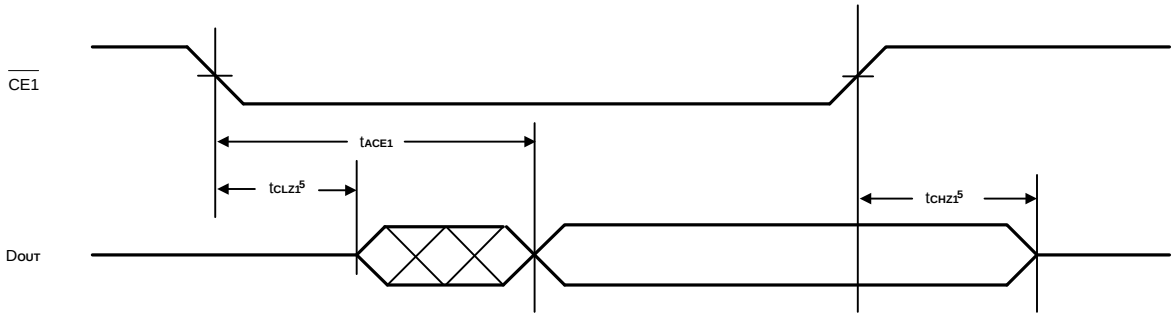
Notes: t_{CHZ1}, t_{CHZ2}, t_{OHZ}, and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

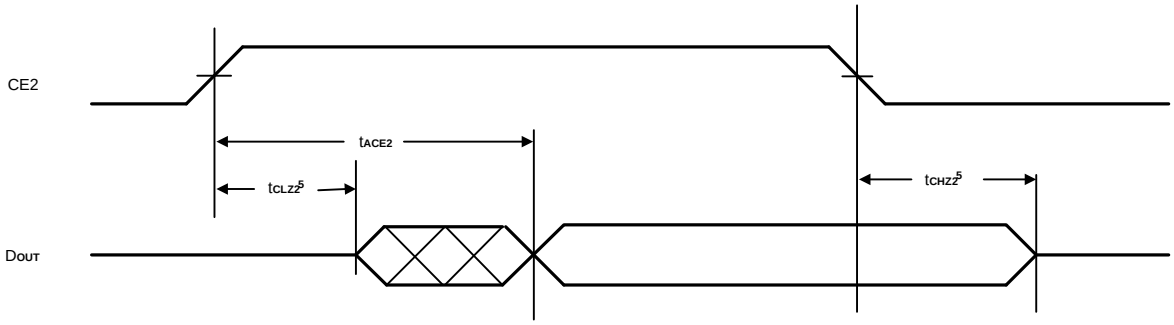
Read Cycle 1 (1, 2, 4)



Read Cycle 2 [1, 3, 4, 6]

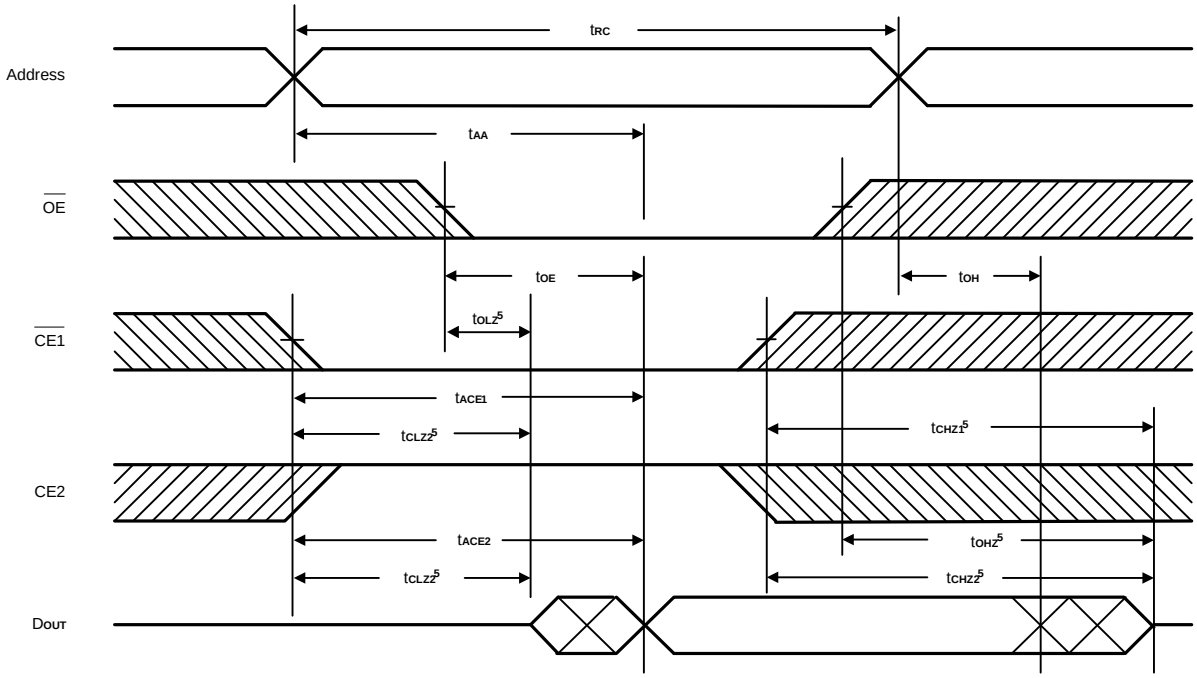


Read Cycle 3 [1, 4, 7, 8]



Timing Waveforms (continued)

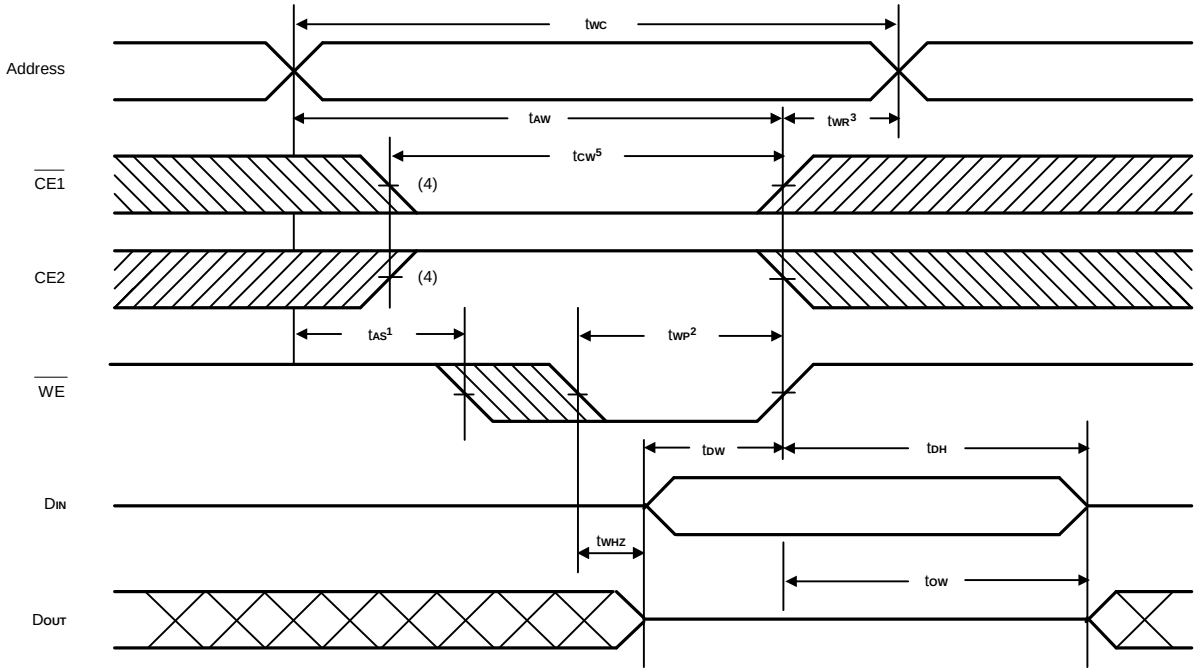
Read Cycle 4 (1)



Notes:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE1}$ = V_{IL} and CE2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CE2 is high.
7. $\overline{CE1}$ is low.
8. Address valid prior to or coincident with CE2 transition high.

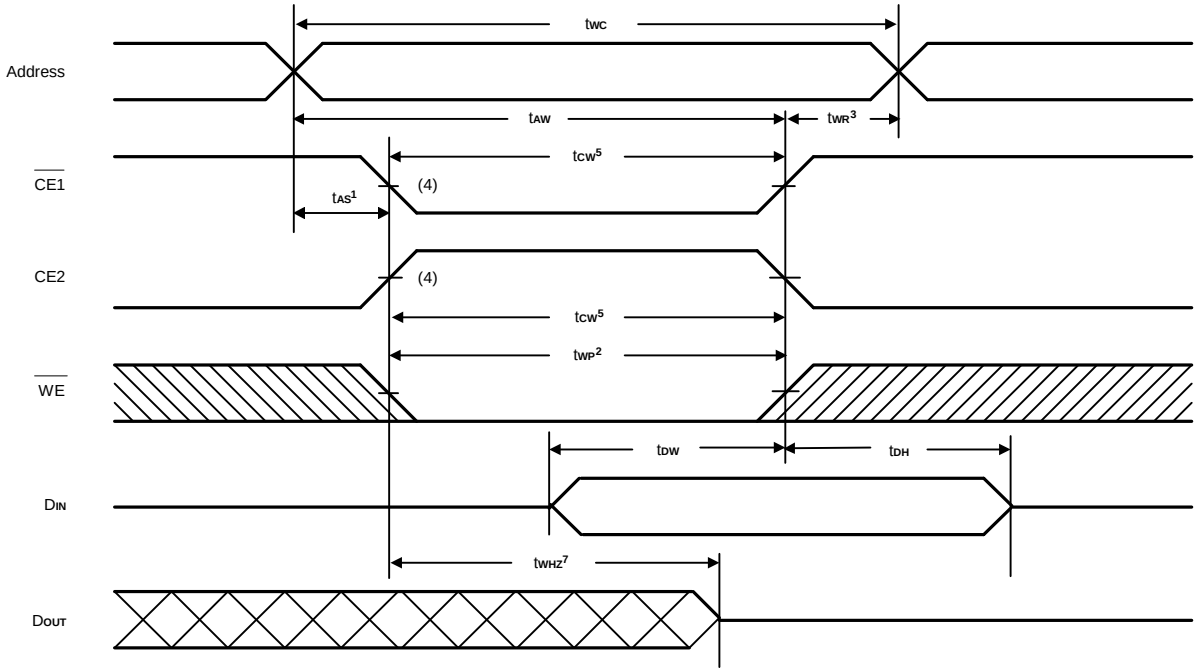
Timing Waveforms (continued)

Write Cycle 1[6]
(Write Enable Controlled)



Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low to the end of the Write cycle.
4. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE}$ going low or CE2 going high to the end of Write.
6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

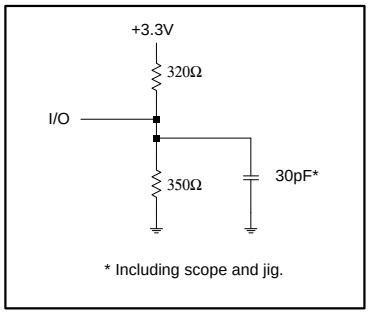


Figure 1. Output Load

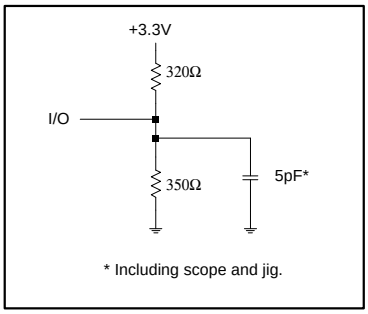
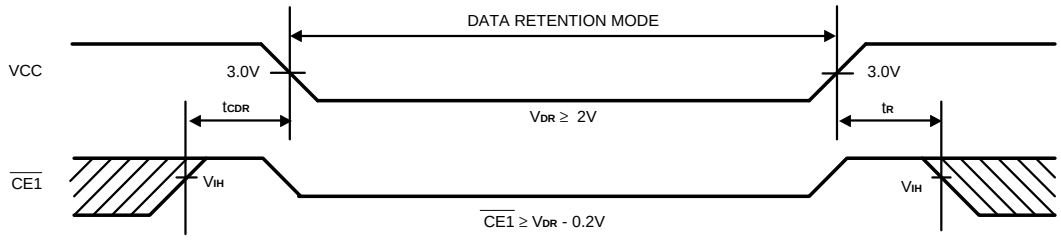


Figure 2. Output Load for t_{CLZ1}, t_{CLZ2}, t_{OHZ}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{WHZ}, and t_{OW}

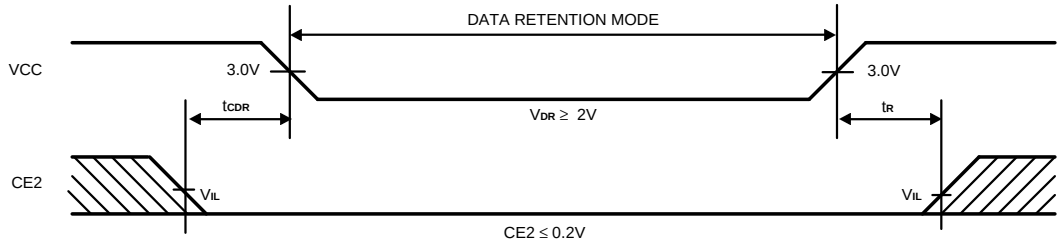
Data Retention Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR1}	VCC for Data Retention	2	3.6	V	$\overline{CE1} \geq$ VCC - 0.2V CE2 ≥ VCC - 0.2V or CE2 ≤ 0.2V
V_{DR2}		2	3.6	V	CE2 ≤ 0.2V $\overline{CE1} \geq$ VCC - 0.2V or $\overline{CE1} \leq$ 0.2V
I_{CCDR1}	Data Retention Current	-	5	mA	VCC = 3.0V $\overline{CE1} \geq$ VCC - 0.2V CE2 ≥ VCC - 0.2V $V_{IN} \geq$ VCC - 0.2V or $V_{IN} \leq$ 0.2V
I_{CCDR2}		-	5	mA	VCC = 3.0V CE2 ≤ 0.2V $\overline{CE1} \leq$ 0.2V $V_{IN} \geq$ VCC - 0.2V or $V_{IN} \leq$ 0.2V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	5	-	ms	

Low VCC Data Retention Waveform (1) ($\overline{CE1}$ Controlled)



Low VCC Data Retention Waveform (2) (CE2 Controlled)



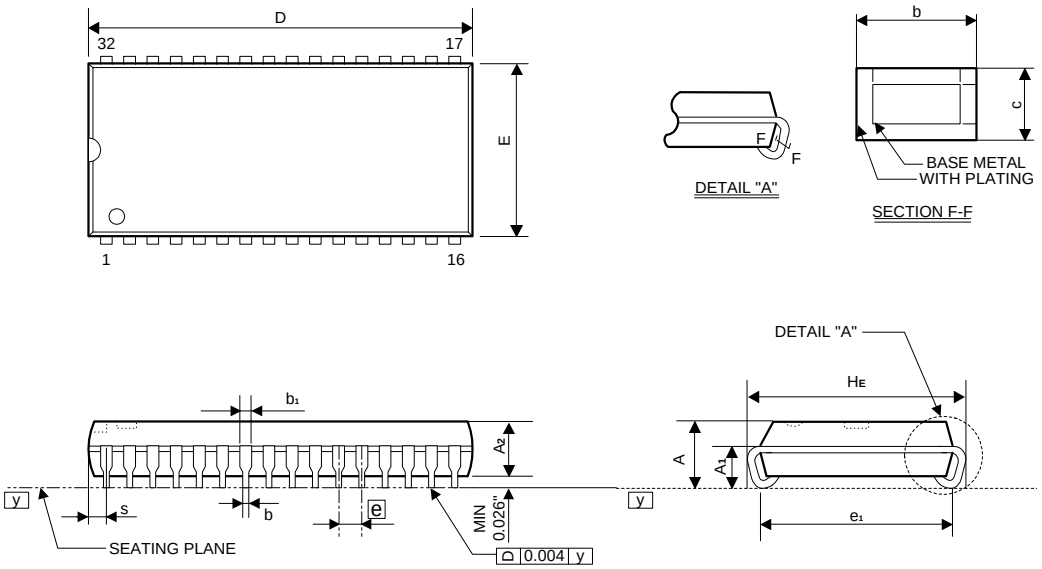
Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
LP61L1024S-12	12	170	10	32L SOJ (300 mil)
LP61L1024V-12	12	170	10	32L TSOP
LP61L1024X-12	12	170	10	32L TSSOP
LP61L1024U-12	12	170	10	36L CSP
LP61L1024S-15	15	170	10	32L SOJ (300 mil)
LP61L1024V-15	15	170	10	32L TSOP
LP61L1024X-15	15	170	10	32L TSSOP
LP61L1024U-15	15	170	10	36L CSP

Package Information

SOJ 32/32LD (300mil BODY) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0128	0.132	0.140	3.25	3.35	3.56
A_1	0.052	-	-	2.08	-	-
A_2	0.095	0.100	0.105	2.41	2.54	2.67
b	0.016	0.018	0.020	0.41	0.46	0.51
b_1	0.026	0.028	0.032	0.66	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.825	0.830	20.83	20.96	21.08
H_E	0.330	0.335	0.340	8.39	8.51	8.63
E	0.295	0.300	0.305	7.49	7.62	7.75
e_1	0.260	0.267	0.274	6.61	6.78	6.96
e	-	0.050	-	-	1.27	-
s	-	-	0.048	-	-	1.22
y	-	-	0.004	-	-	0.10

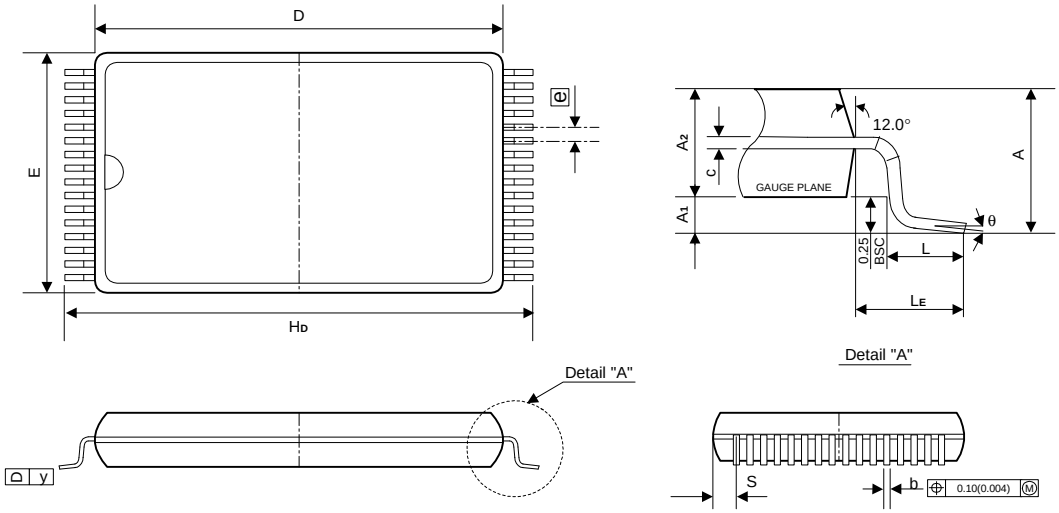
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E doesn't include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information

TSOP 32L TYPE I (8 X 20mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.047 Max.	1.20 Max.
A_1	0.004±0.002	0.10±0.05
A_2	0.039±0.002	1.00±0.05
b	0.008±0.001	0.20±0.03
c	0.006±0.001	0.15±0.02
D	0.724±0.004	18.40±0.10
E	0.315±0.004	8.00±0.10
e	0.020 TYP.	0.50 TYP.
H_D	0.787±0.007	20.00±0.20
L	0.020±0.004	0.50±0.10
L_E	0.031 TYP.	0.80 TYP.
S	0.0167 TYP.	0.425 TYP.
Y	0.004 Max.	0.10 Max.
θ	0° ~ 6°	0° ~ 6°

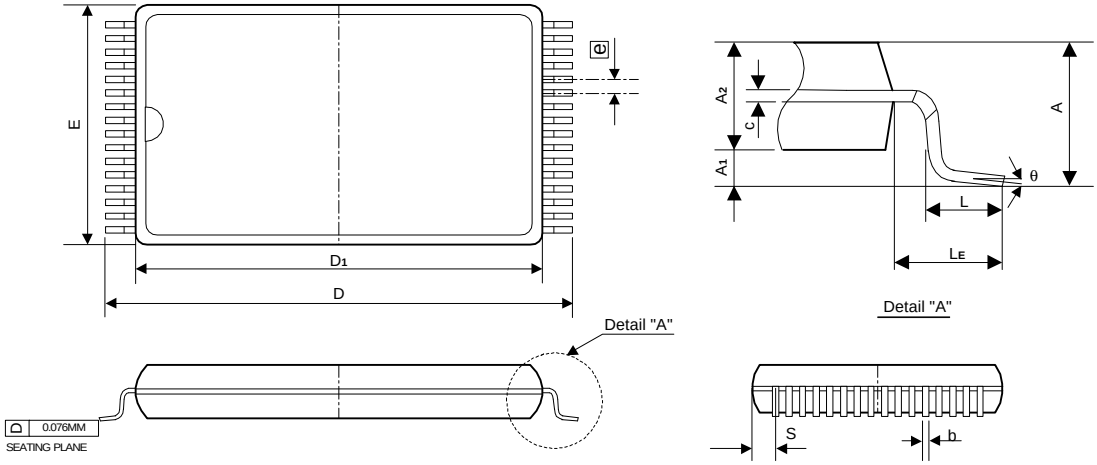
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information

TSSOP 32L TYPE I (8 X 13.4mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.049	-	-	1.25
A_1	0.002	-	-	0.05	-	-
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.0056	0.0059	0.0062	0.142	0.150	0.158
E	0.311	0.315	0.319	7.90	8.00	8.10
e	0.020 TYP			0.50 TYP		
D	0.520	0.528	0.535	13.20	13.40	13.60
D_1	0.461	0.465	0.469	11.70	11.80	11.90
L	0.012	0.020	0.028	0.30	0.50	0.70
L_E	0.0275	0.0315	0.0355	0.700	0.800	0.900
S	0.0109 TYP			0.278 TYP		
θ	0°	3°	5°	0°	3°	5°

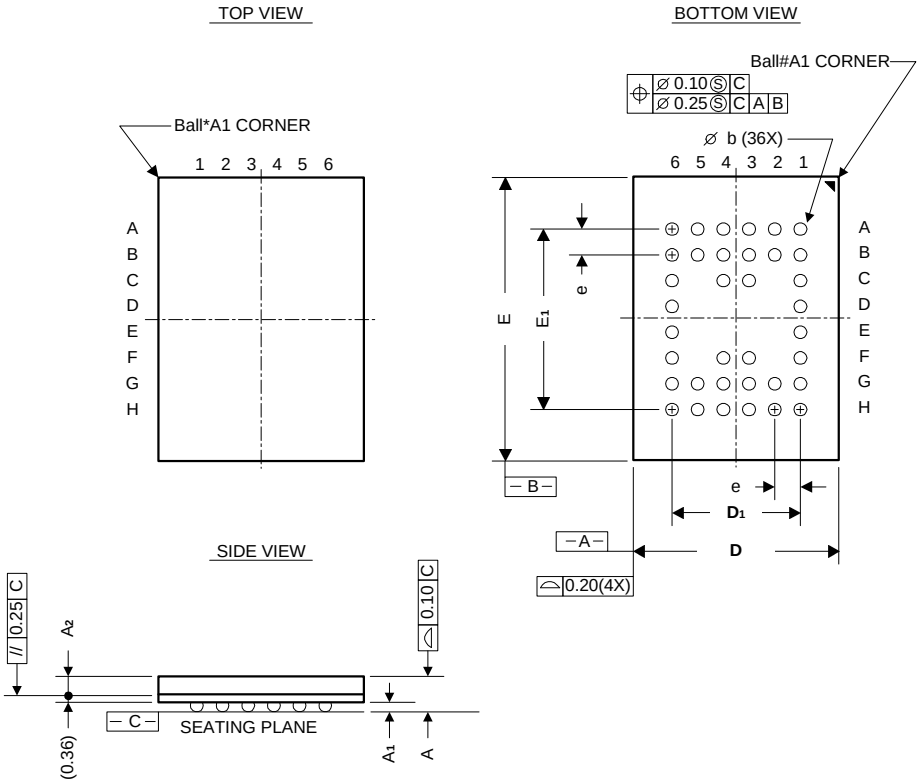
Notes:

1. The maximum value of dimension D_1 includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information

36LD CSP (6 x 8 mm) Outline Dimensions

unit: mm



Symbol	Dimensions in mm		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A_1	0.16	0.21	0.26
A_2	0.48	0.53	0.58
D	5.80	6.00	6.20
E	7.80	8.00	8.20
D_1	---	3.75	---
E_1	---	5.25	---
e	---	0.75	---
b	0.25	0.30	0.35

Note:

1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.
4. THEERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.