SIEMENS

ICs for Communications

Enhanced ISDN Data Access Controller
ISAR 34

PSB 7115 Version 2.1

Firmware Version 1.01

Data Sheet 02.98

DS 2

PSB 7115 **Revision History:**		**Current Version: 02.98**
Previous Version:		09.97
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
247/248	256/257	External Memory Interface timings added
-	188-196	General Purpose I/Os added
126	126	16 bit data path added
173	173	TSL=011 mode removed

IOM®, IOM®-1, IOM®-2, SICOFI®, SICOFI®-2, SICOFI®-4, SICOFI®-4µC, SLICOFI®, ARCOFI® , ARCOFI®-BA, ARCOFI®-SP, EPIC®-1, EPIC®-S, ELIC®, IPAT®-2, ITAC®, ISAC®-S, ISAC®-S TE, ISAC®-P, ISAC®-P TE, IDEC®, SICAT®, OCTAT®-P, QUAT®-S are registered trademarks of Siemens AG.

MUSAC™-A, FALC™54, IWE™, SARE™, UTPT™, ASM™, ASP™ are trademarks of Siemens AG.

Edition 02.98

This edition was realized using the software system FrameMaker®.

Published by Siemens AG,
HL SP,
Balanstraße 73,
81541 München

© Siemens AG 1998.
All Rights Reserved.

Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Semiconductor Group Offices in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components[1] of the Semiconductor Group of Siemens AG, may only be used in life-support devices or systems[2] with the express written approval of the Semiconductor Group of Siemens AG.

1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.

2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

Table of Contents **Page**

1	**General Information**	11
1.1	Features	12
1.2	System Integration	13
1.2.1	ISDN PC/Workstation Adapter with S-Interface	13
1.2.2	ISDN PC / Workstation Adapter with U-Interface	14
1.2.3	ISDN PC / Workstation Adapter as Intelligent NT	15
1.2.4	ISDN Voice/Data Terminal	16
1.2.5	Fax/Modem Pool with Primary Rate Access	17
1.3	Logic Symbol	18
1.4	Device Architecture	19
1.5	Pin Configuration	20
1.5.1	Pin Description	21
2	**Functional Description**	28
2.1	Functional Overview	28
2.2	Clock Generation	29
2.3	Physical Interfaces	31
2.3.1	Host Interface	31
2.3.2	IOM®-2 Interface	34
2.3.3	SAI Interface	35
2.3.4	External Memory Interface	36
2.3.5	General Purpose I/O Interface	37
2.4	Communications Interface	39
2.5	Functional Blocks	42
2.5.1	Buffer	43
2.5.2	SART	45
2.5.2.1	HDLC Mode	45
2.5.2.2	ASYNC Mode	46
2.5.2.3	Binary Mode	47
2.5.3	Pump	48
2.5.3.1	Fax Modulations	48
2.5.3.2	Datamodem Modulations	50
2.5.3.3	Halfduplex Modulations	51
2.5.3.4	V.110	52
2.5.3.5	DTMF	53
2.5.3.6	Bypass Mode	54
2.5.4	IOM®-2 Configuration	55
2.5.5	D-Channel	56
2.5.6	C/I-Channel	56
2.5.7	TIC-Bus Access	57
2.5.8	MONITOR Channel	59
3	**Operational Description**	60

Table of Contents **Page**

3.1 Host Communication 60
3.1.1 Message Structure 61
3.1.2 Interrupt Status Byte 62
3.1.3 Control Registers and Parameters 67
3.1.4 Configuration After Reset 68
3.1.5 Message Transfer from Host to ISAR 34 72
3.1.6 Message Transfer from ISAR 34 to Host 74
3.1.7 Message Overview 76
3.2 Buffer Configuration 79
3.2.1 Buffer Configuration Setup (Host → ISAR 34) 79
3.2.2 Buffer Configuration Request (Host → ISAR 34) 81
3.2.3 Buffer Configuration Response (ISAR 34 → Host) 82
3.2.4 Buffer Control Command (Host → ISAR 34) 84
3.3 Buffer Status 85
3.3.1 Buffer Status Request (Host → ISAR 34) 85
3.3.2 Buffer Status Response (ISAR 34 → Host) 87
3.3.3 Buffer Status Event (ISAR 34 → Host) 89
3.3.3.1 Buffer Specific Status Event (ISAR 34 → Host) 89
3.3.3.2 Buffer General Status Event (ISAR 34 → Host) 90
3.4 SART Configuration 92
3.4.1 SART Configuration Setup - HDLC (Host → ISAR 34) 92
3.4.2 SART Configuration Setup - ASYNC (Host → ISAR 34) 94
3.4.3 SART Configuration Setup - Binary (Host → ISAR 34) 97
3.4.4 SART Configuration Setup - Disable SART (Host → ISAR 34) 99
3.5 SART Data 100
3.5.1 SART Status Events with Receive Data (ISAR 34 → Host) 100
3.5.1.1 SART Status Events with Receive Data - HDLC (ISAR 34 → Host) 101
3.5.1.2 SART Status Events with Receive Data - ASYNC (ISAR 34 → Host) . . 103
3.5.1.3 SART Status Events with Receive Data - Binary (ISAR 34 → Host) 104
3.5.2 SART Control Commands with Transmit Data (Host → ISAR 34) 105
3.5.2.1 SART Control Commands with Transmit Data - HDLC (Host → ISAR 34) . . 105
3.5.2.2 SART Control Commands with Transmit Data - ASYNC (Host → ISAR 34) . 107
3.5.2.3 SART Control Commands with Transmit Data - Binary (Host → ISAR 34) . . 109
3.6 Pump Configuration 110
3.6.1 Pump Configuration Setup (Host → ISAR 34) 110
3.6.1.1 Pump Configuration Setup - Fax Modulations (Host → ISAR 34) 112
3.6.1.2 Pump Configuration Setup - Datamodem Modulations (Host → ISAR 34) . . 114
3.6.1.3 Pump Configuration Setup - Halfduplex Modulations (Host → ISAR 34) 118

Table of Contents **Page**

3.6.1.4 Pump Configuration Setup - V.110 (Host → ISAR 34) 121
3.6.1.5 Pump Configuration Setup - DTMF (Host → ISAR 34) 123
3.6.1.6 Pump Configuration Setup - Bypass Mode (Host → ISAR 34) 126
3.6.2 Pump Control Command (Host → ISAR 34) 127
3.6.2.1 Pump Control Command - Fax Modulations (Host → ISAR 34) 128
3.6.2.2 Pump Control Command - Datamodem Modulations (Host → ISAR 34) 131
3.6.2.3 Pump Control Command - Halfduplex Modulations (Host → ISAR 34) . .131
3.6.2.4 Pump Control Command - V.110 (Host → ISAR 34) 132
3.6.2.5 Pump Control Command - DTMF (Host → ISAR 34) 135
3.6.2.6 Pump Control Command - Bypass Mode (Host → ISAR 34) 136
3.6.2.7 Pump Control Command - C/I-Channel (Host → ISAR 34) 137
3.7 Pump Status 139
3.7.1 Pump Status Request (Host → ISAR 34) 139
3.7.2 Pump Status Response (ISAR 34 → Host) 140
3.7.2.1 Pump Status Response - Fax Modulations (ISAR 34 → Host) 140
3.7.2.2 Pump Status Response - Datamodem Modulations (ISAR 34 → Host) .142
3.7.2.3 Pump Status Response - Halfduplex Modulations (ISAR 34 → Host) . .146
3.7.2.4 Pump Status Response - V.110 (ISAR 34 → Host) 148
3.7.2.5 Pump Status Response - DTMF (ISAR 34 → Host) 152
3.7.2.6 Pump Status Response - Bypass Mode (ISAR 34 → Host) 153
3.7.2.7 Pump Status Response - Pump Disabled (ISAR 34 → Host) 154
3.7.3 Pump Status Events (ISAR 34 → Host) 155
3.7.3.1 Pump Status Events - Fax Modulations (ISAR 34 → Host) 155
3.7.3.2 Pump Status Events - Datamodem Modulations (ISAR 34 → Host) 157
3.7.3.3 Pump Status Events - Halfduplex Modulations (ISAR 34 → Host) 158
3.7.3.4 Pump Status Events - V.110 (ISAR 34 → Host) 159
3.7.3.5 Pump Status Events - DTMF (ISAR 34 → Host) 163
3.7.3.6 Pump Status Events - Bypass Mode (ISAR 34 → Host) 164
3.7.3.7 Pump Status Events - D- and C/I-Channel (ISAR 34 → Host) 165
3.8 IOM®-2 Configuration 166
3.8.1 IOM®-2 Configuration Setup - Path 1 and 2 (Host → ISAR 34) 166
3.8.2 IOM®-2 Configuration Setup - Path 3 (Host → ISAR 34) 169
3.8.3 IOM®-2 Configuration Request (Host → ISAR 34) 170
3.8.4 IOM®-2 Configuration Response - General Code (ISAR 34 → Host) . . .171
3.8.5 IOM®-2 Configuration Response - Path 1 and 2 (ISAR 34 → Host) 172
3.8.6 IOM®-2 Configuration Response - Path 3 (ISAR 34 → Host) 175
3.8.7 IOM®-2 Control Commands - General Code (Host → ISAR 34) 176
3.8.8 IOM®-2 Control Commands - Path 1 and 2 (Host → ISAR 34) 178
3.8.9 IOM®-2 Status Events (ISAR 34 → Host) 180
3.9 MONITOR Channel 181
3.9.1 Buffer Configuration and Status 181
3.9.2 MONITOR Channel Configuration 182

Table of Contents **Page**

3.9.2.1 MONITOR Channel Configuration Setup (Host → ISAR 34) 182
3.9.2.2 MONITOR Channel Configuration Request (Host → ISAR 34) 184
3.9.2.3 MONITOR Channel Configuration Response (ISAR 34 → Host) 184
3.9.3 MONITOR Channel Data 185
3.9.3.1 MONITOR Channel Receive Data (ISAR 34 → Host) 185
3.9.3.2 MONITOR Channel Transmit Data (Host → ISAR 34) 186
3.9.3.3 MONITOR Channel Status Events (ISAR 34 → Host) 187
3.10 GPIO (General Purpose I/Os) 188
3.10.1 GPIO Configuration 189
3.10.1.1 GPIO Configuration - Output Register Set/Reset (Host → ISAR 34) . . . 189
3.10.1.2 GPIO Configuration - Direction (Host → ISAR 34) 191
3.10.1.3 GPIO Configuration - Open Drain Select (Host → ISAR 34) 192
3.10.1.4 GPIO Configuration - Strobed Input (Host → ISAR 34) 193
3.10.1.5 GPIO Configuration - Interrupt Mask (Host → ISAR 34) 195
3.10.2 GPIO Status 197
3.10.2.1 GPIO Status Request (Host → ISAR 34) 197
3.10.2.2 GPIO Status Event/Response (ISAR 34 → Host) 198
3.11 Test/Diagnostics Path 199
3.11.1 Timer Interrupt On/Off(Host → ISAR 34) 199
3.11.2 Timer Interrupt Event (ISAR 34 → Host) 200
3.11.3 Chip Version Request (Host → ISAR 34) 201
3.11.4 Chip Version Response (ISAR 34 → Host) 201
3.11.5 Software Version Request (Host → ISAR 34) 202
3.11.6 Software Version Response (ISAR 34 → Host) 202
3.11.7 Request Selftest Result (ISAR 34 → Host) 203
3.11.8 Selftest Response (ISAR 34 → Host) 203
3.11.9 Soft Reset (Host → ISAR 34) 204
3.11.10 Invalid Message Received (ISAR 34 → Host) 205
3.12 DSP Program Download 206
3.12.1 Structure of File Header 208
3.12.2 Structure of Block Header 210
3.12.3 Structure of Data Blocks 212
3.12.3.1 Jump to Block 212
3.12.3.2 Write Message 213
3.12.3.3 Wait for Next Message 215
3.12.3.4 Wait for Specific Message 217
3.12.3.5 Compare Last Message 219
3.12.3.6 Set Coding Information 221
3.12.3.7 Set Status Information 222
3.12.3.8 Write to Memory 223
3.13 Fax Class 1 Implementation 225
3.13.1 Summary of ISAR 34 Fax Control Commands 226

Table of Contents **Page**

3.13.2 Summary of ISAR 34 Fax Status Events 227
3.13.3 Procedure Termination 228
3.13.4 Fax Pump Startup Procedure 229
3.13.5 HDLC Transmission 230
3.13.6 Binary Transmission 231
3.13.7 HDLC Reception 232
3.13.8 Binary Reception 233
3.13.9 Call Termination 234
3.13.10 Procedure Terminations 234
3.14 Startup Procedures 235
3.14.1 V.8 Negotiation 235
3.14.2 Automode Operation 236

4 Summary of Messages 239

5 Example Configuration Settings 243

6 Detailed Register Description 246
6.1 Register Address Map 246
6.2 Register Description 246

7 Electrical Characteristics 251
7.1 Absolute Maximum Ratings 251
7.2 Recommended Operating Conditions 251
7.3 DC Characteristics 252
7.4 Capacitances 253
7.5 Oscillator Circuit 253
7.6 XTAL1,2 Recommended Typical Crystal Parameters 253
7.7 AC Characteristics 254
7.7.1 Testing Waveform 254
7.7.2 Parallel Host Interface Timing 254
7.7.3 External Memory Interface Timing 258
7.7.4 IOM®-2 Interface Timing 260

8 Package Outlines 261

List of Figures **Page**

Figure 1: ISDN PC/Workstation Adapter with S-Interface 13
Figure 2: ISDN PC/Workstation Adapter with U-Interface 14
Figure 3: ISDN PC/Workstation Adapter as Intelligent NT 15
Figure 4: ISDN Voice/Data Terminal 16
Figure 5: Fax/Modem Pool with Primary Rate Access 17
Figure 6: Logic Symbol 18
Figure 7: Device Architecture 19
Figure 8: Pinout 20
Figure 9: Functional Block Diagram of the ISDN Data Access Controller 28
Figure 10: Clock Generation 29
Figure 11: Clock Mode Applications 30
Figure 12: Register Access in Multiplexed and Non-Multiplexed Mode. 33
Figure 13: Linecard Mode of the IOM-2 Interface 34
Figure 14: Terminal mode of the IOM-2 Interface 35
Figure 15: Memory Configuration - DSP Program Download 36
Figure 16: General Purpose I/O Interface 37
Figure 17: Interrupt Input Signal 38
Figure 18: Host Interface Registers 39
Figure 19: Structure of Interrupt Status Byte 40
Figure 20: Mailbox Interface 41
Figure 21: Communication Buffers 42
Figure 22: Structure of Datapath Buffers 44
Figure 23: HDLC Data Formatting 45
Figure 24: ASYNC Data Formatting 46
Figure 25: Binary Data 47
Figure 26: Fax Modulations 48
Figure 27: Fax Class 1 Support 49
Figure 28: Datamodem Modulations 50
Figure 29: Halfduplex Modulation 51
Figure 30: V.110 Formatting 52
Figure 31: DTMF Detection 53
Figure 32: Pump in Bypass Mode 54
Figure 33: IOM-2 Configuration Parameters 55
Figure 34: TIC-Bus Application 57
Figure 35: Structure of Last Octet within CH2 on DU 57
Figure 36: Structure of Last Octet within CH2 on DD 58
Figure 37: MONITOR Channel Applications 59
Figure 38: Host Communication 60
Figure 39: Message Transfer. 61
Figure 40: Control Registers and Parameters 67
Figure 41: Initialisation Procedure 69
Figure 42: Write Message Transfer 72

List of Figures **Page**

Figure 43: Read Message Transfer 74
Figure 44: Message Directions 75
Figure 45: Binary File Structure 206
Figure 46: Pointer on Data Structures 207
Figure 47: Download Process 209
Figure 48: Block Header Process 211
Figure 49: Data Block Process - Jump to Block 212
Figure 50: Data Block Process - Write Message 214
Figure 51: Data Block Process - Wait for Next Message 216
Figure 52: Data Block Process - Wait for Specific Message 218
Figure 53: Data Block Process - Compare Last Message 220
Figure 54: Data Block Process - Set Coding Information 221
Figure 55: Data Block Process - Set Status Information 222
Figure 56: Data Block Process - Write to Memory 224
Figure 57: Fax Class 1 - Startup Procedure 229
Figure 58: Fax Class 1 - HDLC Transmission 230
Figure 59: Fax Class 1 - Binary Transmission 231
Figure 60: Fax Class 1 - HDLC Reception 232
Figure 61: Fax Class 1 - Binary Reception 233
Figure 62: Fax Class 1 - Call Termination 234
Figure 63: Fax Class 1 - Procedure Terminations 234
Figure 64: V.8 Answering Mode 235
Figure 65: V.8 Originating Mode 236
Figure 66: Automode Answerer 237
Figure 67: Automode Originator 238
Figure 68: Oscillator Circuit 253
Figure 69: Testing Input/Output Waveforms 254
Figure 70: Microprocessor Read Timing 254
Figure 71: Microprocessor Write Timing 255
Figure 72: Multiplexed Address Timing 255
Figure 73: Non-Multiplexed Address Timing 255
Figure 74: Microprocessor Read Timing 256
Figure 75: Microprocessor Write Timing 256
Figure 76: Non-Multiplexed Address Timing 256
Figure 77: External Memory Interface - Write Cycle 258
Figure 78: External Memory Interface - Read Cycle 258
Figure 79: IOM®-2 Timing with Double Rate DCL 260

List of Tables **Page**

Table 1: Clock Mode Settings 30
Table 2: Host Interface Signals 31
Table 3: Bus Operation Modes 32
Table 4: Buffer size 43
Table 5: HIS Structure - Path 1, 2 and 3 63
Table 6: HIS Structure - Path 0 64
Table 7: IIS Structure - Path 1, 2 and 3 65
Table 8: IIS Structure - Path 0 66
Table 9: Configuration Parameters 70
Table 10: Pump Modes 110
Table 11: Pump Modes in Path 1 and 2 111
Table 12: V.110 Remote DTE Status 162
Table 13: Structure of File Header 208
Table 14: Structure of Block Header 210
Table 15: Types of Data Blocks 210
Table 16: Block Structure - BLOCK_TYPE = 1H 212
Table 17: Block Structure - BLOCK_TYPE = 2H 213
Table 18: Block Structure - BLOCK_TYPE = 3H 215
Table 19: Block Structure - BLOCK_TYPE = 4H 217
Table 20: Block Structure - BLOCK_TYPE = 5H 219
Table 21: Block Structure - BLOCK_TYPE = 6H 221
Table 22: Block Structure - BLOCK_TYPE = 7H 222
Table 23: Types of Memory Write Data Blocks 223
Table 24: Block Structure - BLOCK_TYPE = 20H, 21H, 30H, 31H 223
Table 25: Fax Class 1 - Procedure Termination 228

1 General Information

The ISAR 34, ISDN Data Access Controller forms an advanced solution for ISDN applications communicating with remote ISDN as well as analog terminals.
The ISAR 34 PSB 7115 follows its predecessor ISAR PSB 7110 which is capable of modem modulation up to 14400 bit/s (V.32bis). The new ISAR 34 has the similar functional architecture and additionally supports modem modulation up to 33600 bit/s (V.34bis). As well the platform is upgradeable to new modem standards (PCM modems) and is able to run algorithms for audio compression (e.g. G.728) or answering machine alternatively. A special version called "ISAR AC" is available for this purpose

The ISAR 34 is designed for data access over ISDN. It can be used in data terminals combining ISDN and analog functionality for communication with remote subscribers. It can also be integrated in fax/modem pools and routers.
The ISAR AC version fits perfectly into H.320/H.324 video conferencing systems, in which it supports both the modem and audio functions.

It integrates two data formatting units which support binary framing, HDLC and ASYNC, which is an asynchronous data formatting according to ITU-T V.14. The data from the formatting units is input data to a fax/modem modulation or V.110 or transparent framing towards the IOM-2 timeslots. As well one channel DTMF generation and detection is supported in the data pump.

The ISAR 34 operates on the IOM-2 interface in terminal mode (1.536 MHz DCL) and is also designed to operate on line-card IOM-2 interfaces (4.096 MHz DCL).

As the DSP program is downloaded into external memory connected to the memory interface of the ISAR 34, firmware upgrades for new algorithms and future applications are quite easy to realize. For example a further version will fully provide a codec interface to support the Siemens Analog Line Interface Solution ALIS for analog modem applications.

An elaborate mailbox interface with 256 byte buffers in each direction reduces the number of registers to a minimum.

The PSB 7115 ISDN Data Access Controller is a CMOS device offered in a thin quad-flat pack package. It operates from a single 3.3 V supply and the inputs are 5V safe.

SIEMENS

Enhanced ISDN Data Access Controller PSB 7115
ISAR 34

Version 2.1 **CMOS**

1.1 Features

P-TQFP-144-2

- Modem modulation up to 33600 bit/s (V.34bis) including fallback modes
- Fax modulation up to 14400 bit/s (V.17) including fallback modes
- Bit rate adaptation according to V.110 for both B-channels (except during datamodem modulation)
- DTMF generation and detection in one channel
- Two universal formatters supporting ASYNC (ITU-T V.14), HDLC and binary framing of data for B-channel applications
- V.8 rate negotiation
- ISDN D-channel HDLC controller with TIC bus support
- ISDN C/I-channel and MONITOR channel handler
- IOM-2 terminal mode (1.536 MHz), line card mode (4.096 MHz)
- Mailbox interface for host communication
- External memory interface to connect external program and data memory
- Upgradeable to new technologies (e.g. PCM modem)
- 256 byte FIFO per direction for host interface communication of B-channel data
- 9 programmable general purpose I/O lines
- On-Chip PLL for clock generation
- 3.3 V power supply
- Thin QFP-package
- Advanced CMOS technology

Type	Ordering Code	Package
PSB 7115 F V2.1		P-TQFP-144-2

1.2 System Integration

1.2.1 ISDN PC/Workstation Adapter with S-Interface

The ISDN PC or Workstation Adapter is based on the ISAR 34. A PSB 2186, ISAC-S TE forms the S-transceiver and the ISAR 34 provides the HDLC controller to perform the D-channel signalling protocol. External circuitry is required for the S-interfaces which includes the transformer and protection circuitry. The host interface of the ISAR 34 is connected to the host bus.

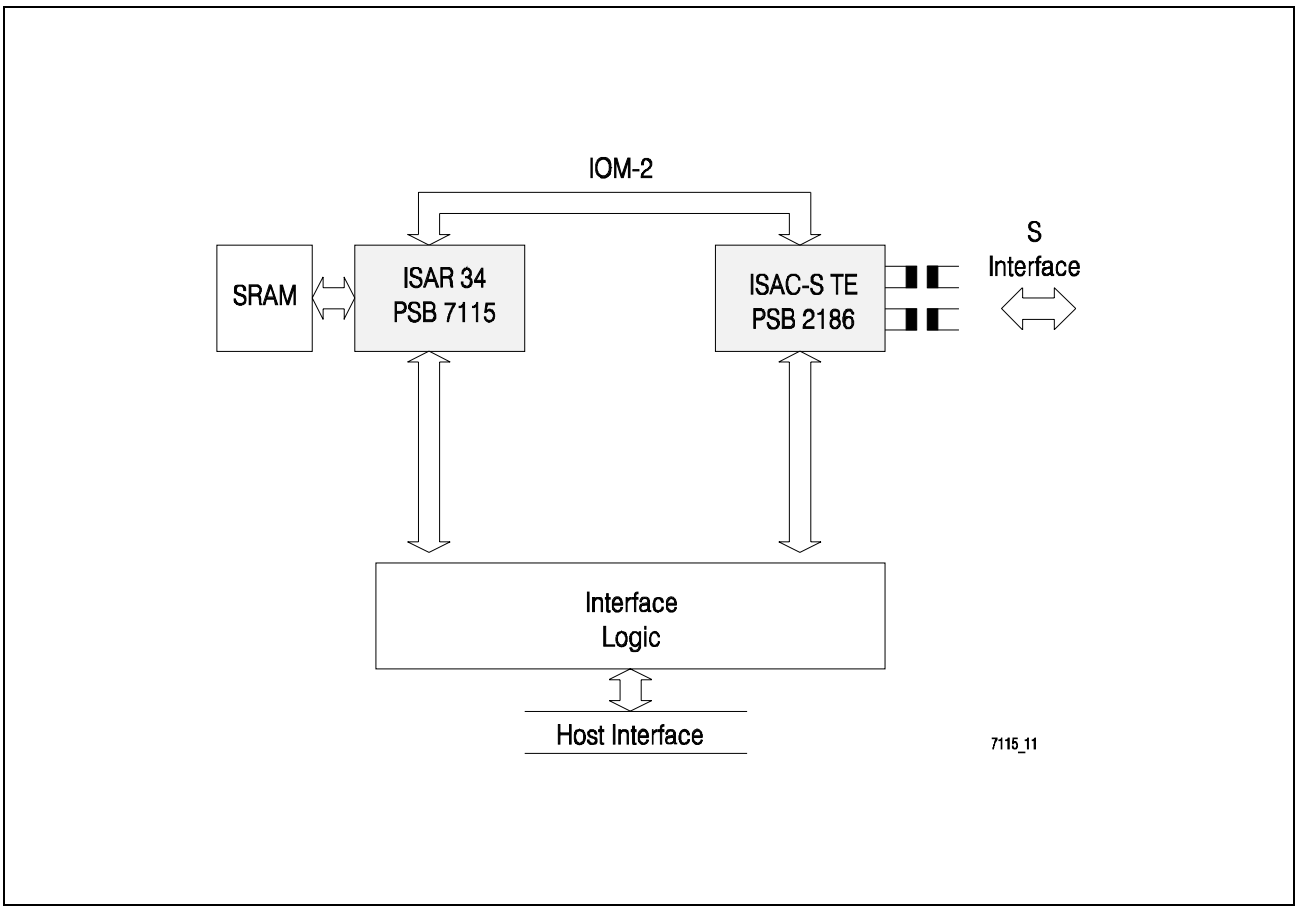


Figure 1 ISDN PC/Workstation Adapter with S-Interface

The ISAR 34 supports HDLC based applications like file transfer, access to packet switches (X.75, V.120, PPP). It also supports communication to terminal adapters which perform bit rate adaptation according to V.110.

A special feature of the ISAR 34 is its support for analog fax/modem applications. Therefore, PCM data is converted to linear data and handled by a V.34bis/V.17 data pump to support data rates up to 33600 bit/s (V.34bis) and 14400 bit/s (V.17).

1.2.2 ISDN PC / Workstation Adapter with U-Interface

Especially for the US market the U-interface formed by the PSB 21910 IEC-Q NTE, is considered as the standard basic rate interface. The ISAR 34 supports these applications in a cost effective way since it includes the D-channel HDLC controller, the command/indicate channel as well as the MONITOR channel. The IOM-2 interface supports TIC bus access.

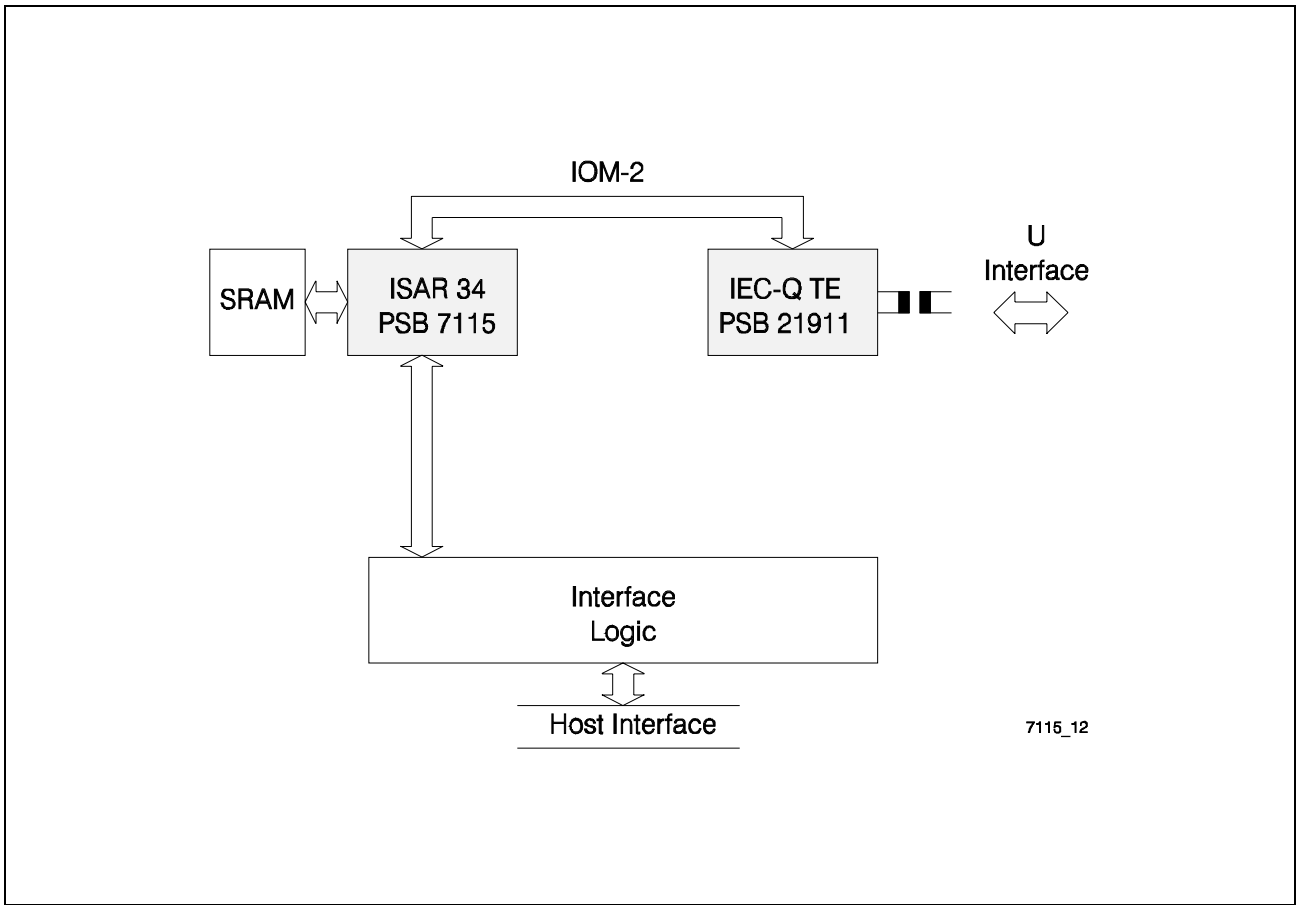


Figure 2 ISDN PC/Workstation Adapter with U-Interface

1.2.3 ISDN PC / Workstation Adapter as Intelligent NT

A variation of the U-interface PC card is called the intelligent NT since it provides the network termination function as part of the card.

The ISAR 34 supports the TIC bus of the IOM-2 interface which controls the D-channel data flow between the local D-channel source inside the ISAR 34 and the D-channel sources on the S-interface. The INTC-Q PEB 8191 is the integration of the S- and U-transceivers, dedicated to intelligent NT applications.

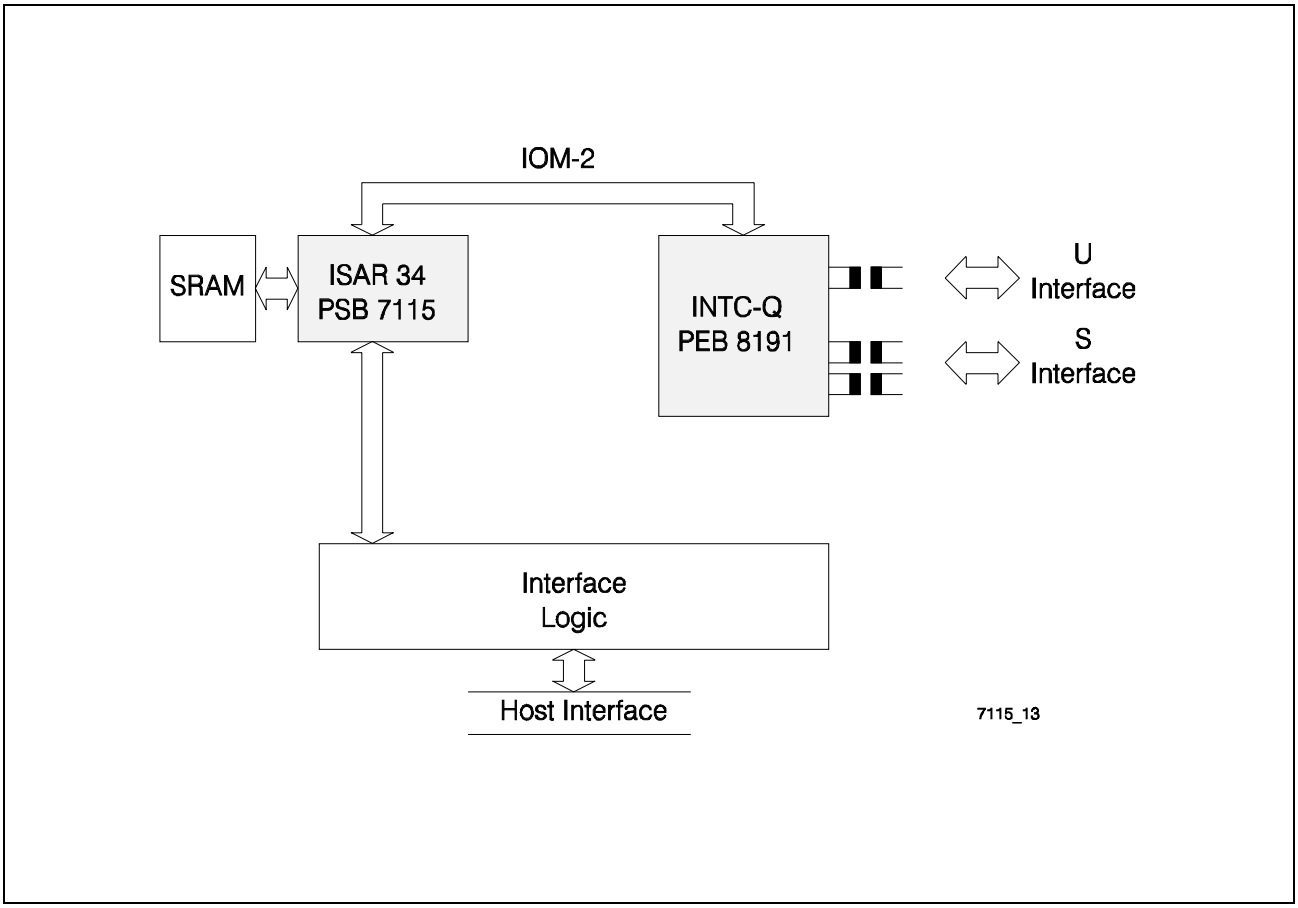


Figure 3 ISDN PC/Workstation Adapter as Intelligent NT

1.2.4 ISDN Voice/Data Terminal

Figure 4 shows a voice data terminal developed on a PC card, where the ISAR 34 provides its fax and modem functionality within a three chip solution. During ISDN calls the ARCOFI-SP PSB 2163 provides for speakerphone functions and includes an additional DTMF generator.

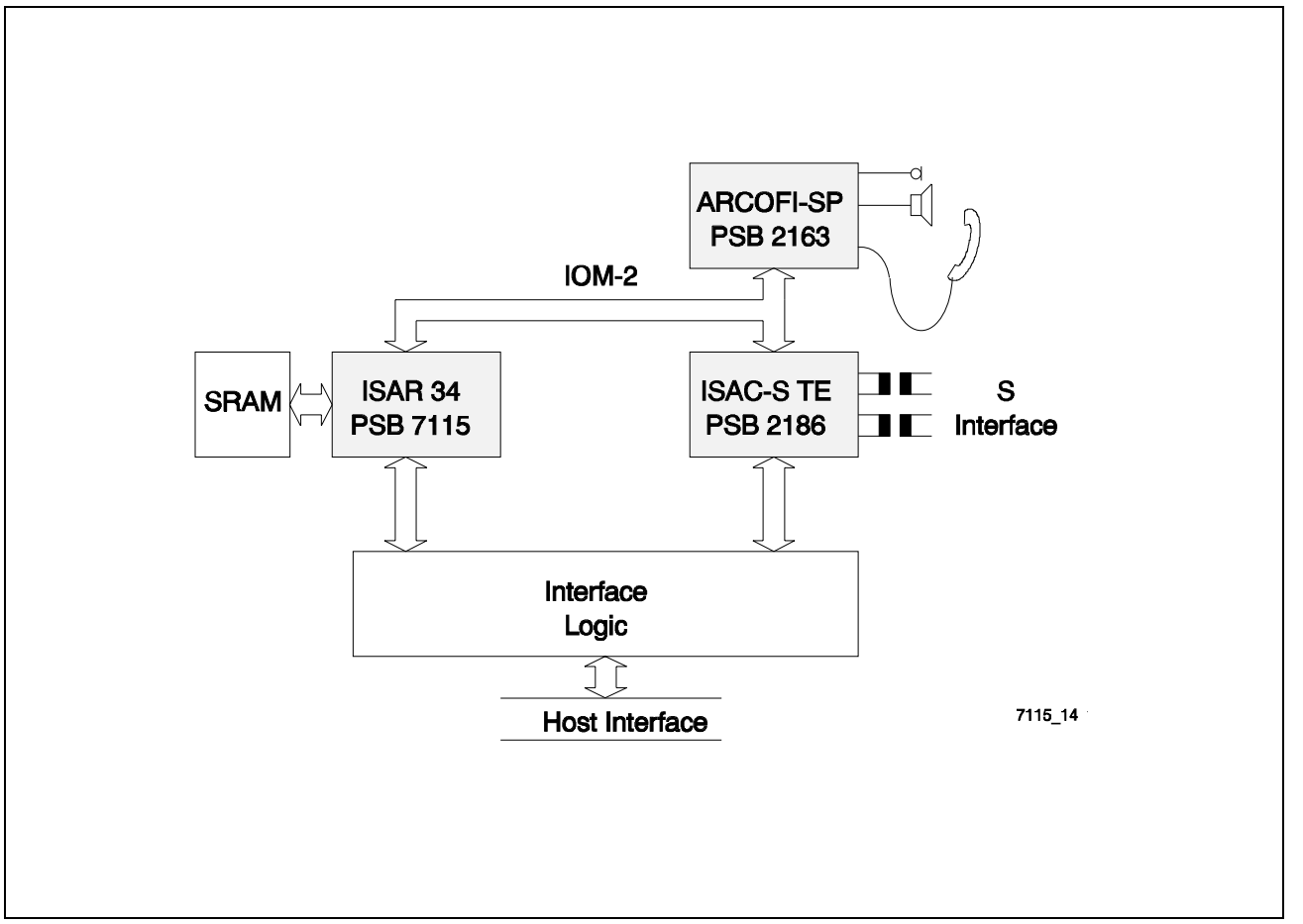


Figure 4 ISDN Voice/Data Terminal

1.2.5 Fax/Modem Pool with Primary Rate Access

Figure 5 shows an application suitable for modem pools or fax servers (fax on demand). The Frame and Line Interface Controller FALC 54 PEB 2254 provides for direct access to the PCM highway, may be programmed to operate in 1.544 Mbit/s (PCM24, T1) or 2.048 Mbit/s (PCM30/E1) carrier systems and provides the complete functionality of a line interface-, framing-, clock generation- and signalling unit. The selection of timeslots on the ISAR 34 is programmable, so they are cascadable in any order.

Depending on whether or not the microprocessor performs a download to external SRAM of the ISAR 34, flash memory may be required or not.

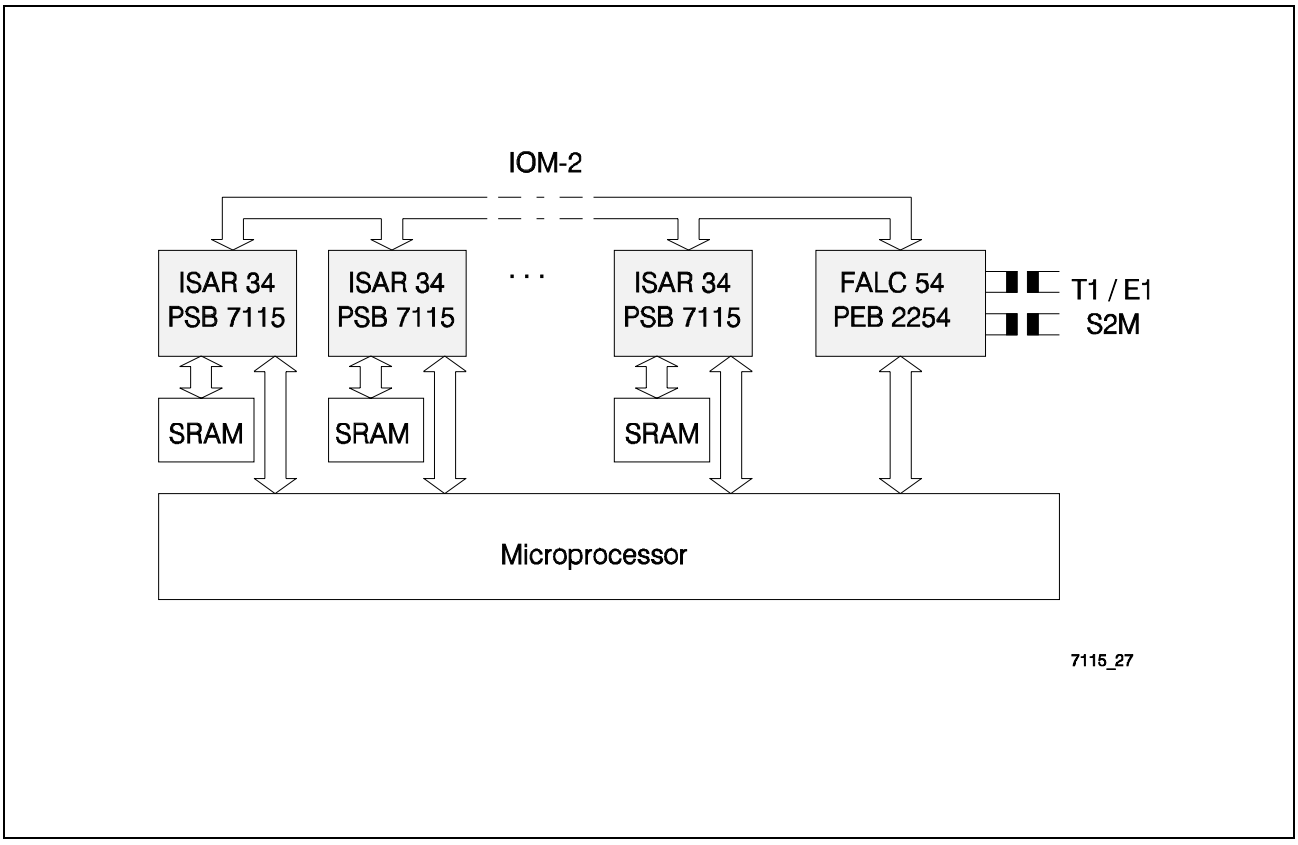


Figure 5 Fax/Modem Pool with Primary Rate Access

1.3 Logic Symbol

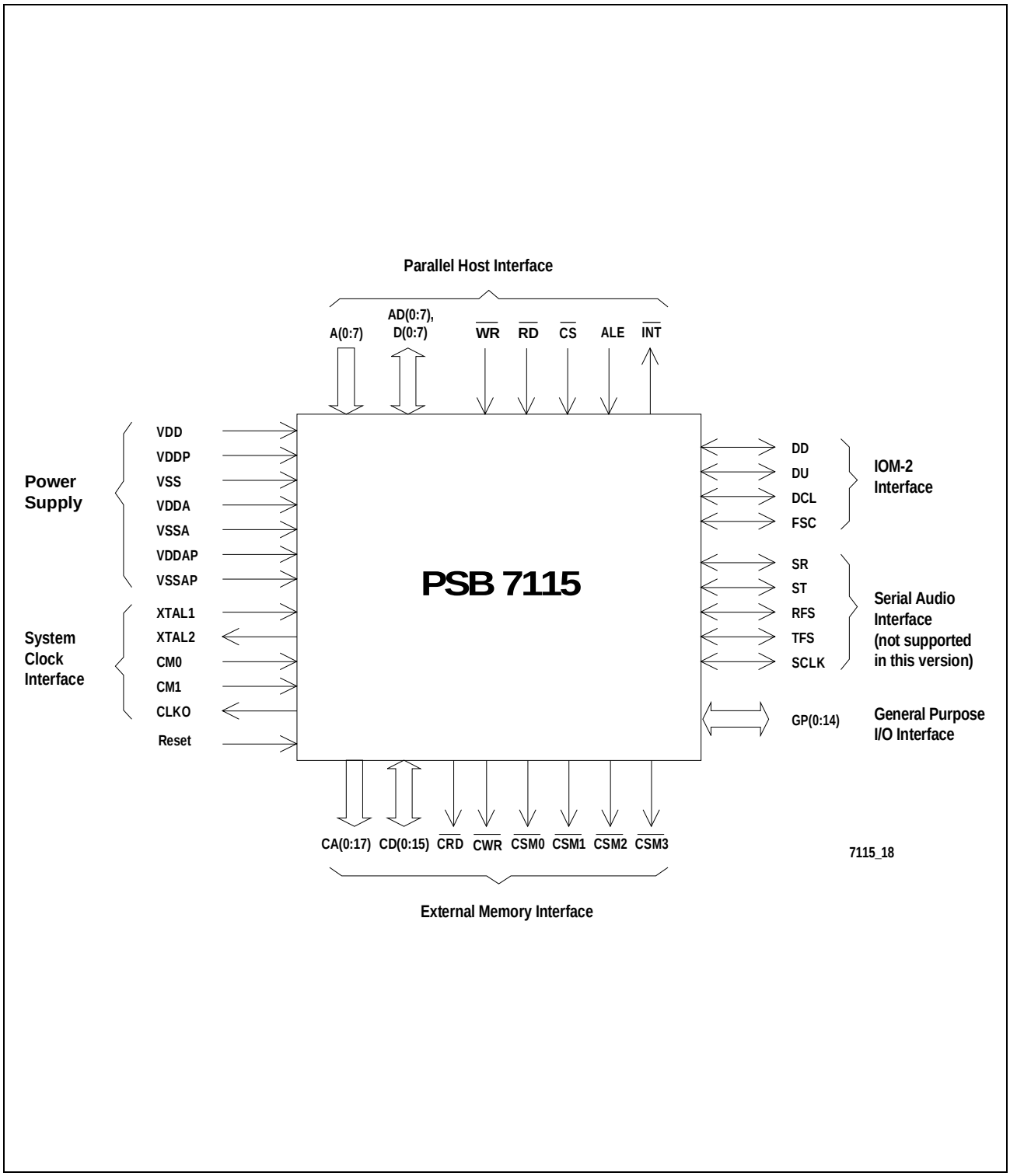


Figure 6 Logic Symbol

1.4 Device Architecture

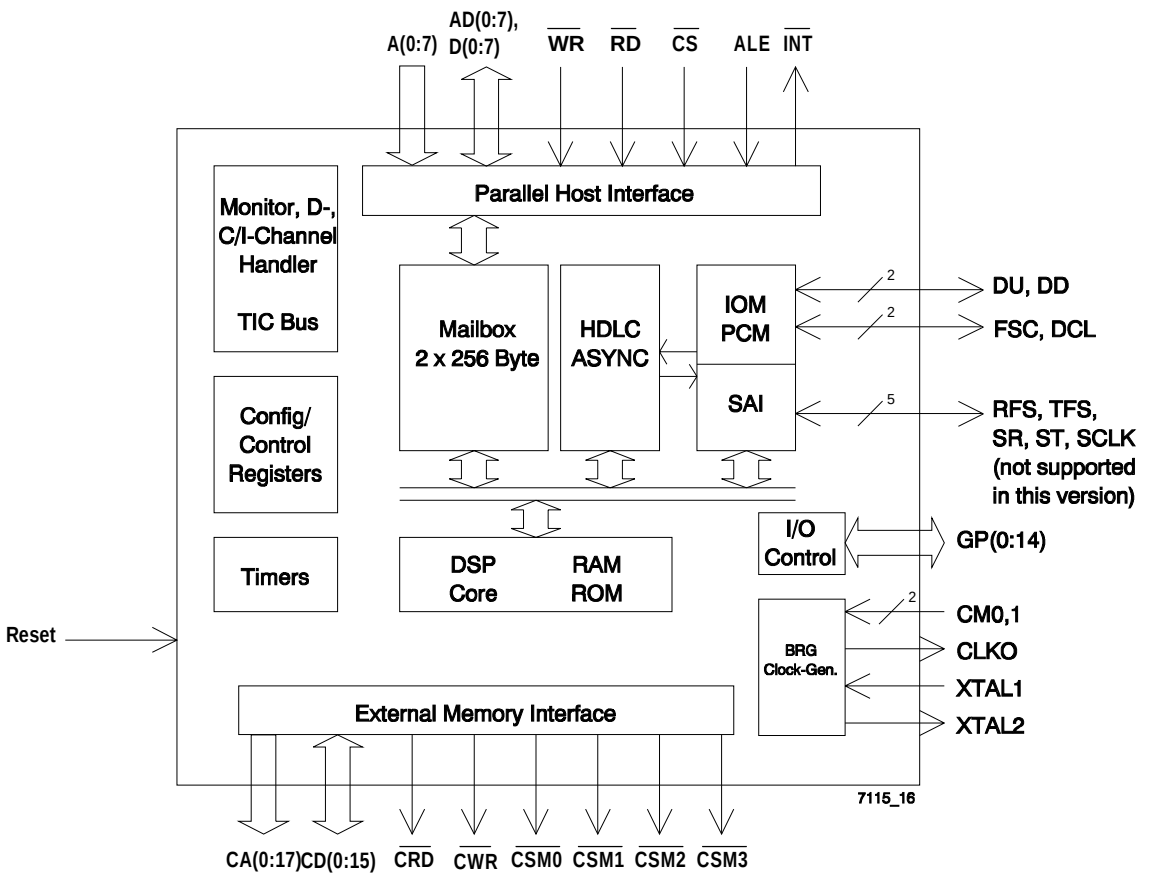


Figure 7 Device Architecture

1.5 Pin Configuration

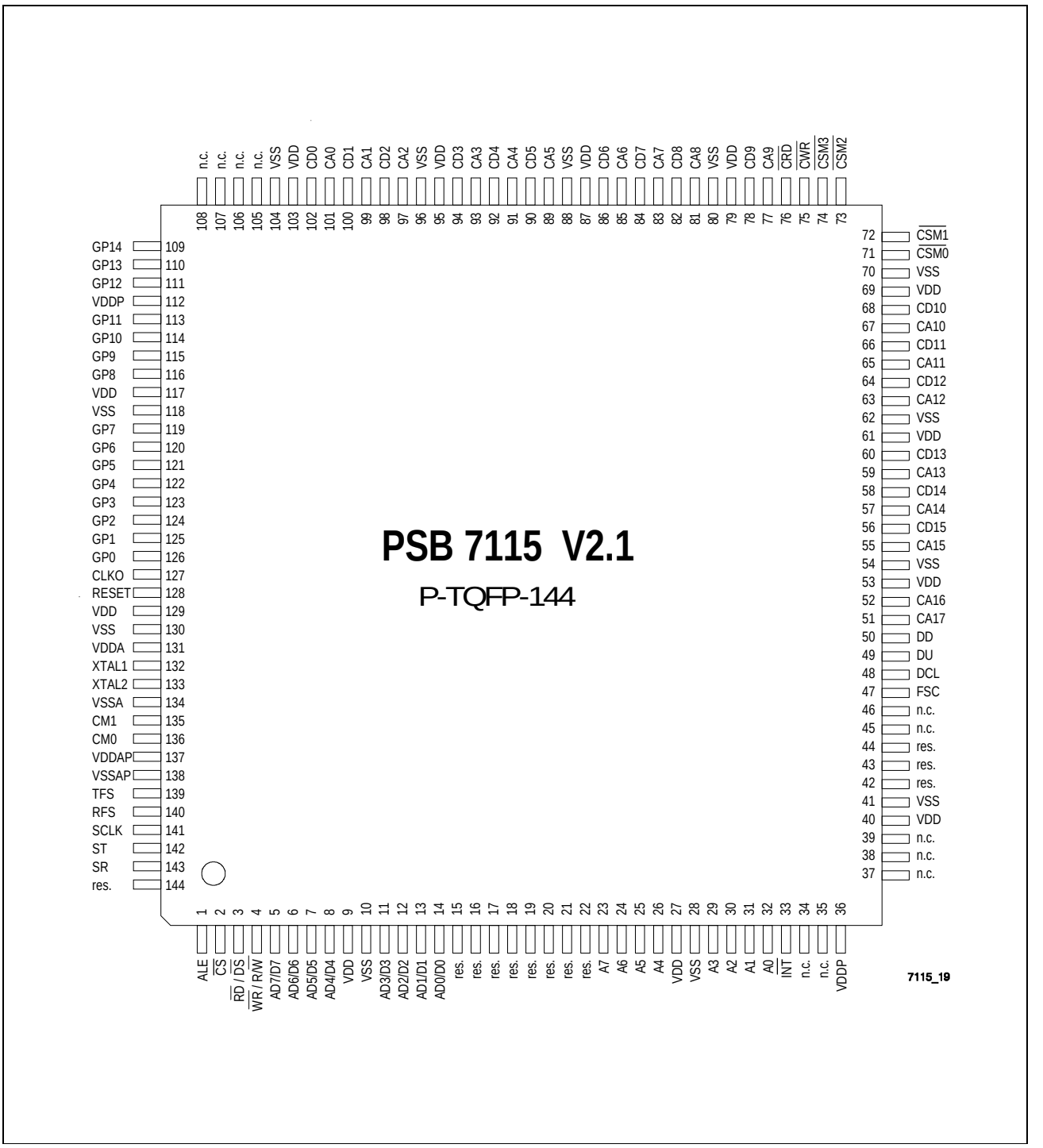


Figure 8 Pinout

1.5.1 Pin Description

Pin No.	Symbol	Input (I) Output (O)	Function
Parallel Host Interface			
14 13 12 11 8 7 6 5	AD0/D0 AD1/D1 AD2/D2 AD3/D3 AD4/D4 AD5/D5 AD6/D6 AD7/D7	I/O I/O I/O I/O I/O I/O I/O I/O	**Multiplexed Bus Mode: Address/Data Bus** Transfers addresses and data between the host and the ISAR 34. **Demultiplexed Bus Mode: Data Bus** Transfers data between the host and the ISAR 34.
32 31 30 29 26 25 24 23	A0 A1 A2 A3 A4 A5 A6 A7	I I I I I I I I	**Demultiplexed Bus Mode (only): Address Bus** Transfers address from the host to the ISAR 34. These pins are not used in multiplexed bus mode, therefore they should be tied to VDD in this mode.
3	$\overline{RD}$ $\overline{DS}$	I I	**Read** This signal indicates a read operation. (Siemens/Intel bus mode). **Data Strobe** The rising edge marks the end of a valid read or write operation. (Motorola bus mode).
4	$\overline{WR}$ R/$\overline{W}$	I I	**Write** This signal indicates a write operation. (Siemens/Intel bus mode). **Read/Write** A "1" identifies a valid host access as a read operation. A "0" identifies the access as a write operation. (Motorola bus mode).
2	$\overline{CS}$	I	**Chip Select** A "0" on this line selects the ISAR 34 for a read/write operation.

1.5.1 Pin Description

Pin No.	Symbol	Input (I) Output (O)	Function
1	ALE	I	**Address Latch Enable** A “1” on this line indicates an address on AD (0:7), that will be latched by the ISAR 34 (multiplexed mode only). This allows the ISAR 34 to be directly connected to a host with multiplexed address/data bus. ALE also selects the interface mode (multiplexed or non-multiplexed).
33	$\overline{\text{INT}}$	O (OD)	**Interrupt Request** This signal is activated, when the ISAR 34 requests an interrupt. This pin is an open drain output.
IOM®-2 Interface			
50	DD	I/O	**Data Downstream** on IOM-2/PCM interface.
49	DU	I/O	**Data Upstream** on IOM-2/PCM interface.
48	DCL	I/O	**Data Clock** Clock frequency is twice the data rate.
47	FSC	I/O	**Frame Sync** Marks the beginning of a physical IOM-2 or PCM frame.
Serial Audio Interface (not supported in this version)			
141	SCLK	I/O	**Serial Clock** Serial clock for SR and ST.
143	SR	I/O	**Serial Data Receive**
142	ST	I/O	**Serial Data Transmit**
140	RFS	I/O	**Receive Frame Sync**
139	TFS	I/O	**Transmit Frame Sync**

1.5.1 Pin Description

Pin No.	Symbol	Input (I) Output (O)	Function
System Clocks			
132	XTAL1	I	**Crystal In or Clock In** If a crystal is used, it is connected across XTAL1 and XTAL2. If a clock signal is provided (via an external oscillator), this signal is input via XTAL1. In this case the XTAL2 output is to be left non-connected.
133	XTAL2	O	**Crystal Out** Left unconnected if a crystal is not used.
136 135	CM0 CM1	I I	**Clock Mode Select** One of four different clock mode options can be selected by CM1,0 tied to VDDP or VSS.
127	CLKO	O	**Clock Out** A buffered output clock equal to the clock input at XTAL1 is provided for further devices on the system.
External Memory Interface			
101 99 97 93 91 89 85 83 81 77 67 65 63 59 57 55 52 51	CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7 CA8 CA9 CA10 CA11 CA12 CA13 CA14 CA15 CA16 CA17	O O O O O O O O O O O O O O O O O O	**C-Bus Address** Used for addressing external program and data memory.

1.5.1 Pin Description

Pin No.	Symbol	Input (I) Output (O)	Function
102 100 98 94 92 90 86 84 82 78 68 66 64 60 58 56	CD0 CD1 CD2 CD3 CD4 CD5 CD6 CD7 CD8 CD9 CD10 CD11 CD12 CD13 CD14 CD15	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	**C-Bus Data** Data bus for external program and data memory.
76	$\overline{\text{CRD}}$	O	**C-Bus Read to external memory** This signal must be connected to the $\overline{\text{RD}}$ input of the external program and data memory.
75	$\overline{\text{CWR}}$	O	**C-Bus Write to external memory** This signal must be connected to the $\overline{\text{WR}}$ input of the external program and data memory.
71 72 73 74	$\overline{\text{CSM0}}$ $\overline{\text{CSM1}}$ $\overline{\text{CSM2}}$ $\overline{\text{CSM3}}$	O O O O	**C-Bus Select line for** **external memory bank #0, #1, #2, #3** This signal must be connected to the $\overline{\text{CS}}$ input of the corresponding memory bank.

1.5.1 Pin Description

Pin No.	Symbol	Input (I) Output (O)	Function
General Control			
128	RESET	I	**Reset input**
126 125 124 123 122 121 120 119 116 115 114 113 111 110 109	GP0 GP1 GP2 GP3 GP4 GP5 GP6 GP7 GP8 GP9 GP10 GP11 GP12 GP13 GP14	I/O	**General Purpose Input/Output** These pins serve as general purpose input/output lines with interrupt input capability. Pins GP0-8 are programmable by host, pins GP9-14 are reserved for testing purpose.

1.5.1 Pin Description

Pin No.	Symbol	Input (I) Output (O)	Function
Power Supply			
10	V_{SS}	I	**Ground** (common to V_{DD} and V_{DDP})
28	V_{SS}	I	
41	V_{SS}	I	
54	V_{SS}	I	
62	V_{SS}	I	
70	V_{SS}	I	
80	V_{SS}	I	
88	V_{SS}	I	
96	V_{SS}	I	
104	V_{SS}	I	
118	V_{SS}	I	
130	V_{SS}	I	
9	V_{DD}	I	**Positive power supply voltage** (3.0 - 3.6 V)
27	V_{DD}	I	
40	V_{DD}	I	
53	V_{DD}	I	
61	V_{DD}	I	
69	V_{DD}	I	
79	V_{DD}	I	
87	V_{DD}	I	
95	V_{DD}	I	
103	V_{DD}	I	
117	V_{DD}	I	
129	V_{DD}	I	
36	V_{DDP}	I	**Positive power supply voltage** (4.5 - 5.5 V)
112	V_{DDP}	I	
134	V_{SSA}	I	**Separate analog ground** (0 V) for Clock Generation Unit.
131	V_{DDA}	I	**Separate analog positive power supply voltage** (3.0 - 3.6 V) for Clock Generation Unit.

1.5.1 Pin Description

Pin No.	Symbol	Input (I) Output (O)	Function
138	V_{SSAP}	I	**Separate analog ground** (0 V) for PLL.
137	V_{DDAP}	I	**Separate analog positive power supply voltage** (3.0 - 3.6 V) PLL.

Reserved Pins

15 16 17 18 19 20 21 22 42 43 44 144	res.		**Reserved** These pins are reserved for further use. They must be connected to VDD.
34 35 37 38 39 45 46 105 106 107 108	n.c.		**Not Connected** These pins are not used and may be left not connected.

2 Functional Description

2.1 Functional Overview

Figure 9 depicts the detailed functional architecture of the ISAR 34 V2.1:

- One modem/fax engine for V.34bis (33600 bit/s), V.17 (14400 bit/s), including fallback modes
- Upgradeable to new modem standards due to flexible firmware download capability
- DTMF receiver / transmitter in one channel
- V.110 formatter in two channels (except during datamodem modulation)
- Two universal formatters SART (Synchronous Asynchronous Receiver Transmitter) supporting ASYNC (ITU-T V.14), HDLC and binary modes
- D-channel HDLC controller
- C/I and MONITOR channel handler
- IOM-2 interface for terminal or line-card applications with TIC bus support
- External memory interface for program and data memory
- Communications Mailbox with 256 bytes per direction

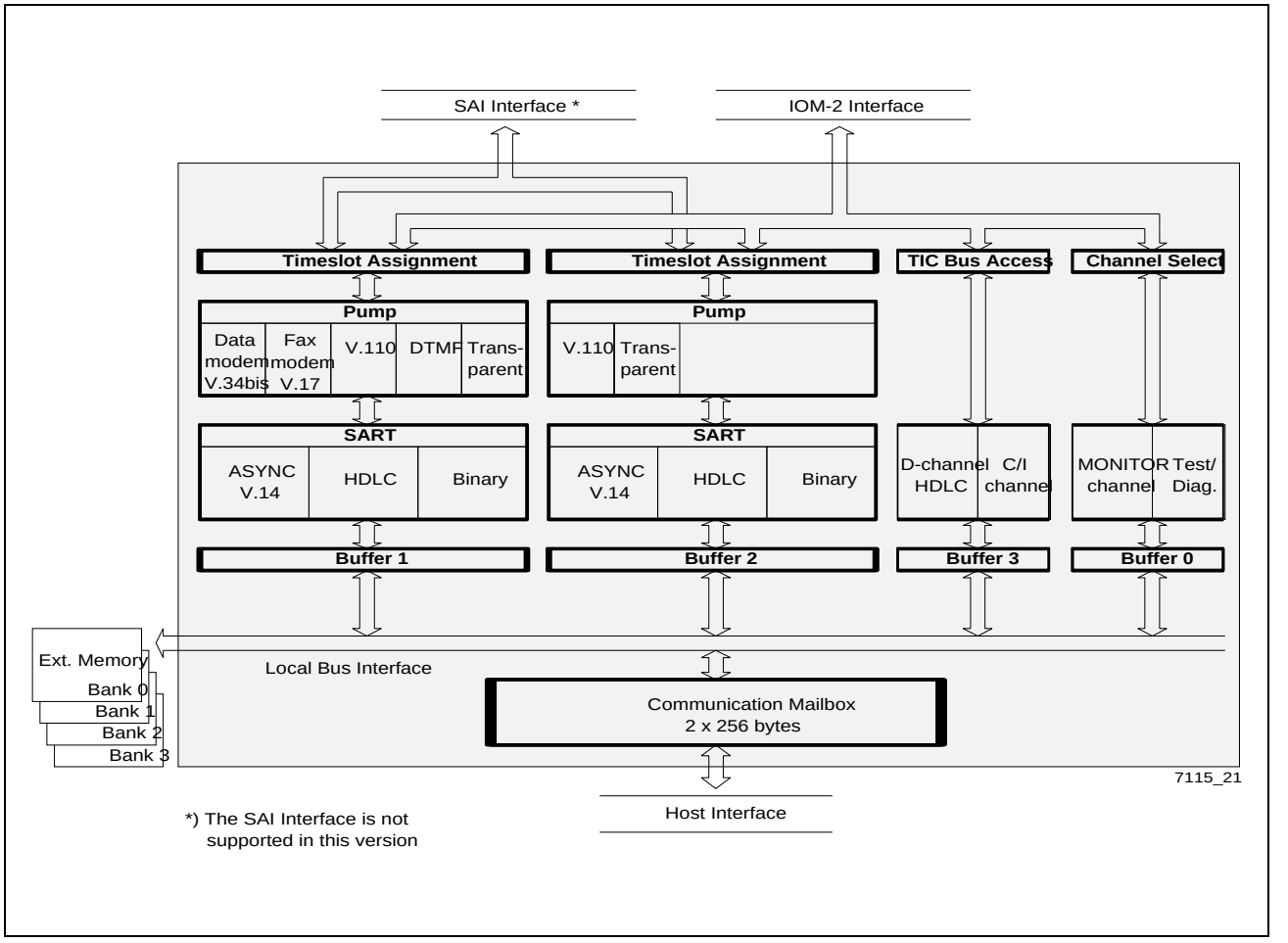


Figure 9 Functional Block Diagram of the ISDN Data Access Controller

2.2 Clock Generation

The chip internal clocks are derived from a crystal connected across XTAL1 and XTAL2 or from an external clock input via pin XTAL1.

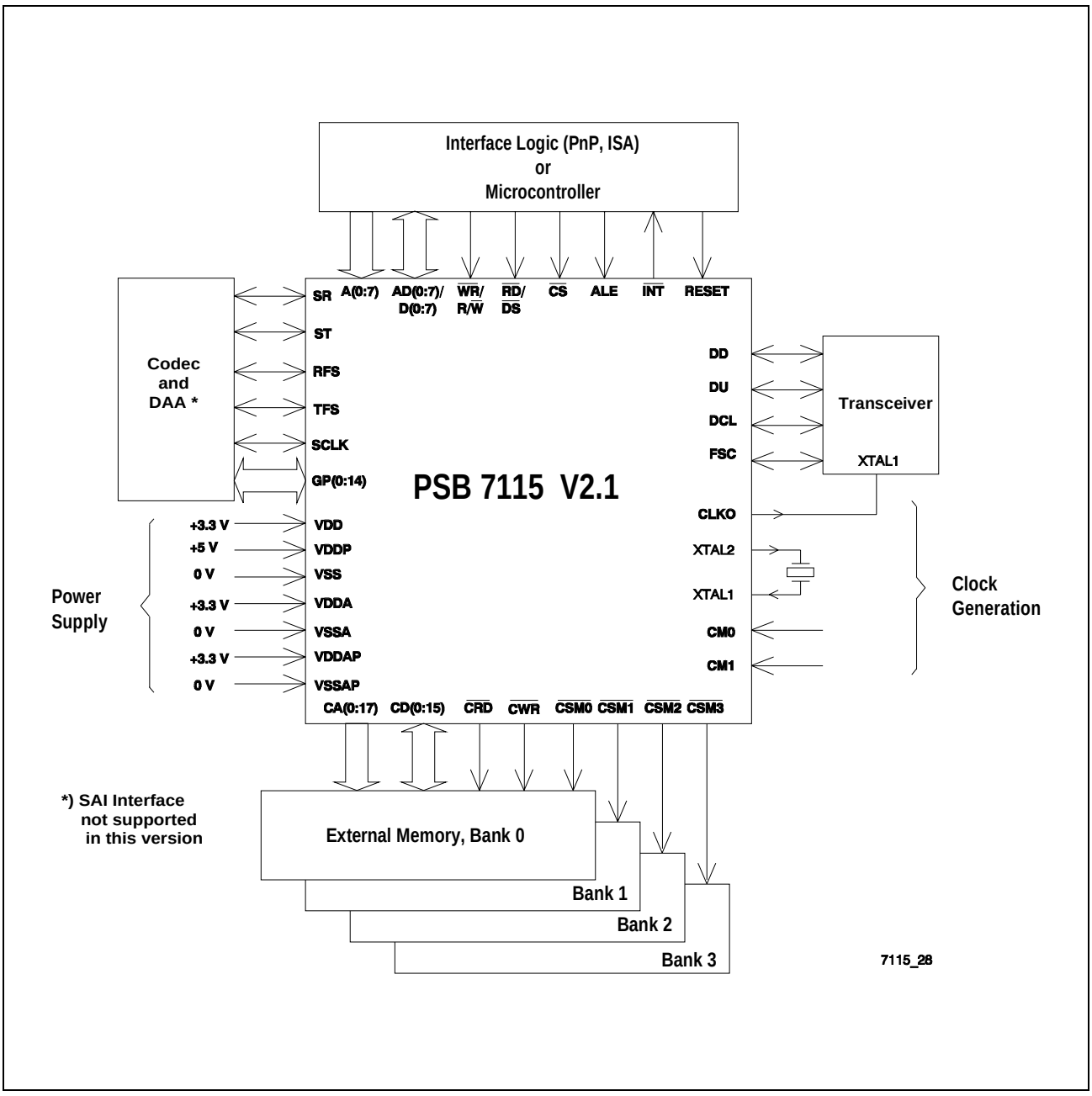


Figure 10 Clock Generation

One of four options can be used for the generation of the internal DSP master clock which is used for the fax/modem pump for example. Other functional blocks derive their clock signal directly from the IOM-2 interface.

An internal PLL derives the DSP clock from a 7.68 MHz, 15.36 MHz or 16.384 MHz source at XTAL1 (see **table 1**). In test mode the internal PLL is bypassed and the DSP clock is directly provided at XTAL1 .

Table 1 Clock Mode Settings

CM1	CM0	Clock at XTAL1	Comment
0	0	DSP clock	Test mode (PLL bypassed)
0	1	7.68 MHz	S-terminal applications
1	0	15.36 MHz	U-terminal applications
1	1	16.384 MHz	Analog modem applications (ALIS)

Note: The clock mode CM1,0 = 11 is reserved for further use as the serial audio interface (SAI) to connect the ALIS is not supported in this version.

At CLKO a buffered output clock equal to the input clock at XTAL1 is provided. This allows for hardware designs that only require one crystal for two or more devices on the system.

The 7.68 MHz crystal is commonly used in terminal equipment with S-interface, e.g. the ISAR 34 together with the S-transceiver ISAC-S TE PSB 2186. One crystal is connected to the ISAR 34 and CLKO is connected to the XTAL1 input of the ISAC-S TE.

For U-terminals a 15.36 MHz crystal is provided at the ISAR 34 and in the same way the U-transceiver IEC-Q TE PSB 21911 derives its input clock from CLKO.

In analog modem applications with the ALIS a 16.384 MHz crystal provides the common clock for ISAR 34 and ALIS. This mode is reserved for further use.

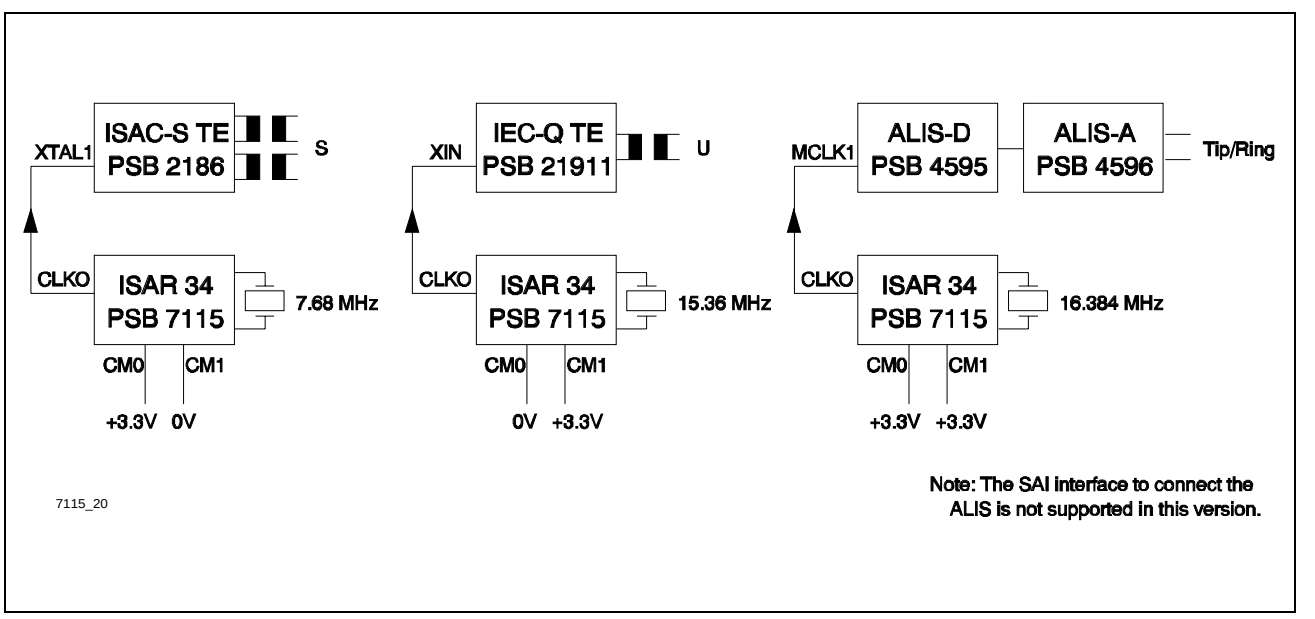


Figure 11 Clock Mode Applications

2.3 Physical Interfaces

The ISAR 34 provides five physical interfaces which are described in the following chapters:

- Host Interface
- IOM-2 Interface
- Serial Audio Interface - SAI (not supported in this version)
- External Memory Interface
- General Purpose I/O Interface

2.3.1 Host Interface

The ISAR 34 is programmed via an 8-bit parallel host interface **(table 2**) that can be operated in multiplexed or non-multiplexed bus mode.

Table 2 Host Interface Signals

Symbol	Input (I) Output (O)	Function
AD(0:7)	I/O	**Address/Data Bus (multiplexed mode)** Transfers addresses and data between the host and the ISAR 34.
D(0:7)		**Data Bus (non-multiplexed mode)** Transfers data between the host and the ISAR 34.
A(0:7)	I	**Address Bus (non-multiplexed mode)** Input address to the ISAR 34 registers.
$\overline{RD}$	I	**Read (Siemens/Intel bus mode)** This signal indicates a read operation.
$\overline{DS}$		**Data Strobe (Motorola bus mode)** The rising edge marks the end of a valid read or write operation.
$\overline{WR}$	I	**Write (Siemens/Intel bus mode)** This signal indicates a write operation.
R/$\overline{W}$		**Read/Write (Motorola bus mode)** A "1" identifies a valid host access as a read operation and a "0" identifies it as a write operation.
$\overline{CS}$	I	**Chip Select** A "0" on this line selects the ISAR 34 for a read/write operation.

Table 2 Host Interface Signals

Symbol	Input (I) Output (O)	Function
ALE	I	**Address Latch Enable** A “1” on this line indicates an address on AD (0:7), that is latched by the ISAR 34 (multiplexed mode only). ALE also selects the interface mode (multiplexed or non-multiplexed).
$\overline{\text{INT}}$	O (OD)	**Interrupt Request** This is the interrupt output line to the host for all mailbox interrupt status requests. It is an open drain output.

The ISAR 34 provides three types of µP buses, which are selected via pin ALE:

Table 3 Bus Operation Modes

1	ALE tied to V_{DD}	**Motorola** type with control signals **$\overline{\text{CS}}$, R/$\overline{\text{W}}$, $\overline{\text{DS}}$**
2	ALE tied to V_{SS}	**Siemens/Intel non-multiplexed** bus type with control signals **$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$**
3	Edge on ALE	**Siemens/Intel multiplexed** address/data bus type with control signals **$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$, ALE**

The occurrence of an edge on ALE, either positive or negative, at any time during the operation immediately selects the interface type 3. A return to one of the other interface types is possible only if a hardware reset is issued.

Note: If the multiplexed address/data bus type 3 is selected, the unused address pins A0-A7 must be tied to V_{DD}.

Since the mailbox structure of the ISAR 34 just requires 9 register locations, the host needs to decode only 4 address lines A0-3 in non-multiplexed bus mode while the other address lines A4-7 are strapped to ’0’. If the Software Reset (bit RST) is not required only 3 address lines A0-2 need to be decoded (address 00h-07h).

All remaining address locations (09h-FFh) are reserved for further use and should not be accessed by the host.

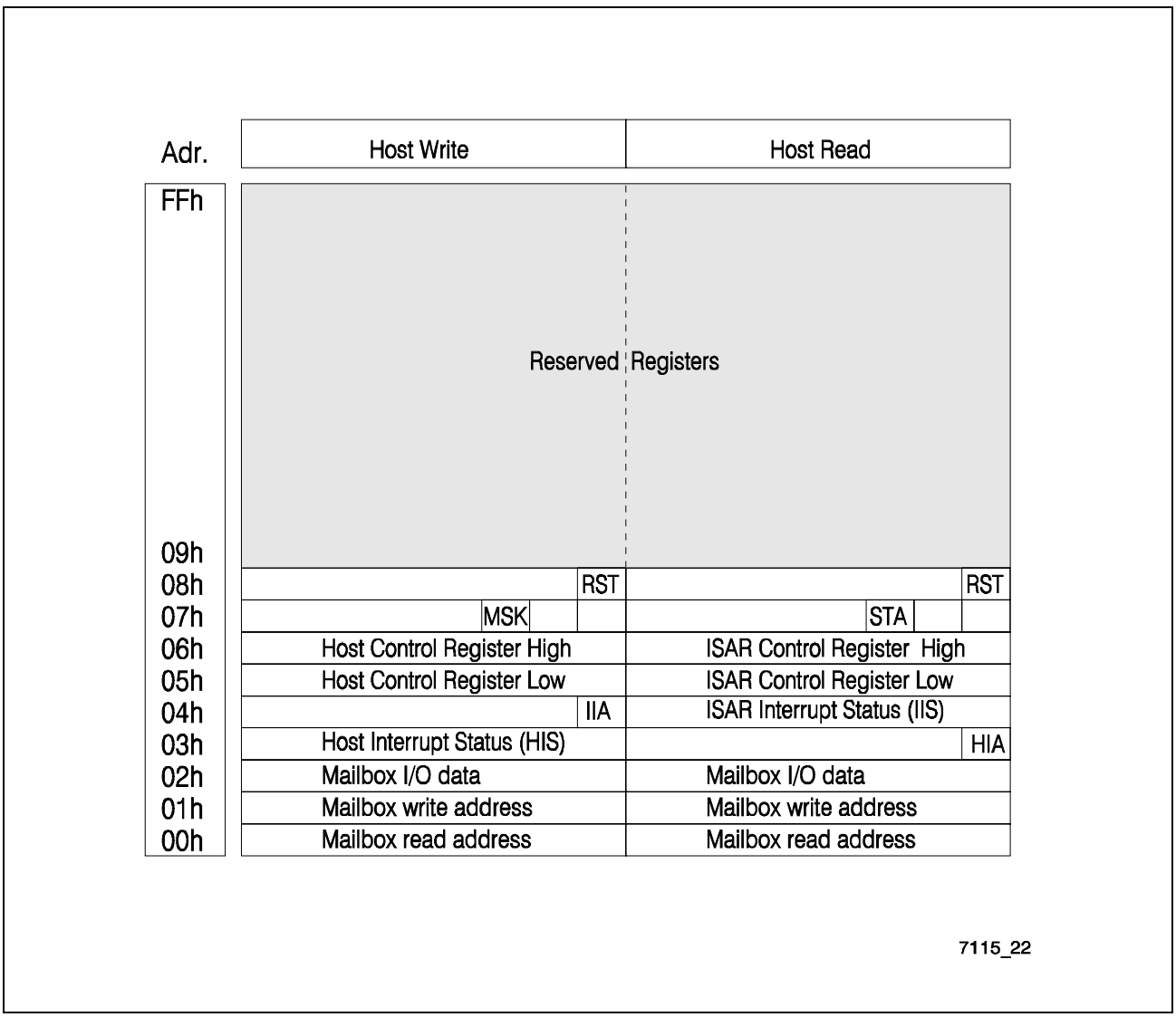


Figure 12 Register Access in Multiplexed and Non-Multiplexed Mode

2.3.2 IOM®-2 Interface

The IOM-2 interface is a 4-wire interface with two data lines (DU and DD), a data clock (DCL) and a frame sync signal (FSC), of which the rising edge indicates the start of an IOM-2 frame (8 kHz). For IOM-2 applications the data clock is typically set to twice the data rate.

IOM®-2 Driver

The output driver of the DD and DU pins is selectable, open drain (default) or push pull. The output drivers are active for the selected time-slot bits and remain tri-state during the rest of the frame.

The control lines FSC and DCL are input or output.

IOM®-2 Frame Structure/Timing Modes

The ISAR 34 supports the IOM-2 terminal and line-card mode.
In terminal mode, the three channel IOM-2 structure is used (see **figure 14**). In line-card mode (see **figure 13**), eight IOM-2 channels can be programmed with flexible time-slot assignment of the B-channel data.

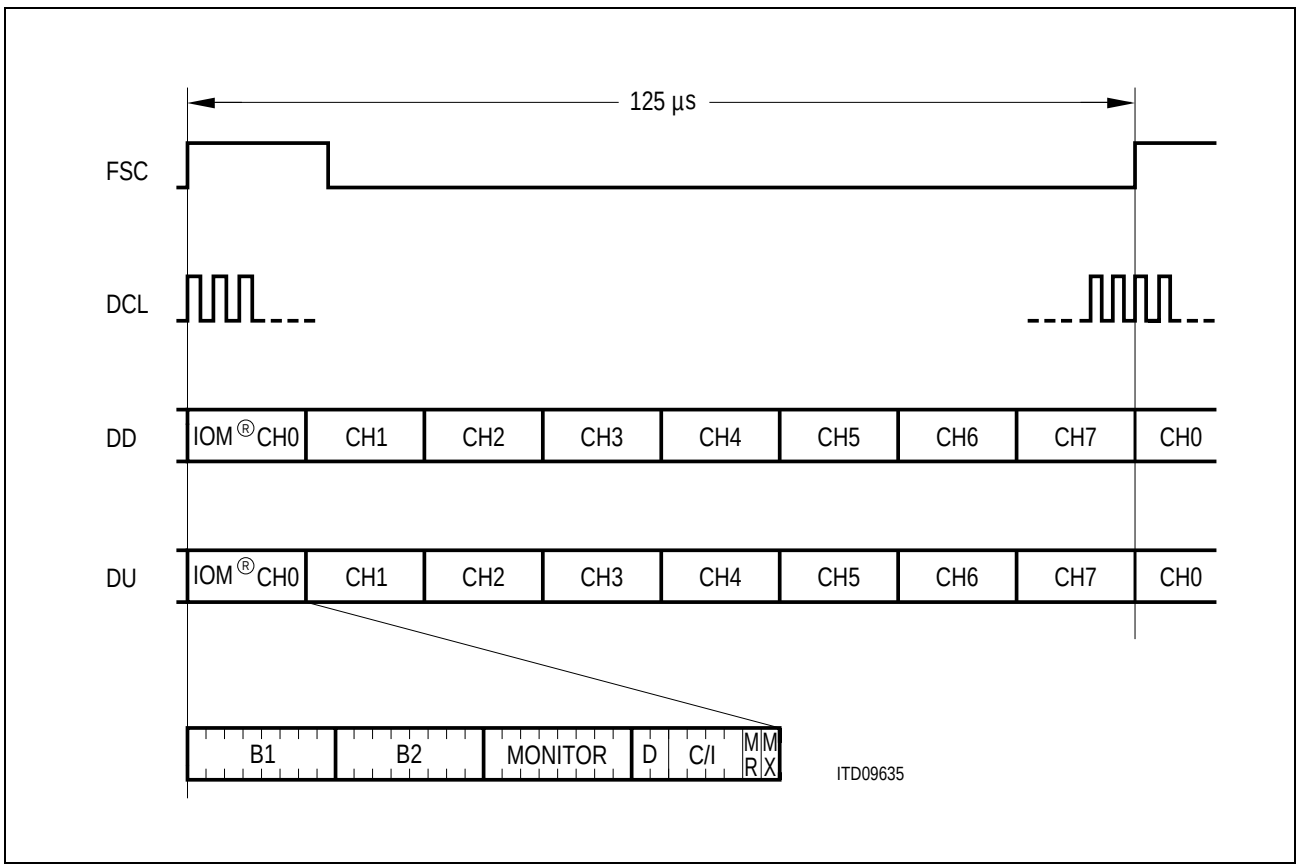


Figure 13 Linecard Mode of the IOM-2 Interface

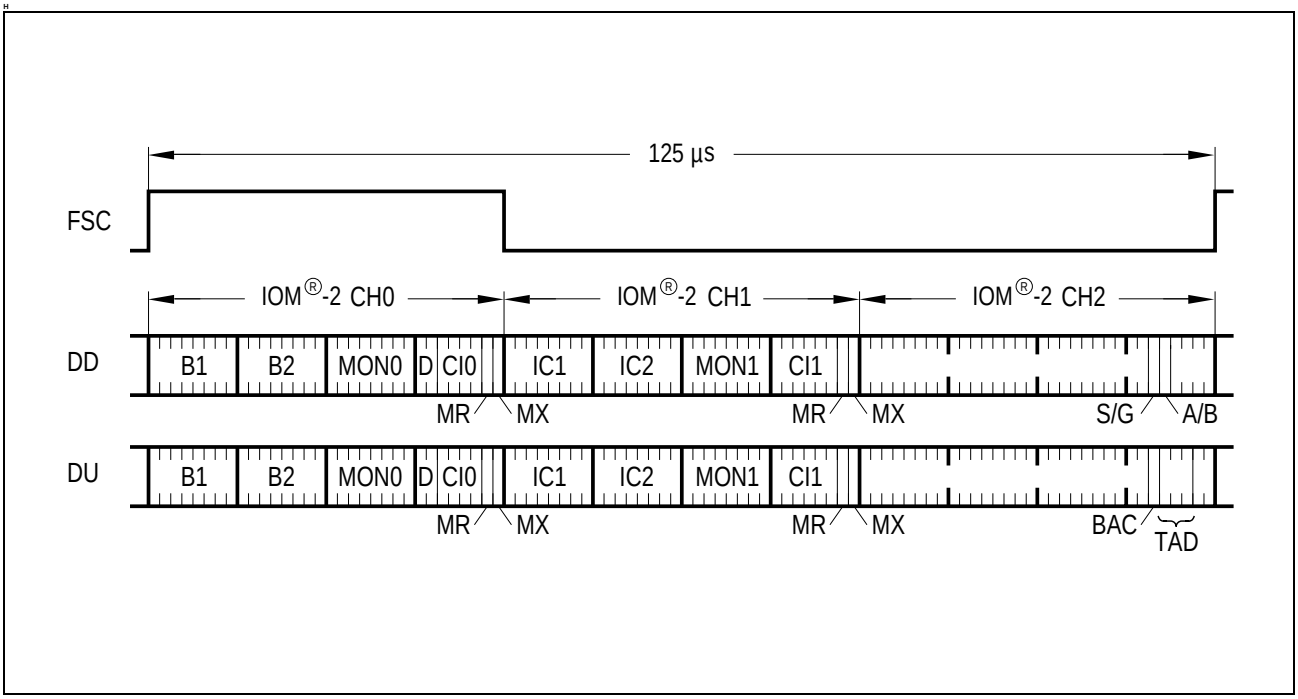


Figure 14 Terminal mode of the IOM-2 Interface

The ISAR 34 is able to make extensive use of the IOM-2 channels as it is able to access all user data timeslots by programming the timeslot number and bit shift.
The MONITOR channel is used for information exchange between the ISAR 34 and other devices connected to the IOM-2 interface. In the C/I-channel real time status information is exchanged between the devices. Both types of information transfer are supported by the ISAR 34 which provides a MONITOR and C/I-channel handler.

In TE mode the TIC bus capability is implemented in the last octet of the third IOM-2 channel (channel 2). This arbitration mechanism which allows the access of up to seven D-channel sources on the IOM-2 interface, is implemented on the ISAR 34.

For detailed information refer to the “IOM-2 Interface Reference Guide”.

2.3.3 SAI Interface

The Serial Audio Interface (SAI) is not supported in this version, but in further versions of the ISAR 34.

2.3.4 External Memory Interface

External memory is required to store operational data and the DSP program. Up to four memory banks with an address range of 256Kx16 each can be addressed, however the specific memory configuration depends on the application.

Generally the platform is capable of the following options:

Operational data is stored in external SRAM whereas the storage of the DSP program code depends on the application. For PC based applications (e.g. plug in card) it can be downloaded into external SRAM, whereas for standalone systems (e.g. settop box) it is stored in non-volatile memory (e.g. flash), so no program download is necessary.

The first version of ISAR 34, which is described in this specification, supports only the DSP Program Download Mode.

DSP Program Download

The DSP program is downloaded from the host into the external memory of the ISAR 34. One memory bank of 128Kx16, 15 ns is connected to $\overline{\text{CSM0}}$ (memory bank 0). The other memory banks ($\overline{\text{CSM1-3}}$) are not used.

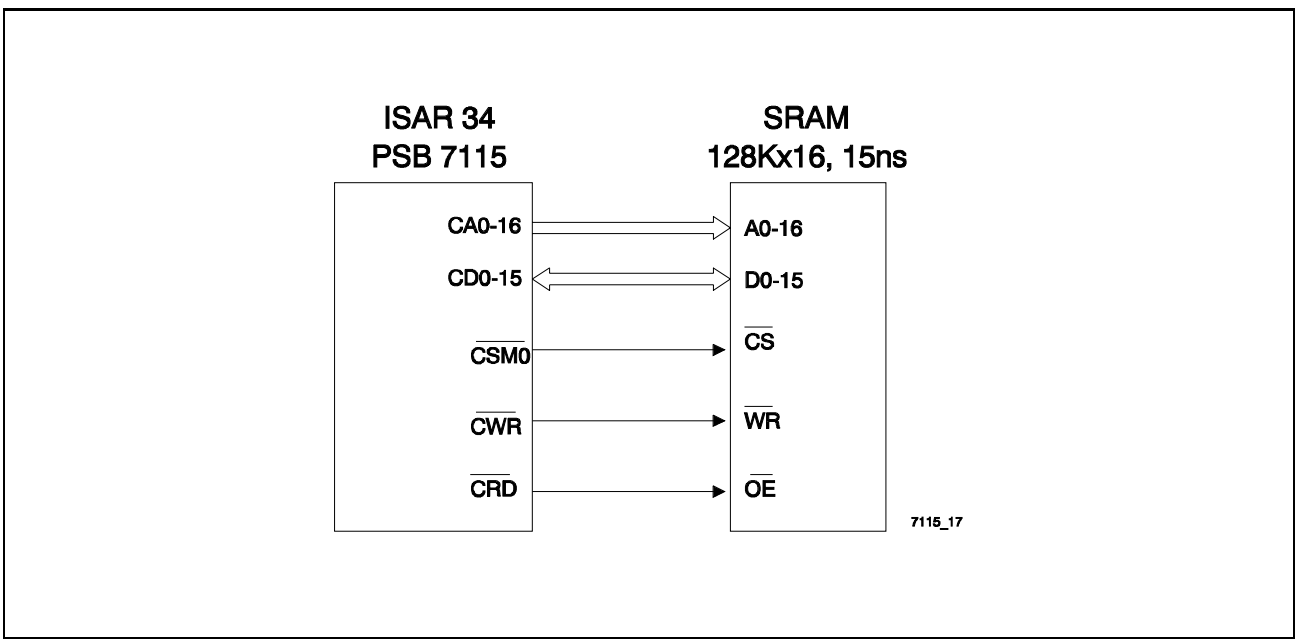


Figure 15 Memory Configuration - DSP Program Download

Other memory configurations (e.g. DSP program in flash memory) can be supported in further versions of the ISAR 34.

2.3.5 General Purpose I/O Interface

The ISAR 34 provides a general purpose I/O interface GPIO that fulfils the requirements for different applications. Each of the 15 pins can individually be programmed as an input or an output. As input they can additionally generate an interrupt. This interface can flexibly be used for general control functions or status indications from external devices. For example in modem applications hook switch and ring detect can be controlled via GPIO-pins.

All kind of data is exchanged between host and ISAR 34 in a message oriented way via the mailbox interface, i.e. the GPIO pins are controlled via the DSP.

The host releases messages to control the GPIO interface, which are:

- Output Request: A logic ’0’ or ’1’ is output on the output port.
- Input Request: The status of the input port is requested.

The ISAR 34 returns messages with the following information:

- Input Response: The status (’0’ or ’1’) of the input port is returned.
- Input Interrupt: A status change on the interrupt input port is indicated.

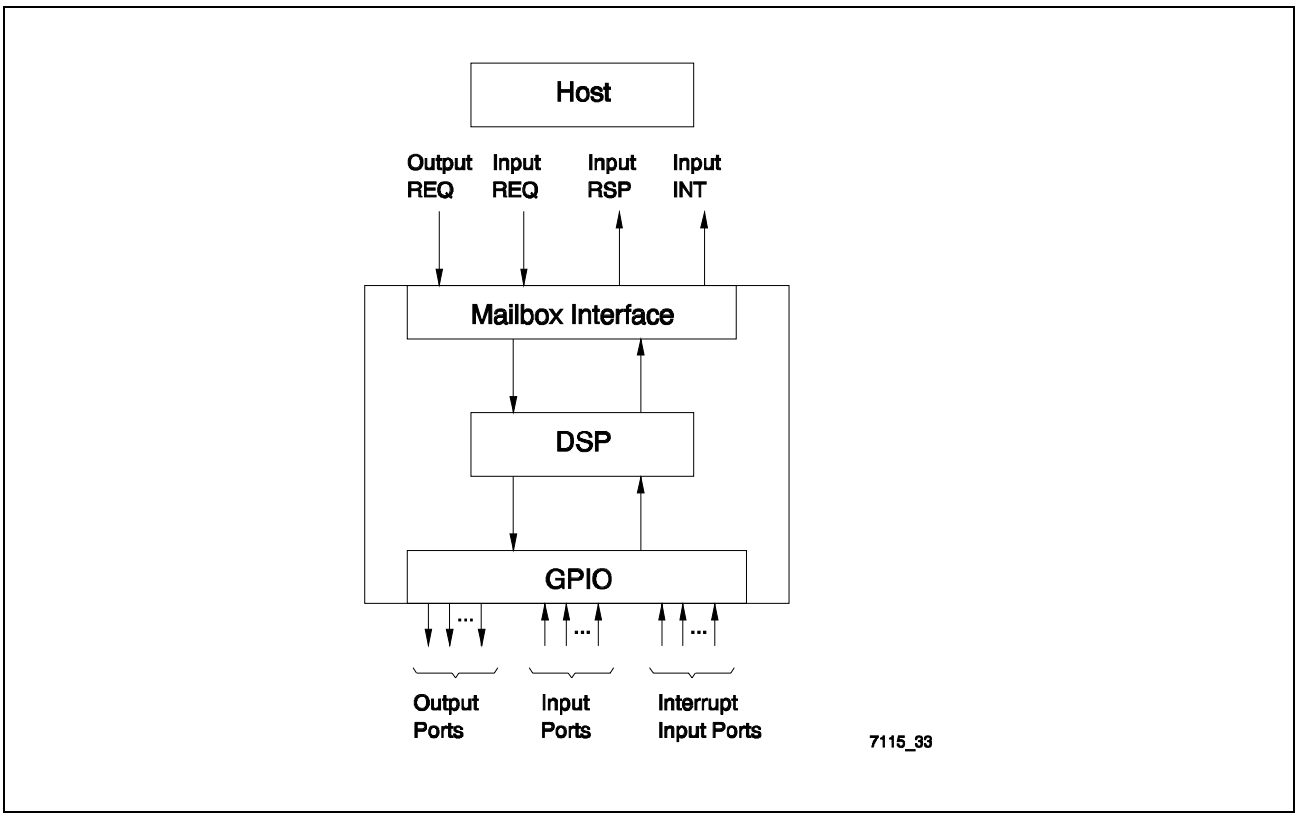


Figure 16 General Purpose I/O Interface

If enabled, a state change on input ports can initiate an interrupt to the host which is generated by the DSP. The status of the corresponding port is read by the host in a status indication message.

The host programs whether a positive or negative signal edge on the input port will release an interrupt to the host (**figure 17**).

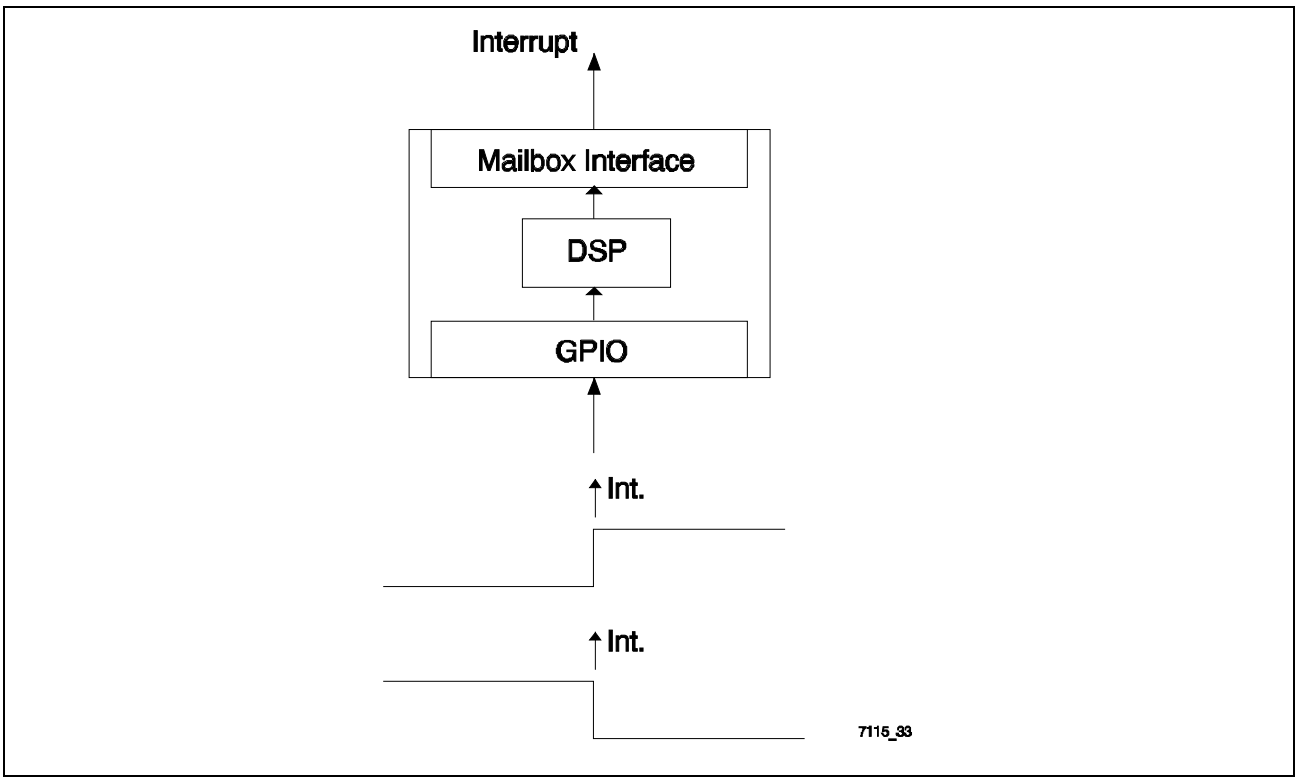


Figure 17 Interrupt Input Signal

2.4 Communications Interface

The ISAR 34 provides a communications interface in terms of a 256 byte mailbox per direction, a 16 bit control word and an 8 bit interrupt register.

Besides that, there is a reset bit (bit 0 of register 08h), an interrupt mask/status bit (bit 2 of register 07h) and two interrupt acknowledge bits (LSB of address location 04h and 03h, respectively).

The address map is shown in **figure 18**, all other address locations are not used.

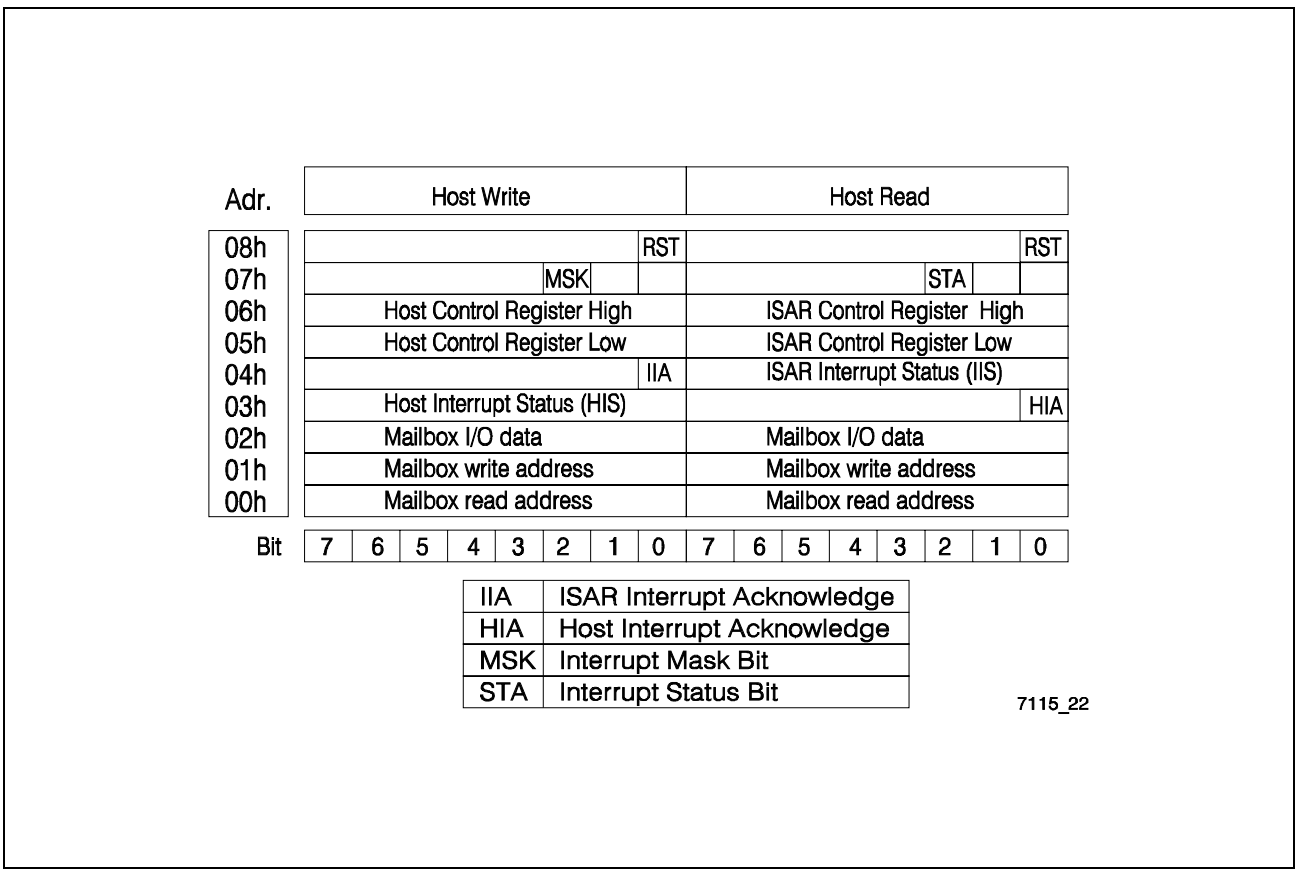


Figure 18 Host Interface Registers

Software Reset Bit (08h Write/Read)

The ISAR 34 is reset by setting and resetting this bit. It has a similar functionality as a hardware reset except this register itself is not affected and the RESET pin is not activated, i.e. the Software Reset has only effect on the internal functions of the ISAR 34.

Interrupt Mask/Status Bit (07h Write/Read)

All interrupt sources can be masked by setting the MSK-bit to ‘0’, so no interrupt is indicated to the host. The status STA-bit indicates whether an interrupt request is pending. If interrupt generation is disabled (MSK=0), requests from the ISAR 34 can be recognized by polling the STA-bit. After reset the interrupt is not masked (MSK=1), however, the mask bit affects only the generation of the interrupt, but not the interrupt status bit from being set.

Host/ISAR Control Registers

The most significant byte of the control register (CTRL MSB) contains configuration, status or control information depending on the type of message.
The least significant byte (CTRL LSB) is used to indicate the number of bytes transferred via the mailbox (Mailbox I/O Data). These mailbox data may contain additional configuration, status or control information as well as receive/transmit data.

Host/ISAR Interrupt Status Byte (HIS/IIS)

The interrupt status byte has a structure that defines the type of message, i.e. it contains information which buffer the message is related to and which functional block of the ISAR 34 the message is related to.

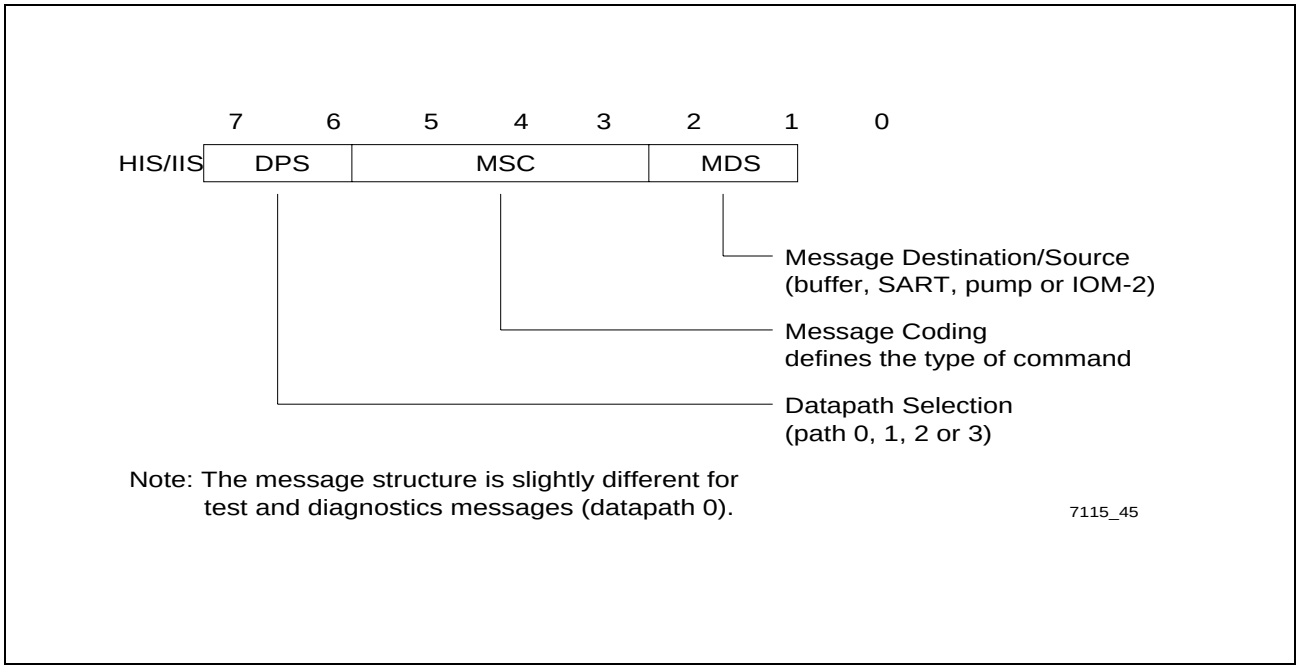


Figure 19 Structure of Interrupt Status Byte

Mailbox

The mailbox is implemented as physically two separate 256-byte memory blocks which is seen from the host as an I/O device. Thus, to read/write a byte from/to the Mailbox, the host accesses a single location (Mailbox I/O data), which is the same address but physically separate location for read and for write direction.

The address is given by an address register directly programmable by the host (Mailbox read/write address). This address is autoincremented every time an access by the host to Mailbox I/O data is performed. Thus, for sequential, fast access, the host only needs to set the start address for the first message byte and all subsequent data bytes can be read/written without reprogramming its address.

For random access to the Mailbox the Host has to reprogram the address register(s).

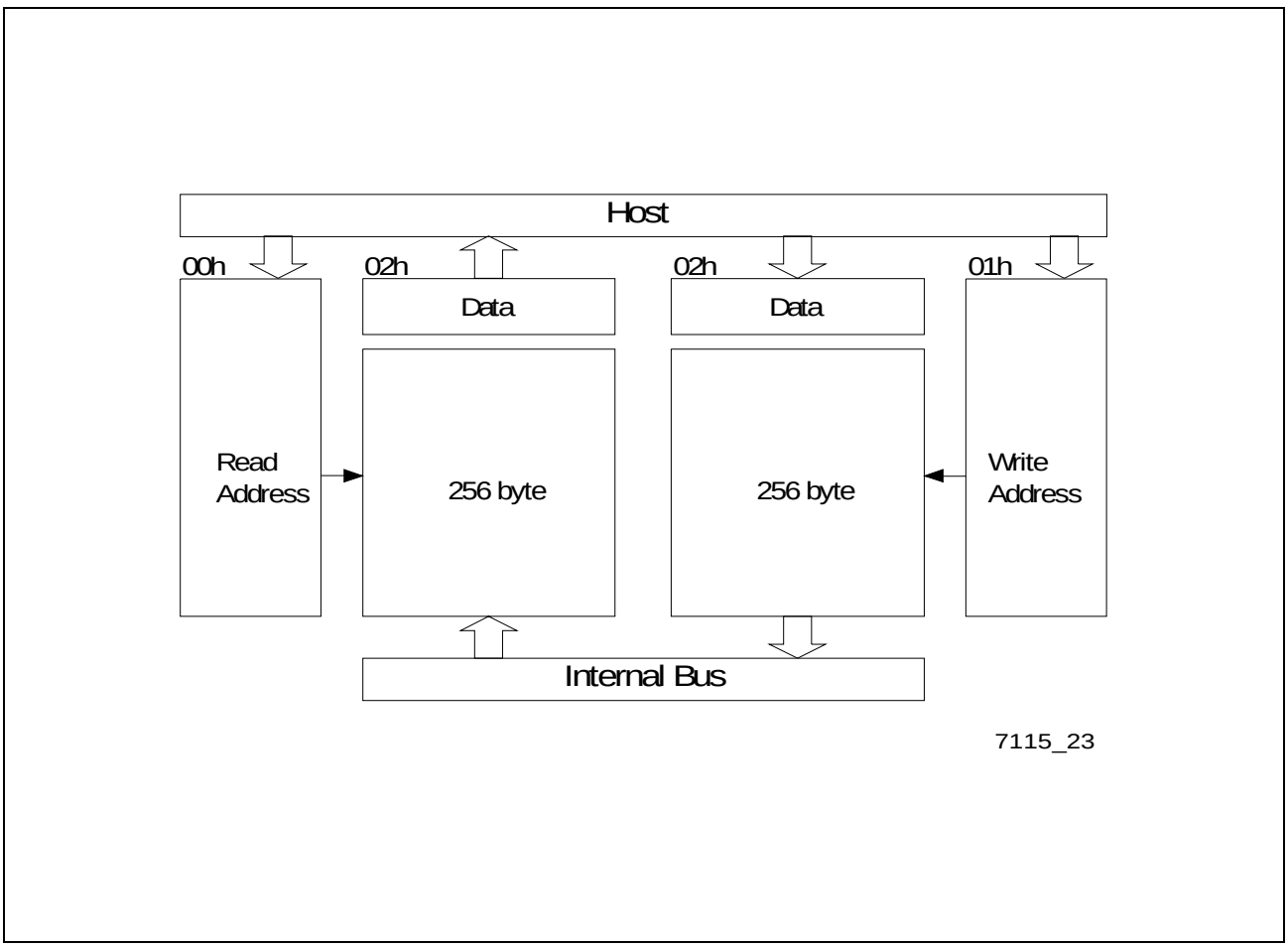


Figure 20 Mailbox Interface

2.5 Functional Blocks

The ISAR 34 host interface provides for merging/splitting of two data paths for B-channel data, one data path for D-channel data and C/I-channel access and a fourth data path for MONITOR channel data and exchange of test/diagnostics messages.

Each path is buffered both in read and write direction and the mailbox is used to access these four buffers.

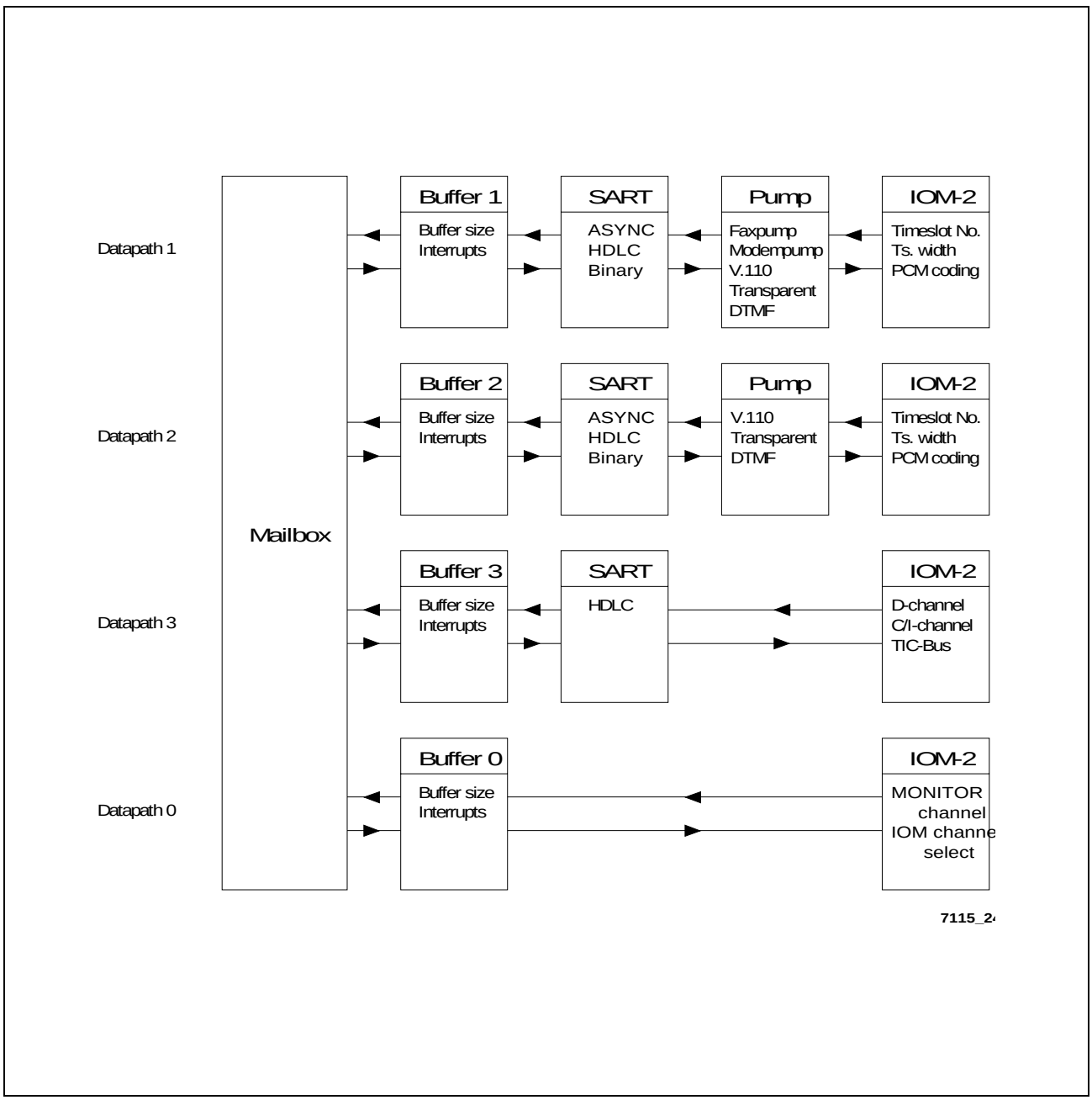


Figure 21 Communication Buffers

Path 1 is used to access the fax/modem engine, a V.110 formatter, a DTMF generator/ detector or for transparent access to the IOM-2 timeslots.

Path 2 is used to access a V.110 formatter or it provides transparent access to the IOM-2 timeslots. This datapath must not be configured to V.110 if path 1 is configured to datamodem modulations at the same time.

Path 1 and 2 integrate a SART (Synchronous Asynchronous Receiver Transmitter) which supports ASYNC, HDLC and binary mode. In ASYNC mode, the characters are formatted according to the ITU-T V.14 standard by start, parity and stop bits. In HDLC mode, the HDLC bit level functions (Flag, CRC, Zero-bit handling) are performed. Binary mode describes a synchronous, transparent mode without formatting.

Path 3 incorporates an HDLC controller for D-channel data transfer and handles the access to the C/I-channel. The ISAR 34 supports the TIC bus arbitration mechanism for those applications where several controllers are connected to the IOM-2 interface.

Path 4 provides a MONITOR channel handler for information exchange with other devices. Messages for test and diagnostics purposes are also transferred via this datapath.

2.5.1 Buffer

The mailbox represents the common host interface for all data paths, which are the two B-Channel paths, the D- and C/I-channel path and the MONITOR channel and test/ diagnostics path. For each data path the read and write direction is buffered with a FIFO (see **figure 22**).

The complete buffer size for one data path is 2x256 byte (path 1, 2 and 3) or 2x64 byte (path 0) per direction. Since the interrupt status byte and the control word is also transferred to the buffer by the ISAR 34, the available FIFO space for user data is reduced by 3 bytes. So messages may contain a maximum number of user data of 253 or 61 byte, respectively.

The maximum possible message length MPL for each path is shown in **table 4**. DPS is the Data Path Select parameter in the Host/ISAR Interrupt status byte (HIS/IIS) of each message.

Table 4 Buffer size

	DPS	MPL	Buffer Size (per direction)
Datapath 0	0 0	61 byte	2 x 64 byte
Datapath 1	0 1	253 byte	2 x 256 byte
Datapath 2	1 0	253 byte	2 x 256 byte
Datapath 3	1 1	253 byte	2 x 256 byte

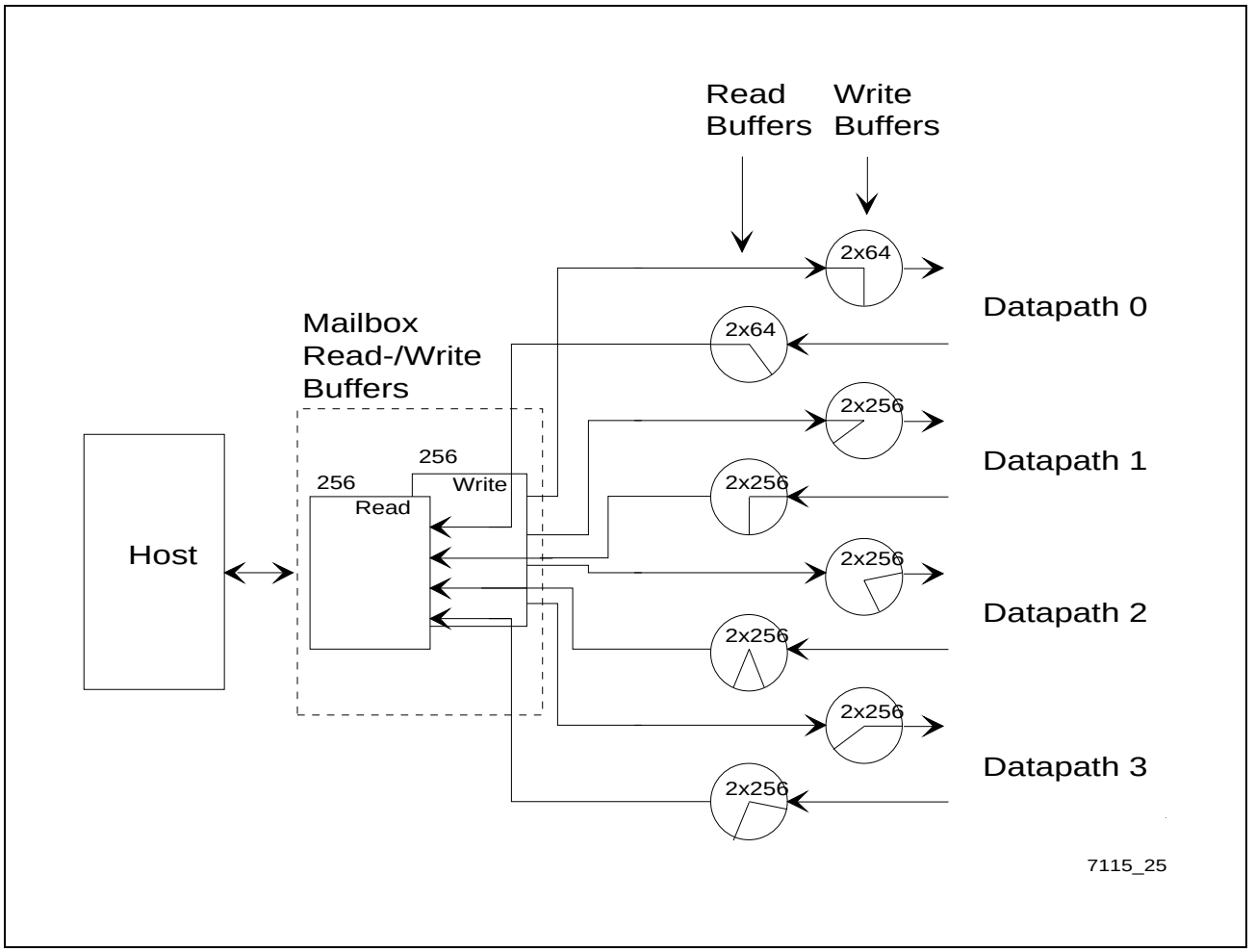


Figure 22 Structure of Datapath Buffers

Buffer Control

After the host has written a message to the write buffer, the ISAR 34 will issue a buffer available interrupt to the host if there is still enough free buffer space for another message of the programmed length (i.e. another message may be written to the mailbox). If the host enters messages into the mailbox which exceed the configured message length, the FIFO buffer may overflow and data might be lost.

If there is no free space available, the ISAR 34 won't issue a data request message.

The buffers can be set a priority to determine the sequence of service if several read buffers request for mailbox service simultaneously.

2.5.2 SART

The SART (Synchronous Asynchronous Receiver Transmitter) can be configured for ASYNC character formatting, HDLC bit level formatting and binary mode. i.e. no bit level formatting. In the figures below the serial audio interface SAI is indicated as future upgrade.

2.5.2.1 HDLC Mode

In HDLC mode, the SART generates/handles the HDLC frame formatting. This includes opening and closing flag, CRC generation/detection and zero-bit insertion (bit stuffing).

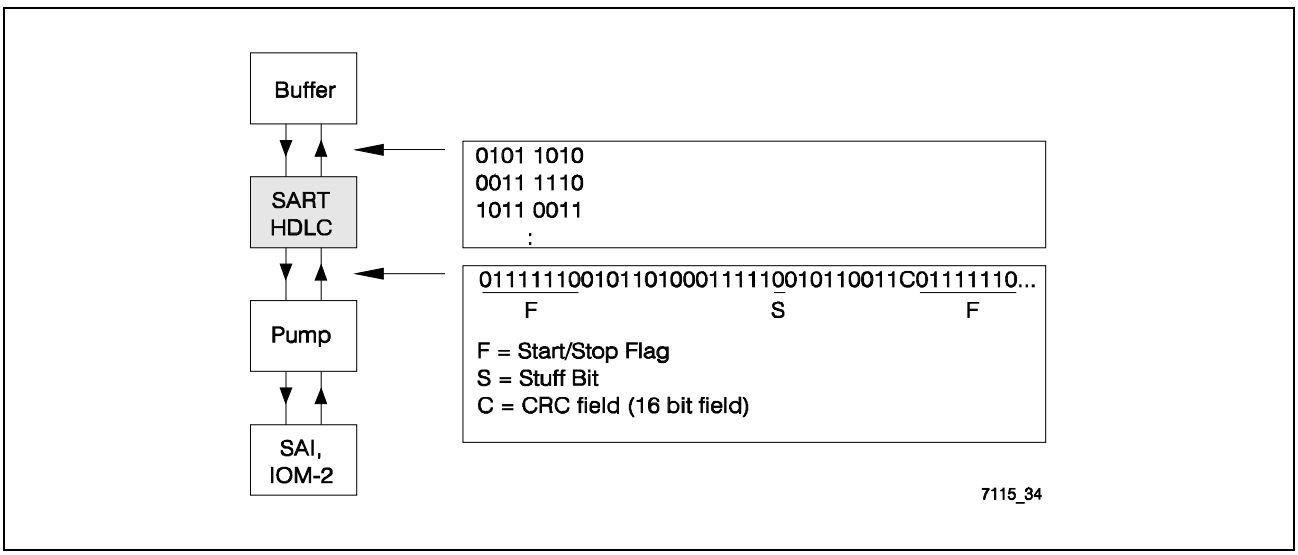


Figure 23 HDLC Data Formatting

Programmable features are:

- CRC: 16 bit length, on/off
- Inter frame timefill: '1' or flags
- Bit stream coding: regular, inverse
- Data underrun operation: Abort generation/frame end (CRC+flag) generation

In transmit direction a frame is started after SART data is available in the transmit FIFO buffer. The frame is continued until a frame end mark has been set in a mailbox command. In this case, the HDLC frame is closed by the CRC value and a closing flag. In case a buffer underrun occurs, the current HDLC frame is closed either by an abort sequence or by CRC and closing flag (programmable).

In receive direction, HDLC frames exceeding the programmed message length are transferred to/from the buffer in data blocks of the configured message length. A message of reduced length may be transferred if a frame start, frame end or error condition is detected. In this case the control word contains the result of the CRC check, verification of integer number of bytes and check of frame end condition.

2.5.2.2 ASYNC Mode

ASYNC denotes an asynchronous formatting of data according to ITU-T specification V.14. In ASYNC mode, the SART adds/removes start, parity and stop bits to each data byte in transmit/receive direction.

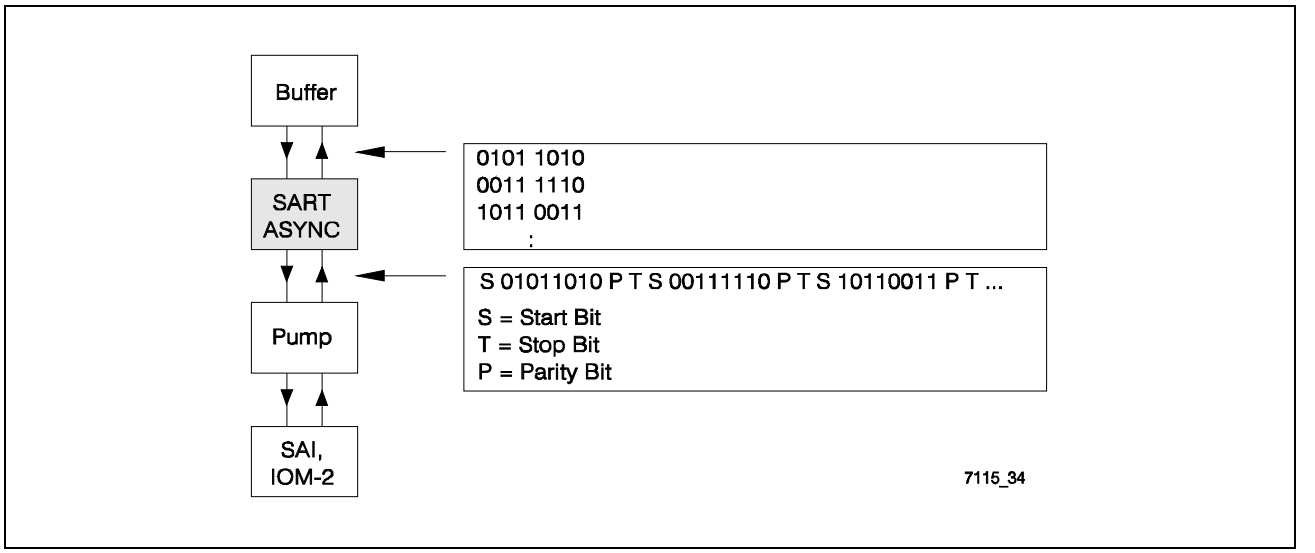


Figure 24 ASYNC Data Formatting

The following options are programmable:

- Character Length: 5, 6, 7, 8 Bit
- No. of stop bits: 1,2
- Parity: No, odd, even, stick parity
- Overspeed range: stop bit deletion: 1 of 8, 1 of 4

The ASYNC formatter supports overspeed handling according to V.14. Therefore a stop bit may be deleted according to the overspeed range.

The ASYNC formatter is able to generate a break signal and to detect a break signal of a minimum length of 2M+3 bits of start bit polarity.

A special option is included to generate V.42 detection timing.

2.5.2.3 Binary Mode

In binary mode no character formatting is performed. Octets are transferred with the least significant bit or most significant bit first.

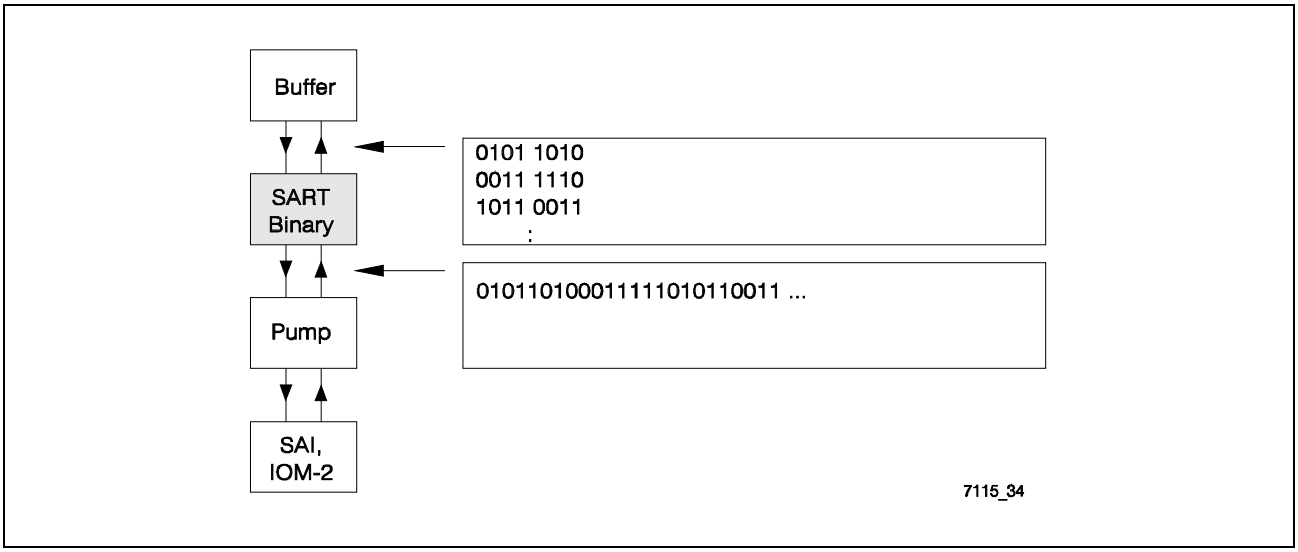


Figure 25 Binary Data

Programmable Features are:

- Idle character generation on data underrun
- Bit swapping (LSB/MSB first)

In transmit direction, data from the transmit buffer is transmitted with the LSB or MSB first. In case of data underrun, i.e. if there's no more data in the transmit buffer, a programmable byte or the last data byte is continuously transmitted.

In receive direction, the data stream is received in octets. Their contents is transferred to the receive buffer .

2.5.3 Pump

Pump in general describes the additional formatting of the SART data (HDLC, ASYNC or binary) which is then forwarded to the IOM-2 interface. In future versions pump data can also be transfered to the serial audio interface (SAI).

The pump modes are:

- Fax modulations (V.17, ...)
- Datamodem modulations (V.34bis, ..)
- Halfduplex modulations
- V.110
- DTMF
- Bypass (transparent data)

All pump modes are available in path 1, path 2 only supports V.110 and bypass mode.

V.110 operation in data path 2 is not supported to run in parallel with datamodem modulations (full duplex modulations) in data path 1.

In the figures below the serial audio interface SAI is indicated as future upgrade.

2.5.3.1 Fax Modulations

The mode fax modulations allows modulation up to V.17 (14400 bit/s).

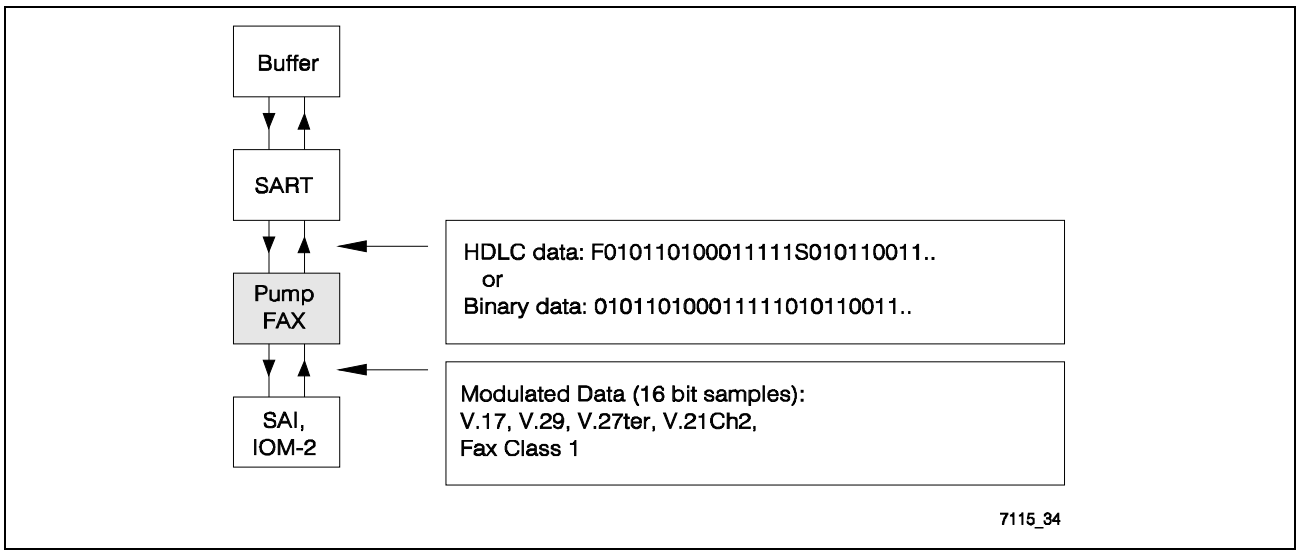


Figure 26 Fax Modulations

Programmable parameters are:

- Originating/Answering Mode
- Enabling/disabling of answer/calling tone
- Transmitter output attenuation
- Modulation scheme (V.17, V.29, V.27ter, V.21 channel 2) set by control commands

In fax modulation mode the ISAR 34 supports the programming interface according to the Fax Class 1 standard EIA/TIA-578. During a fax call different kind of data is transmitted and received, which is HDCL framed data at low speed modulation (V.21Ch2) for exchange of capabilities and call setup/shut down, and binary data at high speed modulation (V.17, V.29 or V.27ter) for document transmission. The host controls these configuration settings by simply issuing a pump control command (FTM, FRM, FTH, FRH) that configures both the pump and the SART, i.e. the host does not need to reconfigure pump and SART separately for the individual fax procedures.

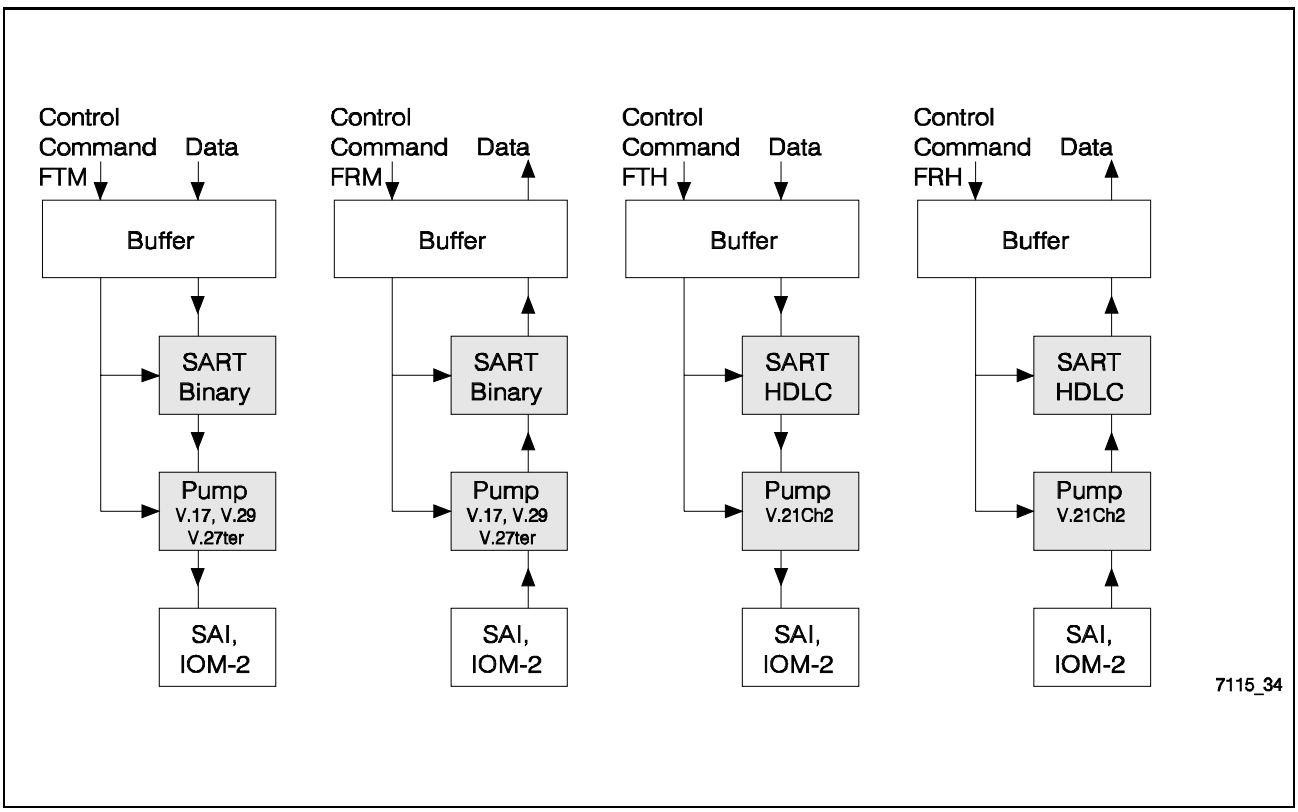


Figure 27 Fax Class 1 Support

2.5.3.2 Datamodem Modulations

This mode allows data modulation up to V.34bis (33600 bit/s).

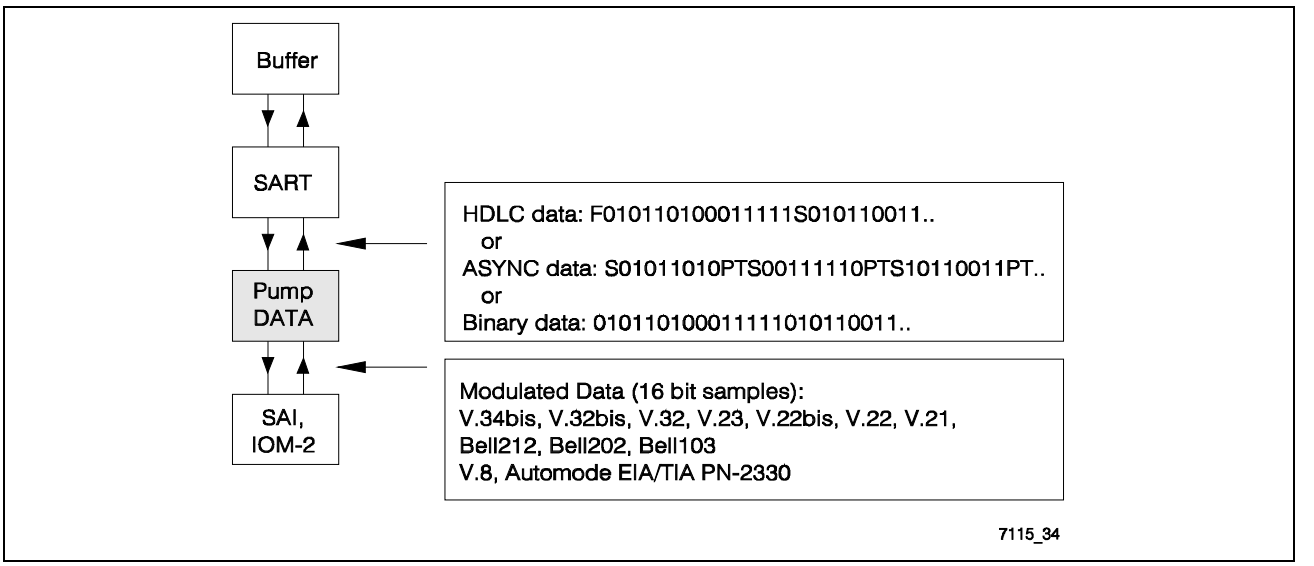


Figure 28 Datamodem Modulations

Programmable parameters are:

- Enabling/disabling of answer/calling tone
- Transmitter output attenuation
- Modulation scheme (V.34bis, V.32bis, V.32, V.23, V.22bis, V.22, V.21, Bell 202, Bell 212, Bell 103)
- Automode (EIA/TIA PN-2330) or dedicated mode
- Modulation options according to the ITU recommendations (fallback rates, retrain, renegotiate, etc.)

2.5.3.3 Halfduplex Modulations

The halfduplex modulations allow modulation up to V.17 (14400 bit/s). In the figures below the serial audio interface SAI is indicated as future upgrade.

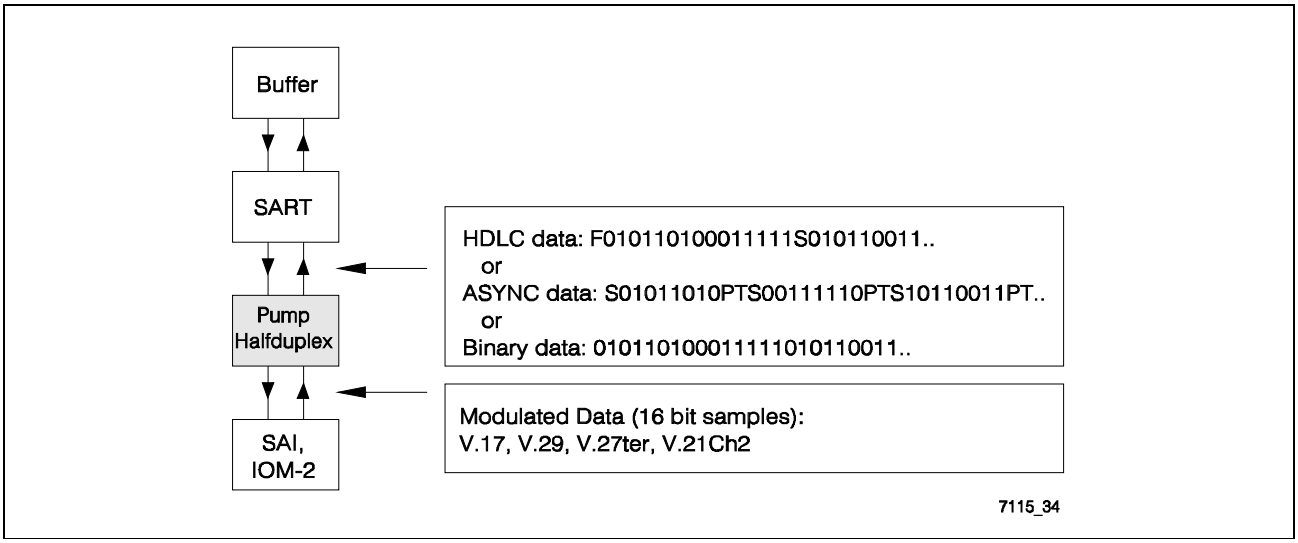


Figure 29 Halfduplex Modulation

Programmable parameters are:

- Enabling/disabling of receive/transmit direction
- Enabling/disabling of echo protector tone
- Transmitter output attenuation
- Modulation scheme (V.17, V.29, V.27ter, V.21)

The modulation schemes which are typically used for fax modulations can be programmed by the host without affecting the SART configuration (see **chapter 2.5.3.1**). In this way the host could handle a fax session by programming the SART and pump (halfduplex modulation) separately, however it is recommended to use the fax mode as it simplifies the control mechanisms of the host (no reconfiguration required).

2.5.3.4 V.110

The V.110 mode allows the framing of SART data for bit rate adaptation according to the ITU-T recommendation V.110.

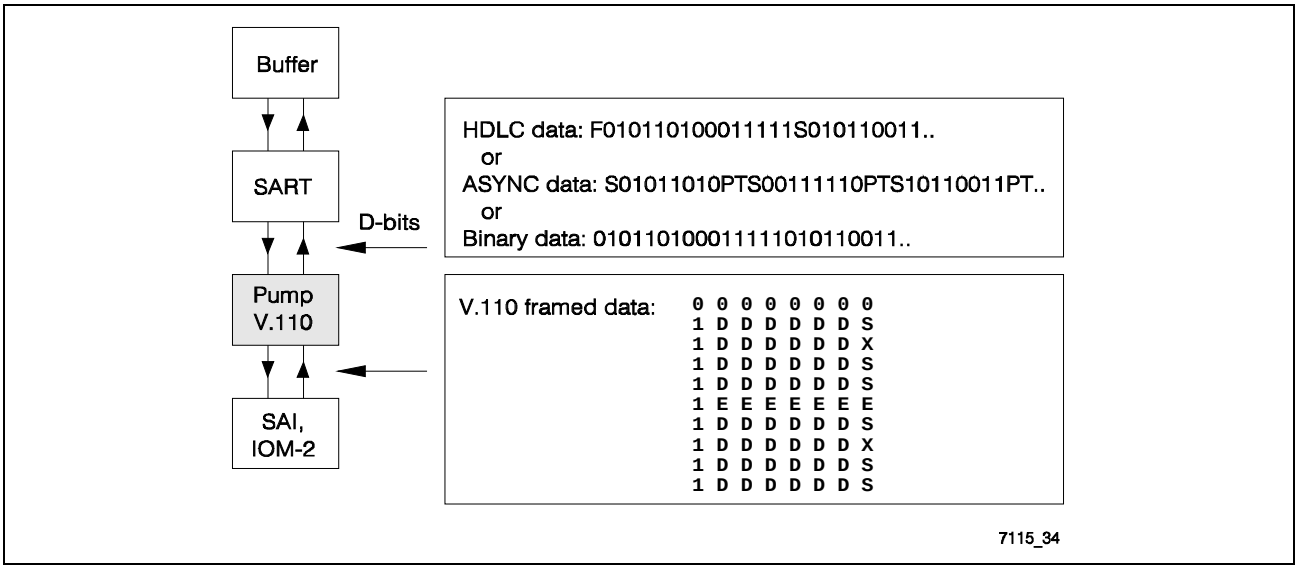


Figure 30 V.110 Formatting

The programmable features are:

- Frame format/data rate
- E-, X-, S-bit control
- Transmitter flow control (X-bits)
- Remote DTE status detection
- Delay of synchronisation

In transmit direction, the V.110 frame is combined with SART data and the state of E-, X- and S-bits. Transmission of the last data byte in the mailbox is indicated to the host (buffer empty condition), which may set control bits.

Flow control by means of the X-bits is supported, which means that data transfer to the SART unit is stopped if indicated by the remote side.

In receive direction, frame synchronization is monitored while the number of frames for synchronisation (normally 1) is programmable. The D-bits are forwarded to the SART and E-, X- and S- bits are forwarded to the host as status events any time they change their state.

Status conditions of the remote DTE can be detected and indicated to the host.

2.5.3.5 DTMF

The ISAR 34 supports DTMF generation and detection in one channel (two channels will be supported in the future).

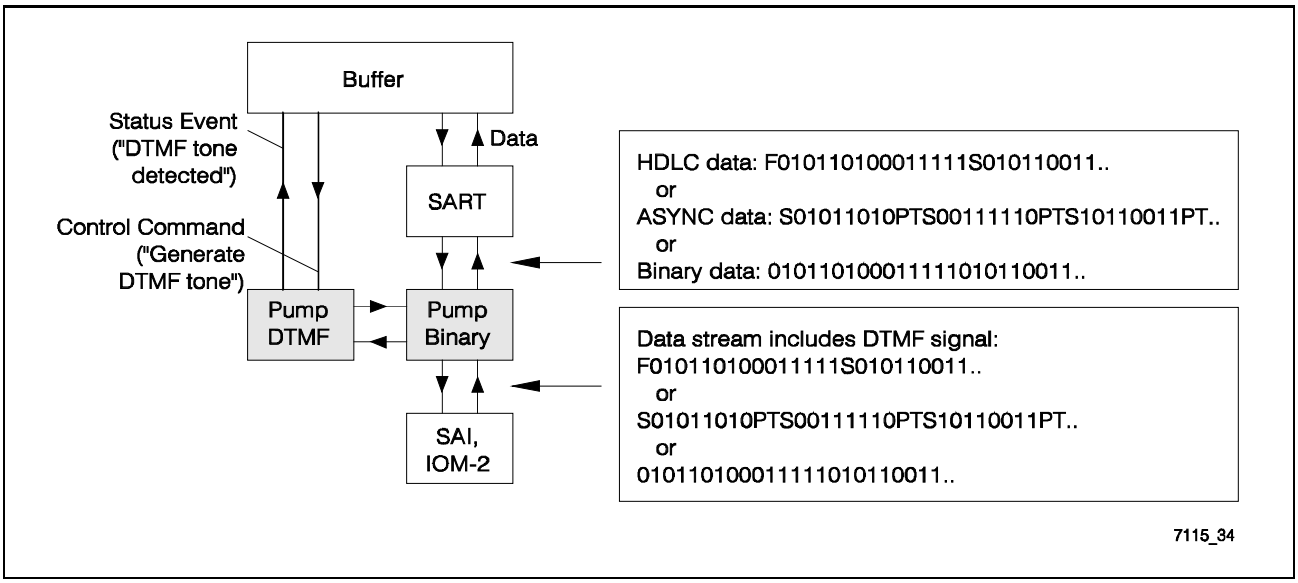


Figure 31 DTMF Detection

DTMF mode allows transparent data transfer between SART unit and data pump while a DTMF detector is active, which indicates received DTMF tones to the host by means of status events.

In order to send a DTMF tone (’0’, ’1’, ’2’, ... , ’9’, ’A’, ’B’, ’C’, ’D’, ’∗’, ’#’) the host releases a control command to the ISAR 34.

The programmable features are:

- Rejection level (minimum required signal level to detect a DTMF tone)
- Twist (maximum allowed level difference of the two frequencies)
- On duration of DTMF tone (1, 2, 3, ..., 255 ms)
- Off duration after DTMF tone (1, 2, 3, ..., 255 ms)
- Transmitter output attenuation

2.5.3.6 Bypass Mode

The bypass mode allows the transparent transfer of a SART formatted digital data stream to the IOM-2 timeslot without additional data formatting by the pump.

In receive direction, data from the IOM-2 timeslot is directly transferred to the SART.

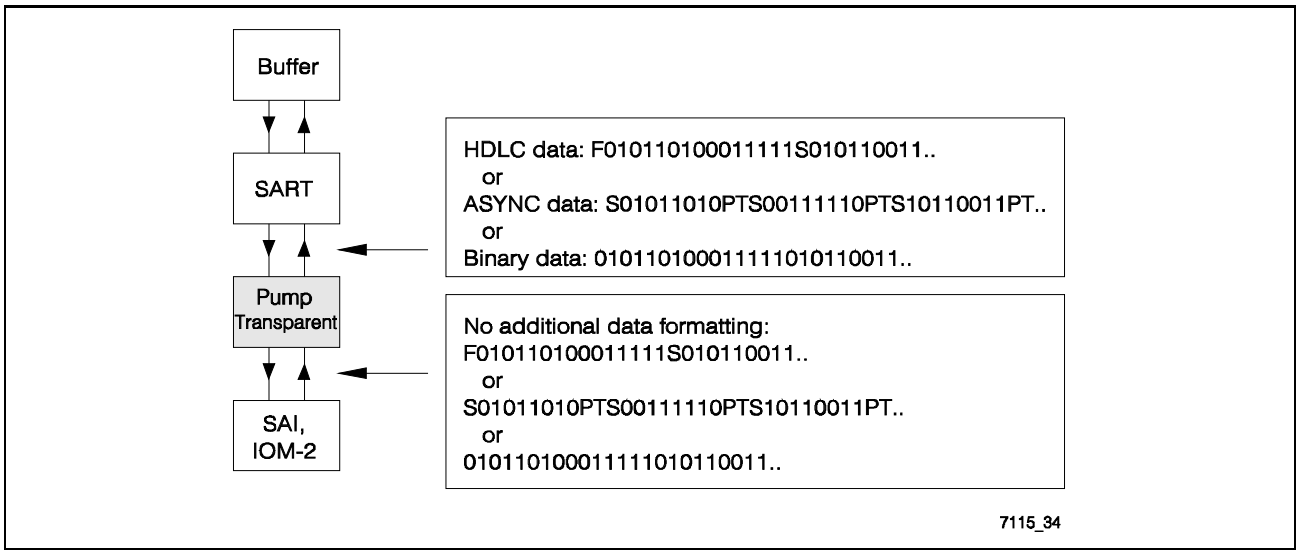


Figure 32 Pump in Bypass Mode

2.5.4 IOM®-2 Configuration

The IOM-2 configurations are separate for each datapath. Via datapath 1 and 2, any timeslot for the output of pump data can be selected.

The following programmable functions are available for path 1 and 2 (**figure 33**):

- Coding (A-law, µ-law or 16-bit linear)
- Timeslot position, i.e. start of timeslot
- Length of timeslot (8 or 16 bit)
- Switching of DU/DD lines

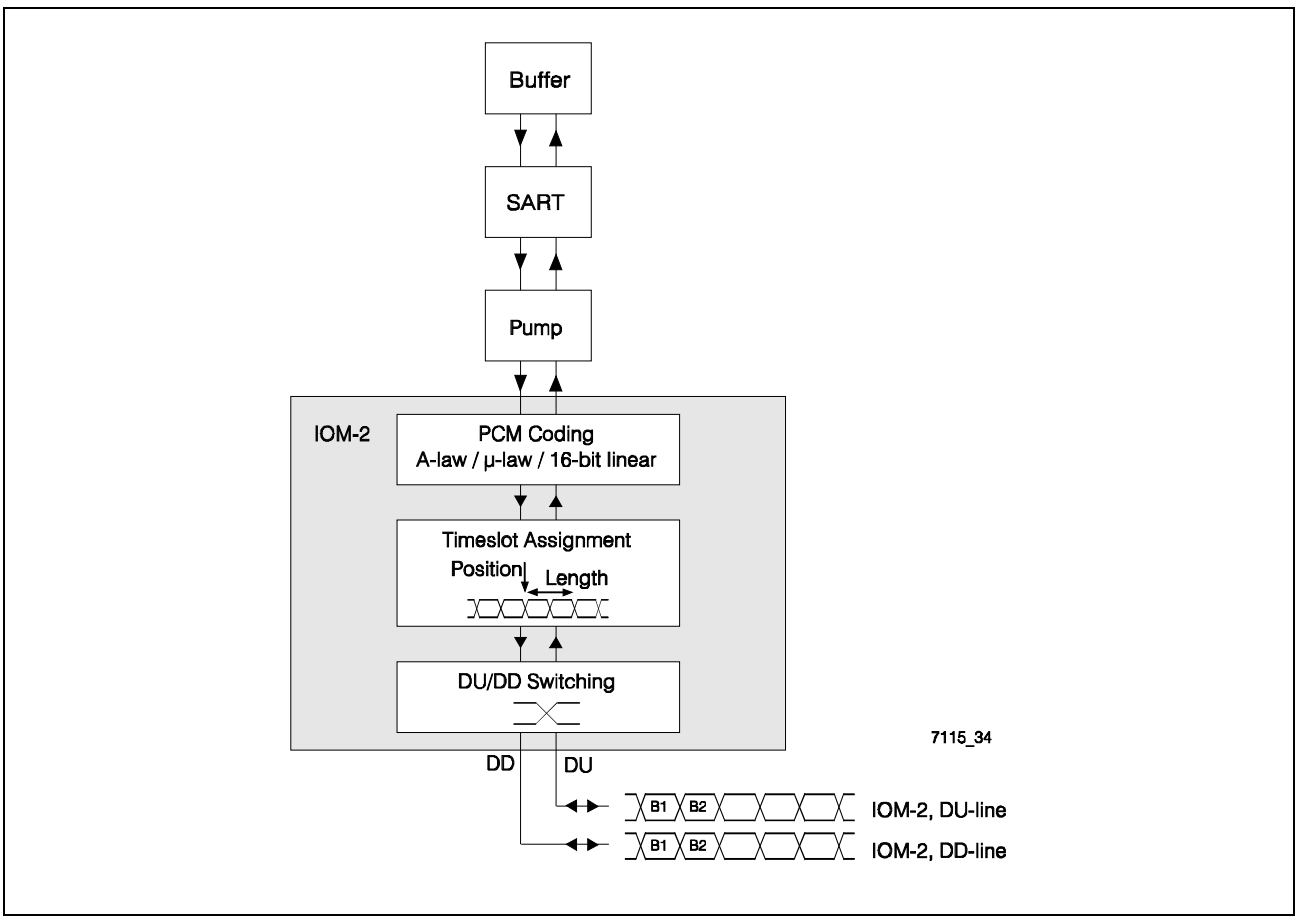


Figure 33 IOM-2 Configuration Parameters

The host must ensure that the programmed timeslots on IOM-2 for path 1 and path 2 do not overlap.

Datapath 3 is dedicated to the D-channel and the C/I-channel timeslot, respectively. The TIC bus access handler which is used in terminal timing mode is operating on the TIC bus channel (3rd channel) on IOM-2.

For the MONITOR channel handler in datapath 0 one of 16 IOM-2 channels can be selected. The access is fixed to the third timeslot (MONITOR channel) of this channel.

2.5.5 D-Channel

The ISAR 34 provides an HDLC controller in datapath 3 which is responsible for the data link layer using HDLC based protocols (LAPD).

The data formatting in path 3 is fixed to HDLC framing, it is not programmable to binary or ASYNC as in path 1 and 2. The timeslot position is fixed to the D-channel timeslot on IOM-2 (first two bits in fourth octett of IOM-2 channel 0). The access to the FIFO buffers for D-channel data is similar as for path 1 and 2.

D-channel access can be performed with or without the TIC-bus access mechanism (see **chapter 2.5.7**).

2.5.6 C/I-Channel

The command/indication channel carries real-time status information between the ISAR 34 and another device connected to the IOM-2 interface.

The ISAR 34 supports the 4-bit C/I0 channel, but it has no access to the 6-bit C/I1 channel.

C/I0 conveys the commands and indications between the layer-1 device and the layer-2 parts of the ISAR 34 and it is used to control the layer-1 activation/deactivation procedures. Access to C/I0 may be arbitrated via the TIC bus access protocol (see **chapter 2.5.7**).

In receive direction the code from layer-1 is continuously monitored and an interrupt is generated to the host anytime a change in the C/I-code is detected. A new code must be found in two consecutive IOM-2 frames to be considered valid and to trigger a C/I-code change interrupt status (double last look criterion).

2.5.7 TIC-Bus Access

The TIC-bus arbitration mechanism which is available in IOM-2 TE mode allows access of several external communication controllers (up to 7) to the layer-1 functions and to the D- and C/I-channel of the transceiver device (**figure 34**).

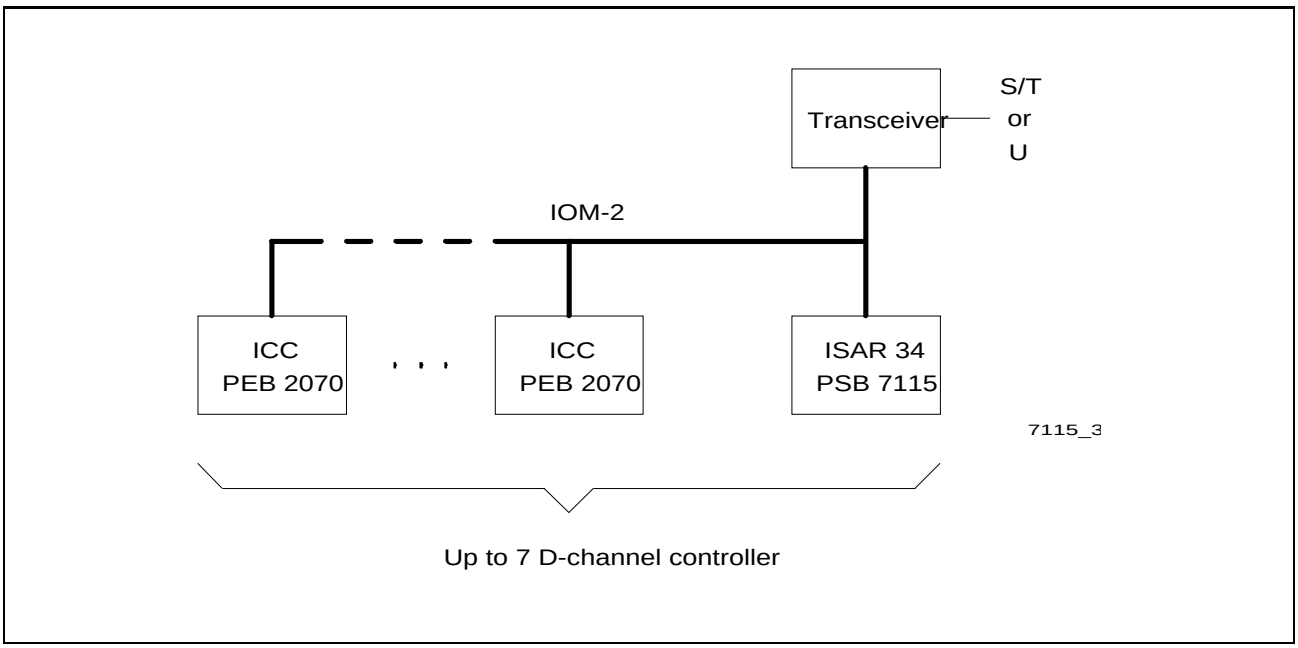


Figure 34 TIC-Bus Application

The TIC-bus is implemented in the last octet of IOM channel 2 (**figure 35 and 36**):

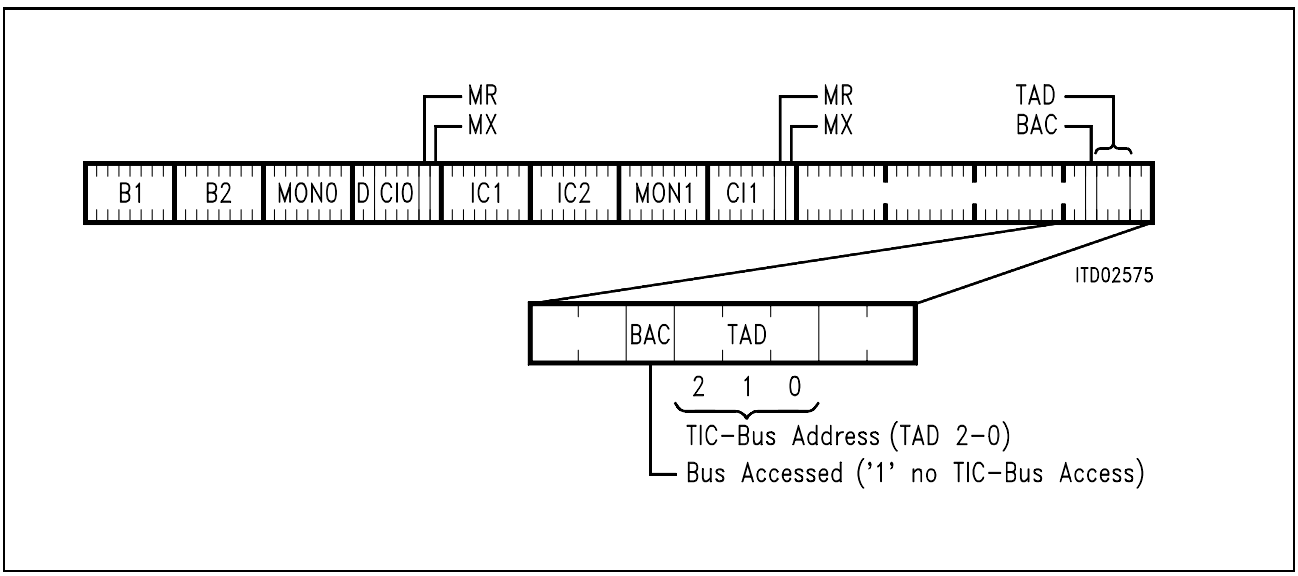


Figure 35 Structure of Last Octet within CH2 on DU

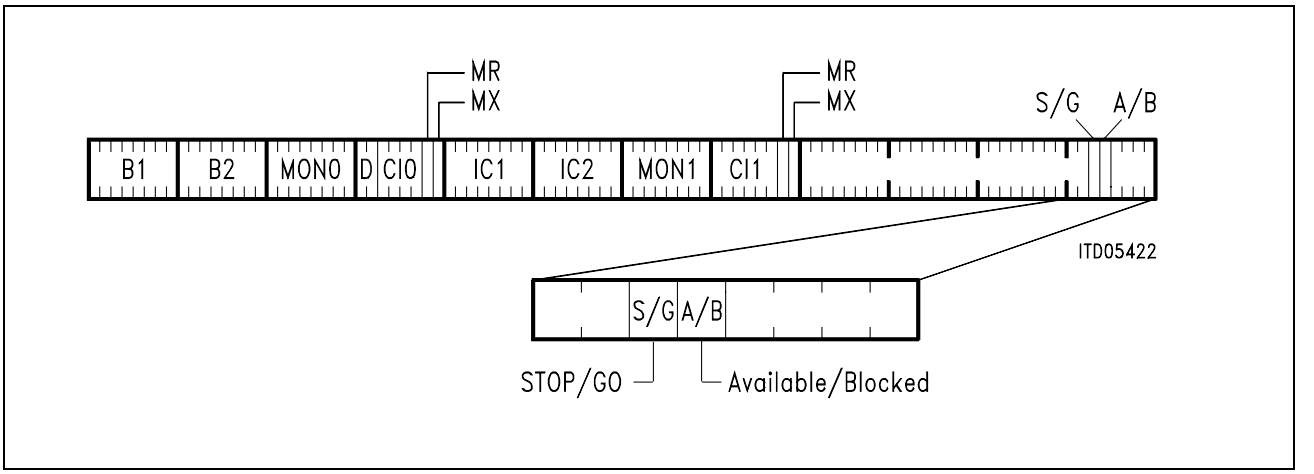


Figure 36 Structure of Last Octet within CH2 on DD

In the case of an access request the ISAR 34 checks the Bus Accessed bit (BAC) for the status "bus free", which is indicated by a logic "1". If the bus is free, the ISAR 34 transmits its individual TIC-bus address and the bus is occupied by the device which sends its address error free. If more than one device attempt to seize the bus simultaneously, the one with the lowest address value wins.

When the TIC bus is seized by the ISAR 34 the bus is identified to other devices as occupied via the BAC bit state "0" until the access request is withdrawn. After a successful bus access. the ISAR 34 is automatically set into a lower priority class, i.e. a new bus access cannot be performed until the status "bus free" is indicated in two successive frames.

If none of the devices connected to the IOM-2 interface request access to the D- and C/I-channels, the TIC-bus address 7 will be present. The device with this address will therefore have access, by default, to the D- and C/I-channels.

The BAC bit is reset to state ’1’ when access to the C/I-channel is no longer requested, to grant other devices access to the D- and C/I-channels.

The availability of the S/T interface D-channel is indicated in the Stop/Go bit (S/G):

S/G=1: stop

S/G=0: go

The stop/go bit is available to other layer-2 devices connected to the IOM-2 interface to determine if they can access the S/T bus D-channel.

The Available/Blocked bit (A/B) is not influenced by the ISAR 34.

2.5.8 MONITOR Channel

The MONITOR channel protocol is a handshake protocol used for information exchange between the ISAR 34 and other devices.

It is necessary for programming and controlling devices attached to the IOM-2 interface, such like layer-1 transceivers (e.g. IEC-Q TE PSB 21911) or peripheral voice/data modules that do not need a parallel microcontroller interface (e.g. ARCOFI -SP PSB 2163).

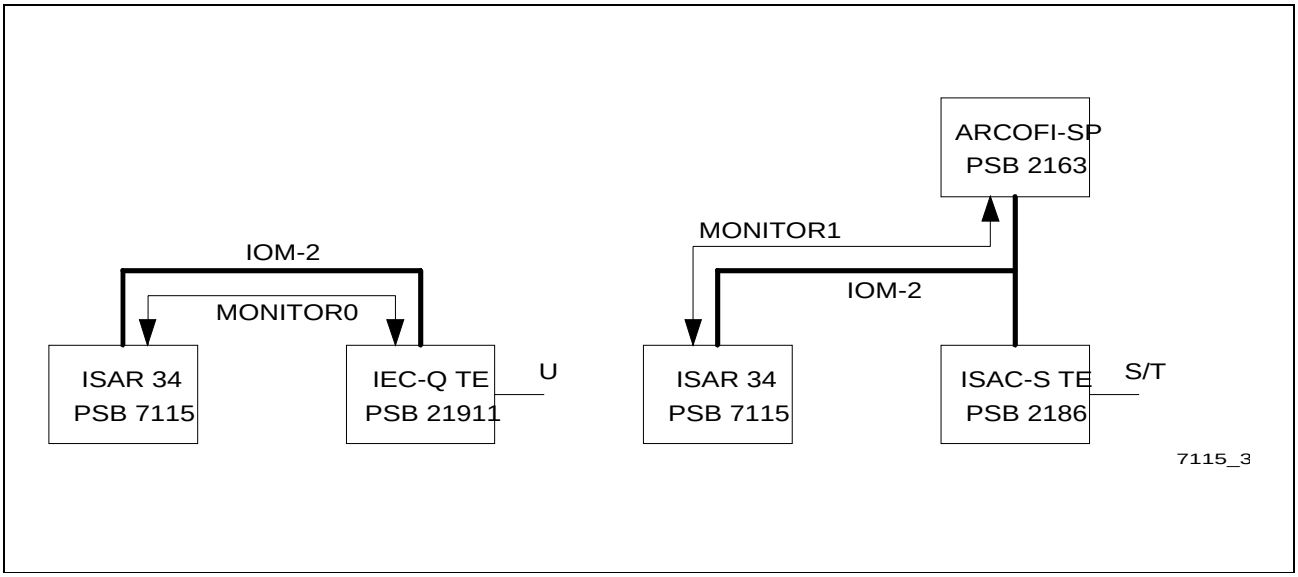


Figure 37 MONITOR Channel Applications

The MONITOR channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the MONITOR channel receive (MR) and MONITOR channel transmit (MX) bits. For example, data is placed onto the MONITOR channel and the MX bit is activated. This data will be transmitted repeatedly once per 8-kHz frame until the transfer is acknowledged via the MR bit.

MR and MX bits are controlled internally by the ISAR 34 according to the MONITOR channel protocol.

3 Operational Description

3.1 Host Communication

The communication between host and ISAR 34 is message oriented. That means all kind of information (B- and D-channel data, configuration data, status events, control commands, etc.) is exchanged by means of data packets that have a specific format depending on the kind of message.

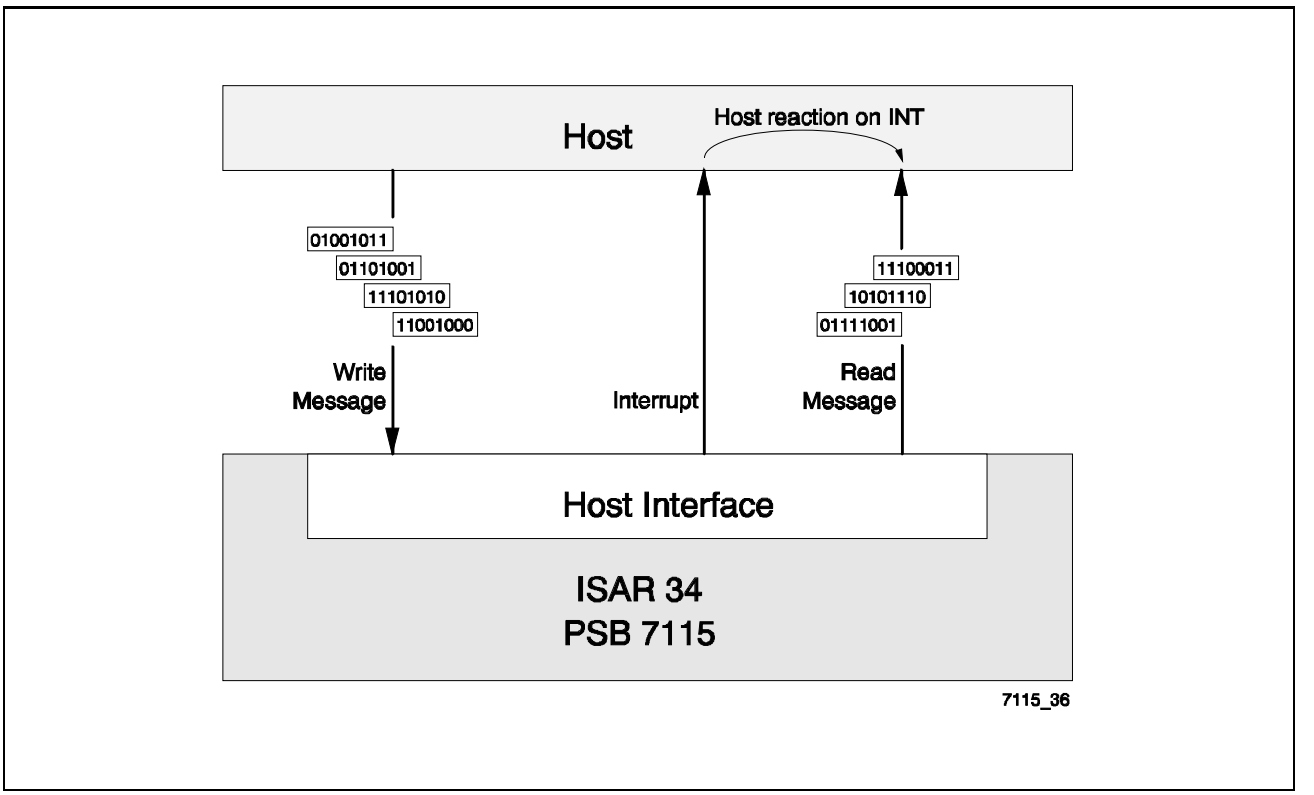


Figure 38 Host Communication

In order to transfer data to the ISAR 34 the host writes messages to the mailbox. In the opposite direction the ISAR 34 releases an interrupt to the host to indicate that a message can be read from the mailbox.

3.1.1 Message Structure

This chapter describes the format of the messages that are used to transfer information between host and ISAR 34. The coding of the individual messages is described in detail in **chapter 3.2** pp.

Depending on the kind of message, the structure and message length may be different.

All messages consist of:

- Interrupt status byte (HIS or IIS)
- Control register MSB (CTRL MSB)
- Control register LSB (CTRL LSB)

For **some messages** a certain number of additional bytes must be written to or read from the mailbox, respectively:

- 1st Parameter
- 2nd Parameter
- :
- N-th Parameter

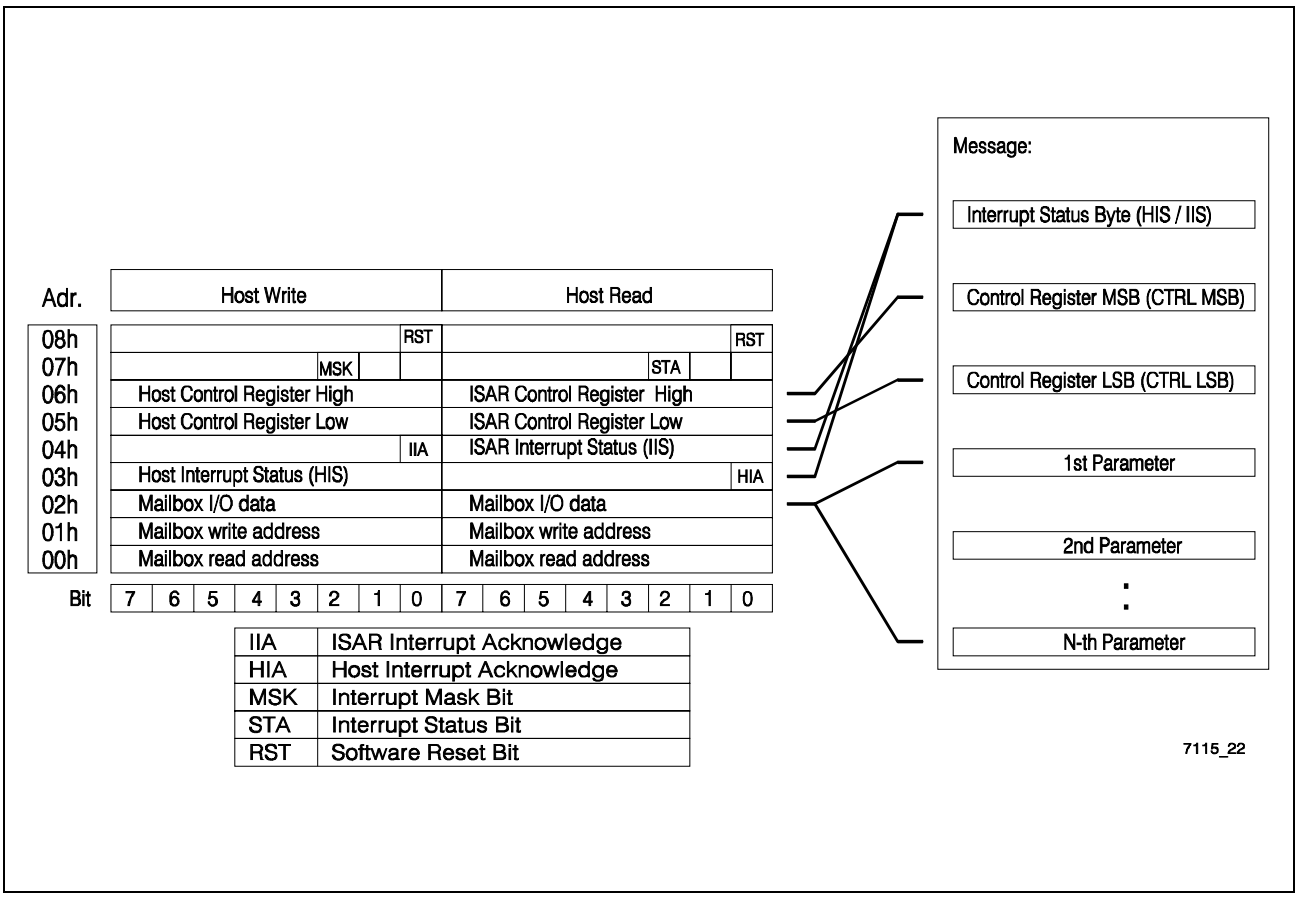


Figure 39 Message Transfer

3.1.2 Interrupt Status Byte

This chapter describes the format of the interrupt status byte which is part of every message transferred between host and ISAR 34. There are two types of interrupt status bytes depending on the direction of data flow:

HIS	**H**ost **I**nterrupt **S**tatus	Host → ISAR 34	Write to Reg. 03h
IIS	**I**SAR 34 **I**nterrupt **S**tatus	ISAR 34 → Host	Read from Reg. 04h

The interrupt status byte has a structure that defines the type of message, i.e. it contains information to which buffer the message is related to, the kind of message and to which functional block of the ISAR 34 the message is related to:

	7	6	5	4	3	2	1	0
HIS/IIS	DPS		MSC				MDS	

DPS … Datapath selection
One of the four data paths (0, 1, 2 or 3) of the ISAR 34 is selected.

MSC … Message coding
MSC defines the type of command (e.g. configuration request, configuration response, status event, control command, …) to perform a certain function.

MDS … Message destination/source
Selects one of the four functional blocks on the ISAR 34 (buffer, SART, data pump and IOM-2) to which the message is sent (host → ISAR 34) or from which a message is originated (ISAR 34 → host).

The coding for the HIS and IIS registers are listed below. It should be noted, that not all code combinations of buffer selection (DPS), message coding (MSC) and message destination/source (MDS) are available at the programming interface.

It is also important to note that the coding for test/diagnostics messages (DPS = 00) does not conform to the above shown structure of MSC and MDS. Instead these bits fully specify an individual message function.

Some of the test/diagnostics messages are only used for DSP download and are not valid after regular operation has started (see **chapter 3.12** DSP Program Download).

Host Interrupt Status Byte (HIS Host → ISAR 34)

The structure for the HIS byte is shown below. Not all combinations of buffer selection, message coding and message destination are available at the programming interface.

Table 5 HIS Structure - Path 1, 2 and 3

7	6	5	4	3	2	1	0	

Datapath Selection (DPS)

0	1							Path 1
1	0							Path 2
1	1							Path 3

Message Coding (MSC)

		1	0	0	0	0	0	Transmit data with SART control command
		0	0	0	1			Request for configuration
		0	0	1	1			Request for status
		1	0	0	1			Configuration setup
		1	0	1	0			Control command

Message Destination/Source (MDS)

						0	0	Command for Buffer
						0	1	Command for SART
						1	0	Command for Pump
						1	1	Command for IOM-2

The HIS structure is different for data path 0 which is used for the MONITOR channel, general control and test/diangostics functions.

Table 6 HIS Structure - Path 0

7	6	5	4	3	2	1	0	
Datapath Selection (DPS)								
0	0							Path 0
Message Coding (MSC)								
		0	0	1	0	0	0	IOM-2 request for configuration
		1	1	1	1	0	0	Buffer Configuration setup
		1	1	1	1	1	0	Buffer control command
		0	1	1	1	0	1	Buffer status request
		1	0	0	1	0	1	Timer interrupt on/off
		0	0	0	1	0	0	Request selftest result
		0	0	0	1	0	1	Request for software version number
		1	1	0	0	0	1	MONITOR channel configuration setup
		0	1	0	0	0	1	MONITOR channel configuration request
		1	1	0	0	0	0	MONITOR channel transmit data
		1	0	1	0	0	0	Soft reset
		0	0	1	0	1	0	GPIO data request
		1	0	1	0	1	0	GPIO configuration command

ISAR 34 Interrupt Status Byte (IIS)

The structure for the IIS byte is shown below. Also for IIS not all combinations of buffer selection, message coding and message destination are available at the programming interface.

One message does not conform to the described structure of DPS, MSC and MDS. It has a general code (IIS = 0), which is used for normal operation and not for test/ diagnostics functions.

Table 7 IIS Structure - Path 1, 2 and 3

7	6	5	4	3	2	1	0	

Datapath Selection (DPS)

0	1							Path 1
1	0							Path 2
1	1							Path 3

Message Coding (MSC)

		1	0	0	0	0	0	Receive data with SART status event
		1	0	0	1			Mailbox contains configuration data
		1	0	1	0			Mailbox contains status event
		1	0	1	1			Mailbox contains status information

Message Destination/Source (MDS)

						0	0	Indication from Buffer
						0	1	Indication from SART
						1	0	Indication from Pump
						1	1	Indication from IOM-2

Note: All messages which are not listed here or described in the detailed message description (starting with chapter 3.2) must be ingored by the host if released from the ISAR 34.

The IIS structure is different for data path 0 which is used for the MONITOR channel, general control and test/diangostics functions.

Table 8 IIS Structure - Path 0

7	6	5	4	3	2	1	0	

Datapath Selection (DPS)

0	0							Path 0

Message Coding (MSC)

		1	0	1	0	0	0	General IOM-2 configuration response
		1	1	1	1	0	1	Buffer status response
		1	1	1	1	1	0	Buffer status event (path 0)
		0	0	0	0	0	0	Buffer status event - buffer available (path 0, 1, 2 and 3)
		1	1	1	1	1	1	Invalid message received
		1	0	0	1	0	0	Selftest response
		1	0	0	1	0	1	Software version number response
		1	1	0	0	0	1	MONITOR channel configuration response
		1	1	0	0	0	0	MONITOR channel receive data
		1	1	0	0	1	0	MONITOR channel status event
		1	0	1	0	1	0	GPIO status event/response
0	1	1	0	1	0	1	0	Timer interrupt event

Note: The timer interrupt is not coded as a path 0 message but for data path 1. However, the use of the timer interrupt does not require path 1 operation, it may be used for any purpose.

3.1.3 Control Registers and Parameters

This chapter describes the structure of the remaining elements of a message, which are control registers, parameters and data.

The most significant byte of the control register (CTRL MSB) contains configuration, status or control information which depends on the type of message.

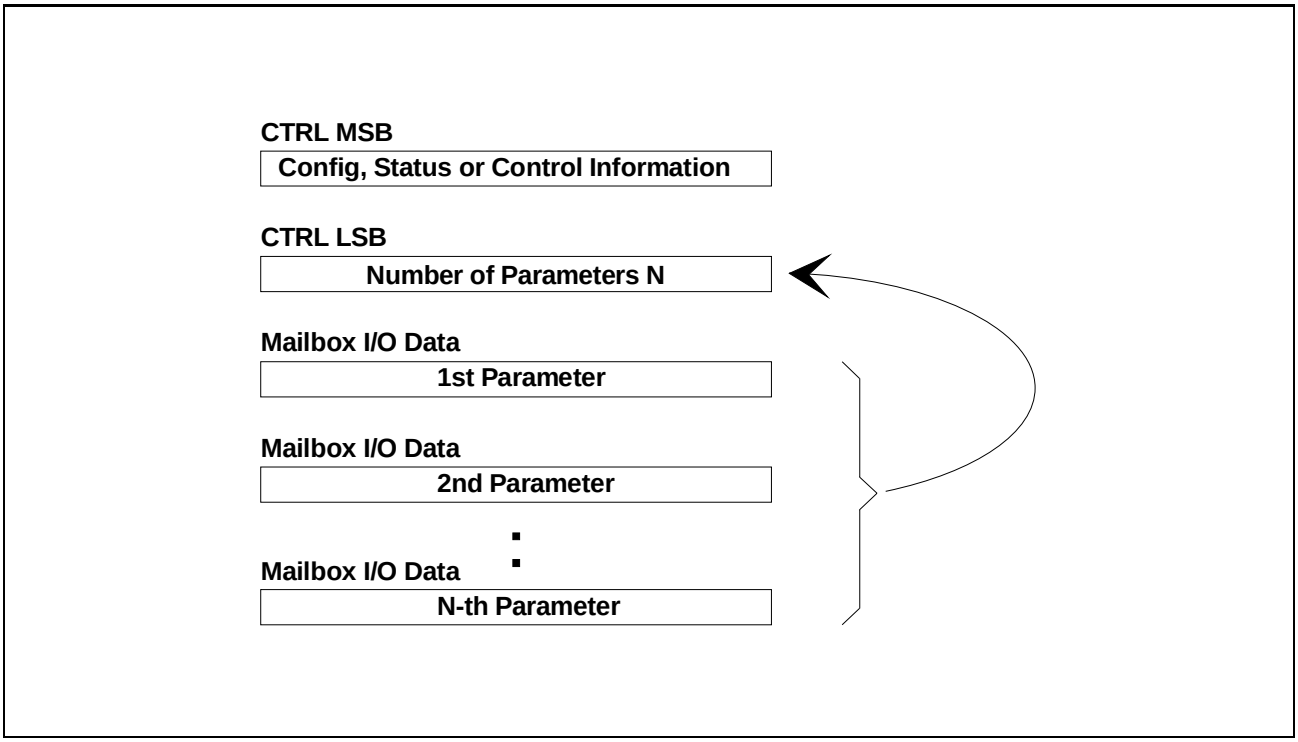


Figure 40 Control Registers and Parameters

The least significant byte of the control register (CTRL LSB) is used to indicate the total number of bytes transferred via the mailbox (Mailbox I/O Data).

These mailbox data may contain additional configuration, status or control information as well as user data in receive/transmit direction **(figure 40)**.

For some of the messages no additional data is written to/read from the mailbox, in this case the CTRL LSB is set to 0.
The structure of the parameters depends on the type of message being transferred and has no fixed format. Therefore it is described with each individual message.

3.1.4 Configuration After Reset

The proceeding after hardware reset is shown in **figure 41**.

This version of the ISAR 34 requires a download of the DSP program into external memory, future versions will be able to store the DSP program in flash memory and may even provide completely new features. The corresponding DSP program is delivered in a binary file together with the device. When this binary file is downloaded, an automatic test of the chip version number is performed within the download procedure, so the host does not need to evaluate it.

After the DSP program download procedures are finished the host checks the global variable STATUS if the download was successful.

The ISAR 34 will also perform an automatic selftest of the chip at the end of the download procedure. The host requests the result of this selftest to ensure that no basic hardware error is given.

The software version number can be read to get information on what features are provided with this version of the DSP program.

The ISAR 34 is now ready for configuration of the functional blocks which should be done in the given sequence (buffer, pump, IOM-2 and SART) and data transfer can be started.

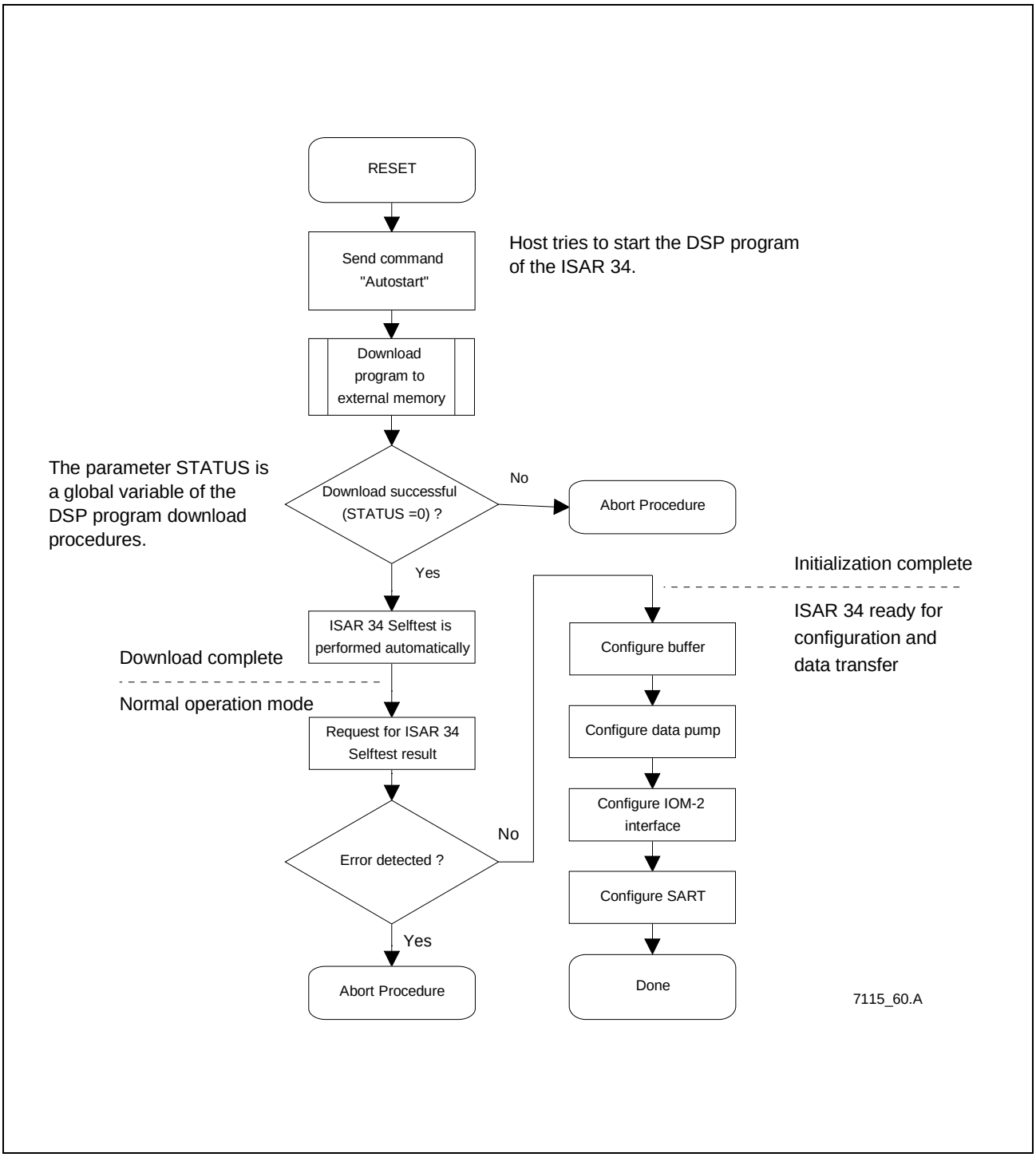


Figure 41 Initialisation Procedure

To establish a link on a data path, the four functional blocks, buffer, data pump, IOM-2 interface and SART must be configured first. Since the configuration of the data pump will reset the whole data path except buffer configuration, the pump should be configured right after buffer configuration.

It is recommended to follow this configuration sequence to provide for proper operation.

The table below shows the configuration parameters for each of the four blocks and the reference to the corresponding parameter setting.

Detailed information about the individual parameters is provided with the corresponding configuration setup messages.

Table 9 Configuration Parameters

Functional Block	Configuration Parameter	Parameter Setting
Buffer	• Buffer base priority	BBP
	• Maximum message length	MML
Data pump	• Pump mode (fax, datamodem, halfduplex modulation, V.110, DTMF, DTMF transmission or bypass)	PMOD
	• Originating/answering mode	OAM
	• Transmitter output attenuation	TOA
	• Calling and answer tones	ATN, CTN
	• Echo protector tone	EPT
	• Guard tone selection	GTS
	• Modulation scheme	V34R, V32R, …
	• Automode operation	AMOD
	• V.8 negotiation	V8
	• Data rate (V.110)	VDR
	• Flow control (V.110)	FCT
	• Rejection level (DTMF)	REL
IOM-2 interface	• IOM-2 access enable/disable	IOM
	• Time slot position	RTSO, RCS TTSO, TCS
	• Time slot length	TSL
	• Switching of DU/DD lines	TXD, RXD
	• Coding (PCM A-law, µ-law)	COD
	• Rate conversion	RCV

Table 9 Configuration Parameters

Functional Block	Configuration Parameter	Parameter Setting
SART	• SART mode (V.14, HDLC, binary, FSK V.14)	SMODE
	• Receive/transmit channel disable (halfduplex modulation)	HDMC
	• HDLC formatting (HDLC regular/inverted, Interframe fill, FCS length, enable/disable FCS, data underrun operation)	HIO IFF FLEN EDF, DUO
	• V.14/FSK V.14 formatting (overspeed range, stop bits, parity bits, character size, buffer flush timeout)	OVSP, SNP, EOP, EDP NSB, CHS, BFT
	• Binary formatting (data underrun operation, bit swapping, data underrun fillword)	DUO, BSW, DUFW

3.1.5 Message Transfer from Host to ISAR 34

The procedure to write a message to the ISAR 34 mailbox is shown in **figure 42**.

The mechanism to access the ISAR 34 mailbox is the same for all messages, which are:

- Configuration setup
- Configuration request
- Status request
- Control commands
- Control commands along with transmit data

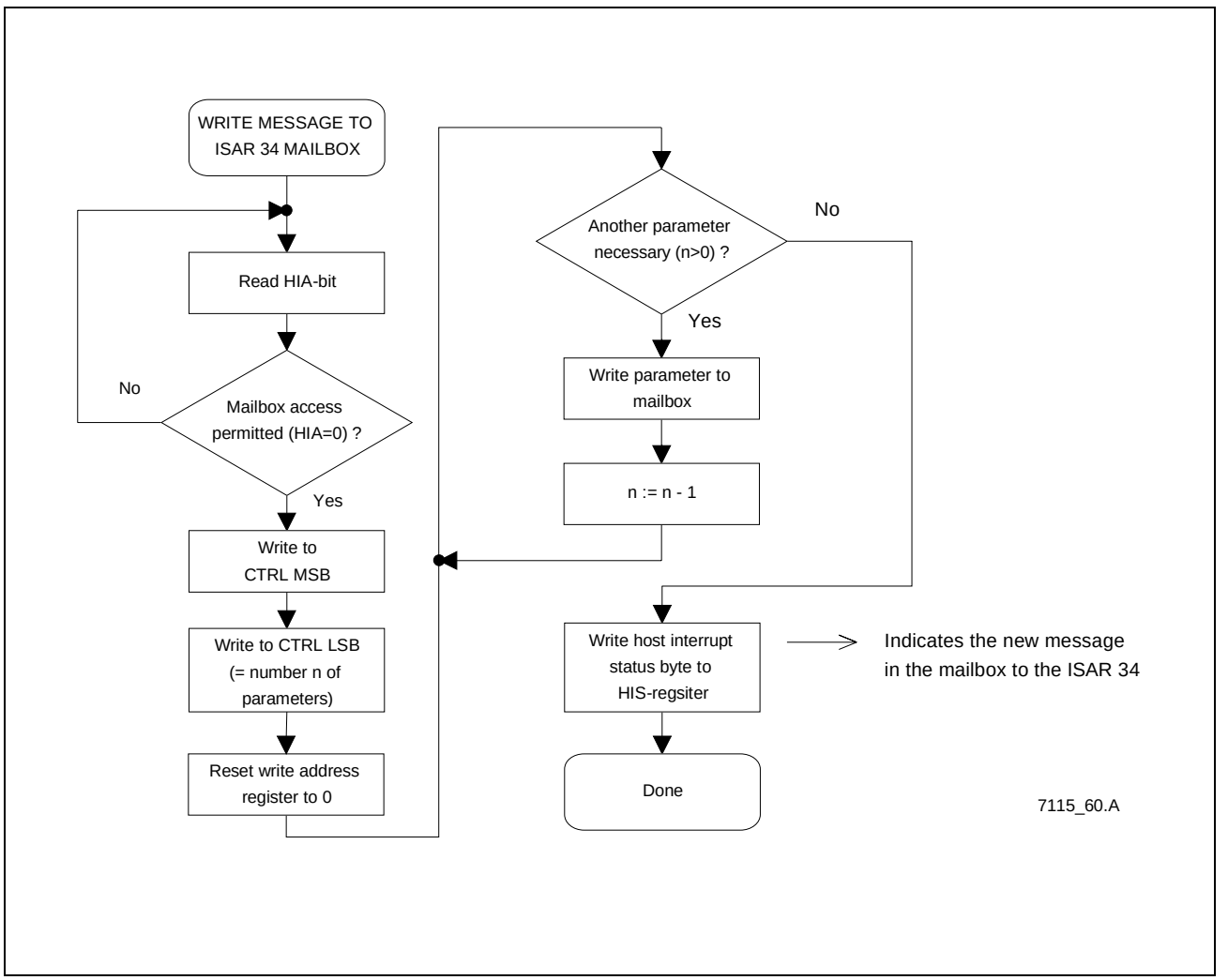


Figure 42 Write Message Transfer

When a message is written to the mailbox, the ISAR 34 will transfer the whole message to the destination buffer which is indicated in the host interrupt status byte (HIS). During that time another message must not be entered by the host, however due to the mailbox structure, the message transfer is performed rather fast and will not delay any host access.

Therefore, before any access to the mailbox is done, the host should read the host interrupt acknowledge bit (HIA), to verify that the registers are available again (HIA = 0) and a new message may be written to the mailbox.

The control registers (CTRL MSB and LSB) should be written first, where the CTRL LSB contains the total number of bytes which will be entered to the mailbox.

Before any data is written to the mailbox (address 02h), the write pointer (address 01h) must be reset to 0. After a byte is written to the mailbox, the write address pointer is autoincremented and doesn't need to be reprogrammed. This allows for fast access to the mailbox.

If there are successive messages with the same mailbox contents, the mailbox data does not need to be written again, as this data is still available in the mailbox memory from the previous message. It allows the host to flexibly reprogram the write pointer and its respective memory location only for those mailbox contents which are different from the previous message.

Important note:

It is important to note that the HIS byte must be entered as the very last byte of the message as this will indicate the new register and mailbox contents to the ISAR 34.

An access to the HIS register will terminate the message transfer and automatically set the HIA bit which is reset again by the ISAR 34 as soon as new data can be entered to the mailbox.

3.1.6 Message Transfer from ISAR 34 to Host

The procedure to read a message from the ISAR 34 mailbox is shown in **figure 43**.

The mechanism to access the ISAR 34 mailbox is the same for all messages, which are:

- Configuration response (initiated by configuration request message)
- Status response (initiated by status request message)
- Status events
- Status events along with receive data

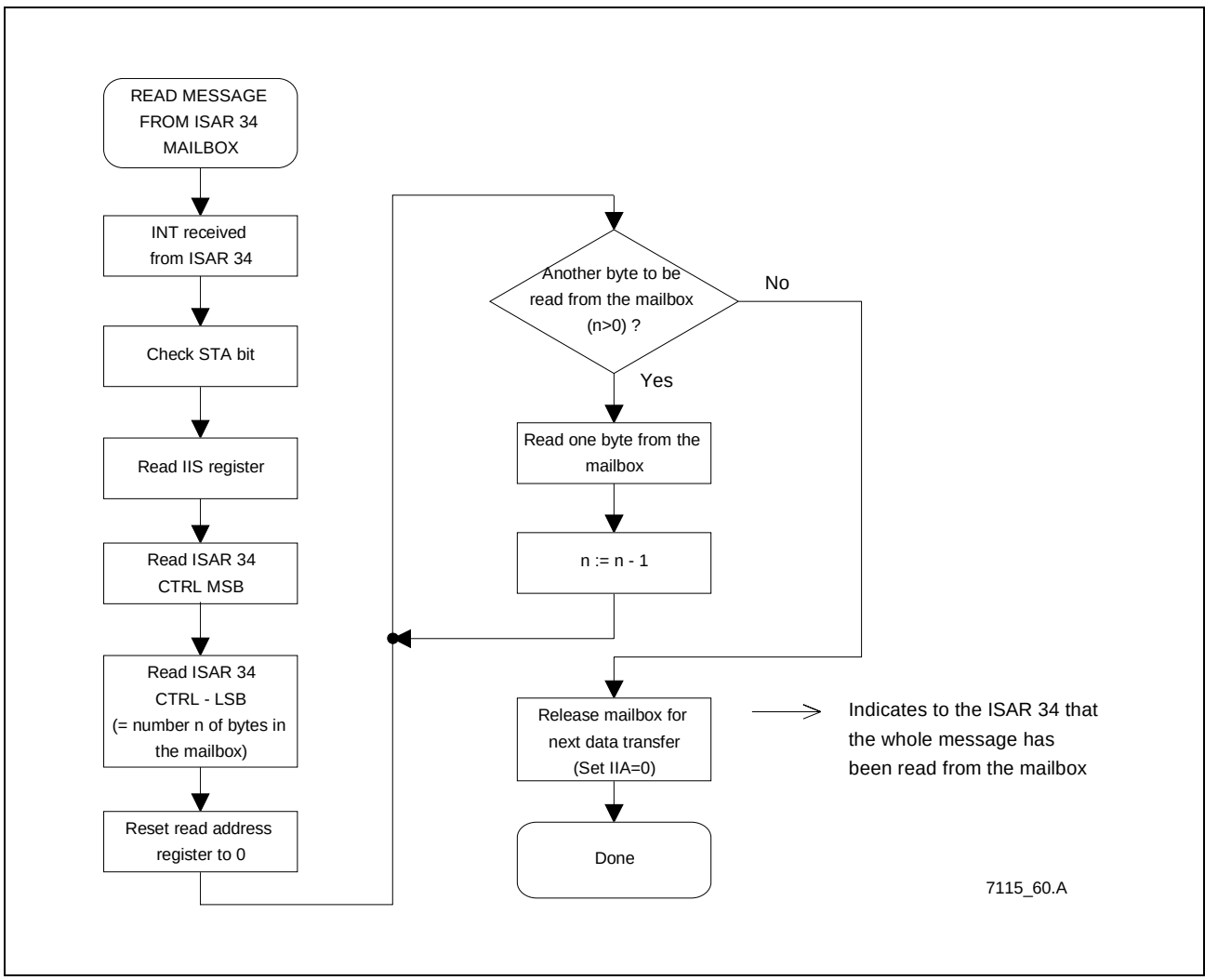


Figure 43 Read Message Transfer

If the ISAR 34 has a message available in the mailbox to be read by the host, it will activate the INT-line, provided the interrupt is not masked (MSK bit). To ensure the interrupt line is activated by the ISAR 34 and not from a different interrupt source in the system (e.g. from the transceiver device), the interrupt status bit STA should be checked.

For the message transfer the ISAR 34 interrupt status register (IIS) should be read first. It defines the type of message and indicates the source where the message was initiated.

Then the CTRL MSB and LSB are read by the host, where the LSB indicates the total number of bytes which are available in the mailbox .

Before data is read from the mailbox (address 02h), the read pointer (address 00h) must be reset to 0 to read the data starting with the first byte in sequence. For each read access to the mailbox the read address pointer is autoincremented and does not need to be reprogrammed by the host. This allows for fast access to the mailbox.

Important note:

It is important to note that the IIA bit must be reset as the very last register access of the message, as this will indicate to the ISAR 34 that the message has been completely read. The mailbox is released and may be filled with new contents.

It is not necessary to read the mailbox if its content is not required by the host, e.g. if data is not valid. The host can discard the contents by just writing the IIA bit as this will release the whole mailbox.

A response message is always initiated by the host releasing a request message to the ISAR 34 (see **figure 44**). The other messages are initiated by the state machine residing on the host side (messages from host to ISAR 34) or residing on the ISAR 34 (messages from ISAR 34 to host).

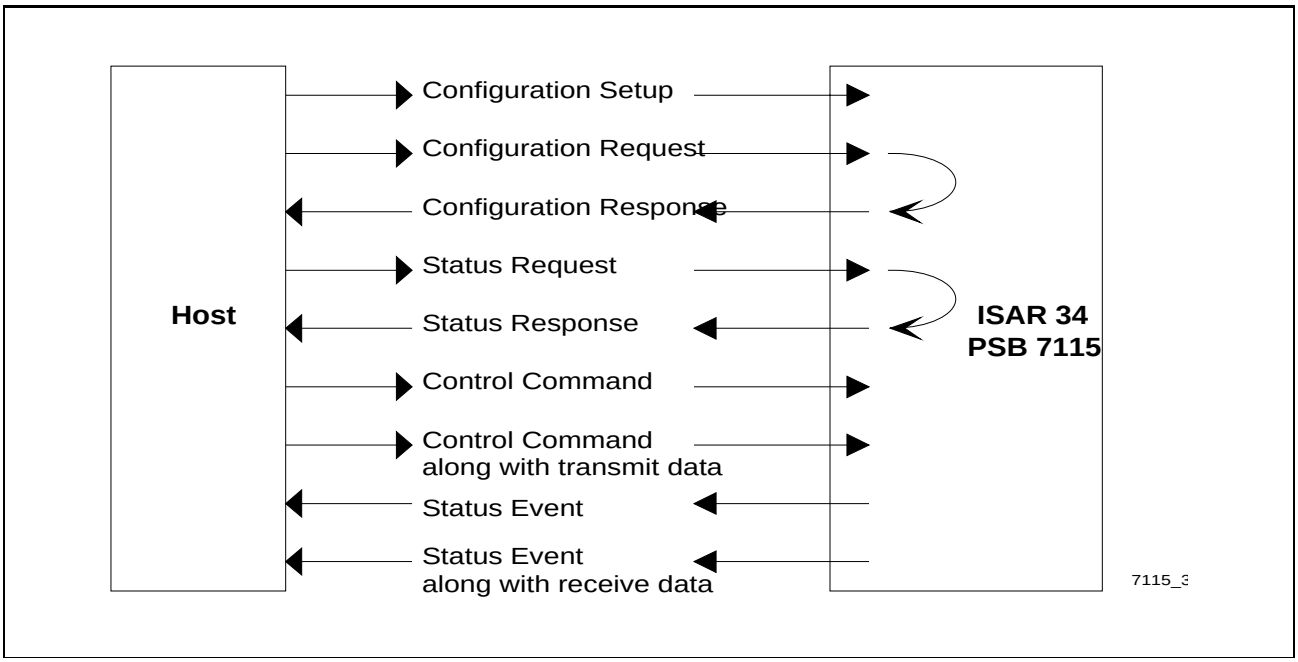


Figure 44 Message Directions

The ISAR 34 releases an interrupt request to the host to indicate that a message must be read from the mailbox. The host can mask the interrupt source (bit MSK = 0) to avoid any interrupt state being indicated to the host by activating the INT-line. However, the mask bit affects only the generation of the interrupt, but not the interrupt status from being set (STA bit) which can be polled by the host.

3.1.7 Message Overview

The data path for the B-channel consists of FIFO buffer, SART, data pump and IOM-2 interface. Transmit/receive data and configuration, status and control information is exchanged between the host and the ISAR 34 by a set of messages.

Buffer Configuration

- Configuration Setup — Host ⇒ ISAR 34

The host sets the priority at which each buffer's request will be serviced by the host and the message length at which data will be transferred between the host and the mailbox.

- Configuration Request — Host ⇒ ISAR 34

The host can request the current configuration, i.e. parameter settings such as base priority and message length.

- Configuration Response — Host ⇐ ISAR 34

After a configuration request by the host, the ISAR 34 will respond with the current parameter settings.

- Control Command — Host ⇒ ISAR 34

The host sends control commands to the ISAR 34 in order to clear or reset buffers.

Buffer Status

- Status Request — Host ⇒ ISAR 34

The host can request the current status of the buffers, i.e. number of messages and free locations in the buffers. Two different types of status responses can be requested.

- Status Response — Host ⇐ ISAR 34

After a status request by the host, the ISAR 34 will respond with the current status information.

- Status Events — Host ⇐ ISAR 34

During data transfer the ISAR 34 indicates to the host, whether the buffer is able to store another message, i.e. if new data can be entered.

SART Configuration

- Configuration Setup Host ⇒ ISAR 34

The host configures the mode (Binary, HDLC, ASYNC) for the SART and sets further parameters depending on the mode.

SART Data

- Status Events with Receive Data Host ⇐ ISAR 34

During data reception the ISAR 34 indicates to the host, when error conditions or mode specific events occur, e.g. when the end of an HDLC frame was detected.

- Control Commands with Transmit Data Host ⇒ ISAR 34

During data transmission the host controls mode specific functions e.g. the HDLC framing (frame start, frame end) and the generation of break signals in ASYNC mode.

Pump Configuration

- Configuration Setup Host ⇒ ISAR 34

The host configures the mode (fax modulations, datamodem modulations, halfduplex modulations, V.110, DTMF, DTMF transmission or by pass) for the data pump and sets further parameters depending on the mode.

- Control Commands Host ⇒ ISAR 34

The host sends control commands to the ISAR 34 in order to enable/disable the pump and to set mode specific control commands (e.g. DTMF tones to be generated).

Pump Status

- Status Request Host ⇒ ISAR 34

The host can request the current configuration of the data pump (pump mode, originating/answering mode).

- Status Response Host ⇐ ISAR 34

After a configuration request by the host, the ISAR 34 will respond with the current parameter settings.

- Status Events Host ⇐ ISAR 34

The ISAR 34 indicates to the host mode specific events that occur during data transfer, such as DTMF tones received or control bit change in V.110.

IOM-2 Configuration

- Configuration Setup Host ⇒ ISAR 34

The host configures the length and position of the IOM-2 timeslots.

- Configuration Request Host ⇒ ISAR 34

The host can request the current IOM-2 configuration, i.e. the current settings of timeslot-length and position.

- Configuration Response Host ⇐ ISAR 34

After a configuration request by the host, the ISAR 34 will respond with the current configuration setting.

- Control Commands Host ⇒ ISAR 34

The host sends control commands to the ISAR 34 for IOM-2 control during normal operation.

GPIO Configuration

- Configuration Setup Host ⇒ ISAR 34

The host configures status, direction, interrupts etc. of the GPIO pins.

GPIO Status

- Status Request Host ⇒ ISAR 34

The host requests the current status of the GPIO pins.

- Status Event/Response Host ⇐ ISAR 34

After a state change on a GPIO with unmasked interrupt, this status event reports the current GPIO status to the host. The same message is used as a status response after a status request from the host.

Important Note:

In future versions of the ISAR 34 the message length for response messages can be different from this Version 2.1, i.e. new parameters may additionally be provided which is indicated by an increased parameter NOM (= number of valid bytes in the mailbox).

If the ISAR 34 in this version provides more parameters than specified herein, the host should ignore all mailbox data that exceeds the message length determined by NOM as specified.

3.2 Buffer Configuration

3.2.1 Buffer Configuration Setup (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS							0	0

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	0	BBP		

	7	6	5	4	3	2	1	0
CTRL LSB	1							

	7	6	5	4	3	2	1	0
1. Parameter	MML							

DPS … Datapath selection
- 00: path 0
- 01: path 1
- 10: path 2
- 11: path 3

MSC … Message coding
The message coding is different for datapath 0 and datapath 1, 2, 3.
- 1111: configuration setup for data path 0 (DPS = 00)
- 1001: configuration setup for data path 1, 2 or 3 (DPS = 01, 10, 11)

BBP … Buffer Base Priority
- 000: priority is not changed by the configuration command
- 001: change base priority to 1 (lowest priority)
- : :
- 111: change base priority to 7 (highest priority)

Reset value: BBP = 4 datapaths 1, 2 and 3 (DPS = 01, 10, 11)
BBP = 5 datapath 0 (DPS = 00)

MML … Maximum Message Length
The maximum message length defines the block size of data that is transferred via the mailbox. A data block that is read from or written to the mailbox has a block size less or equal the maximum message length MML.

The maximum value for MML is limited by the FIFO size (MPL = maximum possible message length) for the respective datapath. MPL can be read by a buffer configuration request message (see next chapter).
The FIFO size depends on the memory configuration of the ISAR 34.

- With external SRAM 128kx16, 15ns:

	MPL	MML (reset value)
path 0	61	32
path 1	253	32
path 2	253	32
path 3	253	32

The buffer priority determines the sequence of service if more than one read buffer request for mailbox service at the same time. In such a case the buffer with highest priority is served first and the priority of all pending buffers is increased by one. After being served, the priority of the serviced buffer is reset to its base value, which is selected by the above given configuration command.

So a buffer with a higher base priority will be served more often than a buffer with a lower base priority, moreover, the higher the difference of two priority values the more often the one buffer will be serviced first.

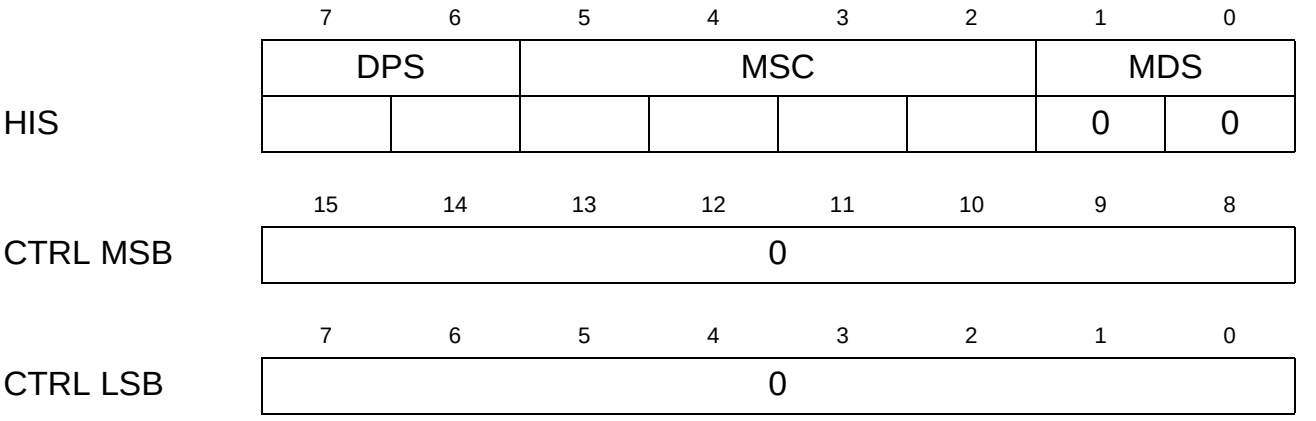
If the additional value (maximum message length) is omitted (CTRL LSB = 0), only the base priority is changed. In this way the buffer base priority can be reconfigured to a different value during normal operation without any loss of data consistency.

By changing the base priority, the current priority is reset to the new base value.

For highest throughput and best internal performance it is recommended to use the highest value for MML.

3.2.2 Buffer Configuration Request (Host → ISAR 34)

The current buffer configuration can be requested by the host. The request is fully specified by the Host Interrupt Status register (HIS), i.e. the mailbox control registers are set to 0 and no parameters are required.

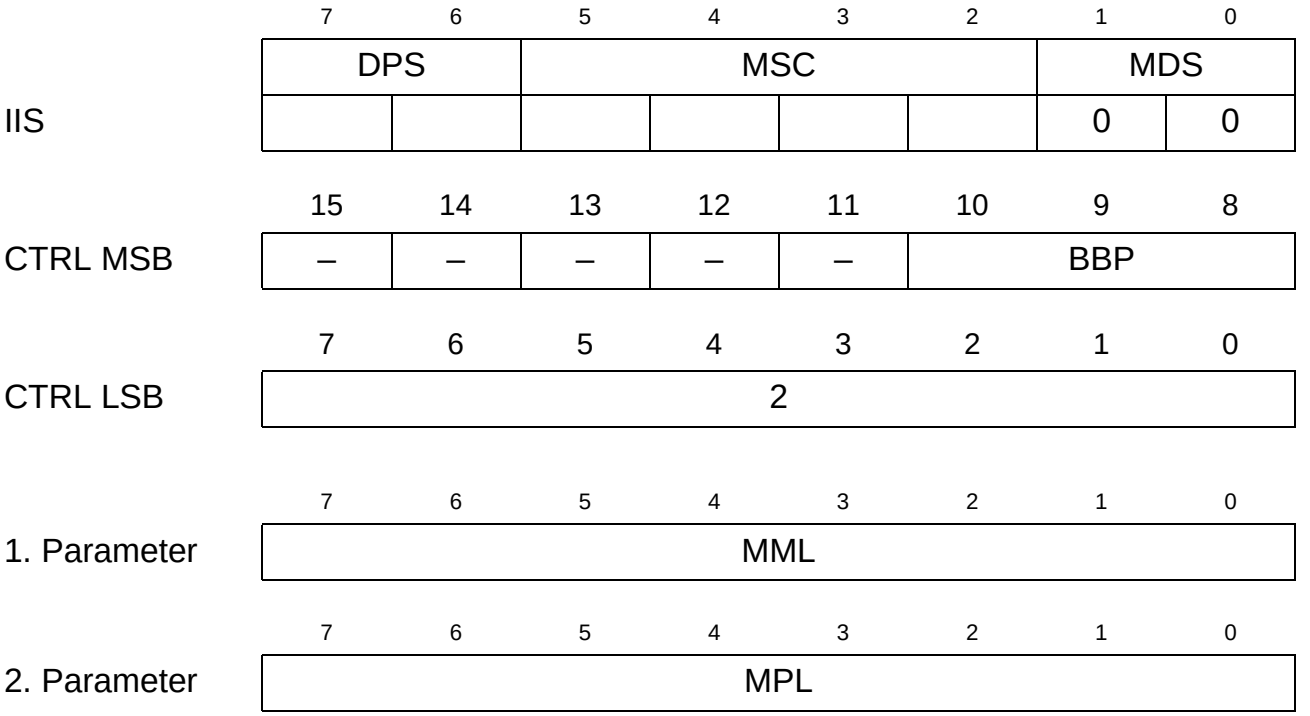


DPS … Datapath selection
- 00: path 0
- 01: path 1
- 10: path 2
- 11: path 3

MSC … Message coding
The message coding is different for datapath 0 and datapath 1, 2, 3.
- 0111: configuration request for datapath 0 (DPS = 00)
- 0001: configuration request for datapath 1, 2 or 3 (DPS = 01, 10, 11)

3.2.3 Buffer Configuration Response (ISAR 34 → Host)

The ISAR 34 provides the configuration data, which was requested by the host, via the mailbox. The coding is similar to the configuration setup.



DSP … Datapath selection
- 00: path 0
- 01: path 1
- 10: path 2
- 11: path 3

MSC … Message coding
The message coding is different for datapath 0 and datapath 1, 2, 3.
- 1111: configuration response from datapath 0 (DPS = 00)
- 1001: configuration response from datapath 1, 2 or 3 (DPS = 01, 10 or 11)

BBP … Current Buffer Base Priority
- 000: not used
- 001: base priority of 1 (lowest priority)
- : :
- 111: base priority of 7 (highest priority)

MML … Currently Selected Maximum Message Length
MML contains the maximum message length that has been configured by the host. If this value has not been programmed by the host, MML contains the reset value for the maximum possible message length (see below).

MPL … Maximum Possible Message Length
MPL contains the maximum possible message length that can be configured.
The value for MPL depends on the memory configuration of the ISAR 34.

- With external SRAM 128kx16, 15ns:

	MPL	MML (reset value)
path 0	61	32
path 1	253	32
path 2	253	32
path 3	253	32

In receive direction the ISAR 34 gathers all received data words from the SART up to the selected message length, before the message is passed to the mailbox. Messages of reduced length may be passed on certain events such like error conditions or HDLC frame end (see **chapter 3.5.1** SART Status Events with Receive Data).

In transmit direction it's the responsibility of the host that transmit messages do not exceed the selected message length, to avoid a buffer overflow and loss of data.

It must be ensured that MML does not exceed MPL in the configuration setup message (see **chapter 3.2.1**). Therefore it is recommended to issue a buffer configuration request message to verify the currently selected (MML) and the maximum possible message length (MPL). Moreover, this enables the software to automatically adapt to the hardware platform, as the ISAR 34 may provide different FIFO buffer sizes depending on the memory configuration in future versions.

3.2.4 Buffer Control Command (Host → ISAR 34)

The I/O-buffer control commands are interpreted immediately after being received by the ISAR 34.

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS								

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	0	0	CRB	

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DPS … Datapath selection
- 00: path 0
- 01: path 1
- 10: path 2
- 11: path 3

MSC … Message coding
The message coding is different for datapath 0 and datapath 1, 2, 3.
- 1111: control command for datapath 0 (DPS = 00)
- 1010: control command for datapath 1, 2 or 3 (DPS = 01, 10 or 11)

MDS … Message destination/source
The destination coding is different for datapath 0 and datapath 1, 2, 3.
- 10: message is addressed to buffer (for DPS = 00)
- 00: message is addressed to buffer (for DPS = 01, 10 or 11)

CRB … Clear / Reset Buffers
- 00: clear receive buffer
- 01: clear transmit buffer
- 10: reset read and write buffers to their initial values

The buffer clear commands do not change the settings of the base priority or the message length.

The reset command clears both, read and write buffers, and reset them to their initial factory settings.

3.3 Buffer Status

3.3.1 Buffer Status Request (Host → ISAR 34)

The request is fully specified by the Host Interrupt Status register (HIS) and the mailbox control registers, i.e. additional parameters are not used. The I/O-buffer status request is serviced immediately after being received by the ISAR 34.

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS								

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	0	0	0	STS

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DPS … Datapath selection
- 00: path 0
- 01: path 1
- 10: path 2
- 11: path 3

MSC … Message coding
The message coding is different for datapath 0 and datapath 1, 2, 3.
- 0111: status request for datapath 0 (DPS = 00)
- 0011: status request for datapath 1, 2 or 3 (DPS = 01, 10 or 11)

MDS … Message destination/source
The destination coding is different for datapath 0 and datapath 1, 2, 3.
- 01: message is addressed to buffer (for DPS = 00)
- 00: message is addressed to buffer (for DPS = 01, 10 or 11)

STS … Status Type Select
The status request will cause the generation of …
- 0: … a status response with additional information about the buffers
- 1: … a buffer available indication

The status response with additional information about messages and free locations in the receive and transmit buffers is described in **chapter 3.3.2**.

The second option allows the host to force the generation of a buffer available indication as specified in **chapter 3.3.3**. However there is a slight difference in the functionality of the resulting indication message:

A buffer available indication that is initiated by the ISAR 34, only contains information about those buffers where a transition from “not enough free space” to “enough free space for another message” occurs. All buffers that are not serviced by that time, will not be indicated in a following buffer available indication that results from the status transition of a different buffer.

However, a status request with STS = 1 forces the ISAR 34 to generate a buffer available indication for the transmit buffer of the selected datapath (specified in the HIS register), even if there is no state transition for that buffer.

This command is useful to force a first data request message from the ISAR 34 after a datapath is fully configured, although the first request message is automatically generated after SART configuration.

3.3.2 Buffer Status Response (ISAR 34 → Host)

The ISAR 34 returns status information about the buffers if requested by the host (see **chapter 3.3.1**).

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS								

	15	14	13	12	11	10	9	8
CTRL MSB	–	–	–	–	RDM3	RDM2	RDM1	RDM0

	7	6	5	4	3	2	1	0
CTRL LSB	6							

	7	6	5	4	3	2	1	0
1. Parameter	NBRL							

	7	6	5	4	3	2	1	0
2. Parameter	NBRM							

	7	6	5	4	3	2	1	0
3. Parameter	NMR							

	7	6	5	4	3	2	1	0
4. Parameter	NBTL							

	7	6	5	4	3	2	1	0
5. Parameter	NBTM							

	7	6	5	4	3	2	1	0
6. Parameter	NMT							

DPS … Datapath selection
- 00: path 0
- 01: path 1
- 10: path 2
- 11: path 3

MSC … Message coding
The message coding is different for datapath 0 and datapath 1, 2, 3.
1111: status response from datapath 0 (DPS = 00)
1011: status response from datapath 1, 2 or 3 (DPS = 01, 10 or 11)

MDS … Message destination/source
The source coding is different for datapath 0 and datapath 1, 2, 3.
01: message is originated from the buffer (for DPS = 00)
00: message is originated from the buffer (for DPS = 01, 10 or 11)

RDM3 - 0 ... Request for next Data Message from Channel 3, 2, 1 or 0
If RDM0, RDM1, RDM2 or RDM3 is set, the corresponding channel 0, 1, 2 or 3 requests for a new data message from the host, i.e. there is enough free buffer space for another message.

NBRL … Number of free bytes in the receive buffer - LSB

NBRM … Number of free bytes in the receive buffer - MSB

NMR … Number of messages in the receive buffer

NBTL … Number of free bytes in the transmit buffer - LSB

NBTM … Number of free bytes in the transmit buffer - MSB

NMT … Number of messages in the transmit buffer

The control register contains additional information about all buffers that currently have buffer space available for a new message. The information is similar as provided in the general status event message which is a kind of “Indication for Buffer available” (see **chapter 3.3.3.2**). However, here the current status of all buffers is indicated regardless whether there is a state transition in the individual buffer.

Detailed information about free locations in receive and transmit buffers and about the number of messages currently stored in the buffers are available from the mailbox. These parameters only refer to the buffer which is associated to the selected data path in IIS register.

Comment

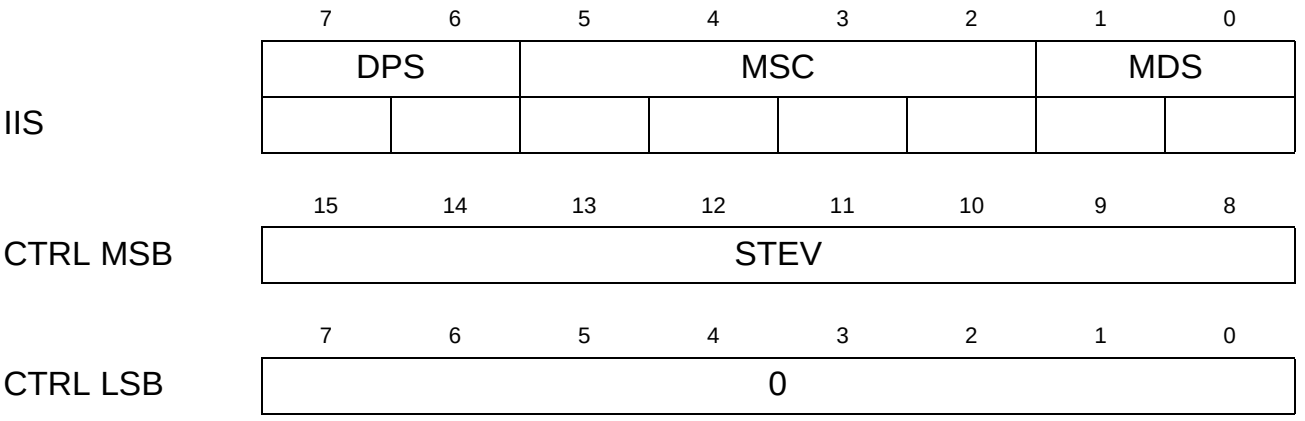
As the HIS register and the control word are internally also written to the buffers a message of length n will always require (n+3) buffer locations.

3.3.3 Buffer Status Event (ISAR 34 → Host)

There are two message types for status events from the buffer:

- Status event that is related to a certain buffer (see **chapter 3.3.3.1**)
- Indication for buffer available - general code for all buffers (see **chapter 3.3.3.2**)

3.3.3.1 Buffer Specific Status Event (ISAR 34 → Host)



DPS … Datapath selection
00: path 0
01: path 1
10: path 2
11: path 3

MSC … Message coding
The message coding is different for datapath 0 and datapath 1, 2, 3.
1111: status event from datapath 0 (DPS = 00)
1010: status event from datapath 1, 2 or 3 (DPS = 01, 10 or 11)

MDS … Message destination/source
The source coding is different for datapath 0 and datapath 1, 2, 3.
10: message is originated from the buffer (for DPS = 00)
00: message is originated from the buffer (for DPS = 01, 10 or 11)

STEV … Status Event Code
1Fh: Transmit Buffer Overflow
2Fh: Receive Buffer Overflow

3.3.3.2 Buffer General Status Event (ISAR 34 → Host)

If a data path is online and the associated write buffer has space available for a new message, the status event message “buffer available” is generated to request new data from the host.

The I/O-buffer control unit generates write buffer status event messages that cover information about all buffers, thus the IIS register contains a general code (IIS = 0). In this way the load for transfering messages is decreased significantly, as a single message may request data for more than one datapath. It is the responsibility of the host to dispatch RDMx to the controller routines of the relevant datapath.

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	RDM3	RDM2	RDM1	RDM0

	7	6	5	4	3	2	1	0
CTRL LSB	0							

RDM3 - 0 ... Request for next Data Message from Channel 3, 2, 1 or 0
If bit RDM3, RDM2, RDM1 or RDM0 is set, the corresponding datapath 0, 1, 2 or 3 requests for a new data message from the host.

A status event is generated by the control unit and indicated to the host when

- at least one of the write buffers changes its state from “not enough free space” to “enough free space for another data message”, or when
- at least one of the write buffers has still enough free space for another message immediately after a new message was written into this buffer.

Only when either of these two states is met, the status event message is generated. If the request is not serviced by the host, the ISAR 34 will not generate a new status event message to request data for that path.

It should be noticed that the corresponding bit for that buffer remains not set in the control register each time another buffer generates an interrupt to request new data.

However a status request message (see **chapter 3.3.1**) can force the generation of an indication for buffer available for a certain buffer.

The general proceeding for data transfer from the host to the transmit buffer would be:

- after Reset and completion of the initialization procedure the ISAR 34 will release an initial status event message with RDM0 = RDM1 = RDM2 = RDM3 = 1
- the host configures buffer, data pump, IOM-2 interface and SART
- the host writes the first message to the buffer (buffer is empty after reset)
- if the remaining buffer space is greater than the programmed message length, there will be an immediate interrupt to the host, who in turn can transfer the next message.
- if the remaining buffer space is smaller than the programmed message length, there will be no interrupt to the host until data is transmitted from the buffer and enough space is available to accept one complete message.
- if there is a request for message to the host and the host has no new message to send, the host should store the request information, so for new data it can immediately continue with transfering it to the buffer.
- the host can force the generation of an indication for buffer available for a certain buffer (see **chapter 3.3.1**).

3.4 SART Configuration

For the B-channel datapaths (path 1 and 2) the configuration setup message requires a specific coding depending on the required SART mode (HDLC, ASYNC or binary). The coding for each mode is described in the following chapters.

The D-channel datapath (path 3) is always operating in HDLC mode, therefore no SART configuration setup is required. As datapath 0 is used for the MONITOR channel and for test/diagnostics functions, there is no SART function and no SART messages are defined.

For SART configuration all parameters have to be set for the corresponding SART mode even though a single parameter may not be different from a previous setting.

Important note:

After configuration of the pump, the configuration information of the SART gets lost, therefore the SART unit must be configured after the pump configuration.

3.4.1 SART Configuration Setup - HDLC (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	0	1	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	HDMC		0	0	SMODE			

	7	6	5	4	3	2	1	0
CTRL LSB	1							

	7	6	5	4	3	2	1	0
1. Parameter	0	0	0	HIO	IFF	FLEN	EDF	DUO

DPS … Datapath selection
01: path 1
10: path 2

HDMC … Halfduplex Mode Configuration
00: Receive and transmit channel are enabled (default)
01: Receive channel is disabled
10: Transmit channel is disabled
11: not used

In halfduplex mode the pump would transfer idle bits in the direction that is currently not in use, so the corresponding receive or transmit channel can be selectively disabled to reduce the interrupt load for not valid data. For all other pump modes except halfduplex mode, HDMC must be set to its default value 00.

SMODE … SART Mode
0000: Disable SART
0010: V.14 mode
0011: HDLC mode
0100: Binary mode
0101: FSK V.14 mode
all other codes reserved

HIO … HDLC Input/Output
0: regular
1: inverted
“Inverted” describes a mode where all bits are changed from “0” to “1” and from “1” to “0” after HDLC formatting.

IFF … Interframe Fill
0: flags
1: “1”

FLEN … FCS length
0: 16 bit FCS
1: 32 bit FCS (not supported in ISAR 34 V2.1)

EDF … Enable/Disable FCS
0: enable FCS (regular HDLC operation)
1: disable FCS
This refers to FCS generation in transmit direction and FCS checking in receive direction.

DUO … Data Underrun Operation
For data underrun in TX direction …
0: … Abort is generated (default)
1: … Frame End (FCS and final flag) is generated

3.4.2 SART Configuration Setup - ASYNC (Host → ISAR 34)

ASYNC denotes an asynchronous formatting of data according to ITU-T V.14. Two separate modes are distinguished for ASYNC which depends on the selected modulation scheme at the data pump.

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	0	1	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	HDMC		0	0	SMODE			

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	0	OVSP	SNP	PSL	EDP	NSB	CHS	

	7	6	5	4	3	2	1	0
2. Parameter	BFT							

DPS … Datapath selection
01: path 1
10: path 2

HDMC … Halfduplex Mode Configuration
00: Receive and transmit channels are enabled (default)
01: Receive channel is disabled
10: Transmit channel is disabled
11: not used

In halfduplex mode the pump would transfer idle bits in the direction that is currently not in use, so the corresponding receive or transmit channel can be selectively disabled to reduce the interrupt load for not valid data.

For all other pump modes except halfduplex mode, HDMC must be set to its default value 00.

SMODE … SART Mode

0000: Disable SART

0010: V.14 mode (used for pump modes V.110, V.32, V.32bis, V.22, V.22bis)

0011: HDLC mode

0100: Binary mode

0101: FSK V.14 mode (used for pump modes V.21, V.23, Bell 103, Bell 202)

all other codes reserved.

There is a difference in the pump modes FSK V.14 and V.14:

- For FSK V.14 the bit alignment during an idle sequence gets lost, since there is only one frequency for the mark bit and so there's no fixed baud rate at the data pump during the idle sequence.
- For V.14 mode there is a data stream that has a fixed bit alignment, since the modulation scheme provides a fixed baud rate even during an idle sequence.

Important Note:

FSK V.14 mode must not be used for any other pump modes than V.21, V.23, Bell 103 and Bell 202.

OVSP … Overspeed Range (Valid only for transmit direction)
Number of stop bits to be deleted

0: 1 of 8

1: 1 of 4

Stop bit deletion during data transmission is initiated by a control command, otherwise all stopbits are generated independent of OVSP setting.
It is only valid for V.14 mode and not supported for FSK V.14.
Overspeed range for the transmitter is an option that can be used to increase the data rate in ASYNC mode by means of the overspeed mechanism that is actually defined for compensating different data rates due to missing synchronism between an AYSNC-receiver and transmitter.

SNP … Stick/Normal Parity

0: normal parity

1: stick parity

PSL … Parity Select
The selection (even, odd, stick 0, stick 1) depends on the setting of SNP:

SNP = 0		SNP = 1	
0:	Odd parity	0:	Parity bit = 1
1:	Even parity	1:	Parity bit = 0

EDP … Enable/Disable Parity Bit

0:	disable parity
1:	enable parity

NSB … Number of Stop Bits

0:	1 Stop bit
1:	2 Stop bits

CHS … Character Size

00:	5 bit
01:	6 bit
10:	7 bit
11:	8 bit

BFT … Buffer Flush Timeout (valid for receive direction only)

0:	Flush timeout disabled	
1:	Flush timeout	= 2 × symbolrate
2:		= 4 × symbolrate
:		:
:		:
254:		= 508 × symbolrate
255:		= 510 × symbolrate

The Buffer flush counter determines the length of a timer that is started when after a single character an idle sequence is being received. This is to ensure, that ASYNC characters are indicated and transferred to the host in case of a long idle sequence even though the message length is not yet complete. If the timeout is disabled, the last datawords remain in the receiver buffer - even during a long idle sequence - until the message length is complete which is then indicated to the host.

For fast data rates a value in the range BFT = 10 … 50 is suitable, whereas for slow data rates (V.21/300 bit/s) a lower value is recommended. The BFT-value should be selected high enough to avoid a too early buffer flush, which would increase the mailbox load.

The symbolrate refers to the selected modulation scheme which is selected for pump configuration.

3.4.3 SART Configuration Setup - Binary (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	0	1	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	HDMC		0	0	SMODE			

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	0	0	0	0	0	0	DUO	BSW

	7	6	5	4	3	2	1	0
2. Parameter	DUFW							

DPS … Datapath selection
01: path 1
10: path 2

HDMC … Halfduplex Mode Configuration
00: Receive and transmit channel are enabled (default)
01: Receive channel is disabled
10: Transmit channel is disabled
11: not used
In halfduplex mode the pump would transfer idle bits in the direction that is currently not in use, so the corresponding receive or transmit channel can be selectively disabled to reduce the interrupt load for not valid data. For all other pump modes except halfduplex mode, HDMC must be set to its default value 00.

SMODE … SART Mode
0000: Disable SART
0010: V.14 mode
0011: HDLC mode
0100: Binary mode
0101: FSK V.14 mode
all other codes reserved

DUO … Data Underrun Operation
For data underrun in TX direction …
0: … previous databyte in TX buffer is continuously transmitted
1: … fillword in mailbox (2nd parameter) is continuously transmitted
The fillword functionality can be used to transmit “1” or “0” or any other 8 bit value without continuous message transfer between host and ISAR 34.

BSW … Bit Swapping
0: LSB is transmitted/received first
1: MSB is transmitted/received first

DUFW … Data Underrun Fill Word
This fillword is transmitted continuously if a data underrun condition occurs in transmit direction.
This functionality is only valid if the DUO bit in the first parameter is set.

3.4.4 SART Configuration Setup - Disable SART (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	0	1	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	SMODE			

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DPS … Datapath selection
01: path 1
10: path 2

SMODE … SART Mode
0000: Disable SART
0010: V.14 mode
0011: HDLC mode
0100: Binary mode
0101: FSK V.14 mode
all other codes reserved

If the SART is disabled, the data received by the pump is not forwarded to the receive buffer.

In transmit direction, a continuous sequence of “1” (marks) are forwarded to the pump if the SART is disabled.

3.5 SART Data

Data together with status information or control commands is exchanged by 2 types of operation, which are described in the following two chapters.

The parameter MDS = 00 indicates that the message is related to the buffer as the user data is transferred to and from the buffers.

However, the whole message is described as a SART message, since status information, originated from the SART control unit and control information which is meant for the SART unit is transferred along with it.

3.5.1 SART Status Events with Receive Data (ISAR 34 → Host)

The SART receiver status, which is always data related, is passed to the host along with any data transfer via the mailbox.

The SART status is coded in the CTRL MSB, while the CTRL LSB indicates the number of data available in the mailbox .

Certain SART receive state changes cause an immediate buffer flush event to the associated interface buffer, i.e. any time when such a state changes, all data in the internal FIFO buffer is transferred to the host even if the buffer was not yet filled up to the programmed message length.

Most status bits are related to the last databyte of the mailbox (e.g. parity error). Others, like “frame start” in HDLC mode are related to the first databyte in the mailbox.

If no bit is set, messages of the predefined length are transferred.

3.5.1.1 SART Status Events with Receive Data - HDLC (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS			1	0	0	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	–	FED	FSD	FAD	RER	CER	–	NMD

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	1st databyte of the message							

	7	6	5	4	3	2	1	0
N. Parameter	N-th databyte of the message							

DPS … Datapath selection

01: path 1
10: path 2
11: path 3

A status information is valid, if the corresponding bit is set to ‘1’:

FED … Frame End detected

FSD … Frame Start detected

FAD … Frame Abort detected

RER … Residue Error detected
Received data is not multiple of 8 bits.

CER … CRC Error detected
Mailbox contains all received data.

NMD … No More Data (only valid with fax modulations pump mode)
NMD indicates that the carrier of the remote fax modem is no longer available.

NOM … Number of Valid Bytes in the Mailbox
Indicates the number N of valid data bytes to be read from the mailbox.

For the “Frame End”-condition, the FCS is contained in the HDLC frame as the last 2 octetts of the message (16 bit FCS).

For all conditions indicated in bit 14 - bit 10 (CTRL MSB), valid data in the buffer is indicated to the host although the message length may not yet be complete. For short frames where the frame length does not exceed the maximum message length (MML), FED and FSD can be set within one message.

Incomplete HDLC frames indicated in bit 12 - 10 are available in the mailbox including the erroneous data word. However, the host does not need to read such a frame from the buffer, it can skip this frame by only setting the ISAR 34 Interrupt Acknowledge bit (IIA).

3.5.1.2 SART Status Events with Receive Data - ASYNC (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS			1	0	0	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	–	–	BRE	BRS	DSD	PER	–	–

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	1st databyte of the message							

	7	6	5	4	3	2	1	0
N. Parameter	N-th databyte of the message							

DPS … Datapath selection

01: path 1
10: path 2

Note: ASYNC mode is not defined for path 3.

A status information is valid, if the corresponding bit is set to ‘1’:

BRE … Break Signal End detected

BRS … Break Signal Start detected

DSD … Deleted Stopbit Detected
It is up to the host to decide whether this indicates a frame error or an allowed stop bit deletion due to overspeed range.

PER … Parity Error

NOM … Number of Valid Bytes in the Mailbox
Indicates the number N of valid data bytes to be read from the mailbox.

Break End occurs with the first character in the mailbox, which is not valid. If the message contains more than one character, all characters starting from the second are valid.

All other status indications (bit 12 - 10) refer to the last character of the message, so the last character is not valid if one of these bits is set.

For all conditions indicated in bit 12 to 10, valid data in the buffer is indicated to the host although the message length may not yet be complete.

For characters with a length of 5, 6 or 7 bits the parity bit is transferred together with the character in bit position 5, 6 or 7 respectively (asuming that the first bit is in position 0). It is not available for 8 bit characters.

3.5.1.3 SART Status Events with Receive Data - Binary (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS			1	0	0	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	–	–	–	–	–	–	–	NMD

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	1st databyte of the message							

	7	6	5	4	3	2	1	0
N. Parameter	N-th databyte of the message							

DPS … Datapath selection

01: path 1
10: path 2

Note: Binary mode is not defined for path 3.

NMD … No More Data (only valid with fax modulations pump mode)
NMD = 1 indicates that the carrier of the remote fax modem is no longer available.

NOM … Number of Valid Bytes in the Mailbox
Indicates the number N of valid data bytes to be read from the mailbox.

3.5.2 SART Control Commands with Transmit Data (Host → ISAR 34)

The SART transmitter control commands, which are data related, are passed to the ISAR 34 along with any data transfer via the mailbox.

The SART control command is coded in the CTRL MSB, while the CTRL LSB indicates the number of data available in the mailbox for transmission.

Messages without data bytes, i.e. messages with CTRL LSB = 0, must not be sent to the ISAR 34.

3.5.2.1 SART Control Commands with Transmit Data - HDLC (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	0	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	0	FED	FST	GFA	0	0	0	NMD

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	1st databyte of the message							

	7	6	5	4	3	2	1	0
N. Parameter	N-th databyte of the message							

DPS … Datapath selection

01: path 1
10: path 2
11: path 3

The control command is valid if the corresponding bit is set to ‘1’:

FED … Frame End
The last databyte in the mailbox is indicated as the last of the HDLC frame.

FST … Frame Start
The first databyte in the mailbox is indicated as the first of the HDLC frame.

GFA … Generate Frame Abort
Initiates the generation of an abort sequence.

NMD … No More Data (only for fax modulations pump mode)
Indicates the end of the data stream and initiates the termination of the current modulation. NMD has the similar effect as the command CMD_ESCAPE, the difference is, that NMD will cause the fax pump to turn off the modulation right after the last valid data and so enable to cope with timings related to certain protocols.
NMD must not be set, if there is another HDLC frame to be sent right after the current FED, as this would cause the flag sequence to be turned off.
After the last message of an HDLC frame has been sent (with FED set), immediately another separate message with NMD must be issued by the host, containing one dummy databyte (CTRL LSB = 1), that will be discarded by the ISAR 34.

Note: NMD is not defined for path 2 and 3.

NOM … Number of Valid Bytes in the Mailbox
Indicates the number N of valid data bytes in the mailbox to be transmitted.

For datapath 3 an abort will be gnerated automatically by the ISAR 34 when a data underrun occurs, i.e. the host has failed to write further D-channel data to the mailbox.

3.5.2.2 SART Control Commands with Transmit Data - ASYNC (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	0	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	SOB	SAB	DSB	V42	0	0

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	1st databyte of the message							

	7	6	5	4	3	2	1	0
N. Parameter	N-th databyte of the message							

DPS … Datapath selection

01: path 1
10: path 2

Note: ASYNC mode is not defined for path 3.

The individual control function is valid if the corresponding bit is set to ‘1’:

SOB … Stop Break Signal

SAB … Start Break Signal

DSB … Delete Stopbits

V42 … Generate V42 detect sequence

NOM … Number of Valid Bytes in the Mailbox. Indicates the number N of valid data bytes in the mailbox to be transmitted.

With SAB a sequence of at least 2M+3 start bits is initiated and SOB enables the host to generate a variable sequence length. If both, SAB and SOB are set within one message, a break signal of exactly 2M+3 start bits is generated.

If DSB is set, every 4th or 8th stopbit is omitted as configured in the SART configuration setup (see **chapter 3.4.2**).

Setting of V42 causes the generation of 12 stopbits between each character in the mailbox.

Bit Alignment

Each of the data bytes written to the mailbox contains one V.14 character with the configured number of data bits. The character is aligned to the LSB position and the unused bit positions must be set to ’0’ by the host software. The LSB (bit D0) is transmitted first in the data stream.

	7	6	5	4	3	2	1	0
5 bit length	0	0	0	D4	D3	D2	D1	D0
6 bit length	0	0	D5	D4	D3	D2	D1	D0
7 bit length	0	D6	D5	D4	D3	D2	D1	D0
8 bit length	D7	D6	D5	D4	D3	D2	D1	D0

3.5.2.3 SART Control Commands with Transmit Data - Binary (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	0	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	0	0	0	NMD

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	1st databyte of the message							

	7	6	5	4	3	2	1	0
N. Parameter	N-th databyte of the message							

DPS … Datapath selection

01: path 1
10: path 2

Note: Binary mode is not defined for path 3.

The control function is valid if the corresponding bit is set to ‘1’:

NMD … No More Data (only for fax modulations pump mode)
Indicates the end of the data stream and initiates the termination of the current modulation. NMD has the similar effect as the command CMD_ESCAPE, the difference is, that NMD will cause the fax pump to turn off the modulation right after the last valid data and so enable to cope with timings related to certain protocols.
After the last message of a binary data stream has been sent, immediately another separate message with NMD must be issued by the host, containing one dummy databyte (CTRL LSB = 1), that will be discarded by the ISAR 34.

NOM … Number of Valid Bytes in the Mailbox
Indicates the number N of valid data bytes in the mailbox to be transmitted.

3.6 Pump Configuration

3.6.1 Pump Configuration Setup (Host → ISAR 34)

The pump is configured by the host. The Host Interrupt Status register (HIS) indicates that a new pump configuration is available in the mailbox registers.

Important Note:

It is important to note that configuration of the pump will reset the whole data path except buffer configuration, i.e. any configuration of the SART and IOM-2 is invalid, therefore the pump should be configured right after buffer configuration and precede SART and IOM-2 configuration.

The LSB of the control register holds the number of additional parameter words which are passed via the mailbox. The maximum number N of parameter words depends on the pump path mode.
The message coding of configuration setup for some of the pump modes is similar in a few of the parameters, however the total message coding is described separately for each of the pump modes which are:

Table 10 Pump Modes

Mode	PMOD
• Fax modulations	001
• Datamodem modulations	010
• Halfduplex modulations	011
• V.110	100
• DTMF	101
• Bypass	111

As the modulation based pump modes (PMOD = 001, 010, 011) are not available in datapath 2, the second channel must not be configured to these pump modes.

The table below shows to which of the pump modes datapath 2 can be configured.

Table 11 Pump Modes in Path 1 and 2

Datapath 1 (DPS = 01)	Datapath 2 (DPS = 10)
Fax modulations	
Datamodem modulations	
Halfduplex modulations	
V.110	V.110 (see note)
DTMF	
Bypass	Bypass

Important Note:

It is important to note that datapath 2 must not be configured to V.110 if path 1 is configured to datamodem modulations at the same time.

3.6.1.1 Pump Configuration Setup - Fax Modulations (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	0	1	1	0	0	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	OAM		0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	4							

	7	6	5	4	3	2	1	0
1. Parameter	0	0	0	0	0	ATN	0	CTN

	7	6	5	4	3	2	1	0
2. Parameter	0	0	0	TOA				

	7	6	5	4	3	2	1	0
3. Parameter	CODD							

	7	6	5	4	3	2	1	0
4. Parameter	CLDD							

OAM … Originating/Answering Mode

00: reserved
01: Pump is set to answering mode
10: Pump is set to originating mode
11: reserved

PMOD … Pump path mode select

000: Disable all (no mailbox entry)
001: Fax modulations
010: Datamodem modulations
011: Halfduplex modulations
100: V.110
101: DTMF
111: Bypass

ATN … Answer Tone
Enables or disables the generation of an answer tone when fax procedures are performed.
0: Answer tone is disabled
1: Answer tone is enabled

CTN … Calling Tone
Enables or disables the generation of a calling tone when fax procedures are performed.
0: Calling Tone is disabled
1: Calling Tone is enabled

TOA … Transmitter Output Attenuation
0: 0 db
1: 1 db
: :
31: 31 db
Recommended value (if not otherwise specified): 6db.

CODD ... Carrier On Detect Duration
0 - 253: This parameter specifies a time length in 100 ms units. Carrier On (RLSD ON) is signaled after a continuous carrier detection of the programmed time span.
254, 255: reserved
Recommended value (if not otherwise specified): 6 (600 ms)

CLDD ... Carrier Loss Detect Duration
This parameter specifies a time length in 100 ms units.
0 - 253: Carrier Off (RLSD OFF) is signaled after a continuous carrier loss of the programmed time span.
254, 255: reserved
Recommended value (if not otherwise specified): 14 (1400 ms)

3.6.1.2 Pump Configuration Setup - Datamodem Modulations (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	0	1	1	0	0	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	OAM		0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	11							

	7	6	5	4	3	2	1	0
1. Parameter	0	0	V22B	0	V22	0	V21	BEL

	7	6	5	4	3	2	1	0
2. Parameter	AMOD	V8	0	0	0	V34	V32	V23

	7	6	5	4	3	2	1	0
3. Parameter	V32R (LSB)							

	15	14	13	12	11	10	9	8
4. Parameter	V32R (MSB)							

	7	6	5	4	3	2	1	0
5. Parameter	V34R (LSB)							

	15	14	13	12	11	10	9	8
6. Parameter	V34R (MSB)							

	7	6	5	4	3	2	1	0
7. Parameter	0	0	0	0	GTS		ATN	CTN

	7	6	5	4	3	2	1	0
8. Parameter	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
9. Parameter	0	0	0	TOA				

	7	6	5	4	3	2	1	0
10. Parameter	CODD							

	7	6	5	4	3	2	1	0
11. Parameter	CLDD							

[10]

OAM … Originating/Answering Mode

00: reserved
01: Pump is set to answering mode
10: Pump is set to originating mode
11: reserved

PMOD … Pump path mode select

000: Disable all (no mailbox entry)
001: Fax modulations
010: Datamodem modulations
011: Halfduplex modulations
100: V.110
101: DTMF
111: Bypass

V22B … V.22bis, 2400 bit/s

0: is not permitted
1: is permitted

V22 … V.22/Bell 212, 1200 bit/s

0: is not permitted
1: is permitted

V21 … V.21/Bell 103, 300 bit/s

0: is not permitted
1: is permitted

BEL … Bell 103, 202 and 212 select

BEL selects whether in parameters V21, V22 and V23 the V.xx or the Bell xxx modulation is selected.

0: Bell modulation is not permitted
1: Bell modulation is permitted

AMOD … Automode operation according to EIA/TIA PN-2330

0: is disabled
1: is enabled

V8 … V.8 negotiation
0: is disabled
1: is enabled

V34 … V.34 modulation
0: is not permitted
1: is permitted

V32 … V.32bis modulation
0: is not permitted
1: is permitted

V23 … V.23/Bell 202, 1200 bit/s /75 bit/s
0: is not permitted
1: is permitted

V32R … V.32/V.32bis available rates
V32R determines the rate signal (specified in ITU V.32bis) that is used in the start-up, retrain and renegotiate procedures. The coding is the same as in the above mentioned recommendation, however some of the most commonly used codings are given below.

0000 0101 0001 0001:	V.32, 4800 bit/s
0000 1101 0001 0001:	V.32, up to 4800 bit/s
0000 0011 0001 0001:	V.32, 9600 bit/s
0000 1111 0001 0001:	V.32, up to 9600 bit/s
0000 1001 1101 0001:	V.32bis, 7200 bit/s
0000 1101 1101 0001:	V.32bis, up to 7200 bit/s
0000 1011 1001 0001:	V.32bis, 9600 bit/s
0000 1111 1101 0001:	V.32bis, up to 9600 bit/s
0000 1001 1011 0001:	V.32bis, 12000 bit/s
0000 1111 1111 0001:	V.32bis, up to 12000 bit/s
0000 1001 1001 1001:	V.32bis, 14400 bit/s
0000 1111 1111 1001:	V.32bis, up to 14400 bit/s

V34R V.34 available rates
V.34R determines the data rates which are permitted for both receive and transmit directions. A specific data rate is selected by a ’1’ in the corresponding bit position (unit is kbit/s). Any combination of the data rates is allowed:

	7	6	5	4	3	2	1	0
V.34R-LSB:	19.2	16.8	14.4	12.0	9.6	7.2	4.8	2.4
V.34R-MSB:	0	0	33.6	31.2	28.8	26.4	24.0	21.6

GTS … Guard Tone Select (for V.22/V.22bis)
- 00: Guard tone disabled
- 01: 550 Hz guard tone enabled
- 10, 11: reserved

ATN … V.25 answer tone
- 0: disabled
- 1: enabled

CTN … CTN … V.25 calling tone
- 0: disabled
- 1: enabled

TOA … Transmitter Output Attenuation
- 0: 0 db
- 1: 1 db
- : :
- 31: 31 db

Recommended value (if not otherwise specified): 6db

CODD ... Carrier On Detect Duration
- 0 - 253: This parameter specifies a time length in 100 ms units. Carrier On (RLSD ON) is signaled after a continuous carrier detection of the programmed time span.
- 254, 255: reserved

Recommended value (if not otherwise specified): 6 (600 ms)

CLDD ... Carrier Loss Detect Duration

This parameter specifies a time length in 100 ms units.
- 0 - 253: Carrier Off (RLSD OFF) is signaled after a continuous carrier loss of the programmed time span.
- 254, 255: reserved

Recommended value (if not otherwise specified): 14 (1400 ms)

The selection of the modulation scheme is contained from the 1st to the 6th parameter. If automode is selected, any modulation which is masked (set to “0”) in one of the parameters, is not tested/used in automode operation. For non-automode the permitted modulation parameters are used to select the data modulation. If more than one modulation is permitted, the highest possible data rate is selected.

The 8th parameter is reserved for further use and must be set to ’0’.

3.6.1.3 Pump Configuration Setup - Halfduplex Modulations (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	0	1	1	0	0	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	OAM		0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	5							

	7	6	5	4	3	2	1	0
1. Parameter	V17C	V17D	V29A	V29B	V29C	V27A	V27B	V21

	7	6	5	4	3	2	1	0
2. Parameter	0	0	0	EPT	0	0	V17A	V17B

	7	6	5	4	3	2	1	0
3. Parameter	0	0	0	TOA				

	7	6	5	4	3	2	1	0
4. Parameter	CODD							

	7	6	5	4	3	2	1	0
5. Parameter	CLDD							

OAM … Originating/Answering Mode
- 00: reserved
- 01: Pump is receiving only
- 10: Pump is transmitting only
- 11: reserved

PMOD … Pump path mode select
- 000: Disable all (no mailbox entry)
- 001: Fax modulations
- 010: Datamodem modulations
- **011: Halfduplex modulations**
- 100: V.110
- 101: DTMF
- 111: Bypass

V17C … V.17, 9600 bit/s
0: is disabled
1: is enabled

V17D … V.17, 7200 bit/s
0: is disabled
1: is enabled

V29A … V.29, 9600 bit/s
0: is disabled
1: is enabled

V29B … V.29, 7200 bit/s
0: is disabled
1: is enabled

V29C … V.29, 4800 bit/s
0: is disabled
1: is enabled

V27A … V.27ter, 4800 bit/s
0: is disabled
1: is enabled

V27B … V.27ter, 2400 bit/s
0: is disabled
1: is enabled

V21 … V.21 Channel 2, 300 bit/s
0: is disabled
1: is enabled

EPT … Echo Protector Tone
0: is disabled
1: is enabled

V17A … V.17, 14400 bit/s
0: is disabled
1: is enabled

V17B … V.17, 12000 bit/s
0: is disabled
1: is enabled

TOA … Transmitter Output Attenuation
0: 0 db
1: 1 db
: :
31: 31 db
Recommended value (if not otherwise specified): 6 db.

CODD ... Carrier On Detect Duration
0 - 253: This parameter specifies a time length in 100 ms units. Carrier On (RLSD ON) is signaled after a continuous carrier detection of the programmed time span.
254, 255: reserved
Recommended value (if not otherwise specified): 6 (600 ms)

CLDD ... Carrier Loss Detect Duration
This parameter specifies a time length in 100 ms units.
0 - 253: Carrier Off (RLSD OFF) is signaled after a continuous carrier loss of the programmed time span.
254, 255: reserved
Recommended value (if not otherwise specified): 14 (1400 ms)

The selection of the modulation scheme is contained in the 1st and 2nd parameter. If more than one modulation is enabled, the highest data rate is selected.

3.6.1.4 Pump Configuration Setup - V.110 (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	0	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	VDR							

	7	6	5	4	3	2	1	0
2. Parameter	0	0	0	0	0	0	0	FCT

DPS … Datapath selection
- 01: path 1
- 10: path 2

PMOD … Pump path mode select
- 000: Disable all (no mailbox entry)
- 001: Fax modulations
- 010: Datamodem modulations
- 011: Halfduplex modulations
- **100: V.110**
- 101: DTMF
- 111: Bypass

VDR … V.110 Data Rate
- 3: 600 bit/s
- 4: 1200 bit/s
- 5: 2400 bit/s
- 6: 4800 bit/s
- 8: 9600 bit/s
- 12: 19200 bit/s
- 20: 38400 bit/s
- 21: 48000 bit/s
- 22: 56000 bit/s (default)
- 23: 56000 bit/s (alternative)
- 24: 64000 bit/s

The default and alternative adaptation of 56 kbit/s to 64 kbit/s are specified in the ITU-T V.110 recommendation.

FCT … Flow Control (X-bits)
- 0: disabled
- 1: enabled

If enabled, the received X-bits are evaluated by the pump control and data from the mailbox is not forwarded to the SART unit for transmission if indicated by the remote side. Additionally, the X-bit change is indicated to the host by means of status events.
Flow control is only supported for SART mode V.14.

Important Note:

In contrast to the recommended initialisation procedure described in **chapter 3.1.4**, the sequence for configuration with pump mode V.110 is slightly different than for all other modes: If the pump should operate in V.110 mode, the IOM-2 interface must be configured as the last functional block, i.e. the sequence for configuration setup should be

1. Buffer configuration
2. Pump configuration (V.110)
3. SART configuration
4. IOM-2 configuration

3.6.1.5 Pump Configuration Setup - DTMF (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	0	1	1	0	0	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	DDIR		0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	6							

	7	6	5	4	3	2	1	0
1. Parameter	REL							

	7	6	5	4	3	2	1	0
2. Parameter	TW_LSB							

	7	6	5	4	3	2	1	0
3. Parameter	TW_MSB							

	7	6	5	4	3	2	1	0
4. Parameter	DON							

	7	6	5	4	3	2	1	0
5. Parameter	DOFF							

	7	6	5	4	3	2	1	0
6. Parameter	0	0	0	TOA				

DDIR ... DTMF Direction Control
00: reserved
01: DTMF transmitter active (no transfer of user data)
10: DTMF receiver active (during transfer of user data)
11: DTMF receiver and transmitter active (not supported in this version)

Transfer of user data is performed while a DTMF detector is active (DDIR=10). In order to transmit DTMF tones the pump must temporarily be configured to "DTMF transmitter active" (DDIR=01) and then reconfigured to "DTMF receiver active" (PMOD=10) again.

PMOD … Pump path mode select

000: Disable all (no mailbox entry)
001: Fax modulations
010: Datamodem modulations
011: Halfduplex modulations
100: V.110
101: DTMF
111: Bypass

REL … Rejection Level (valid for DTMF receiver)

A DTMF signal level which is below REL is not detected by the DTMF receiver. The table for all possible REL values is given below:

0: 0 dBm
1: – 1 dBm
2: – 2 dBm
3: – 3 dBm
: :
: :
93: – 93 dBm

The unit dBm is given with respect to full scale.
It is not recommended to use values above 93.
Recommended value (if not otherwise specified): $28_H = 40_D$ (– 40 dBm)

TW Twist (TW_MSB, TW_LSB; valid for DTMF receiver)

A DTMF tone consists of two tones with different frequency which have a signal level that can vary from another. The parameter Twist defines the difference in level between both frequencies that is accepted by the ISAR 34. The ISAR 34 will not detect a DTMF tone if the corresponding level difference of the received frequencies is greater than Twist.
The parameter TW (= TW_MSB, TW_LSB) is calculated according to the following equation, Twist is the required level difference (to be inserted without its unit dBm):

$$TW = 2^{15} \times 10^{-\frac{Twist + 0,5}{10}}$$

The unit dBm is given with respect to full scale.
Recommended value (if not otherwise specified):

$1214_H = 4628_D$ (8 dBm)

DON ... DTMF ON Duration (valid for DTMF transmitter)
Defines the length of generated DTMF tones (coding see DOFF).

DOFF ... DTMF OFF Duration (valid for DTMF transmitter)
A generated DTMF tone is subsequently followed by a signal pause. The length of this "no signal" phase is defined by DOFF.

0: (not to be used)
1: 1 ms
2: 2 ms
: :
254: 254 ms
255: 255 ms
The coding (given in decimal notation) is equal for DON and DOFF.
Recommended value (if not otherwise specified): 80 ms (for both)

TOA ... Transmitter Output Attenuation (valid for DTMF transmitter)
0: 0 db
1: 1 db
: :
31: 31 db
Recommended value (if not otherwise specified): 6 db.

In DTMF receive mode the octets received from the IOM-2 timeslot are passed transparently through the pump without data formatting, similar to bypass mode.

The DTMF receiver is active to detect DTMF tones in the received data stream and to indicate received DTMF digits to the host. The DTMF receiver interprets the octets received from the IOM-2 timeslot as A-law or µ-law PCM samples, depending on the IOM-2 configuration.

In transmit direction user data coming from the SART is forwarded similar as in bypass mode, i.e. without formatting in the pump. Additionally DTMF tones can be generated by the pump which is transmitted to the IOM-2. DTMF tone generation is performed by the host via DTMF specific pump control commands

3.6.1.6 Pump Configuration Setup - Bypass Mode (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	0	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	DPW	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DPS … Datapath selection
- 01: path 1
- 10: path 2

DPW … Data Path Width
- 0: pump data path is 8 bit
- 1: pump data path is 16 bit

PMOD … Pump path mode select
- 000: Disable all (no mailbox entry)
- 001: Fax modulations
- 010: Datamodem modulations
- 011: Halfduplex modulations
- 100: V.110
- 101: DTMF
- **111: Bypass**

3.6.2 Pump Control Command (Host → ISAR 34)

Control commands for the datapump are related to path 1 or path 2. For D-channel access via path 3 no pump is used, however commands to control the C/I-channel are coded with pump message codings.

3.6.2.1 Pump Control Command - Fax Modulations (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	0	1	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	FCMDL							

	7	6	5	4	3	2	1	0
2. Parameter	FCMDH							

	7	6	5	4	3	2	1	0
3. Parameter	MODC							

or

	7	6	5	4	3	2	1	0
3. Parameter	SLD							

FCMD … Fax Command (FCMDH, FCMDL)
Contains one of the following fax commands which are described in detail further down below. Two (FCMDL and FCMDH) or three (FCMDL, FCMDH and MODC or SLD) additional parameter must be written to the mailbox.

00A7h:	CMD_FTH	(NOM = 3, 3rd Parameter: MODC)
00A5h:	CMD_FRH	(NOM = 3, 3rd Parameter: MODC)
00A8h:	CMD_FTM	(NOM = 3, 3rd Parameter: MODC)
00A6h:	CMD_FRM	(NOM = 3, 3rd Parameter: MODC)
00ACh:	CMD_SIL_DET_ON	(NOM = 3, 3rd Parameter: SLD)
00A2h:	CMD_CONTINUE	(NOM = 2)
00A4h:	CMD__ESCAPE	(NOM = 2)
00ABh:	CMD_SIL_DET_OFF	(NOM = 2)
00A9h:	CMD_HALT	(NOM = 2)

NOM … Number of additional parameters in the mailbox

MODC … Modulation Code

This parameter indicates the particular facsimile modulation and speed selected for the next procedure.

3:	300 bit/s	(V.21 Ch2)
24:	2400 bit/s	(V.27ter)
48:	4800 bit/s	(V.27ter)
72:	7200 bit/s	(V.29)
73:	7200 bit/s	(V.17)
74:	7200 bit/s	(V.17 with short train)
96:	9600 bit/s	(V.29)
97:	9600 bit/s	(V.17)
98:	9600 bit/s	(V.17 with short train)
121:	12000 bit/s	(V.17)
122:	12000 bit/s	(V.17 with short train)
145:	14400 bit/s	(V.17)
146:	14400 bit/s	(V.17 with short train)

SLD … Silence Duration

This parameter determines the silence detect duration associated with the wait for silence procedure.

0:	0
1:	10 ms
2:	20 ms
:	:
255:	2550 ms

The fax control commands of the ISAR 34 are focused on the fax class 1 standard, i.e. the commands have the same function as decribed therein.

As for none of the other operation modes, the fax mode does not require a reprogramming of the complete data path when switching from HDLC formatted low speed data modulation (V.21Ch2) to unformatted high speed data modulation (V.17, V.29, V.27ter) and vice versa. Instead, by simply issuing a fax control command, both SART (binary or HDLC framing) and pump (V.21Ch2, V.17, ...) are reprogrammed without affecting other configuration settings.

Fax Command description:

CMD_FTH	Starts transmission of HDLC frames. The additional parameter MODC (NOM = 3) contains the modulation mode at which data is to be transmitted.
CMD_FRH	Starts reception of HDLC frames. The additional parameter MODC (NOM = 3) contains the modulation mode at which data is to be received.
CMD_FTM	Starts transmission of binary data. The additional parameter MODC (NOM = 3) contains the modulation mode at which data is to be transmitted.
CMD_FRM	Starts reception of binary data. The additional parameter MODC (NOM = 3) contains the modulation mode at which data is to be received.
CMD_SIL_DET_ON	Starts to wait a determined length of time. The additional parameter SLD (NOM = 3) contains the silence duration which has to be waited.
CMD_CONTINUE	Handshake message from the host to indicate that the host is ready to do the task (transmit/receive) which it selected before.
CMD_ESCAPE	This command is a regular escape in receive modes and a break in transmit modes.
CMD_SIL_DET_OFF	Break of silence detection.
CMD_HALT	Shut down from fax pump idle state.

3.6.2.2 Pump Control Command - Datamodem Modulations (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	0	1	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	15	14	13	12	11	10	9	8
1. Parameter	DCMDL							

	15	14	13	12	11	10	9	8
2. Parameter	DCMDH							

DCMD … Datamodem Command (DCMDH, DCMDL)
Contains one of the following datamodem commands, which are mainly used for debug purposes:
00CEh: LOCAL_RENEGOTIATE (only for V.34bis and V.32bis)
00CFh: LOCAL_RETRAIN (only for V.34bis, V.32bis, V.32 and V.22bis)

Command description:

LOCAL_RENEGOTIATE Initiates a V.34bis or V.32bis renegotiation, respectively.

LOCAL_RETRAIN Initiates a V.34bis, V.32bis, V.32 or V.22bis retrain, respectively (depending on the selected modulation scheme).

3.6.2.3 Pump Control Command - Halfduplex Modulations (Host → ISAR 34)

There are no control commands defined for this mode.

3.6.2.4 Pump Control Command - V.110 (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	3							

	15	14	13	12	11	10	9	8
1. Parameter	VCMDL							

	7	6	5	4	3	2	1	0
2. Parameter	VCMDH							

	7	6	5	4	3	2	1	0
3. Parameter (01F0h)	0	0	0	0	0	0	CCT	

or

	7	6	5	4	3	2	1	0
3. Parameter (01F1h)	0	0	0	0	X	SB	SA1	SA0

or

	7	6	5	4	3	2	1	0
3. Parameter (01F2h)	0	E1	E2	E3	E4	E5	E6	E7

or

	7	6	5	4	3	2	1	0
3. Parameter (01F3h)	FRC							

or

	7	6	5	4	3	2	1	0
3. Parameter (01F4h)	1							

or

	7	6	5	4	3	2	1	0
3. Parameter (01F5h)				ROF0	ROF1	RON1	ROFX	RONX

DPS … Datapath selection
01: path 1
10: path 2

VCMD … V.110 Command (VCMDH, VCMDL)
Contains one of the V.110 commands listed below. A third parameter must be written to the mailbox which is different for each of the commands.

01F0h: **Clamp Control**
According to the parameter CCT either user data (CCT=00), 0-bits (CCT=01) or 1-bits (CCT=11) are transmitted.

01F1h: **Set S-,X-bits (for transmitter)**
The S- and X-bit setting is defined in the 3. parameter.

01F2h: **Set E-bits (for transmitter)**
The E-bit setting is defined in the 3. parameter.

01F3h: **Delay of synchronisation (for receiver)**
By default, frame synchronisation is achieved with the first V.110 frame that is received correctly.
This command tells the pump control the number of V.110 frames which must be received correctly before synchronisation is achieved. The 3. parameter defines this number in the range 01h - FFh.

01F4h: **Enable mailbox buffer empty indication (for transmitter)**
If enabled, the ISAR 34 will release a status event to the host as soon as the last data in the mailbox buffer is transmitted and the host can set control bits after the last valid data has been transmitted. The status event will only be released once for a buffer empty condition, for a further state transition from “not empty” to “empty”, the indication has to be reenabled again. The 3. parameter must be set to ’1’.

01F5h: **Enable / Disable DTE control messages**
A status change of the remote DTE is can be indicated to the host by status events (NOM = 0). The host can select the type of status events to be received by enabling (’1’) or disabling the corresponding flag in the 3. parameter.

For the V.110 commands “Set clamp to 0/1” (VCMD = 11h/13h) data must not be entered to the mailbox for transmission. If a clamp is set and continuous 0-bits or 1-bits are transmitted, mailbox data will be discarded by the ISAR 34.

NOM … Number of additional parameters in the mailbox
For some of the commands one additional parameter must be written to the mailbox.

CCT … Clamp Control (required for command 01F0h)
00: Clamp disabled (user data is transmitted)
01: Clamp zero (0-bits are transmitted)
11: Clamp one (1-bits are transmitted)

The value 0 or 1 for each control bit below is directly written to the corresponding bit position within the V.110 frame:

X … X-bit (required for command 01F1h)

SB … S4-, S9-bit (required for command 01F1h)

SA1 … S3-, S8-bit (required for command 01F1h)

SA0 … S1-, S6-bit (required for command 01F1h)

E1-7 … E1-, .. E7-bit (required for command 01F2h)
For the 600 bit/s data rate bit E7 is don't care in the message coding, but is controlled by the pump for multiframe synchronisation.

FRC … Frame Counter (required for command 01F3h)
Denotes the number of V.110 frames that must be received correctly in order to achieve synchronism, e.g. if FRC = 3, three frames must be received correctly, before data is transferred to the receive buffer.

ROF0, ROF1, RON1, ROFX, RONX ... Mask remote DTE status indication (required for command 01F5h)

Indication of corresponding remote DTE status is
0: disabled
1: enabled

3.6.2.5 Pump Control Command - DTMF (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	0	1	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	DCMDL							

	7	6	5	4	3	2	1	0
2. Parameter	DCMDH							

	7	6	5	4	3	2	1	0
3. Parameter	TDIG							

DCMD Dial Command (DCMDH, DCMDL)
005Ah: Transmit DTMF digit (contained in 3. Parameter, NOM=3)

all other codes not supported

TDIG … Transmit DTMF Digit

10h:	‘0’
11h:	‘1’
12h:	‘2’
13h:	‘3’
14h:	‘4’
15h:	‘5’
16h:	‘6’
17h:	‘7’
18h:	‘8’
19h:	‘9’
1Ah:	‘A’
1Bh:	‘B’
1Ch:	‘C’
1Dh:	‘D’
1Eh:	‘∗’
1Fh:	‘#’

It should be noted that the IOM-2 interface must be configured with rate conversion enabled before any DTMF digits can be transmitted.

3.6.2.6 Pump Control Command - Bypass Mode (Host → ISAR 34)

There are no control commands defined for this mode.

3.6.2.7 Pump Control Command - C/I-Channel (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	1	1	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	CIC							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

CIC C/I-channel Command

Contains one of the following control commands for the C/I-channel. The function depends on whether D-channel access is configured with or without TIC bus access (IOM-2 configuration setup):

- **TIC bus disabled** (IOM-2 configuration setup: TIC=0):

8Mh: Transmit C/I code M permanently
This C/I code (coding is included in the low nibble M) is continuously transmitted on the C/I-channel without any mechanism for bus arbitration, i.e. bus access bit BAC and TIC bus address TAD are not evaluated.

- **TIC bus enabled** (IOM-2 configuration setup: TIC=1):

8Mh: Transmit C/I code M (no TIC bus access)
This C/I code (coding is included in the low nibble M) is continuously transmitted on the C/I-channel if no TIC bus access is requested by the ISAR 34 and as long as BAC=1 ("bus free") and TAD=111 (TIC bus address with lowest priority).
Once another device gains TIC bus access, the C/I code M is no longer transmitted and the value 1111_B is transmitted on the C/I-channel by the ISAR 34.
If the ISAR 34 gains TIC bus access, the C/I code N (see below) is transmitted.

9Nh: Transmit C/I code N (TIC bus access)
This C/I code (coding is included in the low nibble N) is transmitted on the C/I-channel if the TIC bus was accessed successfully (i.e. TIC bus access mechanism is used by writing and reading back TAD and evaluating BAC).

- **The command A0h is independent of TIC bus configuration:**

A0h: Request for Current C/I Code
The host requests the ISAR 34 to read the current value on the C/I-channel. Generally, subsequent C/I codes detected by the ISAR 34 are passed to the host in the sequence as they occured.
The command A0h does not break this sequence. It forces the ISAR 34 to read the current value (even if there’s no C/I code change) and forward it to the buffer.
C/I codes are always read according to the "double last look" criterion, i.e. C/I codes are only accepted as valid if two consecutive values are identical.

Important Note:

Before enabling the C/I-channel (IOM-2 configuration setup with CED=1), both C/I codes (contained in CIC=8Mh and 9Nh) must be programmed to ensure the right values are written to the C/I-channel from the beginning.

3.7 Pump Status

3.7.1 Pump Status Request (Host → ISAR 34)

A status register which holds the current status of the data pump path is available on request.

The pump status request is fully specified with the Host Interrupt Status register (HIS). The mailbox control register is not used and must be written to 0.

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			0	0	1	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DPS … Datapath selection
01: path 1
10: path 2

3.7.2 Pump Status Response (ISAR 34 → Host)

3.7.2.1 Pump Status Response - Fax Modulations (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	0	1	1	0	1	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	OAM		0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	RIL							

	7	6	5	4	3	2	1	0
2. Parameter	RIM							

OAM … Originating/Answering Mode
- 00: reserved
- 01: Pump is in answering mode
- 10: Pump is in originating mode
- 11: reserved

PMOD … Selected pump path mode
- 000: Disable all (no mailbox entry)
- **001: Fax modulations**
- 010: Datamodem modulations
- 011: Halfduplex modulations
- 100: V.110
- 101: DTMF
- 111: Bypass

RIL … Rate Index - LSB

RIL contains the data rate at which the pump is currently operating.

0: no speed defined
2: 300 bit/s
5: 2400 bit/s
6: 4800 bit/s
7: 7200 bit/s
8: 9600 bit/s
9: 12000 bit/s
10: 14400 bit/s

RIM … Rate Index - MSB

RIL contains the modulation scheme at which the pump is currently operating, the specific data rate is given in RIL. If RIM is 0, the preceding pump configuration setup was not successful.

0: no modulation scheme configured
21h: V.21 asynchronous (FSK V.14 mode)
27h: V.17
28h: V.29
2Ch: V.27ter

All other codes not supported.

3.7.2.2 Pump Status Response - Datamodem Modulations (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	0	1	1	0	1	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	OAM		0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	5							

	7	6	5	4	3	2	1	0
1. Parameter	RIL							

	7	6	5	4	3	2	1	0
2. Parameter	RIM							

	7	6	5	4	3	2	1	0
3. Parameter	RIT							

	7	6	5	4	3	2	1	0
4. Parameter	–	–	RRT	LRT	–	RRP	CON	NEG

	7	6	5	4	3	2	1	0
5. Parameter	–	CLD	RTY	TMO	–	–	RRN	LRN

OAM … Originating/Answering Mode
- 00: reserved
- 01: Pump is in answering mode
- 10: Pump is in originating mode
- 11: reserved

PMOD … Selected pump path mode

000:	Disable all (no mailbox entry)
001:	Fax modulations
010:	**Datamodem modulations**
011:	Halfduplex modulations
100:	V.110
101:	DTMF
111:	Bypass

RIL … Rate Index - LSB

RIL contains the data rate at which the pump is currently operating (same data rate in receive and transmit direction). For an asymmetrical data rate, RIL indicates the receive data rate.

0:	no speed defined
1:	75 bit/s
2:	300 bit/s
3:	600 bit/s
4:	1200 bit/s
5:	2400 bit/s
6:	4800 bit/s
7:	7200 bit/s
8:	9600 bit/s
9:	12000 bit/s
10:	14400 bit/s
11:	16800 bit/s
12:	19200 bit/s
13:	21600 bit/s
14:	24000 bit/s
15:	26400 bit/s
16:	28800 bit/s
17:	31200 bit/s
18:	33600 bit/s

All other codes not supported.

RIM … Rate Index - MSB

RIM contains the modulation scheme at which the pump is currently operating, the specific data rate is given in RIL. If RIM is 0, the preceding pump configuration setup was not successful.

0:	no modulation scheme configured
02h:	V.22
09h:	V.32
0Ah:	V.32bis
0Bh:	V.34
11h:	V.21 asynchronous (FSK V.14 mode)
14h:	V.23
27h:	V.27ter
28h:	V.29
2Ch:	V.17
51h:	Bell 103
54h:	Bell 202

All other codes not supported.

RIT … Rate Index - Transmit Direction

RIT is only valid for V.34 modulation. It contains the data rate in transmit direction.

0:	no speed defined
5:	2400 bit/s
6:	4800 bit/s
7:	7200 bit/s
8:	9600 bit/s
9:	12000 bit/s
10:	14400 bit/s
11:	16800 bit/s
12:	19200 bit/s
13:	21600 bit/s
14:	24000 bit/s
15:	26400 bit/s
16:	28800 bit/s
17:	31200 bit/s
18:	33600 bit/s

All other codes not supported.

The status information is valid, if the corresponding bit is set:

RRT … Remote Retrain
The pump is in a retrain phase that is initiated by the remote station.

LRT … Local Retrain
The pump is in a retrain phase that is initiated by the local station.

RRP … Retrain / Renegotiate Phase
The pump is in a retrain or renegotiate phase. More details are contained in the status bits RRT, LRT, RRN and LRN.

CON … Connection
The pump has established a logical connection to the remote subscriber, i.e. it has passed the training phase and will continue with data transmission/reception.

NEG … Negotiation
The pump is in the first training phase to establish the modulation.

CLD … Cleardown
This bit is set if there is a reason to terminate and restart the modulation. A reason could be a rate signal without any permitted data rate or a timeout condition for bulk delay (together with setting of TMO).

RTY … Retry
During training phase the remote station has requested for a retrain (V.32bis only).

TMO … Timeout
During training phase the timing conditions for bulk delay were violated.

RRN … Remote Renegotiation
The pump is in a renegotiate phase that is initiated by the remote station.

LRN … Local Renegotiation
The pump is in a renegotiate phase that is initiated by the local station.

3.7.2.3 Pump Status Response - Halfduplex Modulations (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	0	1	1	0	1	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	OAM		0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	RIL							

	7	6	5	4	3	2	1	0
2. Parameter	RIM							

OAM … Originating/Answering Mode
- 00: not used
- 01: Pump is receiving only
- 10: Pump is transmitting only
- 11: not used

PMOD … Selected pump path mode
- 000: Disable all (no mailbox entry)
- 001: Fax modulations
- 010: Datamodem modulations
- **011: Halfduplex modulations**
- 100: V.110
- 101: DTMF
- 111: Bypass

RIL … Rate Index - LSB

RIL contains the data rate at which the pump is currently operating.

0: no speed defined
2: 300 bit/s
5: 2400 bit/s
6: 4800 bit/s
7: 7200 bit/s
8: 9600 bit/s
9: 12000 bit/s
10: 14400 bit/s

All other codes not supported.

RIM … Rate Index - MSB

RIL contains the modulation scheme at which the pump is currently operating, the specific data rate is given in RIL. If RIM is 0, the preceding pump configuration setup was not successful.

0: no modulation scheme configured
21h: V.21 asynchronous (FSK V.14 mode)
27h: V.27ter
28h: V.29
2Ch: V.17

All other codes not supported.

3.7.2.4 Pump Status Response - V.110 (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS			1	0	1	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	6							

	7	6	5	4	3	2	1	0
1. Parameter	RIL							

	7	6	5	4	3	2	1	0
2. Parameter	RIM							

	7	6	5	4	3	2	1	0
3. Parameter	–	–	–	ROF0	ROF1	RON1	ROFX	RONX

	7	6	5	4	3	2	1	0
4. Parameter	–	–	–	–	X	SB	SA1	SA0

	7	6	5	4	3	2	1	0
5. Parameter	–	E1	E2	E3	E4	E5	E6	E7

	7	6	5	4	3	2	1	0
6. Parameter	FRC							

DPS … Datapath selection
01: path 1
10: path 2

PMOD … Selected pump path mode
- 000: Disable all (no mailbox entry)
- 001: Fax modulations
- 010: Datamodem modulations
- 011: Halfduplex modulations
- **100: V.110**
- 101: DTMF
- 111: Bypass

RIL … Rate Index - LSB
RIL contains the data rate at which the pump is currently operating.
- 0: no speed defined
- 3: 600 bit/s
- 4: 1200 bit/s
- 5: 2400 bit/s
- 6: 4800 bit/s
- 8: 9600 bit/s
- 12: 19200 bit/s
- 20: 38400 bit/s
- 21: 48000bit/s
- 22: 56000 bit/s (default)
- 23: 56000 bit/s (alternative)
- 24: 64000 bit/s

All other codes not supported.
RIL = 0 is indicated in V.110 mode if not synchronised.

RIM … Rate Index - MSB
RIL contains the modulation scheme at which the pump is currently operating, the specific data rate is given in RIL. If RIM is 0, the preceding pump configuration setup was not successful, e.g. a wrong data rate was selected for V.110.

- 0: no modulation scheme configured
- C0h: V.110

All other codes not supported.

ROF0, ROF1, RON1, ROFX, RONX … Remote DTE status

Contains information about the status of the remote DTE. The received D- and SA-bits are sampled and compared against different possibilities. A status change is detected by a match of the comparison and indicated by setting the bits as shown below. Several bits in the parameter can be set simultaneously depending on the sampled data, e.g. if ROF0 is set, ROFX will be set, too.
It should be noted, that the status response is not data related, i.e. it contains the remote status that is currently received.

Status	Status Name	Sampled Data		
ROF0	Remote (0, OFF)	D	00000000	00000000
		SA	11111111	11111111
ROF1	Remote (1, OFF)	D	11111111	11111111
		SA	11111111	11111111
RON1	Remote (1, ON)	D	11111111	11111111
		SA	00000000	00000000
ROFX	Remote (X, OFF)	D	XXXXXXXX	XXXXXXXX
		SA	11111111	11111111
RONX	Remote (X, ON)	D	XXXXXXXX	XXXXXXXX
		SA	00000000	00000000

Note: X *= Don't care*

The following parameters contain the value for each X-, S- and E-bit, which is currently received:

X … X-bit

SB … S4-, S9-bit

SA1 … S3-, S8-bit

SA0 … S1-, S6-bit

E1-E7 … E1-bit - E7-bit
For the 600 bit/s data rate bit E7 is always set to 1.

FRC … Frame Counter for delay of synchronisation
Denotes the actual number of frames that must be received correctly in order to achieve synchronism, e.g. if FRC = 3, three frames have to be received correctly, before data is transferred to the receive buffer.

3.7.2.5 Pump Status Response - DTMF (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	0	1	1	0	1	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	DDIR		0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	RIL							

	7	6	5	4	3	2	1	0
2. Parameter	RIM							

DDIR ... DTMF Direction Control
- 00: reserved
- 01: DTMF transmitter active (no transfer of user data)
- 10: DTMF receiver active (during transfer of user data)
- 11: DTMF receiver and transmitter active (not supported in this version)

PMOD … Selected pump path mode
- 000: Disable all (no mailbox entry)
- 001: Fax modulations
- 010: Datamodem modulations
- 011: Halfduplex modulations
- 100: V.110
- **101: DTMF**
- 111: Bypass

RIL … Rate Index - LSB
RIL contains the data rate at which the pump is currently operating.
- 24: 64000 bit/s

RIM … Rate Index - MSB
RIL contains the modulation scheme at which the pump is currently operating, the specific data rate is given in RIL.
- C0h: digital transparent mode

3.7.2.6 Pump Status Response - Bypass Mode (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS			1	0	1	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	RIL							

	7	6	5	4	3	2	1	0
2. Parameter	RIM							

DPS … Datapath selection
- 01: path 1
- 10: path 2

PMOD … Selected pump path mode
- 000: Disable all (no mailbox entry)
- 001: Fax modulations
- 010: Datamodem modulations
- 011: Halfduplex modulations
- 100: V.110
- 101: DTMF
- **111: Bypass**

RIL … Rate Index - LSB
RIL contains the data rate at which the pump is currently operating.
- 24: 64000 bit/s

RIM … Rate Index - MSB
RIL contains the modulation scheme at which the pump is currently operating, the specific data rate is given in RIL.
- C0h: digital transparent mode

3.7.2.7 Pump Status Response - Pump Disabled (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS			1	0	1	1	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	0	PMOD		

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DPS … Datapath selection
- 01: path 1
- 10: path 2

PMOD … Selected pump path mode
- **000: Disable all (no mailbox entry)**
- 001: Fax modulations
- 010: Datamodem modulations
- 011: Halfduplex modulations
- 100: V.110
- 101: DTMF
- 111: Bypass

3.7.3 Pump Status Events (ISAR 34 → Host)

Status events are released to the host by the data pump during data transmission/ reception and contain dynamic information specific for the selected pump mode.

3.7.3.1 Pump Status Events - Fax Modulations (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	0	1	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	FEVTL							

	15	14	13	12	11	10	9	8
2. Parameter	–	–	–	–	–	FEVTH		

FEVT … Fax Event (FEVTH, FEVTL)
Contains the one of the following fax events:

002h: 10 ms timer interrupt (if enabled; see **chapter 3.11.2** Timer Interrupt Event)
0BCh: RSP_READY
0B3h: LINE_TX_HDLC
0B2h: LINE_TX_BINARY
0B1h: LINE_RX_HDLC
0B0h: LINE_RX_BINARY
0B5h: RSP_CONNECT
0B7h: RSP_DISC
0B9h: RSP_FCERROR
0BEh: RSP_SIL_DET
0BAh: FLAGS_DETECT

Fax event description

RSP_READY	Response to configuration fax mode originator or answerer.
LINE_TX_HDLC	Response to CMD_FTH in order to indicate that the modulation has been established.
LINE_TX_BINARY	Response to CMD_FTM in order to indicate that the modulation has been established.
LINE_RX_HDLC	Response to CMD_FRH in order to indicate that the modulation has been established.
LINE_RX_BINARY	Response to CMD_FRM in order to indicate that the modulation has been established.
RSP_CONNECT	Indication that the fax pump is ready to receive or transmit data.
RSP_DISC	Indication that the fax pump has turned off modulation after transmitting all pending data / after the host issues the command CMD_ESCAPE.
RSP_FCERROR	Indication that the fax pump has detected a “wrong” modulation before it releases the event RSP_CONNECT.
RSP_SIL_DET	Indication that the prior selected duration of silence time has occured.
FLAGS_DETECT	Indication that the fax pump has detected flags.

3.7.3.2 Pump Status Events - Datamodem Modulations (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	0	1	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	DEVTL							

	15	14	13	12	11	10	9	8
2. Parameter	–	–	–	–	–	DEVTH		

DEVT … Datamodem Event (DEVTH, DEVTL)
Contains the one of the following datamodem events:

002h: 10 ms timer interrupt (if enabled; see **chapter 3.11.2** Timer Interrupt Event)
018h: CONNECTION_ON
019h: CONNECTION_OFF
020h: V24_OFF
021h: CTS_ON
022h: CTS_OFF
023h: DCD_ON
024h: DCD_OFF
025h: DSR_ON
026h: DSR_OFF
0CCh: REMOTE_RETRAIN
0CDh: REMOTE_RENEGOTIATE
0D4h: GSTN_CLEARDOWN

3.7.3.3 Pump Status Events - Halfduplex Modulations (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	0	1	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	HEVTL							

	15	14	13	12	11	10	9	8
2. Parameter	–	–	–	–	–	HEVTH		

HEVT … Halfduplex modulations Event (HEVTH, HEVTL)

Contains the one of the following datamodem events:

002h: 10 ms timer interrupt (if enabled; see **chapter 3.11.2** Timer Interrupt Event)
018h: CONNECTION_ON
019h: CONNECTION_OFF
020h: V24_OFF
021h: CTS_ON
022h: CTS_OFF
023h: DCD_ON
024h: DCD_OFF
025h: DSR_ON
026h: DSR_OFF
0D4h: GSTN_CLEARDOWN

3.7.3.4 Pump Status Events - V.110 (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS			1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	VEVT_LSB							

	15	14	13	12	11	10	9	8
2. Parameter	–	–	–	–	–	VEVTH		

	7	6	5	4	3	2	1	0
3. Parameter	–	–	–	–	X	SB	SA1	SA0

or

	7	6	5	4	3	2	1	0
3. Parameter	–	E1	E2	E3	E4	E5	E6	E7

or

	7	6	5	4	3	2	1	0
3. Parameter	–	–	–	ROF0	ROF1	RON1	ROFX	RONX

DPS … Datapath selection
01: path 1
10: path 2

VEVT … V.110 Event (VEVT_MSB, VEVT_LSB)
Contains one of the following V.110 events. For some of the events an additional parameter is provided via the mailbox.

002h: **10 ms timer interrupt** (if enabled; see **chapter 3.11.2** Timer Interrupt Event)

1F1h: **Change in S-bits received** (NOM = 3).
The S-bits are specified in the third parameter.

1F2h: **Change in E-bits received** (NOM = 3).
The E-bits are specified in the third parameter.

1F8h: **Synchronisation lost** (NOM = 2).
This event is released for a change from synchronised to not synchronised.

1F9h: **Synchronisation achieved** (NOM = 2).
This event is released for a change from not synchronised to synchronised.

1F6h: **Change in X-bit from 1 → 0 received** (NOM = 2).

1F7h: **Change in X-bit from 0 → 1 received** (NOM = 2).

1F4h: **Mailbox buffer empty** (NOM = 2)
This event indicates to the host, that the last data is transmitted and that the mailbox transmit buffer is empty. This event must be enabled by the host (see **chapter 3.6.2.4** Pump Control Command - V.110) and it is generated only once, i.e. for further state transitions from “not empty” to “empty”, the generation of the status event must be reenabled again.

1F5h: **DTE status** (NOM = 3)
The third parameter contains information about the status of the remote DTE. The received D- and SA-bits are sampled and compared against different possibilities. A status change is detected by a match of the comparison and indicated to the host. The generation of DTE status events can be enabled/ disabled by control commands (see **chapter 3.6.2.4** Pump Control Command - V.110).

NOM … Number of Valid Bytes in the Mailbox
For certain status events one additional parameter is provided via the mailbox.

For the following parameters the received value 0 or 1 for each bit is indicated in the corresponding bit position. The control bits do not represent the real time value that is currently received, but they are data related, i.e. the S-, X- and E-bits are transferred to the host with the corresponding data that was received at the same time.

Information about control bits that are currently received can be requested by the host (see **chapter 3.7.1** Pump status request), additionally the real time value for X, which is needed for flow control, is indicated by two separate status events (VEVT = 01F6h and 01F7h).

X … X-bit

SB … S4-, S9-bit

SA1 … S3-, S8-bit

SA0 … S1-, S6-bit

E1-7 … E1-, .. E7-bit
For the 600 bit/s data rate bit E7 is always set to 1.

ROF0, ROF1, RON1, ROFX, RONX … Remote DTE status

Contains information about the status of the remote DTE. The received D- and SA-bits are sampled and compared against different possibilities. A status change is detected by a match of the comparison and indicated by setting the bits as shown below. Several bits in the parameter can be set simultaneously depending on the sampled data, e.g. if ROF0 is set, ROFX will be set, too.

Table 12 V.110 Remote DTE Status

Status	Status Name	Sampled Data		
ROF0	Remote (0, OFF)	D	00000000	00000000
		SA	11111111	11111111
ROF1	Remote (1, OFF)	D	11111111	11111111
		SA	11111111	11111111
RON1	Remote (1, ON)	D	11111111	11111111
		SA	00000000	00000000
ROFX	Remote (X, OFF)	D	XXXXXXXX	XXXXXXXX
		SA	11111111	11111111
RONX	Remote (X, ON)	D	XXXXXXXX	XXXXXXXX
		SA	00000000	00000000

Note: X = don’t care

It should be noted that the DTE status information is data related and may not represent the value currently be received.

Comment:

After reset the remote DTE status logic is in no state and all status bits (ROF0, ROF1, RON1, ROFX and RONX) are set to 0. The pump will start to search for frame synchronisation.

When synchronisation is achieved, the host will receive the remote DTE status and the S-, X- and E-bits from the pump by means of status events. This information is related to the last V.110 frame that was received for synchronisation, as this frame was received without any sync error. Starting with the subsequent frame, the D-bits of the frame are transferred as valid user data to the SART.

The same mechanism for resynchronisation is used if frame synchronisation is temporarily lost.

3.7.3.5 Pump Status Events - DTMF (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	0	1	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	3							

	7	6	5	4	3	2	1	0
1. Parameter	DEVTL							

	15	14	13	12	11	10	9	8
2. Parameter	–	–	–	–	–	DEVTH		

	7	6	5	4	3	2	1	0
3. Parameter	RDIG							

DEVT ... DTMF Event (DEVTH, DEVTL)
Contains the one of the following DTMF events:
002h: 10 ms timer interrupt (if enabled; see **chapter 3.11.2** Timer Interrupt Event)
057h: DTMF tone detected
(all other codes reserved)

RDIG … Received DTMF Digit
One of the following DTMF digits was detected by DTMF receiver:

10h:	‘0’
11h:	‘1’
12h:	‘2’
13h:	‘3’
14h:	‘4’
15h:	‘5’
16h:	‘6’
17h:	‘7’
18h:	‘8’
19h:	‘9’
1Ah:	‘A’
1Bh:	‘B’
1Ch:	‘C’
1Dh:	‘D’
1Eh:	‘*’
1Fh:	‘#’

3.7.3.6 Pump Status Events - Bypass Mode (ISAR 34 → Host)

No status events defined for this mode.

3.7.3.7 Pump Status Events - D- and C/I-Channel (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	1	1	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	DCIE							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DCIE … D-channel and C/I-channel Event
Contains one of the following events either from the D-channel or from the C/I-channel:

10h: Message Abort
The ISAR 34 detects a S/G bit change to ’1’ (stop) and all D-channel data (i.e. current message and all subsequent messages) in the transmit buffer is cleared, the receive buffer is not affected. The host must write this data to the mailbox again, starting with the beginning of the aborted frame.
However, the ISAR 34 has a short internal buffer for D-channel data to solve collisions on the S-bus, so not all collisions are indicated to the host, but handled automatically by the ISAR 34. Therefore the "Message Abort" will only be released if the conflict could not be solved within the internal data storage of the ISAR 34.

20h: Message Complete
A frame was successfully transmitted on the D-channel.
This flag is used to control the transmission of subsequent D-channel HDLC frames. The host must not start writing data of a new HDLC frame to the ISAR 34 before this flag was set to confirm the successful transmission of the previous frame.

8Mh: C/I Code Change M
A new C/I code (coding is included in M) was received twice (double last look) on the C/I-channel (4th timeslot on IOM-2 channel 0).
When the C/I-channel is enabled by configuration setup, a first C/I Code Change message is indicated to the host with the current C/I information. The C/I information is not related to D-channel data.

3.8 IOM®-2 Configuration

The following commands, requests and responses are used to setup/control the network access of the data paths.

The message coding of both datapaths 1 and 2 (B-channel data) are similar. For datapath 3 (D-channel data) some codings are different and therefore described in separate chapters.

3.8.1 IOM®-2 Configuration Setup - Path 1 and 2 (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	0	1	1	1

	15	14	13	12	11	10	9	8
CTRL MSB	IOM	0	0	0	COD			RCV

	7	6	5	4	3	2	1	0
CTRL LSB	5							

	7	6	5	4	3	2	1	0
1. Parameter	0	0	0	TXD	RXD	TSL		

	7	6	5	4	3	2	1	0
2. Parameter	0	0	RTSO					

	7	6	5	4	3	2	1	0
3. Parameter	0	0	0	0	0	RCS		

	7	6	5	4	3	2	1	0
4. Parameter	0	0	TTSO					

	7	6	5	4	3	2	1	0
5. Parameter	0	0	0	0	0	TCS		

DPS … Datapath selection
01: path 1
10: path 2

IOM … IOM-2 data access
0: disabled
1: enabled

COD … Coding
000: no PCM coding (16-bit linear data)
001: A-law coding (8-bit data)
010: µ-law coding (8-bit data)
all other codes reserved
For the pump modes V.110 and bypass “no PCM coding” must be selected.
A-law and µ-law coding is selected for all modulation related pump modes (fax, datamodem and halfduplex modulation, DTMF and DTMF transmission). If "no PCM coding" is selected in these modes, 16-bit linear values are output on the IOM-2 interface.

RCV … Rate Conversion
RCV refers to internal operation of the device and must be set depending on the pump mode.
0: disabled (for all other pump modes)
1: enabled (for pump modes 001, 010, 011, 110)

TXD … Transmit path switched to
0: DD-line
1: DU-line (reset value)

RXD … Receive path switched to
0: DD-line (reset value)
1: DU-line

TSL … Timeslot length for Receive / Transmit path
000: 8 bit wordlength (reset value)
010: 16 bit wordlength (used to operate with 16 linear codec, e.g. ARCOFI)
all other codes currently not supported

RTSO … Receive Time Slot Offset to FSC
0: 0 bit
1: 8 bit
: :
63: 504 bit
Reset value: RTSO = 0 for path 1
RTSO = 1 for path 2

RCS … Receive Clock Shift

0:	0 bit
1:	1 bit
:	:
7:	7 bit

Reset value: RCS = 0 for path 1 and 2

TTSO … Transmit Time Slot Offset to FSC

0:	0 bit
1:	8 bit
:	:
63:	504 bit

Reset value: TTSO = 0 for path 1
TTSO = 1 for path 2

TCS … Transmit Clock Shift

0:	0 bit
1:	1 bit
:	:
7:	7 bit

Reset value: TCS = 0 for path 1 and 2

Coding and Timeslot Length

Not all combinations of the COD and TSL parameters are supported.

If the pump is configured to digital modes (V.110, PMOD = 100) PCM coding has to be disabled (COD = 000).

If the pump is configured to any of the other modes (fax, datamodem, halfduplex modulations, DTMF or DTMF transmission, PMOD = 001, 010, 011, 101 or 110) either A-law (COD = 001) or µ-law (PMOD = 010) coding is selected to output an 8-bit PCM value to the IOM-2 interface (TSL = 000). If 16-bit linear values should be provided for a codec, PCM coding is disabled (COD = 000) and timeslot length is 16 (TSL = 010).

3.8.2 IOM®-2 Configuration Setup - Path 3 (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	1	1	1	0	0	1	1	1

	15	14	13	12	11	10	9	8
CTRL MSB	DED	TIC	CED	0	0	TAD		

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DED … D-channel enable/disable
D-channel access is ...
0: disabled
1: enabled

TIC … TIC bus enable/disable
Access is performed ...
0: without TIC bus
1: with TIC bus

CED ... C/I-channel enable/disable
C/I-channel access is ...
0: disabled
1: enabled

TAD ... TIC bus address
The TIC bus address is located in the fourth octet of the third subframe on the IOM-2 DU line. It is used for the TIC-channel access procedure (if TIC=1), enabling the connection of several layer-2 D-channel protocol controllers to the IOM-2 interface.

After an IOM-2 configuration setup with D-channel enabled (DED=1), one data request message for buffer 3 will be released by the ISAR 34. Every IOM-2 configuration setup message will reset receive and transmit buffers for the D-channel (datapath 3) even if the specific configuration setting is not changed from a previous configuration (e.g. D-channel remains enabled DED=1).

When the C/I-channel is enabled by configuration setup, a first C/I Code Change message is indicated to the host with the current C/I information. Before enabling the C/I-channel (configuration setup with CED=1), both C/I codes should be programmed (see **chapter 3.6.2.7**) to ensure the right values are written to the C/I-channel from the beginning.

3.8.3 IOM®-2 Configuration Request (Host → ISAR 34)

The current configuration can be read on request by the host. The request is fully specified by the Host Interrupt Status register (HIS), i.e. the control registers and the mailbox are not used for the request command and must be set to 0.

Two types of configuration request messages are defined depending on whether the messages is addressed to a specific datapath (path 1, 2 or 3) or general information on IOM-2 configuration is requested:

- General Configuration Request:

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	0	0	0	0	1	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

- Configuration Request for Specific Channel:

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			0	0	0	1	1	1

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DPS … Datapath selection
- 01: path 1
- 10: path 2
- 11: path 3

3.8.4 IOM®-2 Configuration Response - General Code (ISAR 34 → Host)

This is the repsonse to the General Configuration Request message specified in the previous **chapter 3.8.3**.

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	0	0	1	0	1	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	--	DCL	AMO	--	--	--	--	--

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DCL … Data Clock
0: reserved for further use.
1: the bit clock on the IOM-2 interface is twice the datarate.

AMO … Awake Mode On
If this bit is set to ’1’, the awake mode is active, i.e. the DU line pulled to LOW by the ISAR 34.

*Note: Also see chapter **chapter 3.8.7** for further information.*

3.8.5 IOM®-2 Configuration Response - Path 1 and 2 (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS			1	0	0	1	1	1

	15	14	13	12	11	10	9	8
CTRL MSB	IOM	0	0	0	COD			RCV

	7	6	5	4	3	2	1	0
CTRL LSB	5							

	7	6	5	4	3	2	1	0
1. Parameter	0	0	0	TXD	RXD	TSL		

	7	6	5	4	3	2	1	0
2. Parameter	0	0	RTSO					

	7	6	5	4	3	2	1	0
3. Parameter	0	0	0	0	0	RCS		

	7	6	5	4	3	2	1	0
4. Parameter	0	0	TTSO					

	7	6	5	4	3	2	1	0
5. Parameter	0	0	0	0	0	TCS		

DPS … Datapath selection
01: path 1
10: path 2

IOM … IOM-2 data access
0: disabled
1: enabled

COD … Selected Coding
000: no PCM coding (16-bit linear data)
001: A-law coding (8-bit data)
010: μ-law coding (8-bit data)
all other codes reserved
A-law and μ-law coding is selected for all modulation related pump modes (fax, datamodem and halfduplex modulation, DTMF and DTMF transmission). For all other modes (V.110 and bypass mode) “no PCM coding” must be selected.
If "no PCM coding" is selected for modulation modes, 16-bit linear data is output on the IOM-2 interface.

RCV … Selected Rate Conversion
RCV refers to internal operation of the device and is set depending on the pump mode.
0: disabled (for all other pump modes)
1: enabled (for fax modulations, datamodem modulations, halfduplex modulations and DTMF-transmission)

TXD … Transmit path switched to
0: DD-line
1: DU-line (reset value)

RXD … Receive path switched to
0: DD-line (reset value)
1: DU-line

TSL … Timeslot length for Receive/Transmit path
00x: 8 bit wordlength (reset value)
010: 16 bit wordlength
all other codes currently not supported

RTSO … Receive Time Slot Offset to FSC
0: 0 bit
1: 8 bit
: :
63: 504 bit

Reset value: RTSO = 0 for buffer 1
RTSO = 1 for buffer 2

RCS … Receive Clock Shift

0:	0 bit
1:	1 bit
:	:
7:	7 bit

Reset value: RCS = 0 for buffer 1 and 2

TTSO … Transmit Time Slot Offset to FSC

0:	0 bit
1:	8 bit
:	:
63:	504 bit

Reset value: TTSO = 0 for buffer 1
TTSO = 1 for buffer 2

TCS … Transmit Clock Shift

0:	0 bit
1:	1 bit
:	:
7:	7 bit

Reset value: TCS = 0 for buffer 1 and 2

3.8.6 IOM®-2 Configuration Response - Path 3 (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	1	1	1	0	0	1	1	1

	15	14	13	12	11	10	9	8
CTRL MSB	DED	TIC	CED	0	0	TAD		

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DED … D-channel enable/disable
- 0: D-channel access is disabled
- 1: D-channel access is enabled

TIC … TIC bus enable/disable
- 0: Access is performed without TIC bus
- 1: Access is performed with TIC bus

CED ... C/I-channel enable/disable
- 0: C/I-channel access is disabled
- 1: C/I-channel access is enabled

TAD ... TIC bus address
Contains the programmed TIC bus address.

3.8.7 IOM®-2 Control Commands - General Code (Host → ISAR 34)

The following control commands are not related to a specific datapath but to the IOM-2 interface of the ISAR 34 in general.

Two types of command codings are differentiated regarding the interrupt status register coding (HIS) as shown below:

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	0	0	1	0	1	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	ICMD							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

ICMD … IOM-2 Control Command

20h: Set Awake Mode ON
This command will pull the DU line to LOW.

21h: Set Awake Mode OFF
This command will reset the DU line to normal functionality.

In an ISDN terminal for example the ISAR 34 can be connected to an S-transceiver (e.g. ISAC-S TE PSB 2186). For the transceiver the IOM-2 interface can be switched off in the inactive state, reducing power consumption to a minimum. In this deactivated state the clock line is low and the data lines are high.

For activation the transceiver enables the clock pulses again when the DU line is pulled low by the ISAR 34, i.e. the C/I command TIM = 0000 is received by the layer 1 device (= Set Awake Mode ON).

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS	0	0	1	0	1	0	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	ICMD							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

ICMD … IOM-2 Control Command

00h: Restart ISAR 34

If the IOM clocks are switched off (e.g. S-transceiver is in power down mode or missing clocks due to hardware malfunctions), the ISAR 34 enters a state where all datapaths are disabled. As soon as the clocks are available again, the ISAR 34 is made to leave the inactive state and to check for IOM clocks.

So this command is used to complete the power up procedure. After setting ’Awake Mode ON’ and ’Awake Mode OFF’ (see command above) the host releases the ’Restart ISAR 34’ command and the ISAR 34 will enter the normal mode of operation.

3.8.8 IOM®-2 Control Commands - Path 1 and 2 (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
HIS			1	0	1	0	1	1

	15	14	13	12	11	10	9	8
CTRL MSB	ICMD							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

DPS … Datapath selection
01: path 1
10: path 2

ICMD … IOM-2 Control Command

00h: Stop IOM-2 channel
All activities on the IOM-2 interface are frozen. In transmit direction all bits are written to “1” on the IOM-2 timeslot and in receive direction all bits received from the IOM-2 timeslot are ‘1’.

01h: Restart IOM-2 channel
After IOM-2 activities were stopped (ICMD = 00), data transfer from/to the IOM-2 timeslots is restarted again with the current configuration settings. This command must not be used before the IOM-2 interface is configured.

11h: Loop ON
Transmit data is looped back to the receiver input. In this case the configuration for the timeslot position of the receiver is without any effect.
Additionally, the transmit data itself is written to the programmed transmit timeslot if IOM-2 data access is enabled (IOM=1).
If IOM-2 data access is disabled (IOM = 0), transmit data will not be written to the IOM-2 timeslot but only looped back to the receiver input.

10h: Loop OFF
The loop of transmit data to the receiver input (activated by ICMD = 11h) is switched off. Regular read/write access to the IOM-2 is performed according to the configuration setting.

Important Note:

The control commands “Stop / Restart IOM-2 channel” have a different effect than “IOM-2 data access enable / disable” (IOM-bit) in configuration setup.
The current configuration setting is not affected by “Stop IOM-2 channel”, only transfer of user data between the pump and the IOM-2 timeslots is stopped, which is resumed by the command “Restart IOM-2 channel”.

3.8.9 IOM®-2 Status Events (ISAR 34 → Host)

The following status event is not related to a specific datapath but to the IOM-2 interface of the ISAR 34 in general.

	7	6	5	4	3	2	1	0
	DPS		MSC				MDS	
IIS	0	0	1	0	1	0	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	IEVT							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

IEVT … IOM-2 Status Event

00h: No IOM-2 Clocks

The ISAR 34 indicates that no clocks are provided on the IOM-2 interface. This may be due to the power down mode (e.g. S-transceiver switches off the clocks) or due to malfunctions of the system hardware. By releasing this message, the ISAR 34 enters an inactive state. It ceases to check for IOM clocks and it disables all datapaths, i.e. SART, pump and IOM-2 configuration are reset. However, all user data remains in the buffers and the contents of the receive buffers are sent to the host. This state can be left by the IOM-2 control command ’Restart ISAR 34’.

3.9 MONITOR Channel

The functionality of the MONITOR channel handler is available within the datapath 0, so transfer of messages and data is performed via buffer 0. As the structure of these messages is quite different from the other datapaths, MONITOR channel messges are described separately in this chapter.

Only buffer related messages are identical for all datapaths and not described here.

3.9.1 Buffer Configuration and Status

The coding for buffer configuration and status messages is described in detail in **chapters 3.1** and **3.3**. Additionally the following information should be noted:

- Transmit Buffer

The transmit buffer in datapath 0 is only used for MONITOR channel data. All other messages (host → ISAR 34) which are related to datapath 0 are immediately executed and not transferred from the mailbox to the buffer. So a command to clear transmit buffer 0 will only affect MONITOR channel data.

- Receive Buffer

The receive buffer in datapath 0 is not only used for MONITOR channel data. Besides that also other messages (e.g. messages defined for datapath 0) are transferred via buffer 0.

3.9.2 MONITOR Channel Configuration

3.9.2.1 MONITOR Channel Configuration Setup (Host → ISAR 34)

A configuration setup for MONITOR channel will clear the transmit buffer of datapath 0 but not the receive buffer (see **chapters 3.2** and **3.3**, Buffer Configuration and Status). After configuration with MONITOR channel enable (MCE=1) a data request for buffer 0 is released to the host to indicate that data can be written to the mailbox.

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	1	1	0	0	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	0	0	0	MCE

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	MAM							

	7	6	5	4	3	2	1	0
2. Parameter	MRA							

	7	6	5	4	3	2	1	0
3. Parameter	0	0	0	SLIN	CSEL			

MCE ... MONITOR channel enable/disable
MONITOR channel access is ...
0: disabled
1: enabled

NOM ... Number of valid bytes in the mailbox
If no parameters are written to the mailbox (NOM=0), the previous settings are valid. Not all parameters need to be written to the mailbox for configuration setup if the previous seetings of single parameters are valid, e.g. if SLIN and CSEL are still valid, only MAM and MRA with NOM=2 need to be programmed.

MAM ... MONITOR address mask
Every "1" in this byte marks the bit position where a check is done between the first byte of a received MONITOR data frame and the reference address (MRA). The received MONITOR address will additionally be transferred to the host as the first data byte (see **chapter 3.9.3.1**).

MRA ... MONITOR reference address
This is the reference address for the comparison with the first byte of a received MONITOR data frame. The bit positions which are not marked with a "1" in MAM are don’t care.

SLIN ... Serial line interface switching
Defines the switching of TX/RX data on DU/DD lines.
0: Transmit data on DU, Receive data from DD
1: Transmit data on DD, Receive data from DU

CSEL ... IOM-2 channel Select
Selects one of up to 16 channels on the IOM-2 interface. The MONITOR channel is always the 3rd timeslot in an IOM channel.
0000: channel 0
0001: channel 1
: :
1110: channel 14
1111: channel 15

3.9.2.2 MONITOR Channel Configuration Request (Host → ISAR 34)

The current configuration setting can be requested by the host.

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	0	1	0	0	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

3.9.2.3 MONITOR Channel Configuration Response (ISAR 34 → Host)

The current configuration setting is returned by the ISAR 34 on request. The coding is similar as for the configuration setup message (**chapter 3.9.2.1**).

	7	6	5	4	3	2	1	0
	DPS		MSC					
IIS	0	0	1	1	0	0	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	0	0	0	0	0	0	0	MCE

	7	6	5	4	3	2	1	0
CTRL LSB	3							

	7	6	5	4	3	2	1	0
1. Parameter	MAM							

	7	6	5	4	3	2	1	0
2. Parameter	MRA							

	7	6	5	4	3	2	1	0
3. Parameter	0	0	0	SLIN	CSEL			

3.9.3 MONITOR Channel Data

3.9.3.1 MONITOR Channel Receive Data (ISAR 34 → Host)

	7	6	5	4	3	2	1	0
	DPS		MSC					
IIS	0	0	1	1	0	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	-	MED	MSD	-	-	-	-	-

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	1st databyte of the message							

	7	6	5	4	3	2	1	0
N. Parameter	N-th databyte of the message							

A status information is valid if the corresponding bit is set to "1":

MED ... Message End Detected
The end of a MONITOR channel message is detected.

MSD ... Message Start Detected
The start of a MONITOR channel message is detected. The MONITOR address byte is provided as the first data byte in the mailbox.

NOM ... Number of Valid Bytes in the Mailbox
Indicates the number N of valid data bytes to be read from the mailbox.

The end of a MONITOR message may be detected by the ISAR 34 some time after the last data byte was received and transferred to the host. Therefore, it may occur that the end of a message is indicated in a message without valid data bytes (NOM=0) and the last data byte of that MONITOR message was transferred to the host with the previous receive data message.

3.9.3.2 MONITOR Channel Transmit Data (Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	1	1	0	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	0	MED	MSD	0	0	0	0	0

	7	6	5	4	3	2	1	0
CTRL LSB	NOM							

	7	6	5	4	3	2	1	0
1. Parameter	1st databyte of the message							

	7	6	5	4	3	2	1	0
N. Parameter	N-th databyte of the message							

A status information is valid if the corresponding bit is set to "1":

MED ... Message End
The last byte written to the mailbox with this message is the last byte of the MONITOR message.

MSD ... Message Start
The first byte written to the mailbox represents the beginning of the MONITOR message and is defined as the MONITOR address byte.

NOM ... Number of Valid Bytes in the Mailbox
Indicates the number N of valid data bytes written to the mailbox.

3.9.3.3 MONITOR Channel Status Events (ISAR 34 → Host)

The following status events are released by the ISAR 34 to indicate certain conditions related to the MONITOR channel.

	7	6	5	4	3	2	1	0
	DPS		MSC					
IIS	0	0	1	1	0	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	MEVT							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

MEVT ... MONITOR Channel Event
Contains one of the following events from the MONITOR channel:

10h: Message Abort
The ISAR 34 has detected an abort from the receiver. All messages in the transmit buffer will be deleted.

20h: Message Complete
The receiver has acknowledged the MONITOR message.

3.10 GPIO (General Purpose I/Os)

There are 9 general purpose I/Os available in ISAR 34 that are free programmable by host messages. They can be configured as:

- Input or Output
- Open Drain or Push Pull
- Continous or strobed sampling
- Interrupt masked or unmasked

3.10.1 GPIO Configuration

3.10.1.1 GPIO Configuration - Output Register Set/Reset (Host → ISAR 34)

The output register contains output values for all 9 GPIO pins. If a GPIO pin is configured as input (see below) the corresponding bit is ignored. For all GPIOs that are configured as output, the register reflects the value.

After reset, all GPIOs are input. To achieve glitch-free output value after reset, you may write the output register first and then configure the corresponding pin(s) as output. The previously programmed value will then be output to the line.

The GPIOs can be set or reset or left unaffected with the following command.

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	4							

	7	6	5	4	3	2	1	0
1. Parameter	R(7:0)							

	7	6	5	4	3	2	1	0
2. Parameter	0	0	0	0	0	0	0	R8

	7	6	5	4	3	2	1	0
3. Parameter	S(7:0)							

	7	6	5	4	3	2	1	0
4. Parameter	0	0	0	0	0	0	0	S8

R(8:0) ... Reset GPIO
- 0: The corresponding GPIO is unaffected
- 1: The corresponding GPIO is reset to 0

S(8:0) ... Set GPIO

0: The corresponding GPIO is unaffected

1: The corresponding GPIO is set to 1

Setting and resetting a GPIO in one command must be avoided.

The reset value of the output register is 0.

3.10.1.2 GPIO Configuration - Direction (Host → ISAR 34)

The GPIO direction can be set to input or output or left unaffected with the following command.

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	10h							

	7	6	5	4	3	2	1	0
CTRL LSB	4							

	7	6	5	4	3	2	1	0
1. Parameter	IN(7:0)							

	7	6	5	4	3	2	1	0
2. Parameter	0	0	0	0	0	0	0	IN8

	7	6	5	4	3	2	1	0
3. Parameter	OUT(7:0)							

	7	6	5	4	3	2	1	0
4. Parameter	0	0	0	0	0	0	0	OUT8

IN(8:0) ... Set GPIO to input
- 0: The corresponding GPIO is unaffected
- 1: The corresponding GPIO is set to input (reset)

OUT(8:0) ... Set GPIO to output
- 0: The corresponding GPIO is unaffected
- 1: The corresponding GPIO is set to output

Setting a GPIO to input and output in one command must be avoided.

The reset value of the direction register is input.

3.10.1.3 GPIO Configuration - Open Drain Select (Host → ISAR 34)

The GPIO pins can be set to open drain or push/pull or left unaffected with the following command.

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	20h							

	7	6	5	4	3	2	1	0
CTRL LSB	4							

	7	6	5	4	3	2	1	0
1. Parameter	OD(7:0)							

	7	6	5	4	3	2	1	0
2. Parameter	0	0	0	0	0	0	0	OD8

	7	6	5	4	3	2	1	0
3. Parameter	PP(7:0)							

	7	6	5	4	3	2	1	0
4. Parameter	0	0	0	0	0	0	0	PP8

OD(8:0) ... Set GPIO to open drain
- 0: The corresponding GPIO is unaffected
- 1: internal pullup enabled, GPIO outputs are open drain (reset)

PP(8:0) ... Set GPIO to output
- 0: The corresponding GPIO is unaffected
- 1: internal pullup disabled, GPIO outputs are push/pull

Setting a GPIO to open drain and push/pull in one command must be avoided.

The reset value of the GPIOs is open drain.

When open drain is selected the internal pullup is enabled even if the GPIO is configured as input.

3.10.1.4 GPIO Configuration - Strobed Input (Host → ISAR 34)

The read values of the GPIO pins can be sampled continously (default) or in strobed mode. In the latter case pin 0 must be input and provides the strobe signal. For all other pins strobed mode can be individually enabled. If enabled, the pins are only sampled during pin 0 is low. State changes are ignored during pin 0 is high.

The strobed input mode can be set or reset or left unaffected with the following command.

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	30h							

	7	6	5	4	3	2	1	0
CTRL LSB	4							

	7	6	5	4	3	2	1	0
1. Parameter	C(7:0)							

	7	6	5	4	3	2	1	0
2. Parameter	0	0	0	0	0	0	0	C8

	7	6	5	4	3	2	1	0
3. Parameter	S(7:0)							

	7	6	5	4	3	2	1	0
4. Parameter	0	0	0	0	0	0	0	S8

C(0) ... Enable continous sampling
- 0: The corresponding GPIO is unaffected
- 1: Continous sampling is enabled (reset)

C(8:1) ... Set GPIO to continous sampling
- 0: The corresponding GPIO is unaffected
- 1: The corresponding GPIO is continously sampled (reset)

S(0) ... Enable strobed mode sampling
- 0: The corresponding GPIO is unaffected
- 1: Strobed mode sampling is enabled

S(8:1) ... Set GPIO to strobed mode sampling
- 0: The corresponding GPIO is unaffected
- 1: The corresponding GPIO is sampled in strobed mode if strobed mode is enabled (S(0)=1)

Setting a GPIO to continous and strobed sampling in one command must be avoided.

The reset value of the GPIOs is continous sampling.

3.10.1.5 GPIO Configuration - Interrupt Mask (Host → ISAR 34)

This command configures the general purpose pins which will send an event automatically when a state change is detected. When the interrupt mask is enabled for more than one pin, the host has to figure out which pin caused the event by comparing the new read status with the last one.

The GPIO interrupts can be masked or unmasked or left unaffected with the following command.

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	40h							

	7	6	5	4	3	2	1	0
CTRL LSB	4							

	7	6	5	4	3	2	1	0
1. Parameter	RM(7:0)							

	7	6	5	4	3	2	1	0
2. Parameter	0	0	0	0	0	0	0	RM8

	7	6	5	4	3	2	1	0
3. Parameter	SM(7:0)							

	7	6	5	4	3	2	1	0
4. Parameter	0	0	0	0	0	0	0	SM8

RM(8:0) ... Reset GPIO interrupt mask
- 0: The corresponding GPIO is unaffected
- 1: GPIO interrupt mask is enabled, interrupt is disabled (reset)

SM(8:0) ... Set GPIO interrupt mask
- 0: The corresponding GPIO is unaffected
- 1: GPIO interrupt mask is disabled, interrupt is enabled

Setting and resetting a GPIO interrupt mask in one command must be avoided.

The reset value of the GPIO interrupts masks is 0 (interrupts disabled).

3.10.2 GPIO Status

3.10.2.1 GPIO Status Request (Host → ISAR 34)

The host requests the GPIO status. The real status at the output pin is returned, independent of whether the pin is configured as input or output. When an output pin is configured as open drain, the status value may be different from the output value ("wired AND").

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	0	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

3.10.2.2 GPIO Status Event/Response (ISAR 34 → Host)

The GPIO status may be an event or a response, depending on configuration.

When the interrupt of a general purpose pin is enabled (IMx=1) and the corresponding status changes, the new status of all 9 pins is reported to the host as a Status Event.

Independent of that the host may send a Status Request (see above). As a consequence the ISAR 34 will report the current status as a Status Response.

Note: GPIO pins are sampled on a 10 msec basis. Thus, the maximum switching frequency on a GPIO should be less than 50 Hz (maximum observable switching frequency).

	7	6	5	4	3	2	1	0
	DPS		MSC					
IIS	0	0	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	ST(7:0)							

	7	6	5	4	3	2	1	0
2. Parameter	x	x	x	x	x	x	x	ST8

ST(8:0) ... Reflects the current status of the general purpose pin.

x ... Don’t care, maybe 1 or 0.

3.11 Test/Diagnostics Path

The test/diagnostics path is used for test and diagnostics, general configuration and control (not related to a specific data path) and as an answer channel for certain status/ configuration requests to the data channels.

3.11.1 Timer Interrupt On/Off(Host → ISAR 34)

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	1	0	0	1	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	CMD							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

CMD … Command for general configuration
20h: Timer interrupt off
21h: Timer interrupt on
If enabled, a 10 ms timer interrupt is generated to the host. This can be used for certain driver software implementations that require hardware interrupts. As this is normally used in applications with data modulations, the interrupt request message is coded as a message related to buffer 1 (see **chapter 3.11.2**), however, it can be used for purposes within other buffers, too.
Using the timer interrupt increases the message load between the ISAR 34 and the host significantly.

3.11.2 Timer Interrupt Event (ISAR 34 → Host)

The “Timer Interrupt Event” message is generated once per 10 ms if enabled by the “General Configuration” message in **chapter 3.11.1**.

	7	6	5	4	3	2	1	0
	DPS		MSC					
IIS	0	1	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	EVTL							

	15	14	13	12	11	10	9	8
2. Parameter	–	–	–	–	–	EVTH		

EVT ... Timer Interrupt Event (EVTH, EVTL)
002h: 10 ms timer interrupt
Depending on the selected mode other pump mode specific events may be released to the host.

3.11.3 Chip Version Request (Host → ISAR 34)

The host can request the version number of the chip by the following request message.

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	1	0	0	1	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

3.11.4 Chip Version Response (ISAR 34 → Host)

The ISAR 34 returns the version number of the chip if requested by the host.

	7	6	5	4	3	2	1	0
	DPS		MSC					
IIS	0	0	1	0	0	1	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	0							

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	CVNL							

	15	14	13	12	11	10	9	8
2. Parameter	CVNH							

CVN … Chip Version Number (CVNH, CVNL)

0101h: ISAR 34 Version 2.1
all other codes currently not supported.

Important Note:

The chip version request and response messages are only valid after a hardware reset. These messages must not be used after the firmware download.

3.11.5 Software Version Request (Host → ISAR 34)

The host can request the version number of the DSP software by the following request message.

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	0	0	0	1	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	10h							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

3.11.6 Software Version Response (ISAR 34 → Host)

The ISAR 34 returns the version number of the DSP software if requested by the host.

	7	6	5	4	3	2	1	0
	DPS		MSC					
IIS	0	0	1	0	0	1	0	1

	15	14	13	12	11	10	9	8
CTRL MSB	10h							

	7	6	5	4	3	2	1	0
CTRL LSB	2							

	7	6	5	4	3	2	1	0
1. Parameter	SVNL							

	7	6	5	4	3	2	1	0
2. Parameter	SVNH							

SVN … Software Version Number (SVNH, SVNL)
Contains the version number of the DSP software on the device:

0101h: Version 1.01
all other codes currently not supported.

3.11.7 Request Selftest Result (ISAR 34 → Host)

After download of the DSP program the ISAR 34 automatically performs a selftest, which will check for memory errors or missing IOM-2 clocks.

The result of the selftest can be requested by the host and possible error conditions are contained in the “Selftest Response” message (see **chapter 3.11.8**).

	7	6	5	4	3	2	1	0
	DPS		MSC					
IIS	0	0	0	0	0	1	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	40h							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

3.11.8 Selftest Response (ISAR 34 → Host)

The selftest result requested by the host (see **chapter 3.11.7**) will result in a response message containing information about possible error conditions.

	7	6	5	4	3	2	1	0
	DPS		MSC					
IIS	0	0	1	0	0	1	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	40h							

	7	6	5	4	3	2	1	0
CTRL LSB	1							

	7	6	5	4	3	2	1	0
1. Parameter	0	0	PRO	DRO	PRR	MB1	MB0	PLL

PRO ... Program ROM error

DRO ... Data ROM error

PRR … Program RAM error

MB1 … Internal memory error (bank 1)

MB0 … Internal memory error (bank 0)

PLL … PLL initialization error

3.11.9 Soft Reset (Host → ISAR 34)

The soft reset has a similar function as the hardware reset or power on reset. All configuration settings are reset and the buffers are cleared.

	7	6	5	4	3	2	1	0
	DPS		MSC					
HIS	0	0	1	0	1	0	0	0

	15	14	13	12	11	10	9	8
CTRL MSB	RCMD							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

RCMD … Reset Command

40h: Soft reset, if DCL=0 (currently not supported)
41h: Soft reset, if DCL=1

The command coding for the soft reset depends on the setting of the DCL parameter which can be read by a general IOM-2 configuration request message (see **chapter 3.8.3**). The value of DCL is returned by the corresponding IOM-2 configuration response message (see **chapter 3.8.4**).
The ISAR 34 currently supports DCL=1 and RCMD=41h.

3.11.10 Invalid Message Received (ISAR 34 → Host)

If the host issues a message to the ISAR 34 with an HIS coding that is not specified, the ISAR 34 will respond with the following error message to indicate that an invalid message coding was detected.

	7	6	5	4	3	2	1	0
	DPS		MSC					
IIS	0	0	1	1	1	1	1	1

	15	14	13	12	11	10	9	8
CTRL MSB	INV							

	7	6	5	4	3	2	1	0
CTRL LSB	0							

INV … Invalid HIS coding
Contains the invalid HIS register coding of the message which was released by the host.

3.12 DSP Program Download

In the ISAR 34 PSB 7115 V2.1 the DSP program is downloaded through the host interface into the external memory. The binary file that includes the DSP program is provided together with the device.

The data structure within the file is shown in **figure 45**.

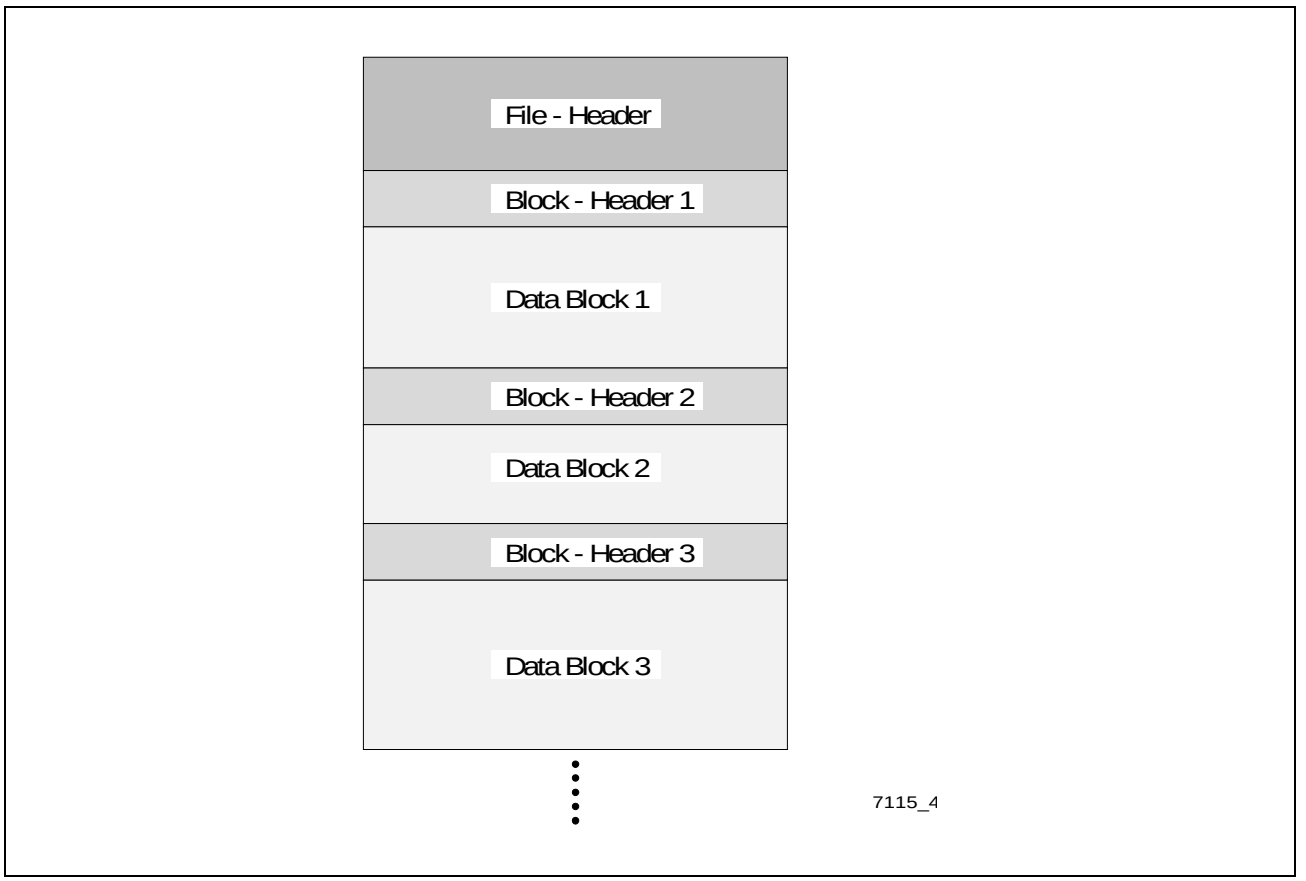


Figure 45 Binary File Structure

The file is devided into a file header and a number of individual data blocks, each of which is preceeded by a block header.

The file header contains general information such like file type identifier and version number. One data field contains the pointer BLOCK_PTR to the first block header (**figure 46**). The block header defines the type of data contained in the subsequent data block, which implies the host to perform a certain action (e.g. read/write data from/to the ISAR 34, compare received message with given data, ...).

The data block contains the detailed information that is required by the host to perform that action. This includes complete message codings, data which transferred to the ISAR 34 and message codings for comparison of received messages. If the current data block is finished, a pointer (NEXT_PTR) indicates to the start of the next block header. For certain types of data blocks a decision is made by the host so one of two pointers

(TRUE_PTR or FALSE_PTR) is finally selected. If a timeout condition is specified for a data block the next valid block in case of a time out condition is indicated by TIMEOUT_PTR.

All pointers are specified with respect to the beginning of the file.

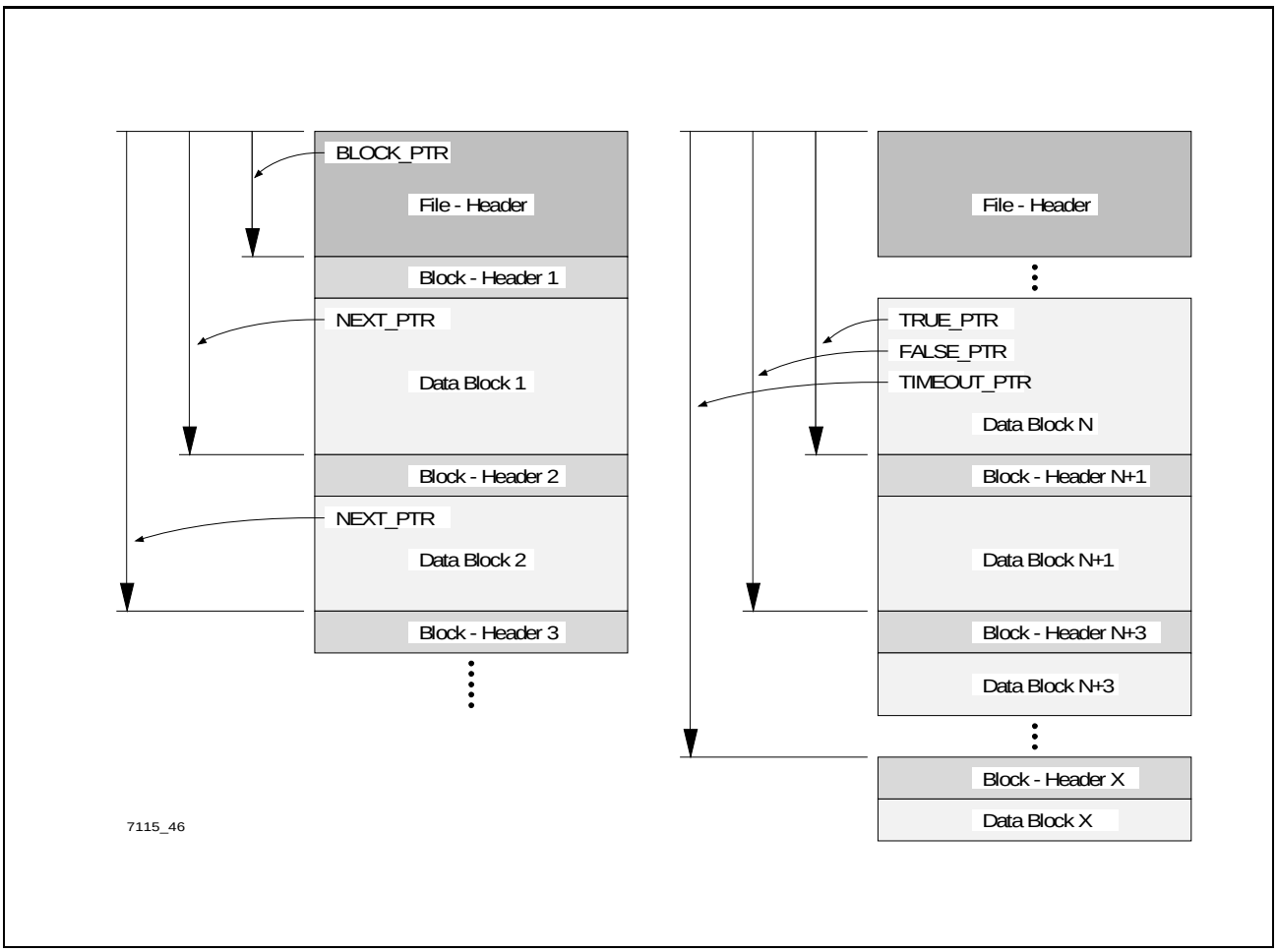


Figure 46 Pointer on Data Structures

The following chapters show all details for the complete download mechanism.

First the structure of the file header and the main routine for the program download is described.

Then follows the different types of block headers and how block headers must be be handled in general.

The different block types are covered in separate chapters with flow charts that show how the host has to process the block data.

3.12.1 Structure of File Header

The structure and contents of the file header are shown in **table 14**.

Certain fields of data must be checked by the host. These are the file identification number (FILE_ID), the product identification number (PRODUCT_ID) which must be within the given range and the block pointer (BLOCK_PTR) that indicates the beginning of the first block header.

Other data fields contain optional information that can be neglected such like the version number (VERSION_NO), the name of the device (PRODUCT_NAME), the manufacturer identification (MANUFCT_ID), the header extension pointer (HEAD_EXT_PTR) and the timestamp of the file in PC format (TIMESTAMP).

Table 13 Structure of File Header

Offset	Type	Field	Contents
0	byte [16]	FILE_ID	"ZNELEKRE_HCIRLU\00"
16	byte [16]	VERSION_NO	"Version_01.00_\00"
32	byte [16]	PRODUCT_NAME	"ISAR_34,_V2.1_\00"
48	byte [64]	MANUFCT_ID	"Copyright_1997,_Siemens_AG_\00"
112	dword [1]	PRODUCT_ID	00000010_H ... 00000015_H
116	dword [1]	HEAD_EXT_PTR	00000000_H
120	dword [1]	TIMESTAMP	
124	dword [1]	BLOCK_PTR	

Note: The offset of the individual data fields is indicated in bytes and decimal notation. The sequence of bytes for the field types "word" and "dword" within the binary file is least significant byte first.
A blank space in the column "Contents" is marked by an underscore "_". If the maximum length of the field is not used, the string is terminated by a zero byte (\00).

As already mentioned in the previous chapter, the parameter BLOCK_PTR points to the beginning of the first block header with respect to the beginning of the file.

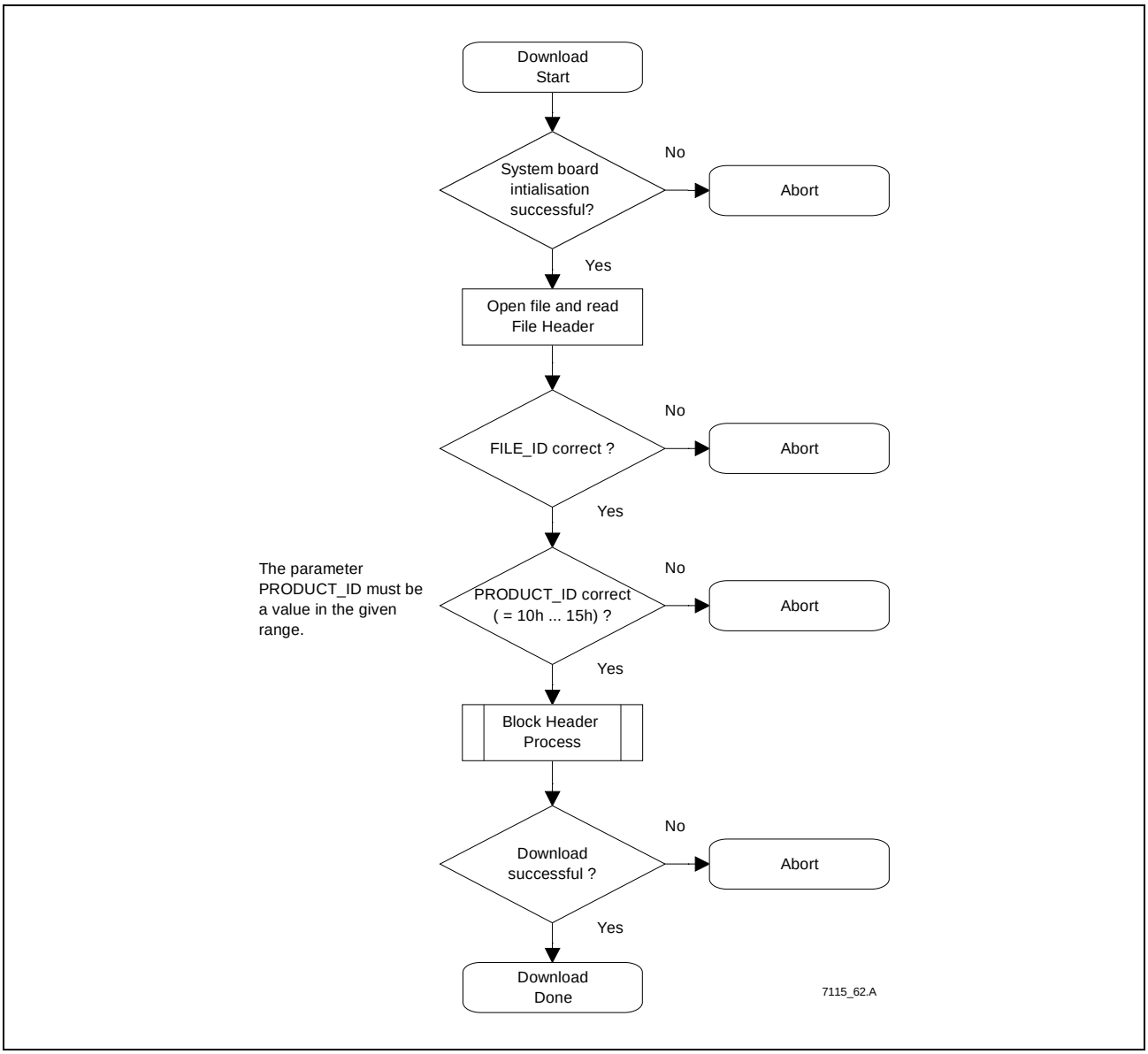


Figure 47 Download Process

3.12.2 Structure of Block Header

The structure and contents of the block header are shown in **table 14**.

The block header is directly followed by the data block. The type of data contained in there is specified in the first data field BLOCK_TYPE of the block header. All BLOCK_TYPE codings for this version are listed in **table 15** and described in detail in the following chapters.

If the host reads a BLOCK_TYPE parameter which is not described in this specification, the data block should be ignored and the next block header pointed to by UNKNOWN_PTR should be read.

Table 14 Structure of Block Header

Offset	Type	Field	Contents
0	dword [1]	BLOCK_TYPE	(see **table 15**)
4	dword [1]	UNKNOWN_PTR	

The following types of data blocks must be evaluated by the host. All other codings are reserved and should be ignored (see UNKNOWN_PTR).

Table 15 Types of Data Blocks

BLOCK_TYPE	Function
00000001_H	Jump to a specific block.
00000002_H	Write message to the ISAR 34.
00000003_H	Wait for next message from the ISAR 34.
00000004_H	Wait for a specific message from the ISAR 34.
00000005_H	Compare the last received message with given message coding.
00000006_H	Set coding information.
00000007_H	Set status information.
00000020_H	Write internal data memory.
00000021_H	Write internal program memory.
00000030_H	Write external data memory.
00000031_H	Write external program memory.

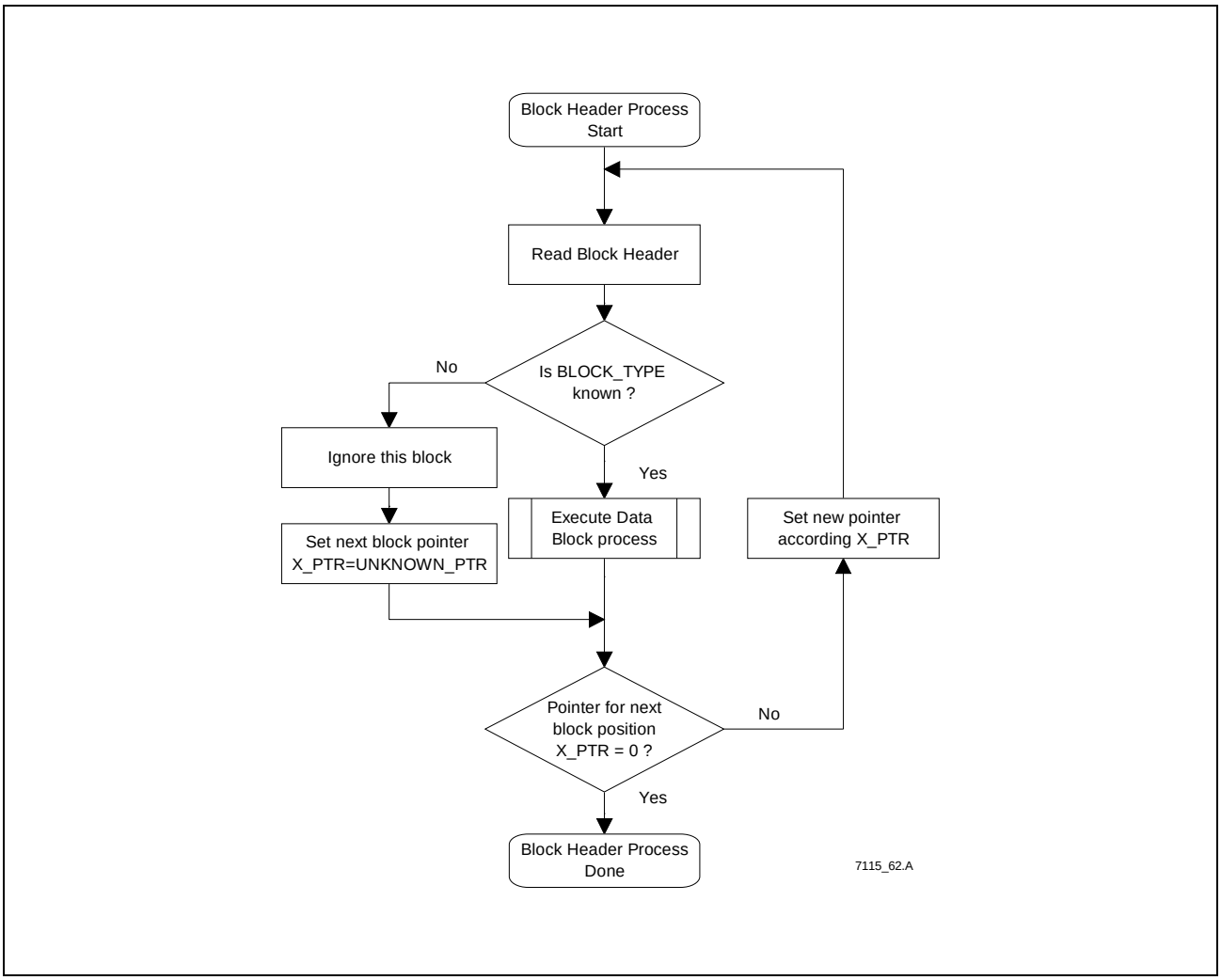


Figure 48 Block Header Process

The pointer for the next block position (XXXX_PTR) is determined depending on the type of the current data block. The new pointer can be defined as NEXT_PTR, TRUE_PTR, FALSE_PTR or TIMEOUT_PTR.

3.12.3 Structure of Data Blocks

The data blocks directly follow the block header. The type of data block is indicated by the BLOCK_TYPE parameter in the block header. The length of a data block can be fixed or variable, in the latter case a criteria is given in the specific data block for the block end.

The structure and contents of the individual data blocks are described in the following chapters. A detailed description on how the host should treat each block is shown in a flow chart diagram. If the host is told to read or write a message from/to the ISAR 34 the general mechanisms for message transfer should be used as during normal operation mode (see **chapter 3.1**).

3.12.3.1 Jump to Block

This data structure contains a single parameter. The host is told to jump to the next data block which is indicated by the pointer NEXT_PTR.

Table 16 Block Structure - BLOCK_TYPE = 1_H

Offset	Type	Field
0	dword [1]	NEXT_PTR

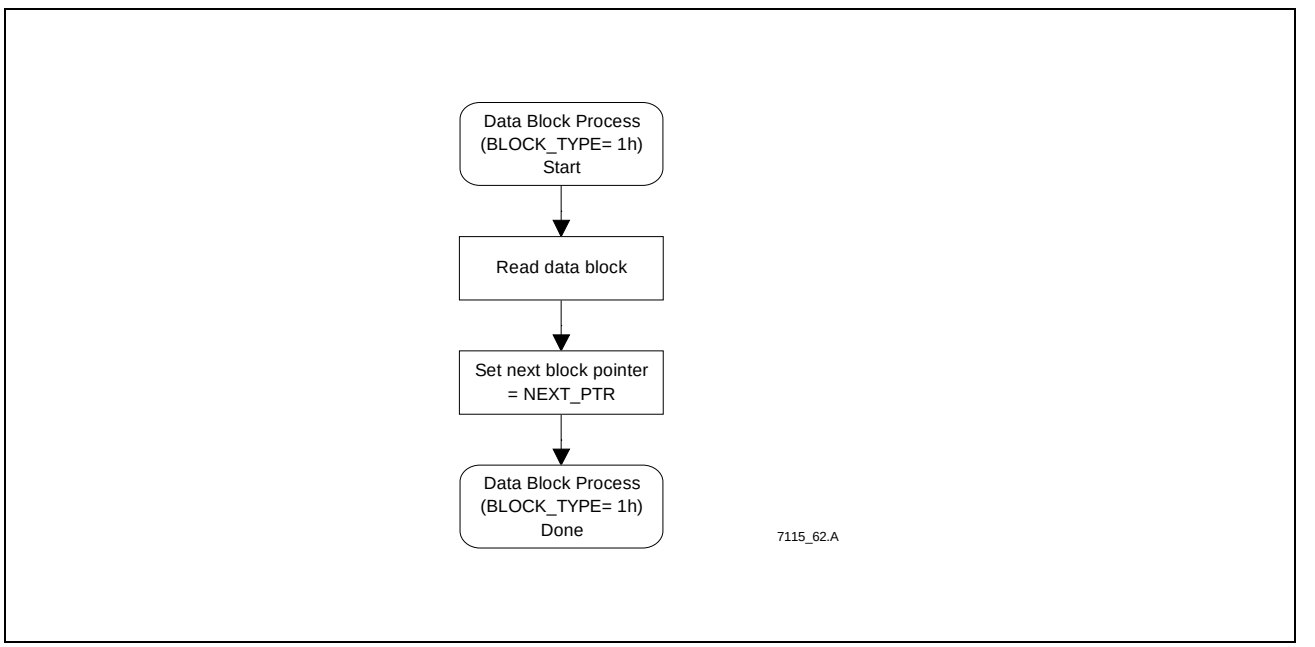


Figure 49 Data Block Process - Jump to Block

3.12.3.2 Write Message

This data block tells the host to write a message to the ISAR 34. The complete message coding is given in the data block. The coding for each of the message parameters is given in 16-bit words, however the MSB is don't care and only the LSB is valid and written to the ISAR 34.

The number of bytes (length of parameter MBOX) which are written to the ISAR 34 mailbox are indicated by the parameter CTRL_LSB, so the length of the complete data block is not fixed but depends on the length of the MBOX field.

If the message is successfully written to the ISAR 34, the host jumps to the next block indicated by NEXT_PTR.

If the mailbox is not released by the ISAR 34 within a specified time (parameter TIMEOUT) the host proceeds with the next block indicated by TIMEOUT_PTR. Both parameters are not given in this data block, but they are global variables (see **chapter 3.12.3.6**).

Table 17 Block Structure - BLOCK_TYPE = 2_H

Offset	Type	Field
0	dword [1]	NEXT_PTR
4	word [1]	HIS
6	word [1]	CTRL_MSB
8	word [1]	CTRL_LSB
10	word [n]	MBOX

Note: For the data fields HIS, CTRL_MSB, CTRL_LSB and MBOX only the LSB values are evaluated. The MSBs are don't care.
The length of the MBOX field n is determined by CTRL_LSB.

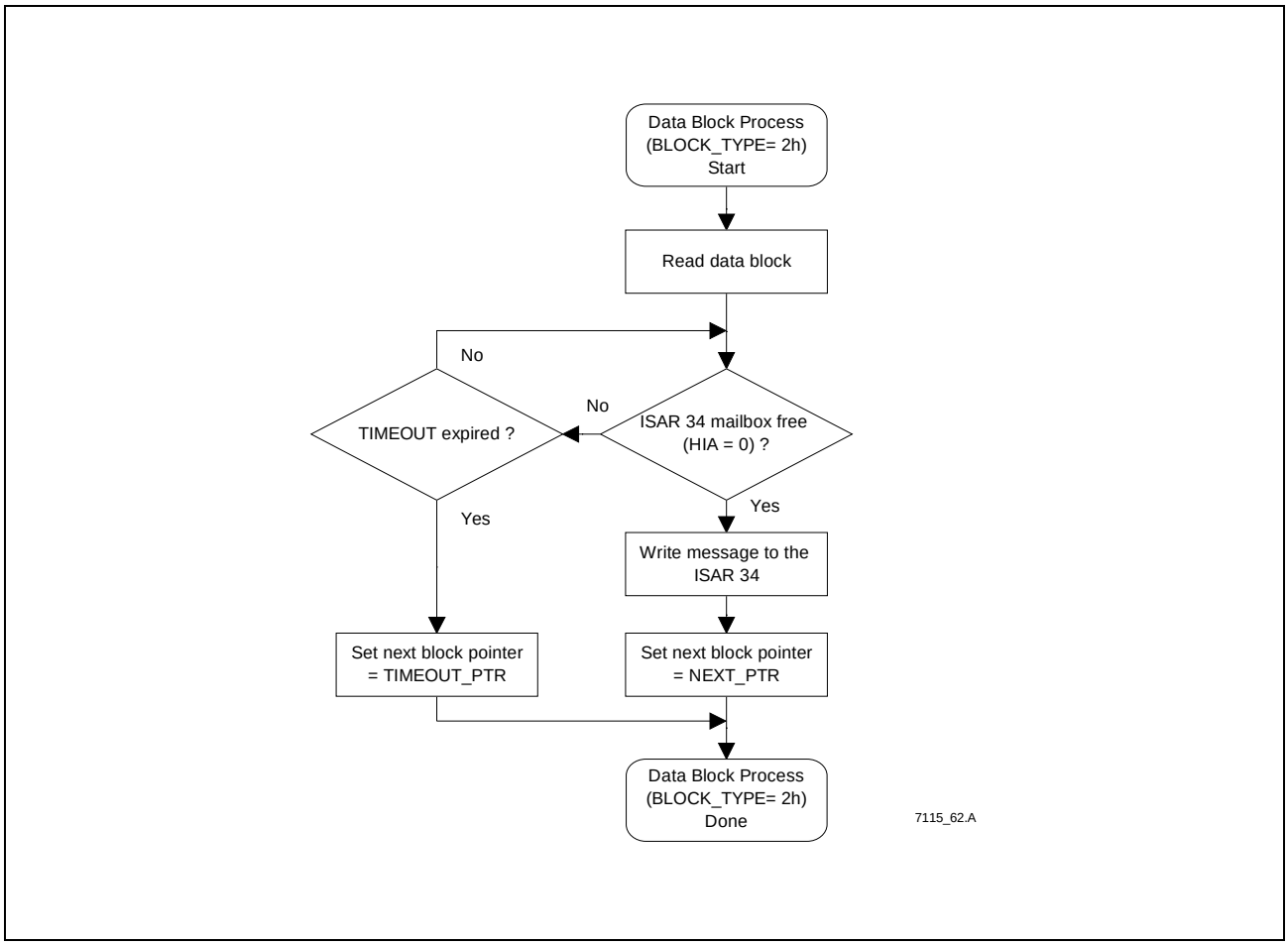


Figure 50 Data Block Process - Write Message

3.12.3.3 Wait for Next Message

The next message that is received from the ISAR 34 is evaluated by the host. If this message is identical to the message coding given in the data block, then the host jumps to the block indicated by TRUE_PTR.

If the message coding is different, the next block to be processed by the host is indicated by FALS_PTR.

In case this message is not received within a specified time (parameter TIMEOUT) the host proceeds with the next block indicated by TIMEOUT_PTR. Both parameters are not given in this data block, but they are global variables (see **chapter 3.12.3.6**).

Table 18 Block Structure - BLOCK_TYPE = 3_H

Offset	Type	Field
0	dword [1]	TRUE_PTR
4	dword [1]	FALSE_PTR
8	word [1]	IIS
10	word [1]	CTRL_MSB
12	word [1]	CTRL_LSB
14	word [n]	MBOX

Note: For the data fields IIS, CTRL_MSB, CTRL_LSB and MBOX only the LSB values are evaluated. The MSBs are don't care.
The length of the MBOX field n is determined by CTRL_LSB.

Received messages must always be stored by the host (see **chapter 3.12.3.5**).

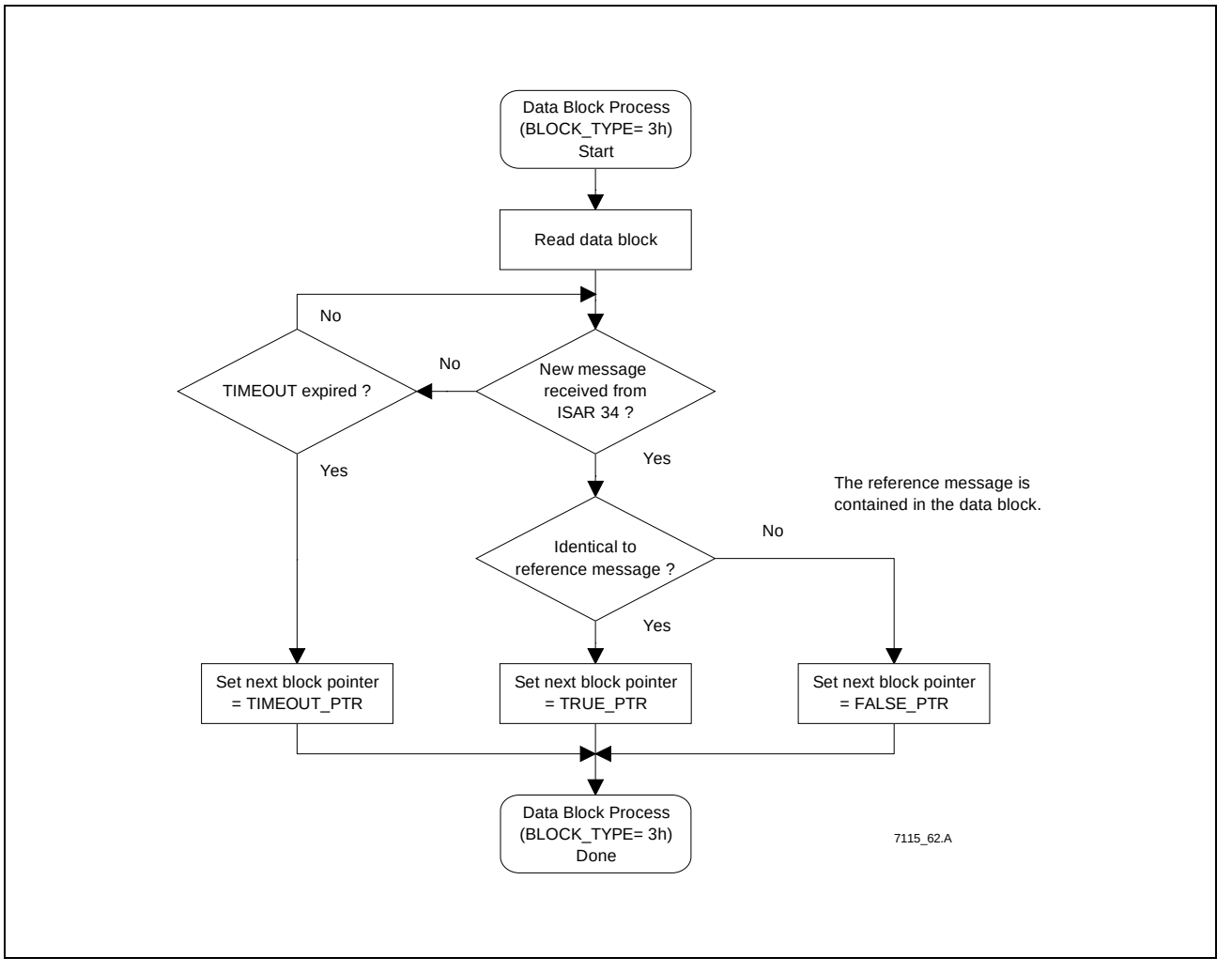


Figure 51 Data Block Process - Wait for Next Message

3.12.3.4 Wait for Specific Message

The host compares all messages received from the ISAR 34 with the message coding given in the data block. If the required message is received, the host proceeds with the next block indicated by TRUE_PTR. All other messages are discarded.

If this message is not received within a specified time (parameter TIMEOUT) the host proceeds with the next block indicated by TIMEOUT_PTR. Both parameters are not given in this data block, but they are global variables (see **chapter 3.12.3.6**).

Table 19 Block Structure - BLOCK_TYPE = 4_H

Offset	Type	Field
0	dword [1]	TRUE_PTR
4	word [1]	IIS
6	word [1]	CTRL_MSB
8	word [1]	CTRL_LSB
10	word [n]	MBOX

Note: For the data fields IIS, CTRL_MSB, CTRL_LSB and MBOX only the LSB values are evaluated. The MSBs are don't care.
The length of the MBOX field n is determined by CTRL_LSB.

Received messages must always be stored by the host (see **chapter 3.12.3.5**).

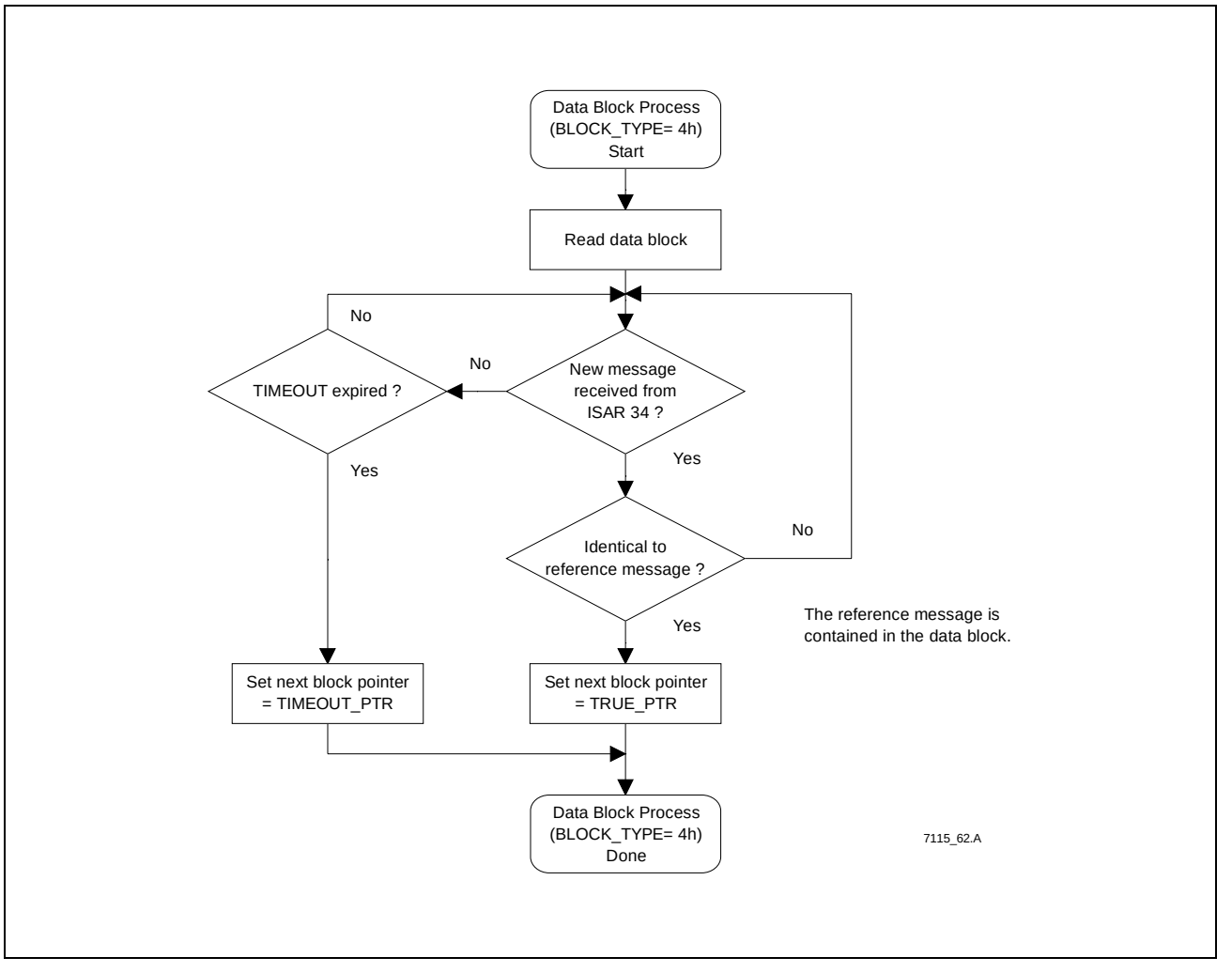


Figure 52 Data Block Process - Wait for Specific Message

3.12.3.5 Compare Last Message

Generally, during the download procedure the host always has to store the last message received from the ISAR 34. A new message will always overwrite the previous one.

In contrast to the last two chapters where the host waits for new messages, here the host compares the last message received from the ISAR 34 with the given message coding in the data block.

If this message is identical to the given message coding the host jumps to the block indicated by TRUE_PTR. If the message coding is different, the next block to be processed by the host is indicated by FALS_PTR.

Table 20 Block Structure - BLOCK_TYPE = 5_H

Offset	Type	Field
0	dword [1]	TRUE_PTR
4	dword [1]	FALSE_PTR
8	word [1]	IIS
10	word [1]	CTRL_MSB
12	word [1]	CTRL_LSB
14	word [n]	MBOX

Note: For the data fields IIS, CTRL_MSB, CTRL_LSB and MBOX only the LSB values are evaluated. The MSBs are don't care.
The length of the MBOX field n is determined by CTRL_LSB.

To store messages from the ISAR 34 the host should be prepared to store up to 256 byte of data from the mailbox (MBOX).

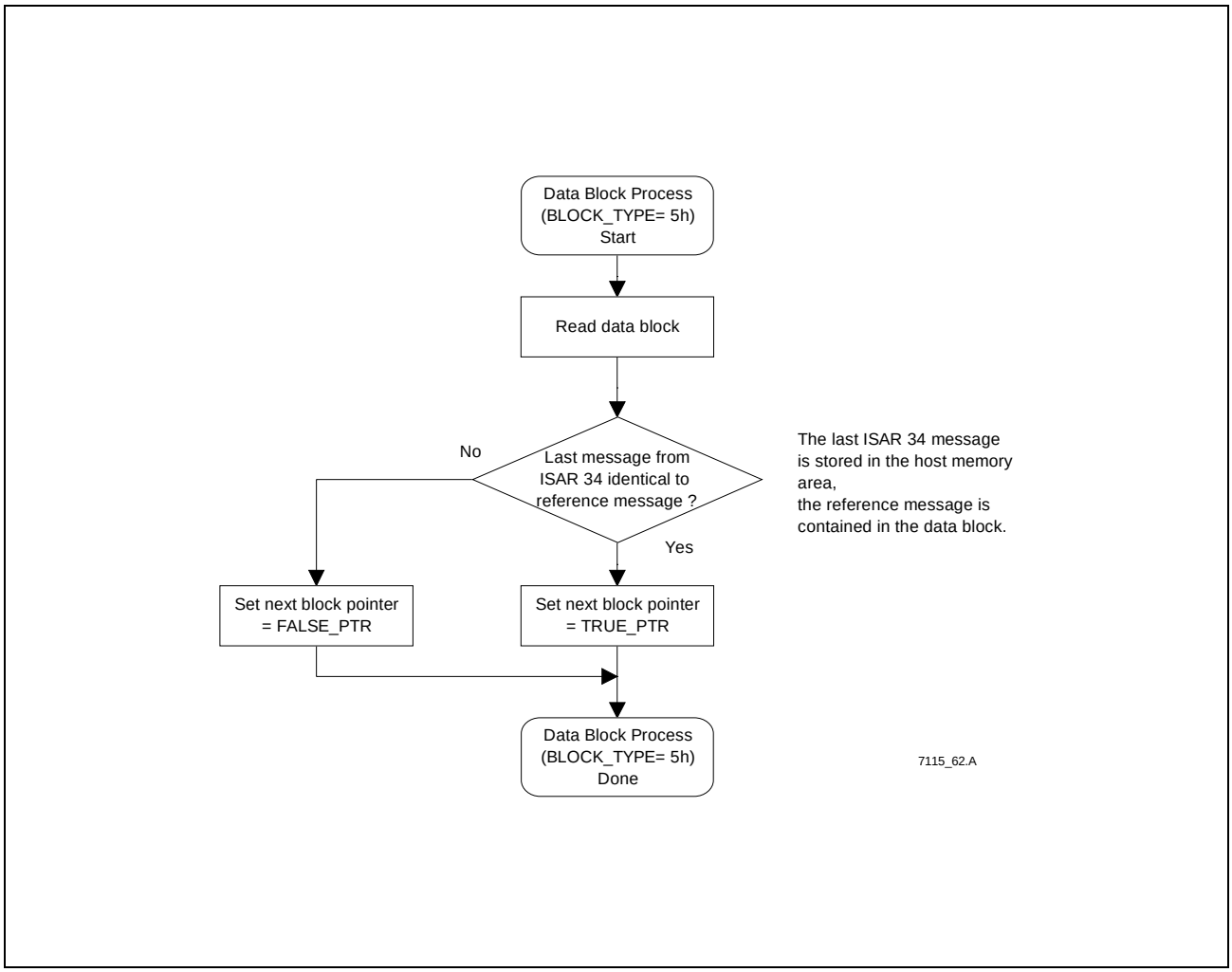


Figure 53 Data Block Process - Compare Last Message

3.12.3.6 Set Coding Information

During the download procedures four global variables (TIMEOUT_PTR, TIMEOUT, HIS and CTRL_MSB) are used for some of the data blocks.

If a parameter (e.g. HIS or CTRL_MSB) is not specified as a local variable in a specific data block, the parameter setting from the global variable is to be used. These global variables are initialized by the host when the procedures are started and they are modified when this data block occurs. The global variables are used by the data blocks BLOCK_TYPE = 20_H, 21_H, 30_H and 31_H.

Some data blocks make use of a timer. The timeout value is specified in milliseconds [ms] by TIMEOUT. If a timeout condition occurs the host jumps to the next data block indicated by TIMEOUT_PTR.

After the four variables are set the host jumps to the next block indicated by NEXT_PTR.

Table 21 Block Structure - BLOCK_TYPE = 6_H

Offset	Type	Field	Initial value:
0	dword [1]	NEXT_PTR	
4	dword [1]	TIMEOUT_PTR	0
8	dword [1]	TIMEOUT	0400_H (= 1024 ms)
12	word [1]	HIS	0
14	word [1]	CTRL_MSB	0

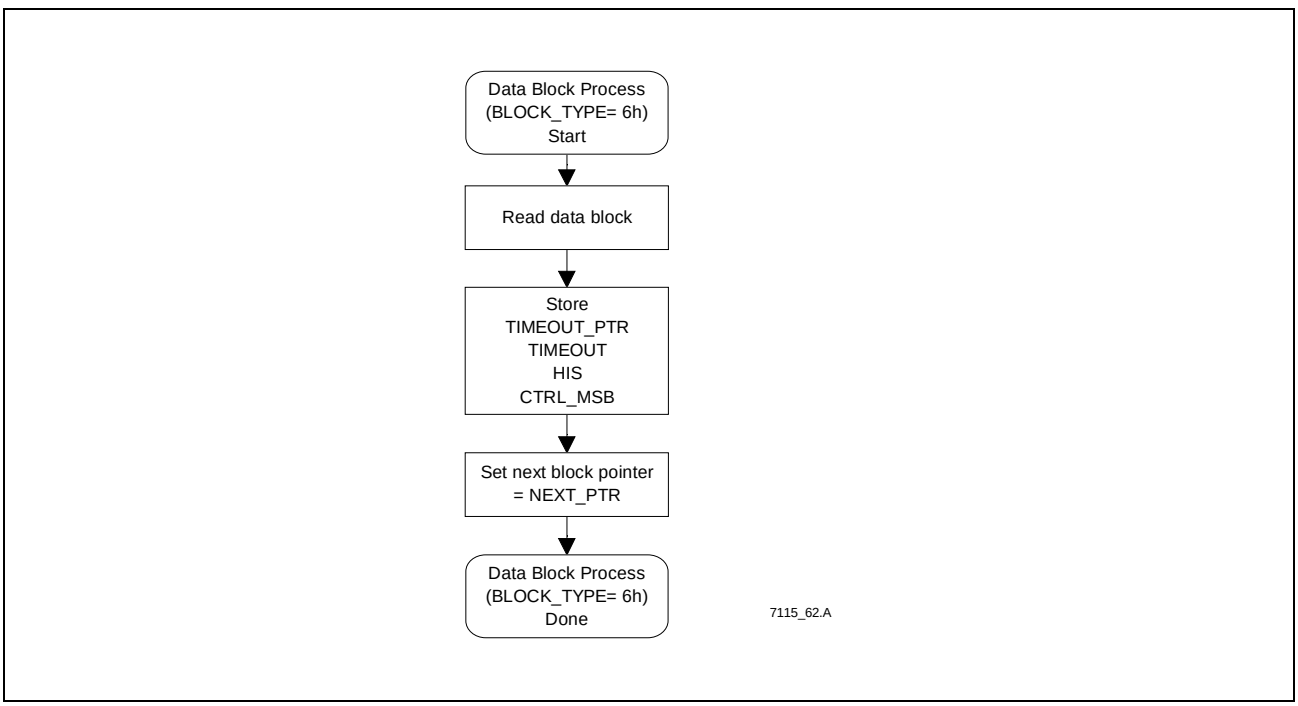


Figure 54 Data Block Process - Set Coding Information

3.12.3.7 Set Status Information

A status flag is used to indicate whether the complete download procedure succeeded or failed. This flag is not required for the download mechanism itself but it is used as an indication to the host. The host implements a variable STATUS that is intialized with the value = $FFFF_H$ and modified with every "Set Status Information" block.

When this block occurs the status flag must be set by the host according to the parameter STATUS of the data block. After that the host jumps to the next block indicated by NEXT_PTR.

Table 22 Block Structure - BLOCK_TYPE = 7_H

Offset	Type	Field
0	dword [1]	NEXT_PTR
4	word [1]	STATUS

Since the flag can be modified several times during the download the host must not evaluate it until the end of the download file is reached, i.e. the final information whether the download is successful or not is only valid after the download procedures are finished.

The STATUS flag indicates that the DSP program download was ...

STATUS = 0: ... successful
STATUS ≠ 0: ... not successful

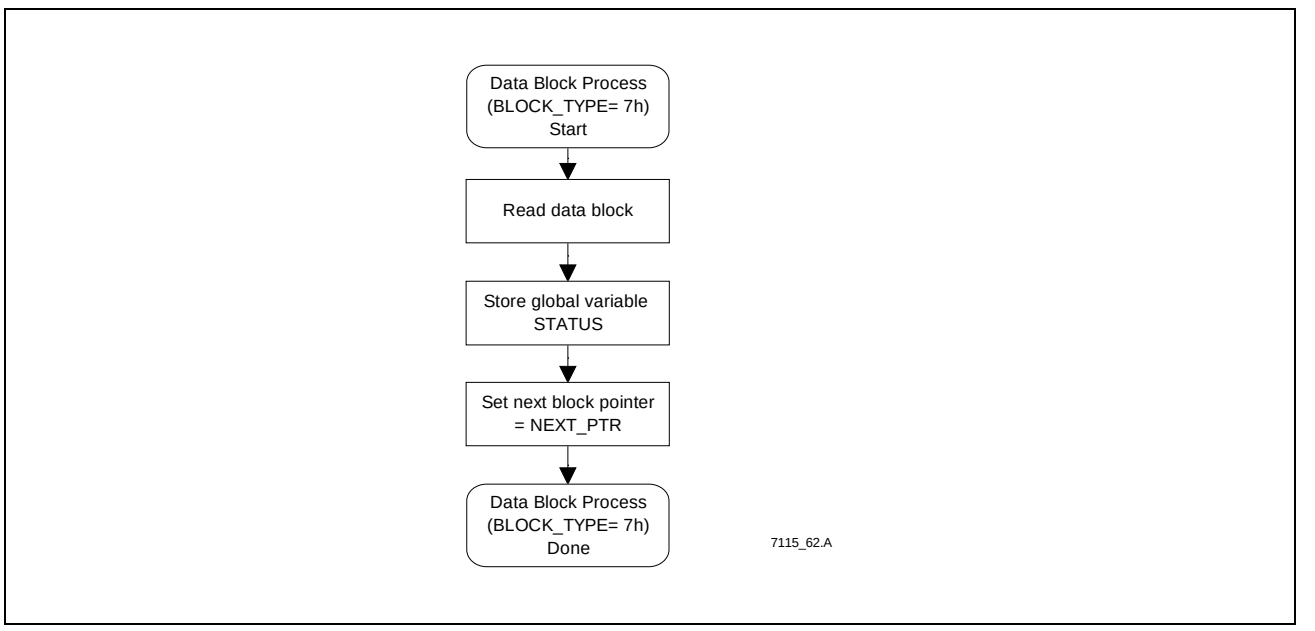


Figure 55 Data Block Process - Set Status Information

3.12.3.8 Write to Memory

The host writes data to the memory of the ISAR 34. Four different block types are distinguished relating to the target memory to which data is downloaded, however the structure of the data blocks is identical and the download mechanism is rather similar.

Table 23 Types of Memory Write Data Blocks

BLOCK_TYPE	Function
00000020_H	Write internal data memory.
00000021_H	Write internal program memory.
00000030_H	Write external data memory.
00000031_H	Write external program memory.

The host writes a message to the ISAR 34 that contains the code for program or data memory. The mechnism to write a message is shown in detail in the flow charts. The parameters like START_ADDR and LENGTH, as well as the code data (MBOX) itself is contained in the data block.

If the write message is acknowledged by the ISAR 34, the host jumps to the next data block indicated by TRUE_PTR. If a different message than acknowledge is received, the next valid block is indicated by FALSE_PTR.

If a timeout condition occurs (parameter TIMEOUT) the host proceeds with the next block indicated by TIMEOUT_PTR. Both parameters are not given in this data block, but they are global variables (see **chapter 3.12.3.6**).

Table 24 Block Structure - BLOCK_TYPE = 20_H, 21_H, 30_H, 31_H

Offset	Type	Field
0	dword [1]	TRUE_PTR
4	dword [1]	FALSE_PTR
8	dword [1]	START_ADDR
12	dword [1]	LENGTH
16	word [n]	DATA

Note: The length of the DATA field n is determined by LENGTH.

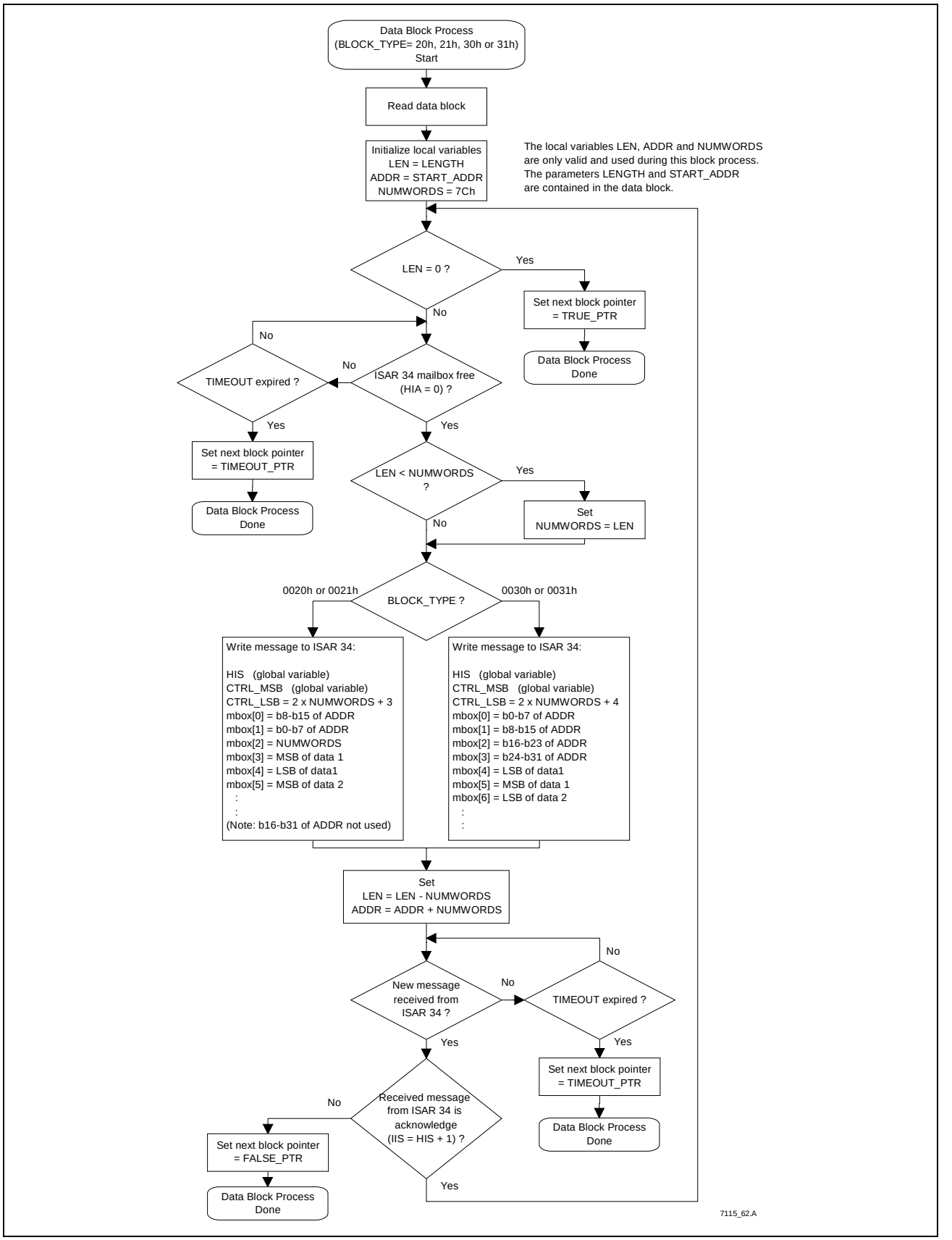


Figure 56 Data Block Process - Write to Memory

3.13 Fax Class 1 Implementation

This chapter gives more details on the implementation of fax group 3 on the ISAR 34 PSB 7115. It is expected that the controlling protocol residing on the host is either an implementation of the Service Class 1 Command Set (EIA/TIA-578) or ITU-T T.30.

It must be noted that for pump mode “Fax Modulations”, the SART unit is not to be configured as described in chapter 3.4 SART Configuration. Transmission and reception of HDLC framed and binary data is only controlled by pump control commands (see **chapter 3.6.2.1**) and pump status events (see **chapter 3.7.3.1**), i.e. the SART must not be reconfigured to HDLC or binary mode.

However, data is transferred by use of SART data messages together with framing dependent control commands and status events (see **chapters 3.5.1** and **3.5.2** SART Data).

Fax Pump Control

• Pump control commands	Host → ISAR 34	3.6.2.1
• Pump status events	ISAR 34 → Host	3.7.3.1

Fax Data Transfer

• SART control commands - along with transmit data	Host → ISAR 34	3.5.2
• SART status events - along with receive data	ISAR 34 → Host	3.5.1

For configuration of the whole data path, first the buffer should be configured and then the pump and the IOM-2 interface. Configuration of SART and pump to the required framing and modulation scheme (e.g. HDLC framing and 300 bit/s /V.21Ch2) is set by single pump control commands as mentioned above. Further configuration data (modulation and silence duration) is passed by additional parameters to the pump control commands.

3.13.1 Summary of ISAR 34 Fax Control Commands

CMD_FTH	Starts transmission of HDLC frames. The SART is set to HDLC mode and the pump is set to modulation mode. The additional parameter contains the datarate of the pump modulation mode (V.21Ch2) at which data is to be transmitted.
CMD_FRH	Starts reception of HDLC frames. The SART is set to HDLC mode and the pump is set to modulation mode. The additional parameter contains the datarate of the pump modulation mode (V.21Ch2) at which data is to be received.
CMD_FTM	Starts transmission of binary data. The SART is set to binary mode and the pump is set to modulation mode.The additional parameter contains the datarate of the pump modulation mode (V.17, V.29, V.27ter) at which data is to be transmitted.
CMD_FRM	Starts reception of binary data. The SART is set to binary mode and the pump is set to modulation mode.The additional parameter contains the datarate of the pump modulation mode (V.17, V.29, V.27ter) at which data is to be received.
CMD_SIL_DET_ON	Starts to wait a determined length of time. The additional parameter contains the silence duration which is to be waited. It is not mandatory and can be omitted , if the previous setting of this parameter is still valid.
CMD_CONTINUE	Handshake message from the host to indicate that the host is ready to do the task (transmit/receive) which it selected before.
CMD_ESCAPE	This command is a regular escape in receive modes and a break in transmit modes.
CMD_SIL_DET_OFF	Break of silence detection.
CMD_HALT	Shut down from fax pump idle state.

3.13.2 Summary of ISAR 34 Fax Status Events

RSP_READY	Response to CMD_ANSWER and CMD_ORIGINATE
LINE_TX_HDLC	Response to CMD_FTH in order to indicate that the modulation has been established.
LINE_TX_BINARY	Response to CMD_FTM in order to indicate that the modulation has been established.
LINE_RX_HDLC	Response to CMD_FRH in order to indicate that the modulation has been established.
LINE_RX_BINARY	Response to CMD_FRM in order to indicate that the modulation has been established.
RSP_CONNECT	Indication that the fax pump is ready to receive or transmit data.
RSP_DISC	Indication that the fax pump has turned off modulation after transmitting all pending data / after the host issues the command CMD_ESCAPE
RSP_FCERROR	Indication that the fax pump has detected a “wrong” modulation before it releases the event RSP_CONNECT.
RSP_SIL_DET	Indication that the prior selected duration of silence time has occured
FLAGS_DETECT	Indication that the fax pump has detected flags.

3.13.3 Procedure Termination

In response to control commands generated by the host, the fax pump invokes various procedures. Another procedure cannot be invoked until the previous procedure has been terminated. Procedure termination may either be indicated by the fax pump or commanded by the host. The table below shows the termination indications and commands for each of the procedures.

Table 25 Fax Class 1 - Procedure Termination

Prodedure	**Indication of Procedure Termination** (ISAR 34 → Host)	**Command for Procedure Termination** (Host → ISAR 34)
Start as Originator	RSP_READY	CMD_ESCAPE
Start as Answerer	RSP_READY	CMD_ESCAPE
HDLC Transmit	RSP_DISC	CMD_ESCAPE
HDLC Receive	RSP_FCERROR	CMD_ESCAPE
Binary Transmit	RSP_DISC	CMD_ESCAPE
Binary Receive	RSP_FCERROR	CMD_ESCAPE
Wait for Silence	RSP_SIL_DET	RSP_SIL_DET_OFF

When no procedure is currently active, the fax pump is in an idle state. During the idle state, the command CMD_ESCAPE will be ignored by the fax pump, however, the host may issue the command CMD_HALT to shut down the fax pump. This is normally done when a fax session has ended and the telephone connection is released.

3.13.4 Fax Pump Startup Procedure

The host configures the fax pump either as originator or answerer when a physical connection has been established. After initialisation, the fax pump responds with RSP_READY, indicating, that it is ready for the next procedure.

At this point the host must issue either a command CMD_FRH or CMD_FTH depending upon if the host is answering or originating a facsimile connection. The interaction of the host and the faxpump is as shown in the flow charts for transmission and reception of HDLC and binary data.

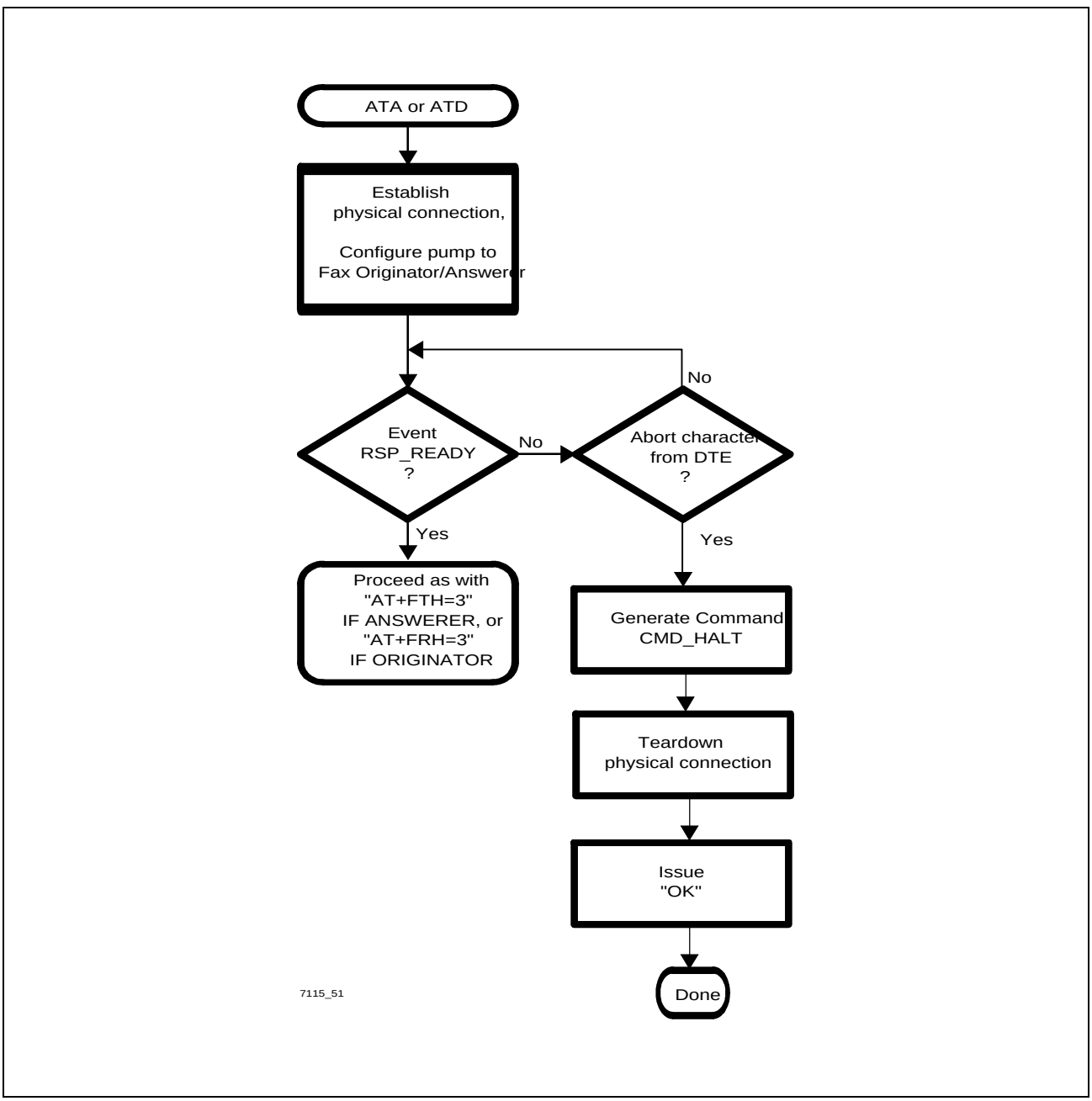


Figure 57 Fax Class 1 - Startup Procedure

3.13.5 HDLC Transmission

A host can control HDLC frame transmission during a fax group 3 session by issuing the command CMD_FTH to the fax pump. HDLC transmission is specified by the T.30 procedure during the exchange of control information. Some applications may alternatively implement HDLC framing directly, they would then use binary transmission for the transmission of their HDLC bit stream.

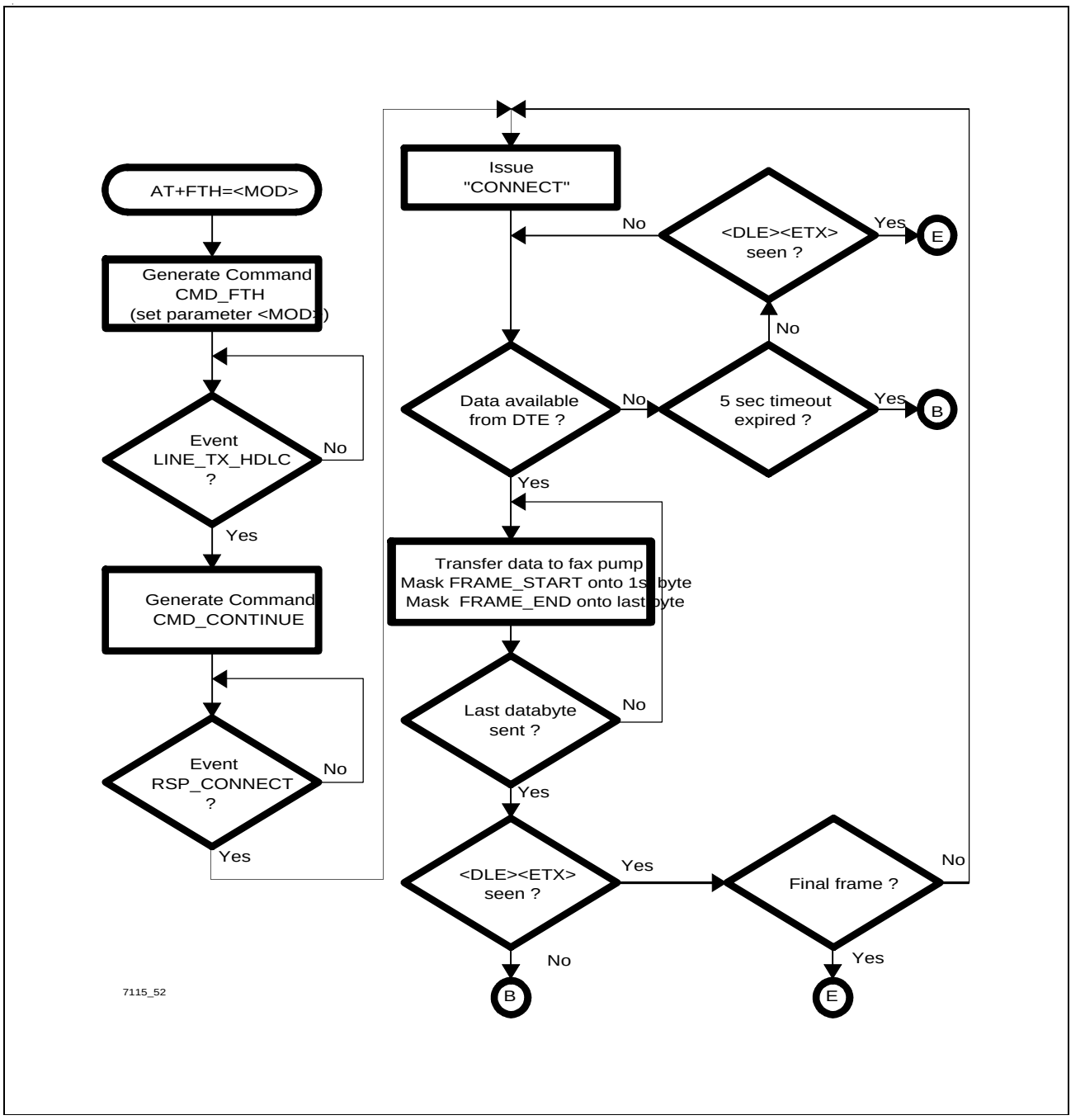


Figure 58 Fax Class 1 - HDLC Transmission

3.13.6 Binary Transmission

A host can control binary transmission during a fax group 3 session by issuing the command CMD_FTM to the fax pump. Binary transmission is specified by the T.30 procedure during the exchange of image.

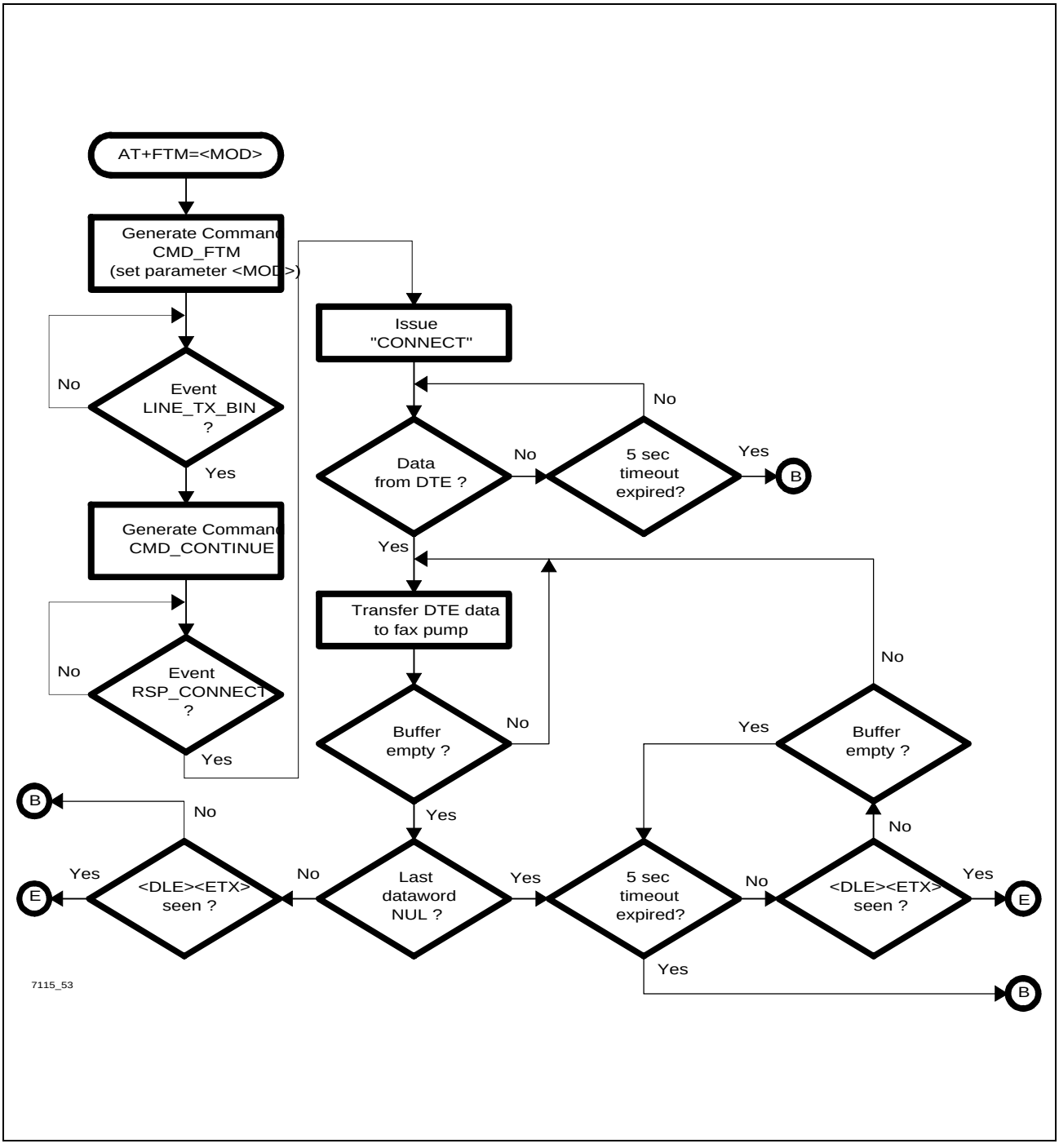


Figure 59 Fax Class 1 - Binary Transmission

3.13.7 HDLC Reception

A host can control HDLC frame reception during a fax group 3 session by issuing the command CMD_FRH to the fax pump. HDLC reception is specified by the T.30 procedure during the exchange of control information. Some applications may alternatively implement HDLC framing directly, they would then use binary reception for the reception of their HDLC bit stream.

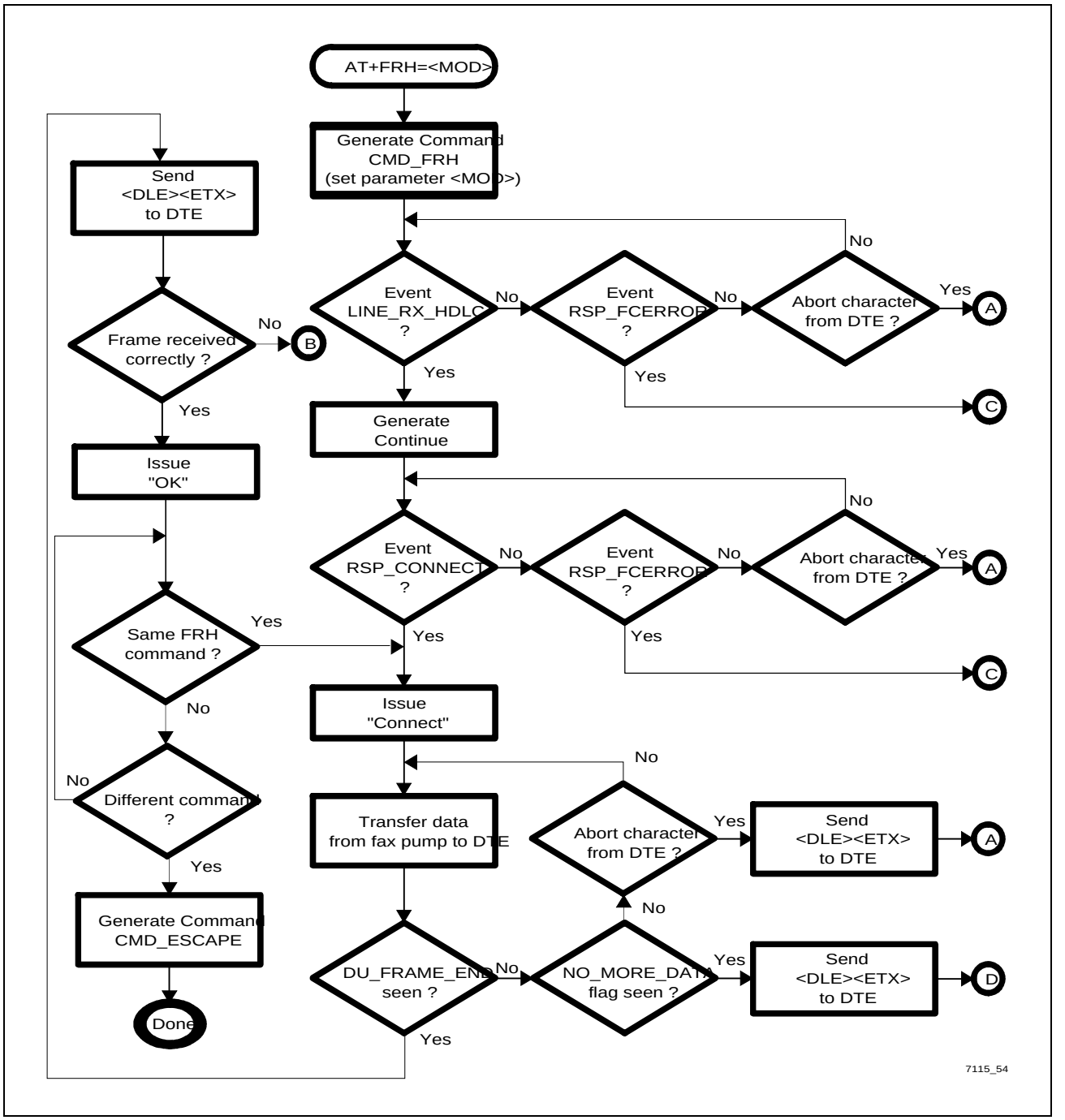


Figure 60 Fax Class 1 - HDLC Reception

3.13.8 Binary Reception

A host can control binary reception during a fax group 3 session by issuing the command CMD_FRM to the fax pump. Binary reception is specified by the T.30 procedure during the exchange of image.

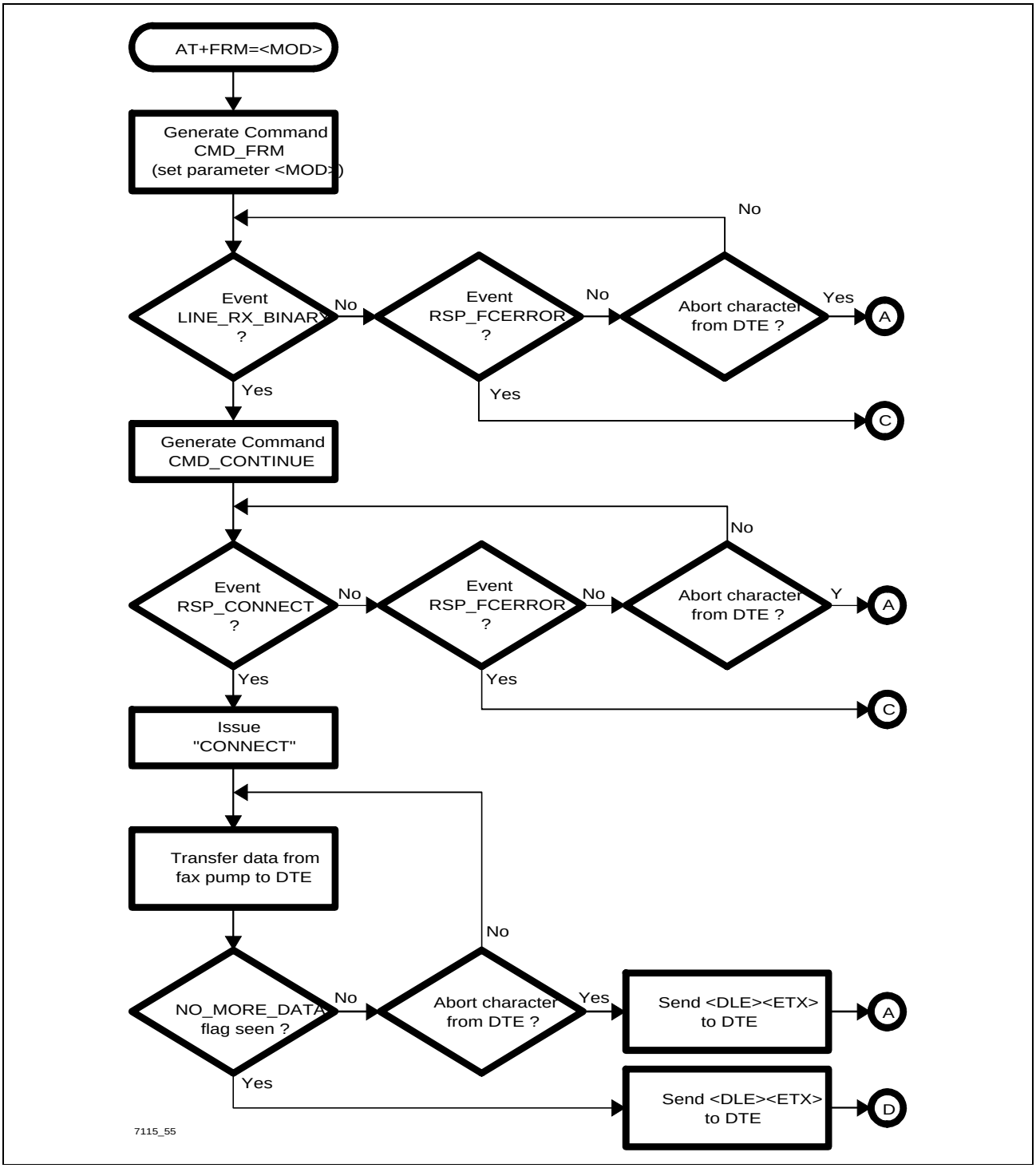


Figure 61 Fax Class 1 - Binary Reception

3.13.9 Call Termination

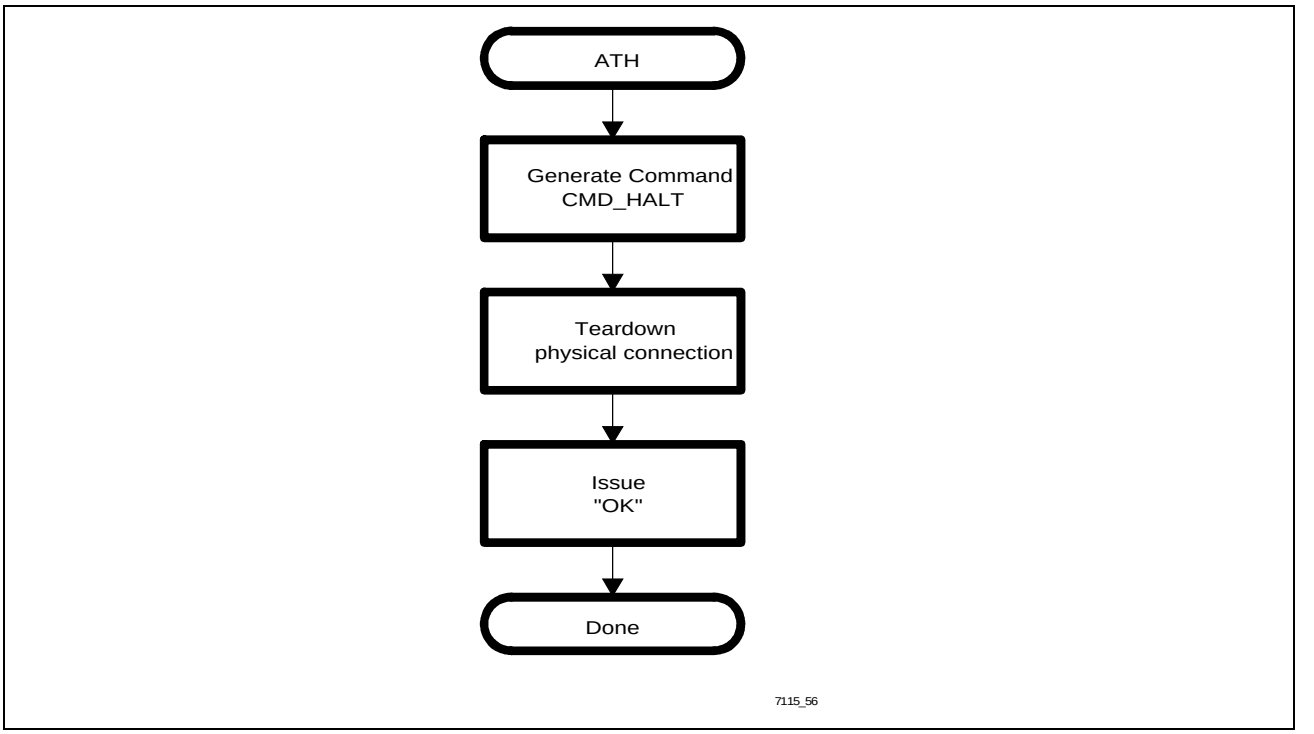


Figure 62 Fax Class 1 - Call Termination

3.13.10 Procedure Terminations

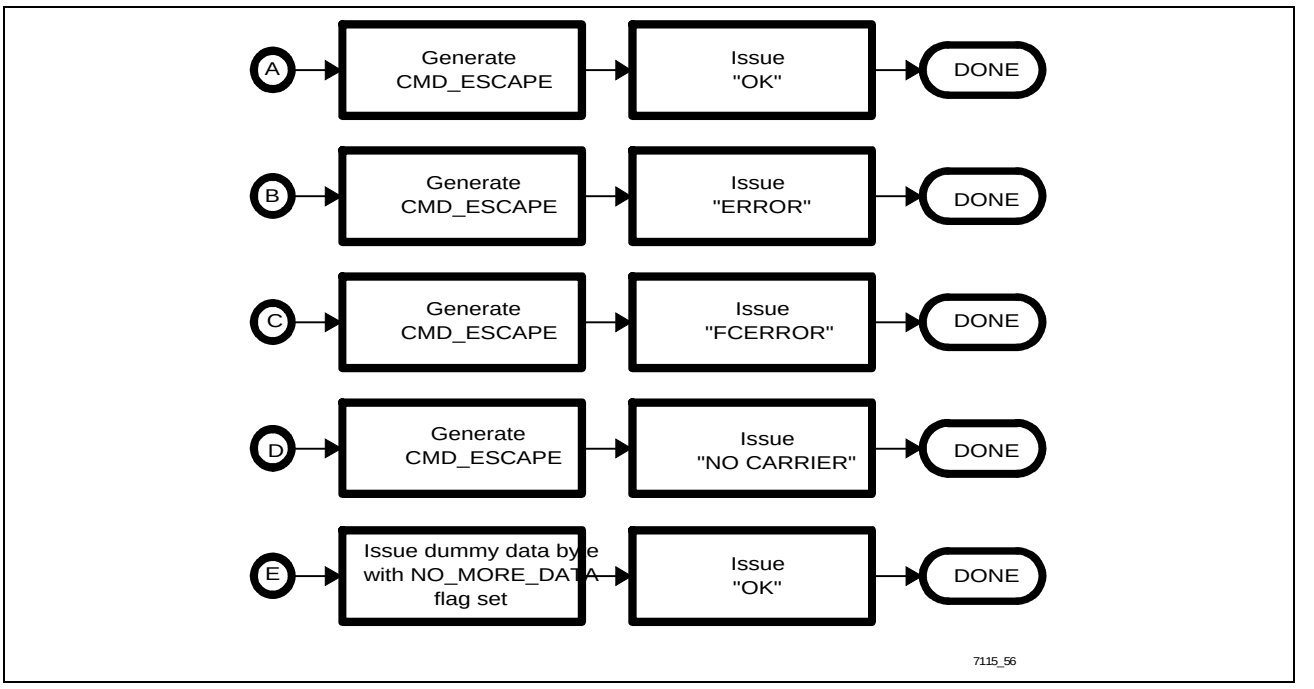


Figure 63 Fax Class 1 - Procedure Terminations

3.14 Startup Procedures

After a physical connection between two modems has been established, certain procedures can be started before signals are exchanged which are specific to a particular modem standard (V.34bis, V.32bis, ...). These procedures are used to determine the type of modulation at which data is transferred right after completion of the startup procedure.

The ISAR 34 is able to make use of the negotiation standard ITU-T V.8 and the Automode operation according to EIA/TIA PN-2330, which are described in the following chapters. After the host configures the datapump to data modem modulations with startup procedures (V.8, automode) enabled, it can request the selected modulation scheme from the ISAR 34 as soon as the modulation has been established between both modems.

3.14.1 V.8 Negotiation

In V.8 mode the answerer starts with transmitting the answer tone ANSam and monitors the reception of the call tone. If the originator does not indicate V.8 capability or the V.8 procedures fail, the ISAR 34 will proceed with Automode answerer operation.

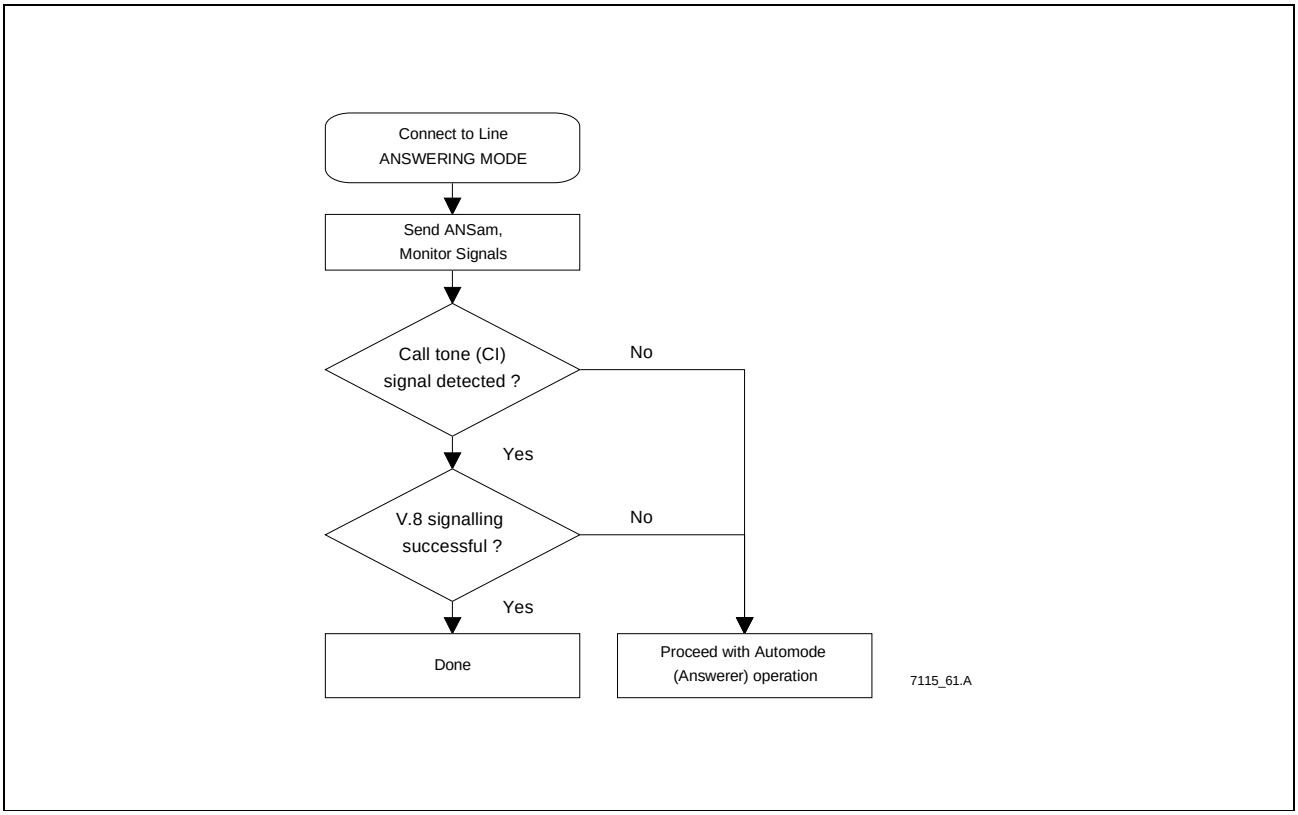


Figure 64 V.8 Answering Mode

The V.8 originator starts with transmission of the call tone while monitoring for the answering tone. If the answerer does not indicate V.8 capability or the V.8 procedures fail, the ISAR 34 will proceed with Automode originator operation.

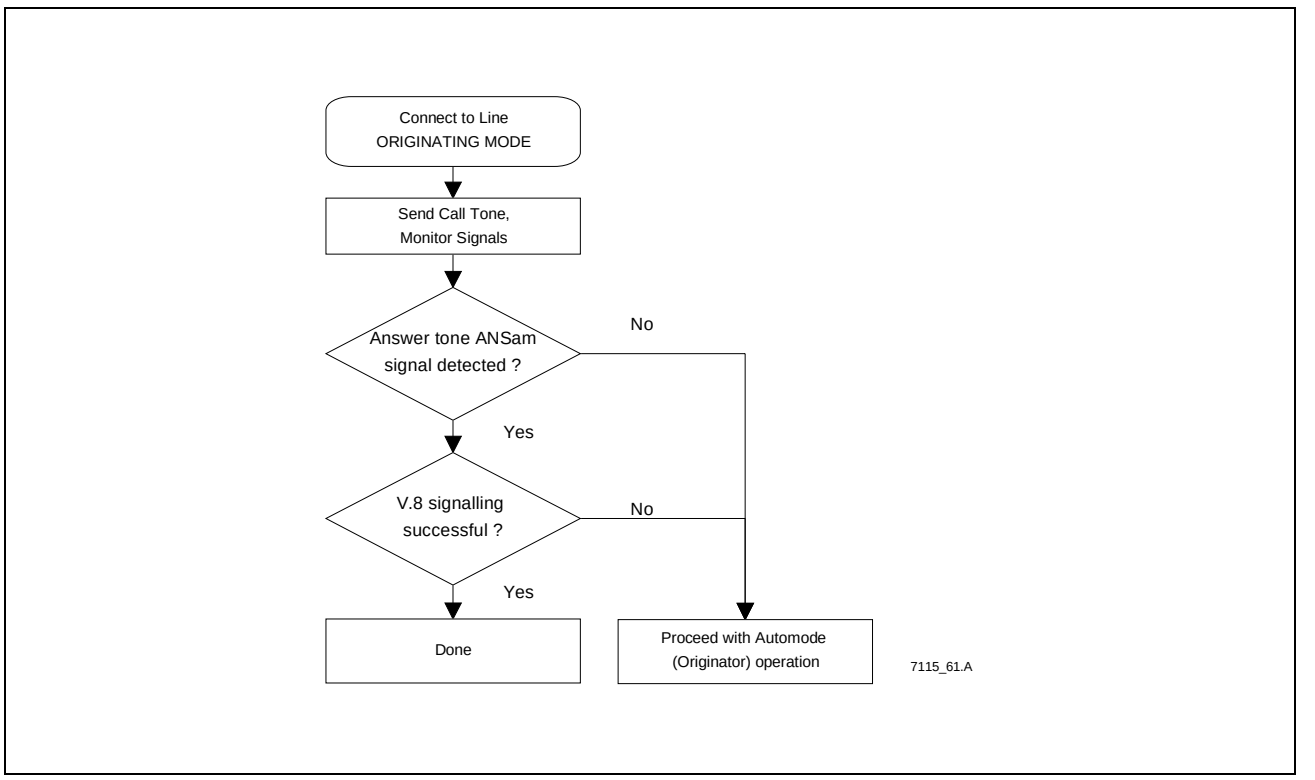


Figure 65 V.8 Originating Mode

V.34bis modulation can only be achieved by using the V.8 negotiation mechansim as the automode operation does not provide for the upgrade from V.32bis to V.34bis. In other words, if V.8 is not used or V.8 fails, V.34bis modulation can not be selected.

3.14.2 Automode Operation

Automode selection is available based on EIA/TIA PN-2330.

When enabled, the datapump will determine the communication standard supported by the remote modem and configure itself according. That means the modulation scheme and the data rate is automatically set without any host control.

The following figures show the flowcharts corresponding to the DSP algorithm used in supporting automode originating and answering mode. The signals indicated in both figures relate to the ITU-T V.32bis specification.

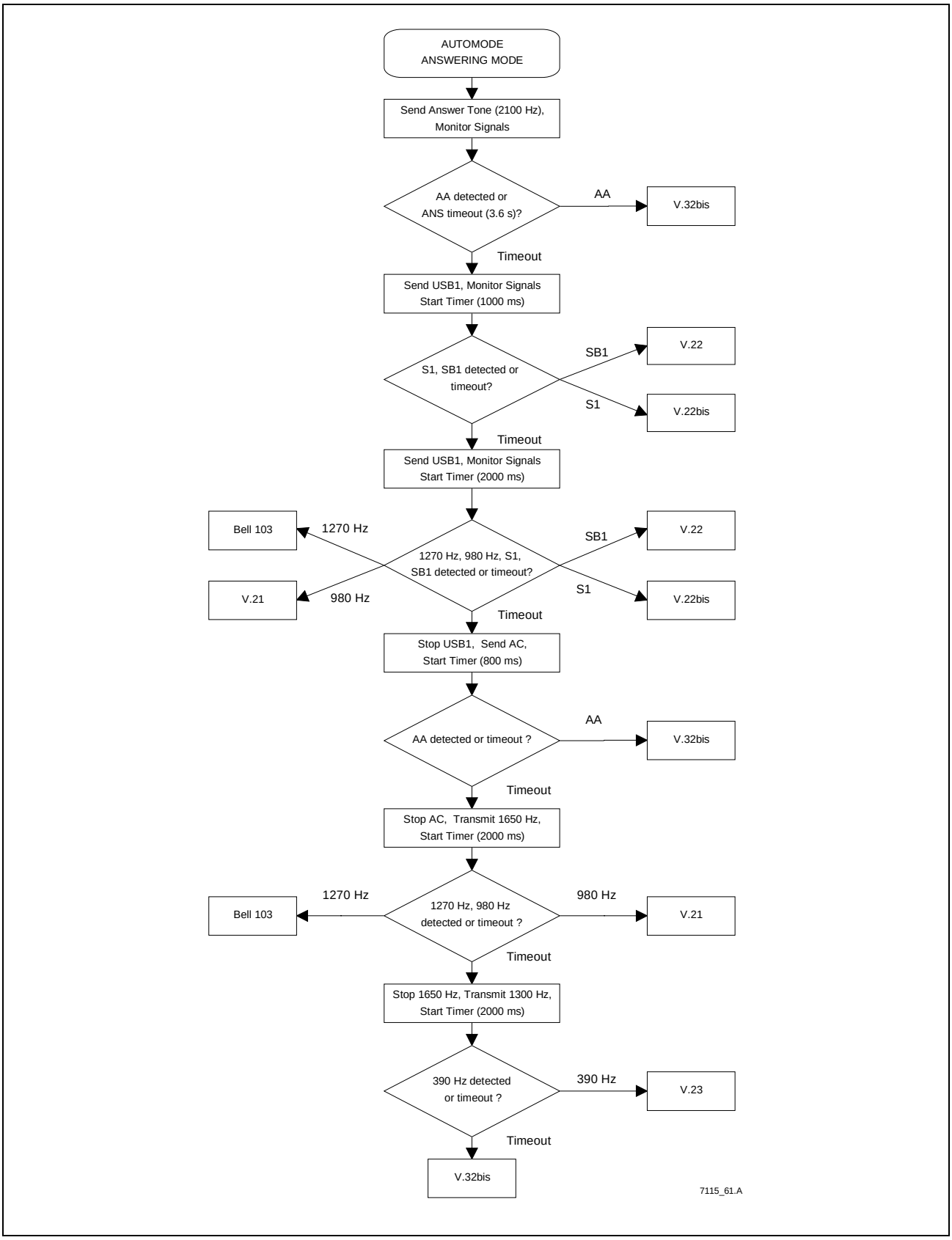


Figure 66 Automode Answerer

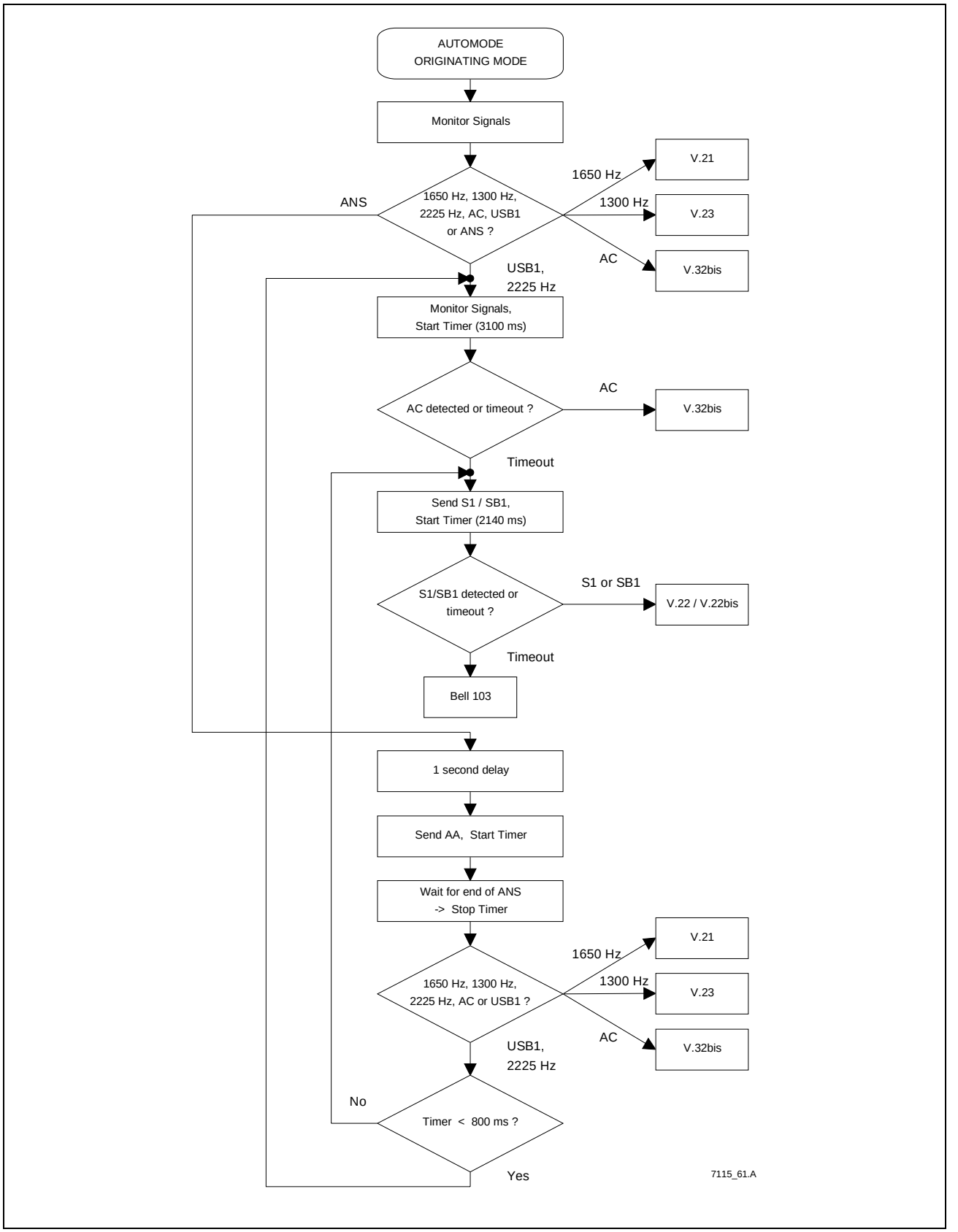


Figure 67 Automode Originator

4 Summary of Messages

Functional Block	Mode	Message Type	Read/ Write	HIS/IIS		CTRL MSB	CTRL LSB	1. Parameter 4. Parameter	2. Parameter 5. Parameter	3. Parameter ... Parameters
Buffer		Configuration Setup	WR	DPS MSC 0 0		0 0 0 0 0 BBP	1	MML		
Buffer		Configuration Request	WR	DPS MSC 0 0		0	0			
Buffer		Configuration Response	RD	DPS MSC 0 0		- - - - - BBP	2	MML	MFL	
Buffer		Control Command	WR	DPS MSC MDS		0 0 0 0 0 0 CRB	0			
Buffer		Status Request	WR	DPS MSC MDS		0 0 0 0 0 0 0 STS	0			
Buffer		Status Response	RD	DPS MSC MDS		- - - - RDMB -2 -1 -0	6	NBRL	NBRM	NMR
								NBTL	NBTM	NMT
Buffer		Status Event - Specific	RD	DPS MSC MDS		STEV	0			
Buffer		Status Event - General	RD	0 0 0 0 0 0 0 0		- - - - RDMB -2 -1 -0	0			
SART	HDLC	Configuration Setup	WR	DPS 1 0 0 1 0 1		HDMC 0 0 SMODE	1	0 0 0 HIO IRF RLEN EDF DUO		
SART	ASYNC	Configuration Setup	WR	DPS 1 0 0 1 0 1		HDMC 0 0 SMODE	2	0 OVSP SNP PSL EDP NSB CHS	BFT	
SART	Binary	Configuration Setup	WR	DPS 1 0 0 1 0 1		HDMC 0 0 SMODE	2	0 0 0 0 0 0 DUO BSW	DUFW	
SART	Disabled	Configuration Setup	WR	DPS 1 0 0 1 0 1		0 0 0 0 SMODE	0			
SART	HDLC	Status Event with Receive Data	RD	DPS 1 0 0 0 0 0		-FED FSD FAD RER CER NMD	NDM	1st data byte	2nddata byte	.... data bytes
SART	ASYNC	Status Event with Receive Data	RD	DPS 1 0 0 0 0 0		- - BRE BRS DSD PER - -	NDM	1st data byte	2nddata byte	.... data bytes
SART	Binary	Status Event with Receive Data	RD	DPS 1 0 0 0 0 0		- - - - - - - NMD	NDM	1st data byte	2nddata byte	.... data bytes
SART	HDLC	Control Command with Transmit Data	WR	DPS 1 0 0 0 0 0		0 FED PST GFA 0 0 0 NMD	NDM	1st data byte	2nddata byte	.... data bytes
SART	ASYNC	Control Command with Transmit Data	WR	DPS 1 0 0 0 0 0		0 0 SOB SAB DSB V42 0 0	NDM	1st data byte	2nddata byte	.... data bytes
SART	Binary	Control Command with Transmit Data	WR	DPS 1 0 0 0 0 0		0 0 0 0 0 0 0 NMD	NDM	1st data byte	2nddata byte	.... data bytes
Pump	Fax Modulations	Configuration Setup	WR	0 1 1 0 0 1 1 0		OAM 0 0 0 PMOD	4	0 0 0 0 0 ATN 0 CTN CLDD	0 0 0 TOA	CCDD
Pump	Datamodem Modulations	Configuration Setup	WR	0 1 1 0 0 1 1 0		OAM 0 0 0 PMOD	11	0 0 V22B 0 V22 0 V21 BEL V32R (MSB)	AMOD V8 0 0 0 V34 V32 V23 V34R (LSB)	V32R (LSB) V34R (MSB)
								0 0 0 0 GTS ATN CTN CCDD	0 0 0 0 0 0 0 0 CLDD	0 0 0 TOA

7115_70

Summary of Messages

Functional Block	Mode	Message Type	Read/ Write	HIS/IIS	CTRL MSB	CTRLLSB	1. Parameter 4. Parameter	2. Parameter 5. Parameter	3. Parameter ... Parameters
Pump	Halfduplex Modulations	Configuration Setup	WR	0 1 1 0 0 1 1 0	OAM 0 0 0 PMOD	5	V17C V17D V29A V29B V29C V27A V27B V21 CODD	000 EPT 0 0 V17A V17B CLDD	0 0 0 TOA
Pump	V.110	Configuration Setup	WR	DPS 1 0 0 1 1 0	0 0 0 0 0 PMOD	2	VDR	0 0 0 0 0 0 0 FCT	
Pump	DTMF	Configuration Setup	WR	0 1 1 0 0 1 1 0	DDIR 0 0 0 PMOD	6	REL DON	TW_LSB DOFF	TW_MSB 0 0 0 TOA
Pump	Bypass	Configuration Setup	WR	DPS 1 0 0 1 1 0	0 0 0 0 0 PMOD	0			
Pump	Fax Modulations	Control Command	WR	0 1 1 0 1 0 1 0	0	NOM	FCMDL	FCMDH	MODC or SLD
Pump	Datamodem Modulations	Control Command	WR	0 1 1 0 1 0 1 0	0	2	DCMDL	DCMDH	
Pump	Halfduplex Modulations	Control Command	WR	not defined					
Pump	V.110	Control Command	WR	DPS 1 0 1 0 1 0	0	3	VCMDL 0 0 0 0 X SB SA1 SA0 or: 1 or:	VCMDH 0 E1 E2 E3 E4 E5 E6 E7 or: 0 0 0 RQF0 RQF1 RON1 RQFX RONX	0 0 0 0 0 0 0 CCT or: FRC or:
Pump	DTMF	Control Command	WR	0 1 1 0 1 0 1 0	0	3	DCMDL	DCMDH	TDIG
Pump	C/I-Channel	Control Command	WR	1 1 1 0 1 0 1 0	CIC	0			
Pump	Bypass	Control Command	WR	not defined					
Pump	(all modes)	Status Request	WR	DPS 0 0 1 1 1 0	0	0			
Pump	Fax Modulations	Status Response	RD	0 1 1 0 1 1 1 0	OAM 0 0 0 PMOD	2	RIL	RIM	
Pump	Datamodem Modulations	Status Response	RD	0 1 1 0 1 1 1 0	OAM 0 0 0 PMOD	5	RIL - - RRT LRT - RRP CON NEG	RIM - CLD RTY TMO - - RRN LRN	RIT
Pump	Halfduplex Modulations	Status Response	RD	0 1 1 0 1 1 1 0	OAM 0 0 0 PMOD	2	RIL	RIM	
Pump	V.110	Status Response	RD	DPS 1 0 1 1 1 0	0 0 0 0 0 PMOD	6	RIL - - - - X SB SA1 SA0	RIM - E1 E2 E3 E4 E5 E6 E7	- - - RQF0 RQF1 RON1 RQFX RONX FRC
Pump	DTMF	Status Response	RD	0 1 1 0 1 1 1 0	DDIR 0 0 0 PMOD	2	RIL	RIM	
Pump	Bypass	Status Response	RD	DPS 1 0 1 1 1 0	0 0 0 0 0 PMOD	2	RIL	RIM	
Pump	Disabled	Status Response	RD	DPS 1 0 1 1 1 0	0 0 0 0 0 PMOD	0			

7115_71

Summary of Messages

Functional Block	Mode	Message Type	Read/ Write	HIS / IIS		CTRL MSB	CTRL LSB	1. Parameter 4. Parameter	2. Parameter 5. Parameter	3. Parameter ... Parameters
Pump	Fax Modulations	Status Events	RD	0 1	1 0 1 0 1 0	0	2	REVTL	- - - - - REVTH	
Pump	Datamodem Modulations	Status Events	RD	0 1	1 0 1 0 1 0	0	2	DEVTL	- - - - - DEVTH	
Pump	Halfduplex Modulations	Status Events	RD	0 1	1 0 1 0 1 0	0	2	HEVTL	- - - - - HEVTH	
Pump	V.110	Status Events	RD	DPS	1 0 1 0 1 0	0	NOM	VEVTL or: - E1 E2 E3 E4 E5 E6 E7	- - - - - VEVTH or: - - - - ROF0 ROF1 RON1 ROFX RONX	- - - - X SB SA1 SA0
Pump	DTMF	Status Events	RD	0 1	1 0 1 0 1 0	0	3	DEVTL	- - - - - DEVTH	RDIG
Pump	Bypass	Status Events	RD	not defined						
Pump	D- and C/I- Channel	Status Events	RD	1 1	1 0 1 0 1 0	DCIE	0			
IOM-2		Configuration Setup - Path 1 and 2	WR	DPS	1 0 0 1 1 1	ICM 0 0 0 COD RCV	5	0 0 0 TXD RXD TSL	0 0 RTSO	0 0 0 0 0 RCS
								0 0 TTSO	0 0 0 0 0 TCS	
IOM-2		Configuration Setup - Path 3	WR	1 1	1 0 0 1 1 1	DED TIC CED 0 0 TAD	0			
IOM-2		Configuration Request - General	WR	0 0	0 0 1 0 0 0	0	0			
IOM-2		Configuration Request - Specific	WR	DPS	0 0 0 1 1 1	0	0			
IOM-2		Configuration Response - General	RD	0 0	1 0 1 0 0 0	- DCL AMD - - - - -	0			
IOM-2		Configuration Response - Path 1 and 2	RD	DPS	1 0 0 1 1 1	ICM 0 0 0 COD RCV	5	0 0 0 TXD RXD TSL	0 0 RTSO	0 0 0 0 0 RCS
								0 0 TTSO	0 0 0 0 0 TCS	
IOM-2		Configuration Response - Path 3	RD	1 1	1 0 0 1 1 1	DED TIC CED 0 0 TAD	0			
IOM-2		Control Command - General	WR	0 0	1 0 1 0 0 0	ICMD	0			
				0 0	1 0 1 0 0 1	ICMD	0			
IOM-2		Control Command - Path 1 and 2	WR	DPS	1 0 1 0 1 1	ICMD	0			
IOM-2		Status Events	RD	0 0	1 0 1 0 0 1	IEVT	0			

7115_72

Summary of Messages

Functional Block	Mode	Message Type	Read/ Write	HIS / IIS	CTRL MSB	CTRL LSB	1. Parameter 4. Parameter	2. Parameter 5. Parameter	3. Parameter ...Parameters
Channel 0	MONITOR Channel	Configuration Setup	WR	0 0 1 1 0 0 0 1	0 0 0 0 0 0 0 MCE	NOM	MAM	MRA	0 0 0 SLIN CSEL
Channel 0	MONITOR Channel	Configuration Request	WR	0 0 0 1 0 0 0 1	0	0			
Channel 0	MONITOR Channel	Configuration Response	RD	0 0 1 1 0 0 0 1	0 0 0 0 0 0 0 MCE	3	MAM	MRA	0 0 0 SLIN CSEL
Channel 0	MONITOR Channel	Receive Data	RD	0 0 1 1 0 0 0 0	- MED MSD - - - - -	NOM	1st data byte	2nd data byte	... data bytes
Channel 0	MONITOR Channel	Transmit Data	WR	0 0 1 1 0 0 0 0	0 MED MSD 0 0 0 0 0	NOM	1st data byte	2nd data byte	... data bytes
Channel 0	MONITOR Channel	Status Event	RD	0 0 1 1 0 0 1 0	MEVT	0			
Channel 0	General Purpose IOs	GPIO Output Register Set/Reset	WR	0 0 1 0 1 0 1 0	0	4	R(7:0) S8	R8	S(7:0)
Channel 0	General Purpose IOs	GPIO Direction Select	WR	0 0 1 0 1 0 1 0	10h	4	IN(7:0) OUT8	IN8	OUT(7:0)
Channel 0	General Purpose IOs	GPIO Open Drain Select	WR	0 0 1 0 1 0 1 0	20h	4	OD(7:0) PP8	OD8	PP(7:0)
Channel 0	General Purpose IOs	GPIO Strobed Input	WR	0 0 1 0 1 0 1 0	30h	4	C(7:0) S8	C8	S(7:0)
Channel 0	General Purpose IOs	GPIO Interrupt Mask	WR	0 0 1 0 1 0 1 0	40h	4	RM(7:0) SM8	RM8	SM(7:0)
Channel 0	General Purpose IOs	GPIO Status Request	WR	0 0 0 0 1 0 1 0	0	0			
Channel 0	General Purpose IOs	GPIO Status Event/Message	RD	0 0 1 0 1 0 1 0	0	2	ST(7:0)	ST8	
Test/Diag.		Timer Interrupt On / Off	WR	0 0 1 0 0 1 0 1	CMD	0			
Test/Diag.		Timer Interrupt Event	RD	0 1 1 0 1 0 1 0	0	2	EVTL	- - - - - EVTH	
Test/Diag.		Software Version Request	WR	0 0 0 0 0 1 0 1	10h	0			
Test/Diag.		Software Version Response	RD	0 0 1 0 0 1 0 1	10h	2	SVNL	SVNH	
Test/Diag.		Request Selftest Result	WR	0 0 0 0 0 1 0 1	40h	0			
Test/Diag.		Selftest Response	RD	0 0 1 0 0 1 0 0	40h	1	0 0 PRO DRO PRR MB1 MB0 0		
Test/Diag.		Soft Reset	WR	0 0 1 0 1 0 0 0	RCMD	0			
Test/Diag.		Invalid Message Received	RD	0 0 1 1 1 1 1 1	INV	0			
The following two messages are not defined after the DSP program download is finished:									
Test/Diag.		Chip Version Request	WR	0 0 1 0 0 1 0 0	0	0			
Test/Diag.		Chip Version Response	RD	0 0 1 0 0 1 0 1	0	2	CVNL	CVNH	

7115_73

5 Example Configuration Settings

To give a better understanding how to program each of the parameters, some examples are given below for each of the functional blocks.

The mechanism to transfer messages from the host to the ISAR 34 is described in **chapter 3.1.5**. It should be noted, that the host interrupt status register (HIS) must only be written as the last register access for the message.

Buffer Configuration

Set channel 1 to buffer base priority 5 and maximum message length of 32:

Control Reg. MSB	=	05h
Control Reg. LSB	=	01h
1. Parameter	=	20h
HIS	=	64h

Set channel 2 to buffer base priority 3 without changing the maximum message length:

Control Reg. MSB	=	03h
Control Reg. LSB	=	0
No parameters		
HIS	=	A4h

Set channel 2 to maximum message length 32 without changing the buffer base priority:

Control Reg. MSB	=	0
Control Reg. LSB	=	1
1. Parameter	=	20h
HIS	=	A4h

SART Configuration

Set channel 1 to HDLC mode with regular I/O, “1” as interframe fill and 16 bit FCS length. In case of data underrun, FCS and final flag should be generated automatically (TX direction):

Control Reg. MSB	=	03h
Control Reg. LSB	=	01h
1. Parameter	=	09h
HIS	=	65h

Set channel 2 to V.14 mode (synchronous modulation) with overspeed range "1 of 4", even parity, two stop bits, 6 bit character size and a buffer flush timeout of 32:

Control Reg. MSB	=	02h
Control Reg. LSB	=	02h
1. Parameter	=	5Dh
2. Parameter	=	20h
HIS	=	A5h

Pump Configuration

Set channel 1 to faxmodulations in originating mode, 6 db transmitter output attenuation, calling tone enabled, carrier on detect duration of 800 ms and carrier loss detect duration of 2000 ms:

Control Reg. MSB	=	81h
Control Reg. LSB	=	04h
1. Parameter	=	01h
2. Parameter	=	06h
3. Parameter	=	08h
4. Parameter	=	14h
HIS	=	66h

Important Note:

If the pump is set to faxmodulations, the SART must not be configured as this is controlled by fax control commands which support implementation of fax class1 (see **chapter 3.13** Fax Class 1 Implementation).

Set channel 1 to automode data modulation in answering mode with 8 db transmitter output attenuation with answer tone enabled and all modulation schemes are disabled except V.32bis with data rates up to 12000 bit/s only. V.8 is disabled, the carrier on detect duration is 600 ms and carrier loss detect duration is 1400 ms:

Control Reg. MSB	=	42h
Control Reg. LSB	=	0Bh
1. Parameter	=	0
2. Parameter	=	82h
3. Parameter	=	0Fh
4. Parameter	=	F1h
5. Parameter	=	0
6. Parameter	=	0
7. Parameter	=	02h
8. Parameter	=	0
9. Parameter	=	08h
10. Parameter	=	06h
11. Parameter	=	0Eh
HIS	=	66h

IOM®-2 Configuration

Set channel 1 to the first timeslot on the IOM-2 interface with 8-bit timeslot length and regular switching of TX/RX paths. PCM data is A-law encoded and rate conversion is enabled (typical IOM-2 configuration for pump modes fax, datamodem and halfduplex modulations):

Control Reg. MSB	=	83h
Control Reg. LSB	=	05h
1. Parameter	=	10h
2. Parameter	=	0
3. Parameter	=	0
4. Parameter	=	0
5. Parameter	=	0
HIS	=	67h

Set channel 2 to the third timeslot on the IOM-2 interface with 8-bit timeslot length and mapping of transmitter and receiver to DD and DU of IOM-2 respectively. PCM data is µ-law encoded. This configuration might be used e.g. for pump mode DTMF:

Control Reg. MSB	=	84h
Control Reg. LSB	=	05h
1. Parameter	=	08h
2. Parameter	=	02h
3. Parameter	=	0
4. Parameter	=	02h
5. Parameter	=	0
HIS	=	A7h

The configuration of the IOM-2 interface has to make sure that the selected timeslots for channel 1 and 2 do not overlap, even if one of the channels is currently disabled by setting the IOM-bit to 0.

6 Detailed Register Description

6.1 Register Address Map

Address	Read								Write							
	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
08h								RST								RST
07h	–	–	–	–	–	MSK	–	–	–	–	–	–	–	STA	–	–
06h	Host Control Register High								ISAR 34 Control Register High							
05h	Host Control Register Low								ISAR 34 Control Register Low							
04h	–	–	–	–	–	–	–	IIA	ISAR 34 Interrupt Status (IIS)							
03h	Host Interrupt Status (HIS)								–	–	–	–	–	–	–	HIA
02h	Mailbox I/O data															
01h	Mailbox write address															
00h	Mailbox read address															

6.2 Register Description

Reset Bit Read/Write Address 08h

Value after Reset: xxxx xxx0

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	RST

RST … ISAR 34 Reset

The host resets the ISAR 34 by writing RST=1 and it is active until this bit is reset again (RST=0). The host must ensure that the reset is active for at least 2 ms, which has the same function as a hardware reset.

Interrupt Mask Bit Write Address 07h

Value after Reset: xxxx x1xx

7	6	5	4	3	2	1	0
–	–	–	–	–	MSK	–	–

MSK … Interrupt mask

All internal interrupt sources can be masked by setting MSK to ‘0’. In this case the interrupt is not indicated by activating the interrupt line, however it remains internally stored and pending until the MSK bit is set to ‘1’ (i.e. the interrupt is enabled).

Interrupt Status Bit Read Address 07h

Value after Reset: xxxx x0xx

7	6	5	4	3	2	1	0
–	–	–	–	–	STA	–	–

STA … Interrupt status

The STA bit indicates an interrupt status of the ISAR 34. If set to ‘1’, an internal interrupt is pending.

Host/ISAR 34 Control Register High Write/Read Address 06h

7	6	5	4	3	2	1	0

The MSB of the control word contains configuration, status or control information, depending on the message specified by the HIS/IIS register.

Host/ISAR 34 Control Register Low Write/Read Address 05h

7	6	5	4	3	2	1	0

The LSB of the control word contains the number of additional bytes in the mailbox, which depends on the message specified by the HIS/IIS register.

ISAR 34 Interrupt Acknowledge Bit Write Address 04h

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	IIA

IIA … ISAR 34 Interrupt Acknowledge

After reading a complete message from the ISAR 34 mailbox, the host sets IIA to ‘0’ to indicate to the ISAR 34, that the current message transfer is complete and a new message transfer may be started.

ISAR 34 Interrupt Status Read Address 04h

7	6	5	4	3	2	1	0
IIS							

The ISAR 34 interrupt status register (IIS) contains the source of the interrupt, i.e. buffer 0, 1, 2 or 3, the kind of indication (configuration, status or received data) and the indication source (buffer, SART, pump or IOM-2).

Host Interrupt Status (HIS) Write Address 03h

7	6	5	4	3	2	1	0

The host interrupt status register (HIS) contains the destination of the transferred message, i.e. buffer 0, 1, 2 or 3, the kind of command (request message, configuration, control or transmit data) and the functional block (buffer, SART, pump or IOM-2).

Host Interrupt Acknowledge Bit Read Address 03h

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	HIA

HIA … Host Interrupt Acknowledge

When transfering a message to the ISAR 34 mailbox, the final write access to the host interrupt register will automatically set the HIA bit. The ISAR 34 will reset HIA as soon as the ISAR 34 is capable to accept another message.

Mailbox I/O Data Write/Read Address 02h

7	6	5	4	3	2	1	0

The mailbox contains configuration, status and control information in addition to the control register MSB as well as transmit and receive data. The number of bytes in the mailbox is indicated in the control register LSB.

Mailbox Write Address Write/Read Address 01h

7	6	5	4	3	2	1	0

This register indicates the current write address on the mailbox buffer.
Before any data is written to the mailbox, the write address must be reset to 0 by the host. For any access to mailbox I/O data, the address pointer will be autoincremented and does not need to be programmed. This is the recommended way for sequential, fast access to the mailbox.
For random access, the host has to reprogram the write address pointer.

Mailbox Read Address Write/Read Address 00h

7	6	5	4	3	2	1	0

This register indicates the current read address on the mailbox buffer.
Before the mailbox contents of a message are read, the read address must be reset to 0 by the host. For any access to mailbox I/O data, the address pointer will be autoincremented and does not need to be programmed. This is the recommended way for sequential, fast access to the mailbox.
For random access, the host has to reprogram the read address pointer.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Supply Voltage	V_{DD}	– 0.3 to 4.2	V
Supply Voltage	V_{DDA}	– 0.3 to 4.2	V
Supply Voltage	V_{DDAP}	– 0.3 to 4.2	V
Supply Voltage	V_{DDP}	– 0.3 to 6.0	V
Voltage of pin with respect to ground: XTAL1, XTAL2	V_S	– 0.3 to V_{DDA} + 0.5	V
Voltage of any other pin with respect to ground	V_S	If V_{DDP} < 3 V: – 0.3 to V_{DD} + 0.5 If V_{DDP} > 3 V: – 0.3 to V_{DDP} + 0.5	V V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: The ISAR 34 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

7.2 Recommended Operating Conditions

V_{DD} = 3.0 to 3.6 V; V_{DDP} = 4.5 to 5.5 V, V_{SS} = 0 V

V_{DDA} = 3.0 to 3.6 V, V_{SSA} = 0 V

V_{DDAP} = 3.0 to 3.6 V, V_{SSAP} = 0 V

7.3 DC Characteristics

Conditions: see above (Recommended Operating Conditions); T_A = 0 to + 70 °C.

All pins except XTAL1, XTAL2:

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
High-Level Input Voltage	V_{IH}	2.0		V	
Low-Level Input Voltage	V_{IL}		0.8	V	
High-Level Output Voltage	V_{OH}	2.4		V	I_{OH} = – 400 µA
Low-Level Output Voltage	V_{OL}		0.45	V	I_{OL} = 7 mA DU, DD, CA(0:17), CD(0:15), $\overline{CRD}$, $\overline{CWR}$, $\overline{CSM0\text{-}3}$, FSC, DCL, INTN, SR, ST (50 pF) I_{OL} = 2 mA all others (30 pF)
Input leakage current	I_{LI}	– 10	10	µA	0 V < V_{IN} < V_{DDP}
Output leakage current	I_{LO}	– 10	10	µA	0 V < V_{OUT} < V_{DDP}
V_{DD} + V_{DDA} + V_{DDAP} supply current	I_{DDS}		150	mA	V.34+ connection
V_{DDP} supply current	I_{DDPS}		3	mA	V.34+ connection

For the sequence of applying supply voltage to the ISAR 34 it is necessary that first the V_{DDP} and then the V_{DD} / V_{DDA} / V_{DDAP} supply is switched on. Simultanous ramp up of both supplies is allowed.

Applying voltages to signal pins when power supply is not active (circuit not under bias) may cause damage. Refer to paragraph “Absolute Maximum Ratings”.

When power supply is switched on, the pads do not reach their stable bias until after 2 µs (maximum).

7.4 Capacitances

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input capacitance	C_{IN}		7	pF	
I/O capacitance	$C_{I/O}$		7	pF	
Load capacitance	C_L		20	pF	XTAL1,2

7.5 Oscillator Circuit

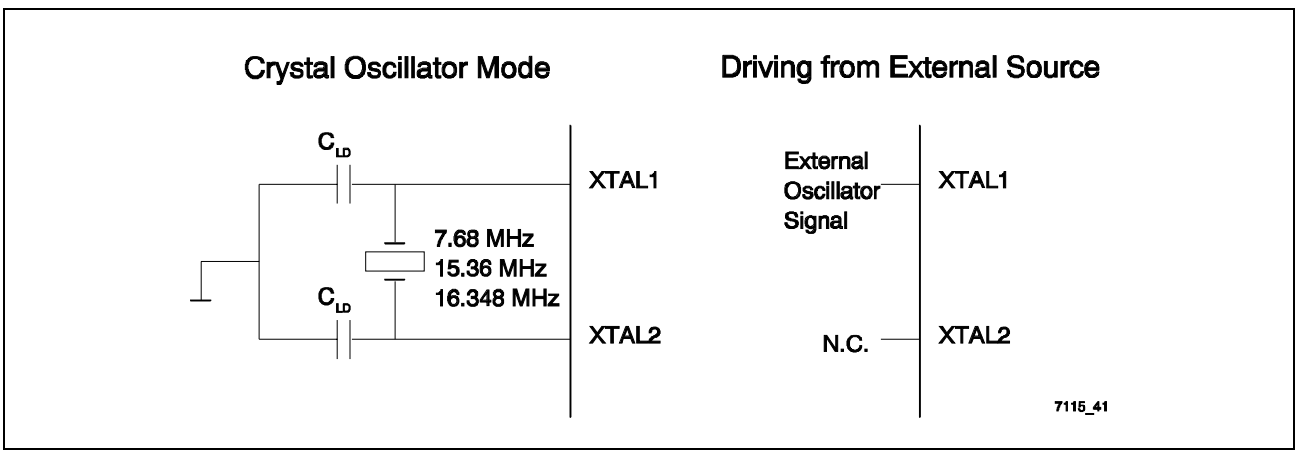


Figure 68 Oscillator Circuit

7.6 XTAL1,2 Recommended Typical Crystal Parameters

Parameter	Symbol	Limit Values	Unit
Frequency (CM0,1 = 10)	f	7.680	MHz
Frequency (CM0,1 = 01)	f	15.360	MHz
Frequency (CM0,1 = 11)	f	16.348	MHz
Frequency calibration tolerance		max. 100	ppm
Discrete capacitances	C_{LD}	≤ 33	pF
Resonance Resistor	R_r	≤ 50	Ω
Oscillator mode		fundamental	

Note: The discrete capacitances C_{LD} depend on the recommended crystal specification. Typical values for C_{LD} are 22 ... 33 pF.

7.7 AC Characteristics

7.7.1 Testing Waveform

Conditions as above (Recommended Operating Conditions) at T_A = 0 to 70 °C.

Inputs are driven to 2.4 V for a logical ‘1’ and to 0.45 V for a logical ‘0’. Timing measurements are made at 2.0 V for a logical ‘1’ and 0.8 V for a logical ‘0’. The AC testing input/output waveforms are shown in the figure below.

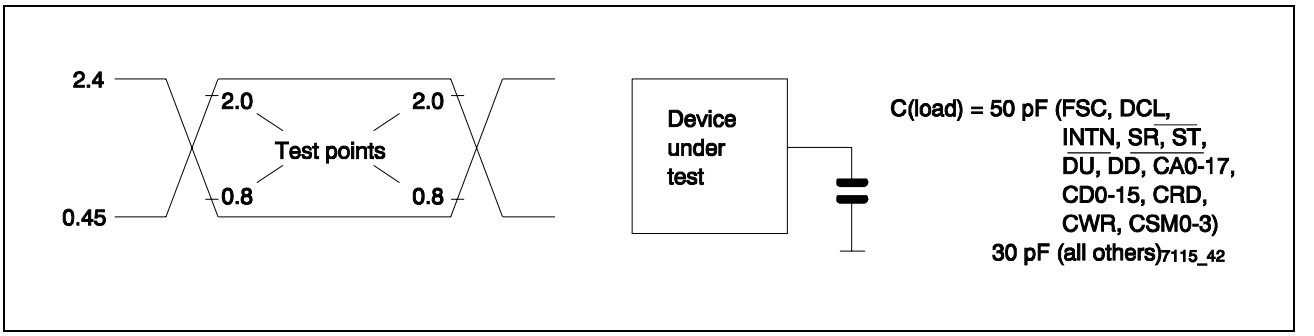


Figure 69 Testing Input/Output Waveforms

7.7.2 Parallel Host Interface Timing

Siemens/Intel Bus Mode

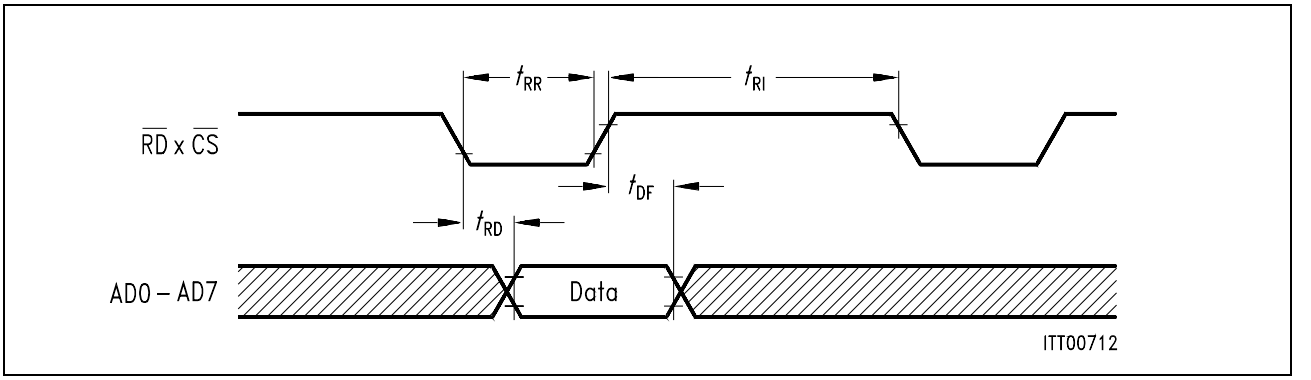


Figure 70 Microprocessor Read Timing

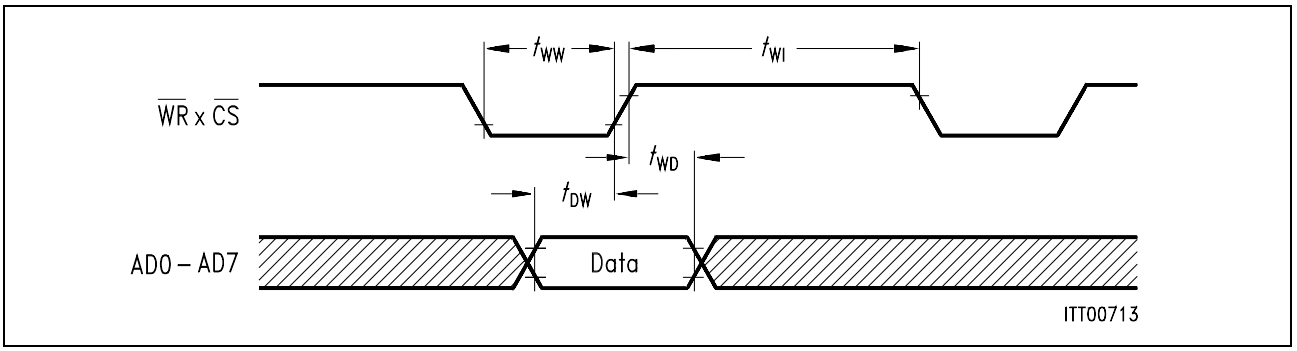


Figure 71 Microprocessor Write Timing

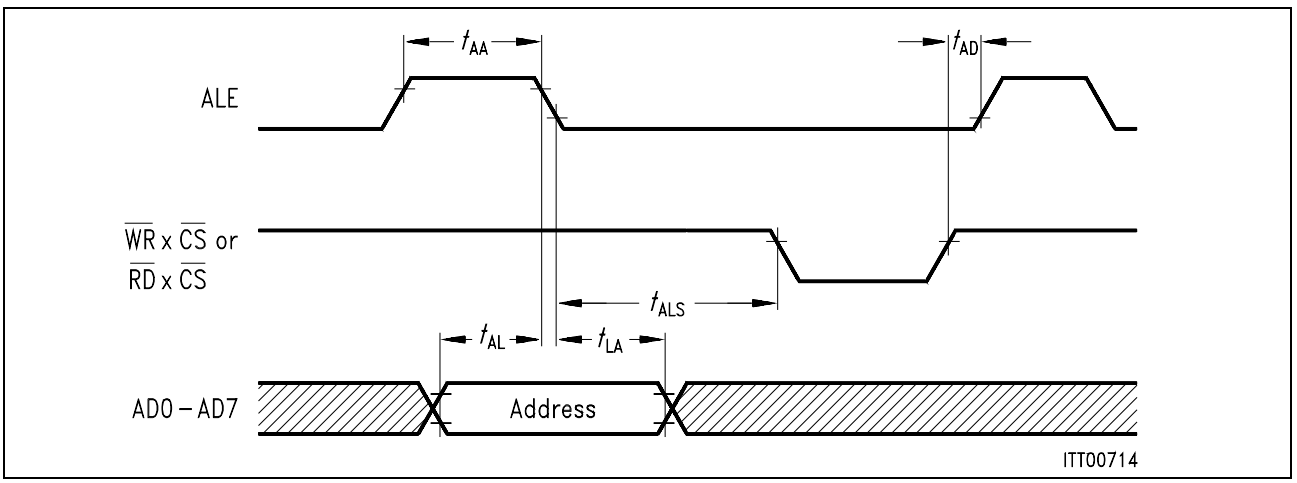


Figure 72 Multiplexed Address Timing

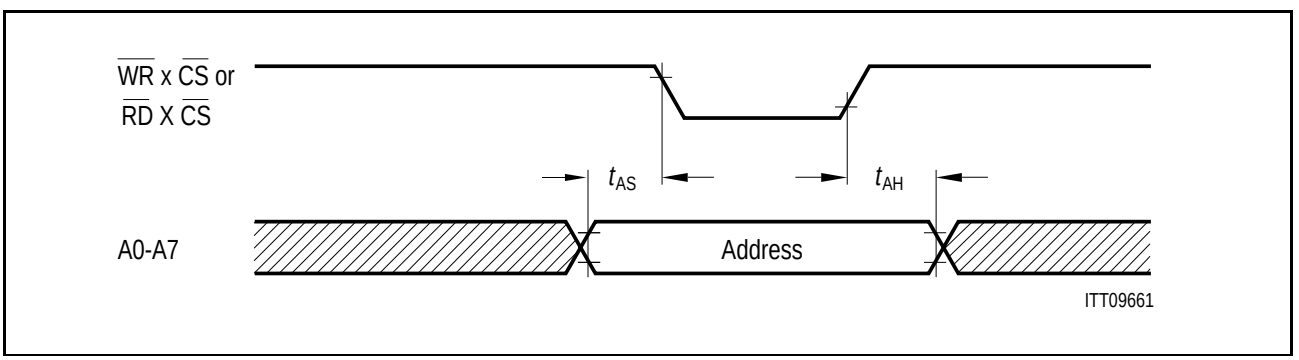


Figure 73 Non-Multiplexed Address Timing

Motorola Bus Mode

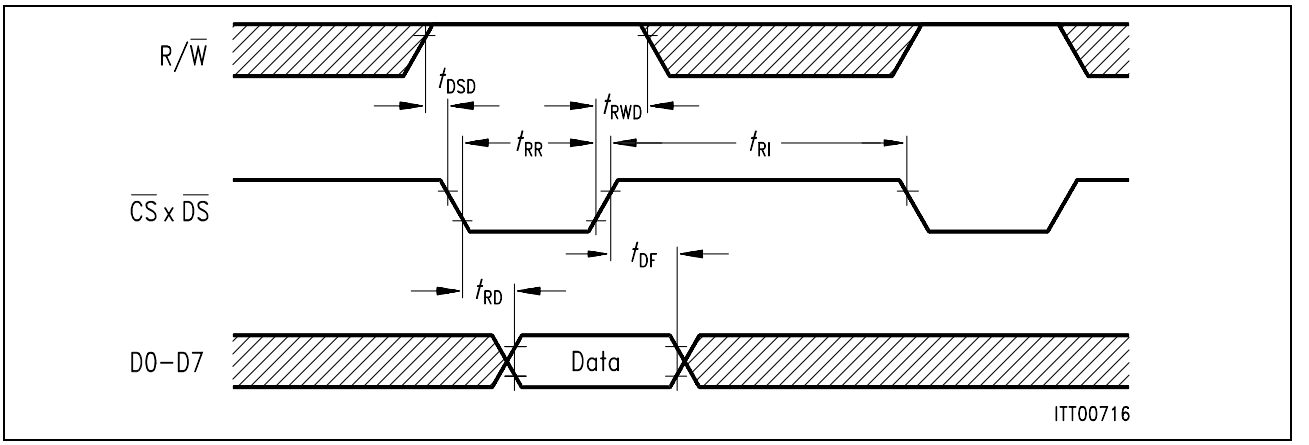


Figure 74 Microprocessor Read Timing

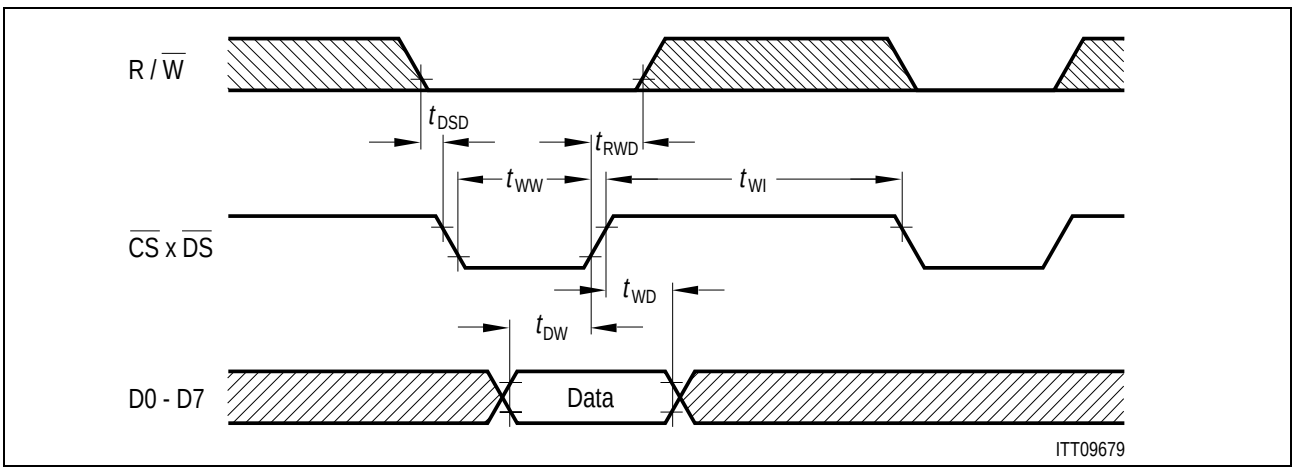


Figure 75 Microprocessor Write Timing

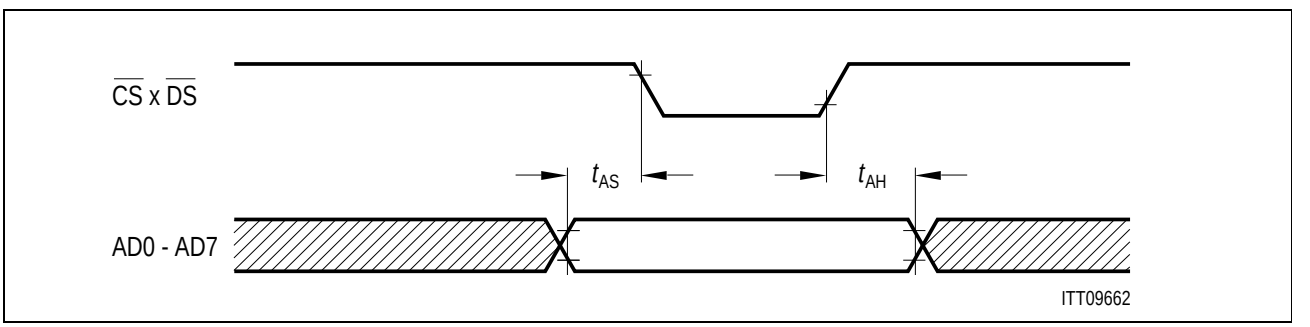


Figure 76 Non-Multiplexed Address Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	15		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time	t_{AS}	25		ns
Address hold time	t_{AH}	10		ns
ALE guard time	t_{AD}	15		ns
$\overline{DS}$ delay after R/$\overline{W}$ setup	t_{DSD}	0		ns
R/$\overline{W}$ hold from $\overline{CS}$ x $\overline{DS}$ inactive	t_{RWD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Data output delay from $\overline{RD}$	t_{RD}		110	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{W}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{W}$ x $\overline{CS}$	t_{DW}	35		ns
Data hold time $\overline{W}$ x $\overline{CS}$	t_{WD}	10		ns
$\overline{W}$ control interval	t_{WI}	70		ns

7.7.3 External Memory Interface Timing

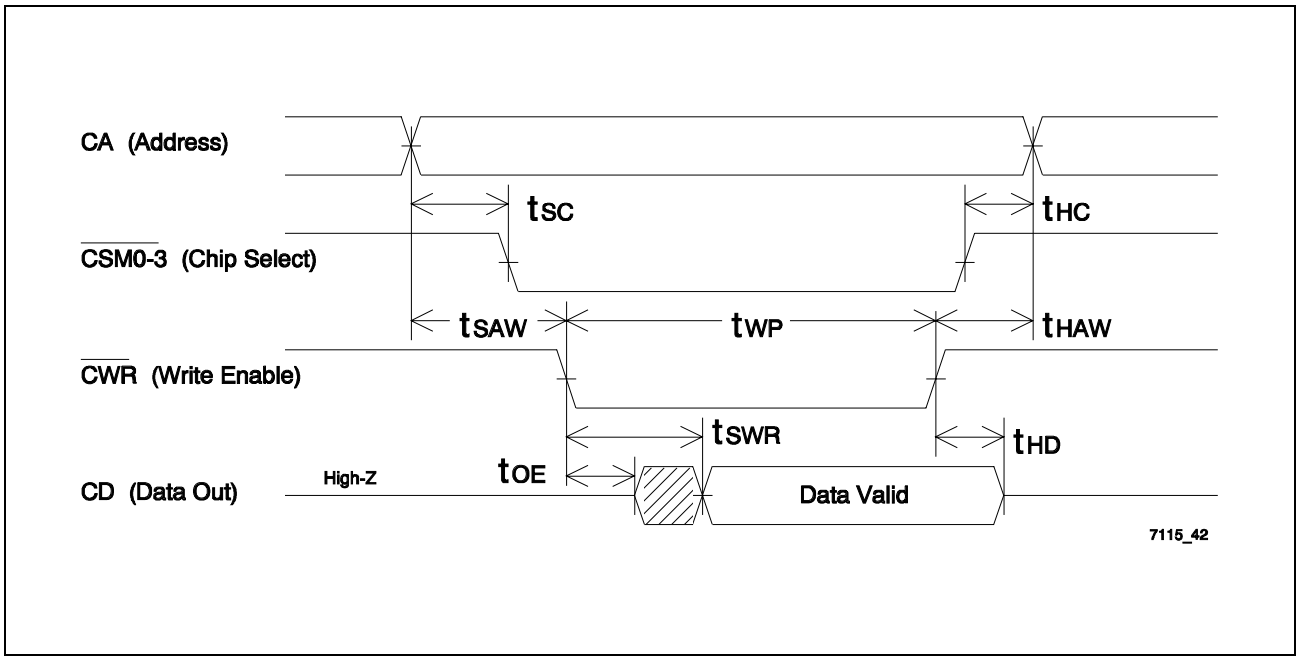


Figure 77 External Memory Interface - Write Cycle

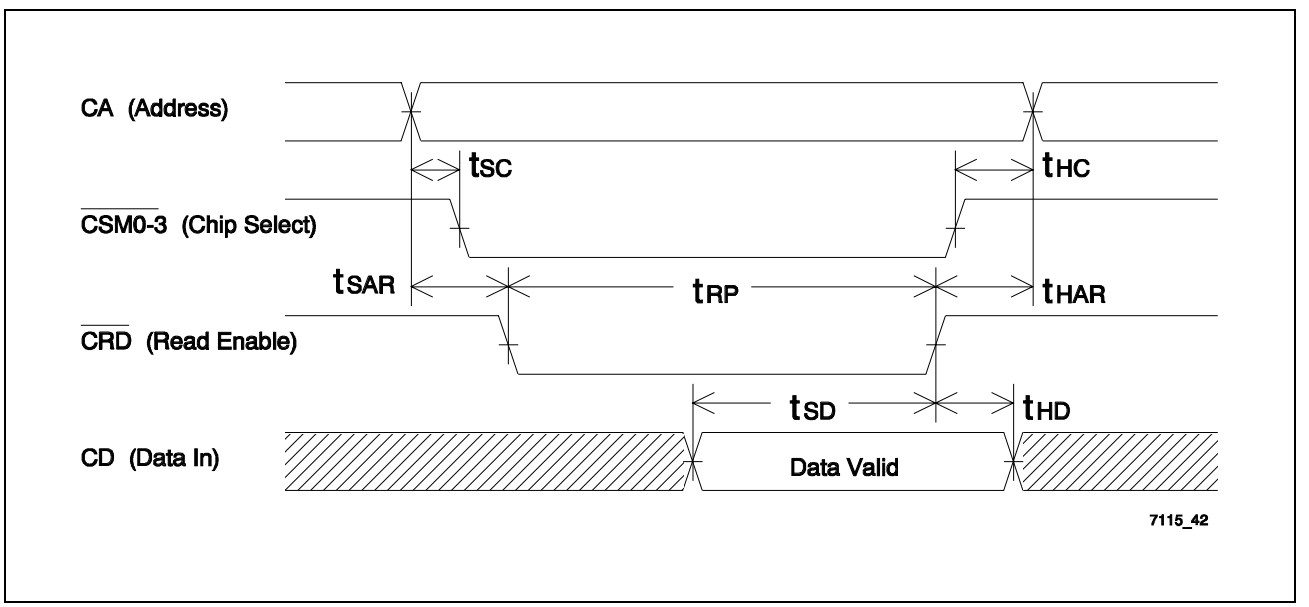


Figure 78 External Memory Interface - Read Cycle

Electrical Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Chip Select Setup Time	t_{SC}	-2.3	1.0	ns
Chip Select Hold Time	t_{HC}		1.0	ns
Address Setup Time Write	t_{SAW}	4.0		ns
Address Hold Time after End of Write	t_{HAW}	1.3		ns
Write Pulse Width	t_{WP}	25.0		ns
CWR low to Output Enable	t_{OE}	1.0		ns
CWR low to Data valid	t_{SWR}		12.5	ns
Data Hold Time	t_{HD}	0	1.0	ns
Read Pulse Width	t_{RP}	38.5		ns
Address Setup Time Read	t_{SAR}	-4.0	1.0	ns
Address Hold Time after End of Read	t_{HAR}	1.0		ns
Data Setup Time	t_{SD}	18.5		ns

7.7.4 IOM®-2 Interface Timing

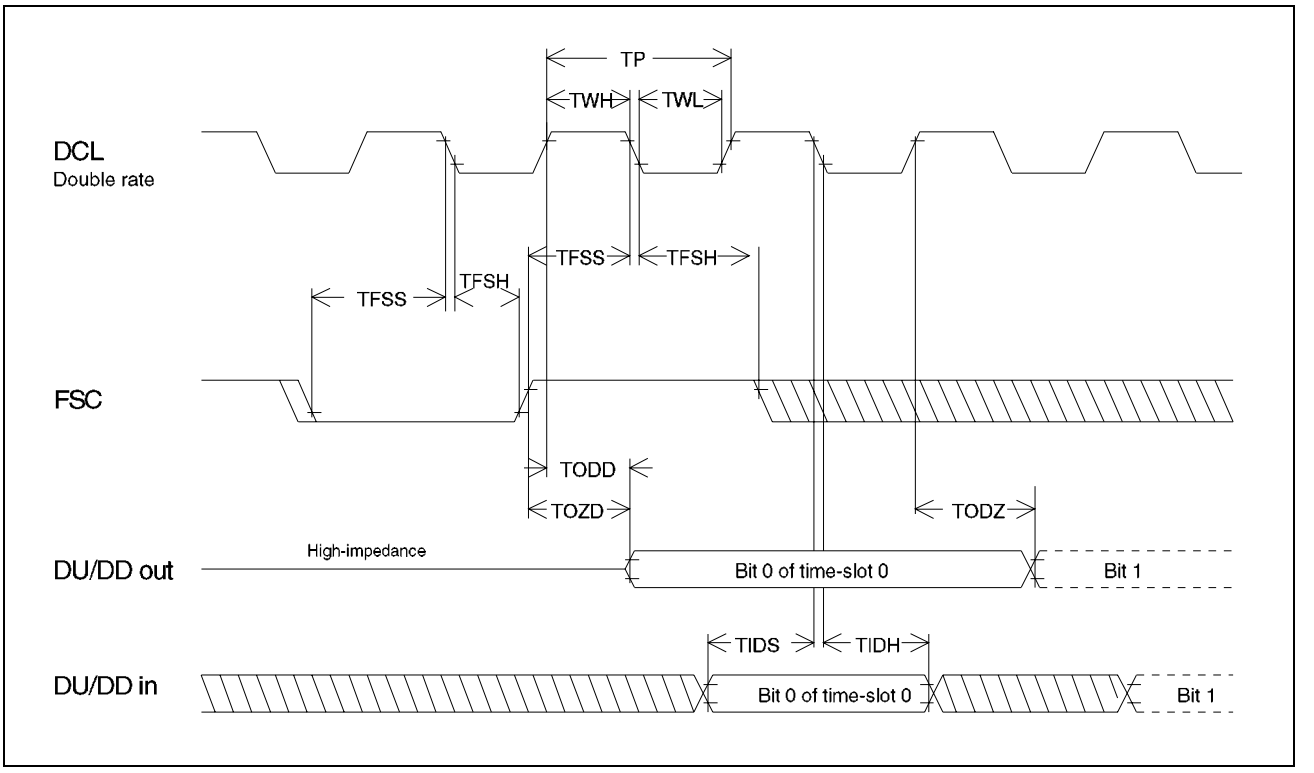
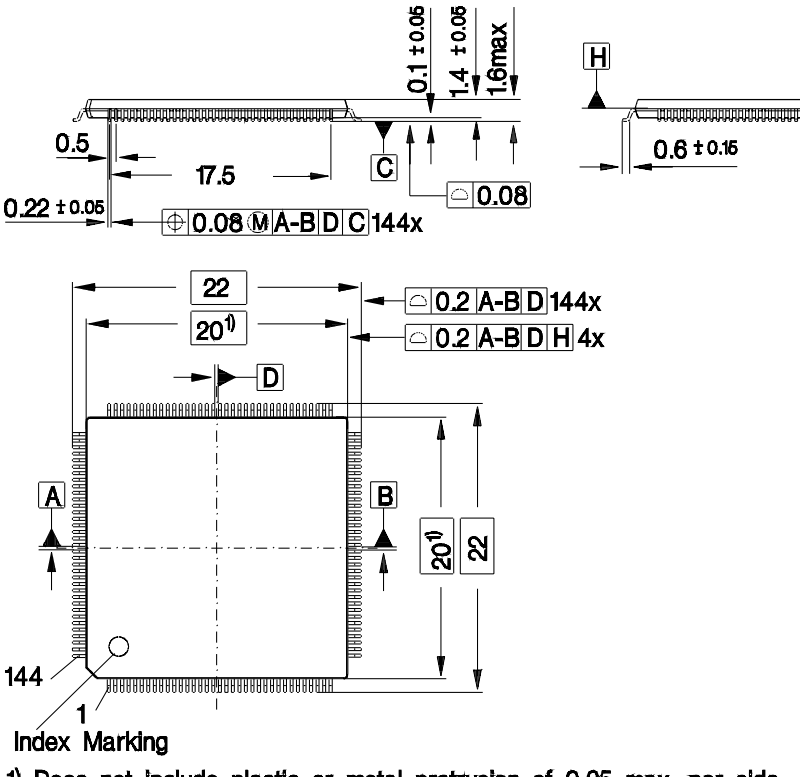


Figure 79 IOM®-2 Timing with Double Rate DCL

Parameter	Symbol	Limit Values		Unit
		min.	max.	
DCL period	T_P	244		ns
DCL high	T_{WH}	100		ns
DCL low	T_{WL}	100		ns
Frame sync setup	T_{FSS}	40		ns
Frame sync hold	T_{FSH}	40		ns
Output data from high impedance to active	T_{OZD}		100	ns
Output data delay from clock	T_{ODD}		100	ns
Output data from active to high impedance	T_{ODZ}		80	ns
Input data setup	T_{IDS}	20		ns
Input data hold	T_{IDH}	40		ns

8 Package Outlines

P-TQFP-144-2
(Plastic Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPP0 5616

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

A
Absolute maximum ratings 251
AC characteristics 254
ASYNC mode 46
B
Binary file structure 206
Binary mode 47
Block header 210
Buffer 43
  configuration request 81
  configuration response 82
  configuration setup 79
  control command 84
  general status event 90
  specific status event 89
  status request 85
  status response 87
Bypass mode 54
C
C/I-channel 56
Capacitances 253
Chip version
  request 201
  response 201
Communications interface 39
Control registers 67
Crystal 29
Crystal parameters 253
D
Datamodem modulations 50
DC characteristics 252
D-channel 56
Device architecture 19
DSP program download 206
DTMF 53
E
Electrical characteristics 251
Example configuration settings 243
External memory interface 36
  timing 258
F
Fax Class 1 implementation 225
  binary reception 233
  binary transmission 231
  call termination 234
  HDLC reception 232
  HDLC transmission 230
  procedure termination 228, 234
  startup procedure 229
Fax modulations 48
File header 208
Functional blocks 42
Functional description 28
G
General purpose I/O interface 37
GPIO (General Purpose IOs) 188
H
Halfduplex modulations 51
HDLC mode 45
HIS 62
Host communication 60
Host interface 31
  timing 254
I
IIS 62
Interrupt status byte 62

Invalid messages 205
IOM-2
configuration 55
configuration request 170
configuration response
general code 171
path 1 and 2 172
path 3 175
configuration setup
path 1 and 2 166
path 3 169
control commands
general code 176
path 1 and 2 178
status events 180
IOM-2 interface 34
timing 260
L
Logic symbol 18
M
Mailbox 39, 41
Message overview 76
Message structure 61
Message transfer 72
MONITOR channel 59
buffer configuration and status 181
configuration request 184
configuration response 184
configuration setup 182
RX data 185
status events 187
TX data 186
O
Operational description 60
Oscillator circuit 253
P
Package outlines 261
Physical interfaces 31
Pin
configuration 20
description 21
PLL 30
Pump 48
configuration setup
bypass mode 126
datamodem modulations 114
DTMF 123
fax modulations 112
halfduplex modulations 118
V.110 121
control command
bypass mode 136
C/I-Channel 137
datamodem modulations 131
DTMF 135
fax modulations 128
halfduplex modulations 131
V.110 132
status events
bypass mode 164
D- and C/I-channel 165
datamodem modulations 157

DTMF 163
fax modulations 155
halfduplex modulations 158
V.110 159
status request 139
status response
bypass mode 153
datamodem modulations 142
DTMF 152
fax modulations 140
halfduplex modulations 146
pump disabled 154
V.110 148
Pump configuration 110
R
Recommended operating conditions 251
Register description 246
Rejection level 53
Reset 68
S
SAI interface 35
SART 45
configuration setup
ASYNC 94
binary 97
disable SART 99
HDLC 92
control commands with TX data
ASYNC 107
binary 109
HDLC 105
status events with RX data
ASYNC 103
binary 104
HDLC 101
Selftest
request 203
response 203
Software reset 39, 204
Software version
request 202
response 202
Startup procedures 235
automode operation 236
V.8 negotiation 235
Summary of messages 239
System integration 13
T
Test/diagnostics path 199
Testing waveform 254
TIC-Bus Access 57
Timer interrupt
event 200
on/off 199
Twist 53
V
V.110 52
V.8 235