Fuji Switching Power Supply Control IC

Green Mode PWM-IC

FA5639

Application Note

April-2011
Fuji Electric co.,Ltd.

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Caution)

- The contents of this note subject to change without notice due to improvement.
- The application examples or the parts constants in this note are shown to help your design.
  Variation of parts and service condition are not fully taken into account.
  Before use, a design with due consideration for these variations and conditions shall be conducted.

1. Overview

FA5639 is a current mode type switching power supply control IC possible to drive a power MOSFET directly. Despite of a small package with 8 pins, it has a lot of functions and it is best suited for power saving at the light load and decreasing external parts. Moreover it enables to realize a reduced space and a high cost-performance power supply.

2. Features

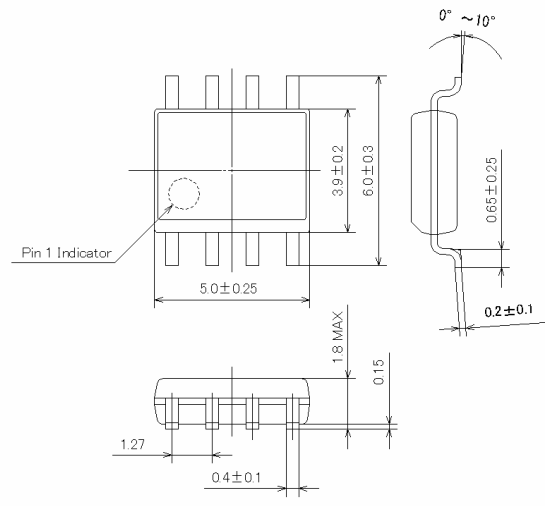
- Excellent Power Saving by lowering the oscillation frequency depending on the load at light load.
- Low power consumption by a built-in startup circuit.
- Overload protection function with a few number of external components.
- Current Minus detection. Power Saving of the revision of the input voltage of OLP.
- Latch pin for an external signal: Over Temperature Protection, Over Voltage Protection etc.
- Built-in drive circuit possible to connect to a power MOSFET directly.
  Output current: 1.0A (sink), 0.5A (source)
- VCC Under-Voltage Lock-Out function (UVLO).

Function list

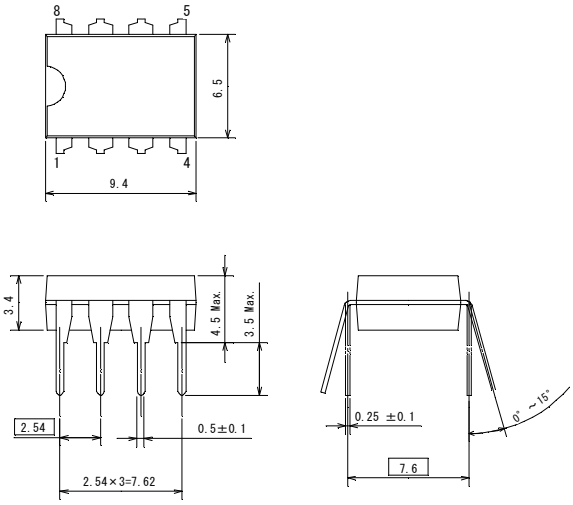
Part Number	Switching frequency	OLP type	IS pin VthIS
FA5639	100kHz(typ.)	Latch	VthIS= -1.0V

3. Outline drawing

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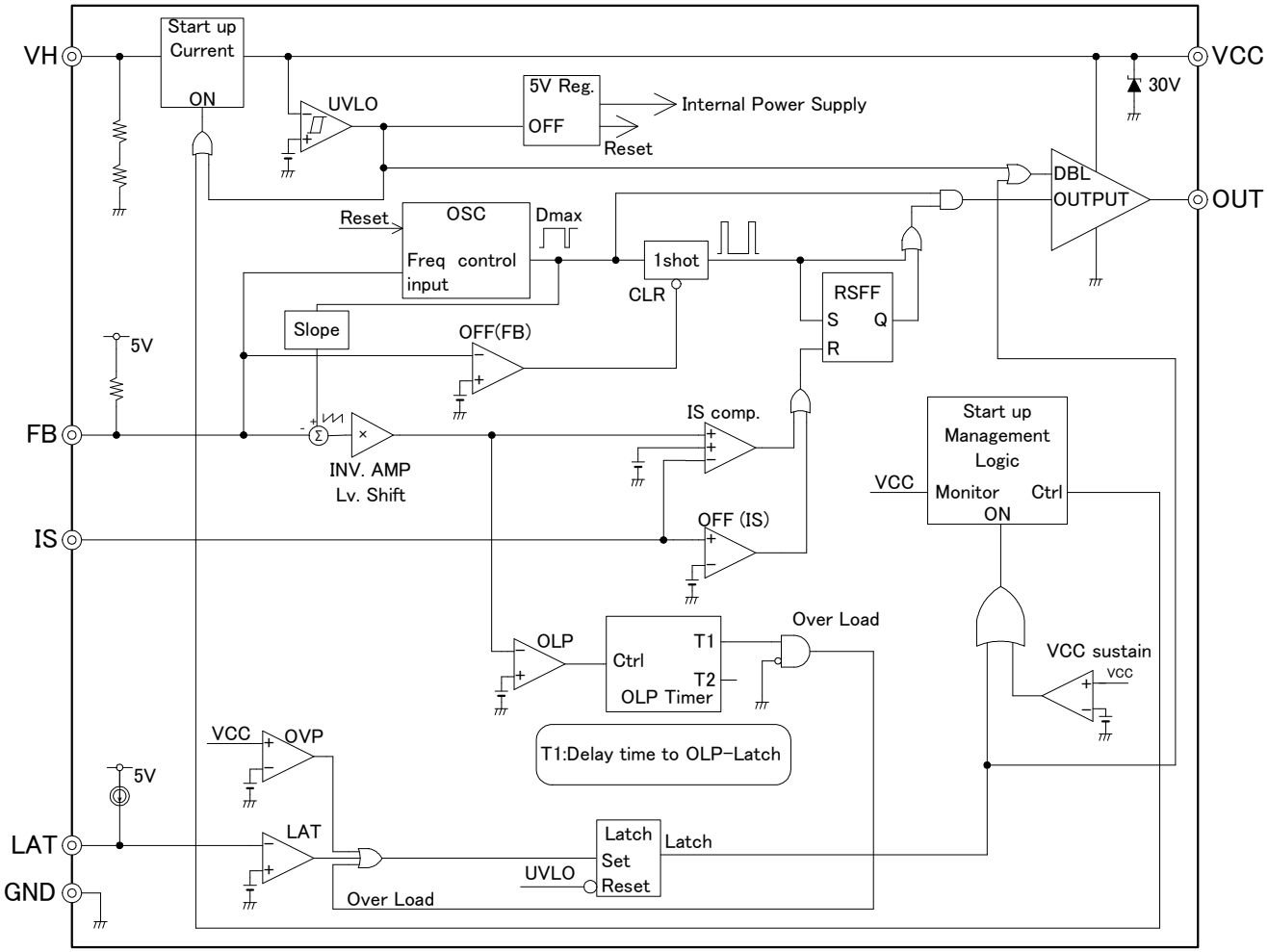
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Unit :(mm)

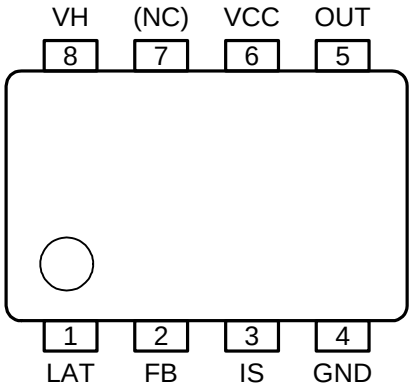
4. Block diagram

FA5639 (Over Load Protection: Latch Shutdown type)



5. Functional description of pins

Pin No.	Pin Name	Pin function
1	LAT	External latch signal
2	FB	Feed back input
3	IS	Current sense (Input)
4	GND	Ground
5	OUT	Driver Output
6	VCC	Power supply
7	(NC)	(unused)
8	VH	High voltage input (750V max.)



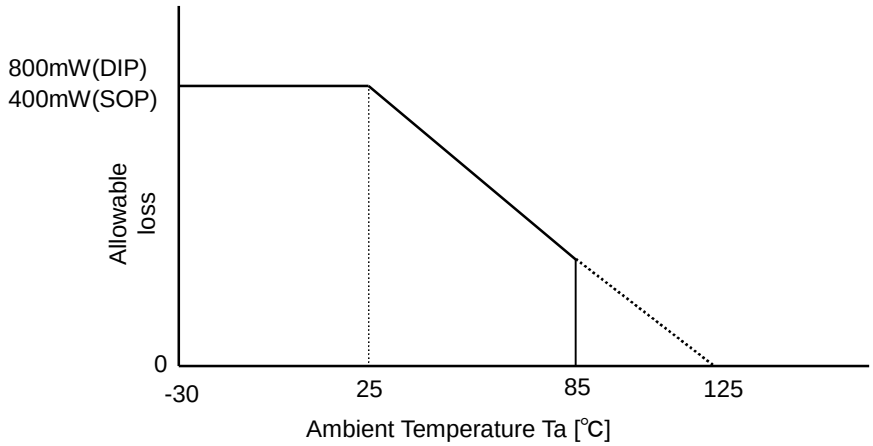
6. Rating & characteristics

"+" shows sink and "–" shows source in current prescription.

(1) Absolute maximum rating

Item		Symbol	Rating	Unit
Power supply voltage		VCC	28	V
OUT pin output peak current		IOH	-0.5	A
		IOL	+1.0	A
OUT pin voltage		VOUT	-0.3 to VCC+0.3	V
FB pin voltage		VFB	-0.3 to 5.0	V
IS pin voltage		VIS	-2.0 to 5.0	V
LAT pin voltage		VLAT	-0.3 to 5.0	V
VH pin input voltage		VVH	-0.3 to 750	V
Total loss (Ta=25℃)	SOP	Pd	400	mW
	DIP	Pd	800	mW
Junction temperature in operation		Tj	-30 to +125	℃
Storage temperature		Tstg	-40 to +150	℃

Allowable loss reduction characteristics



(2) Recommended operating condition

Item	Symbol	MIN	TYP	MAX	Unit
VCC Power supply voltage	VCC	10	18	24	V
High input voltage	VVH	80		650	V
VH pin Resistance	RVH	2		10	kΩ
LAT pin capacity	CLAT	0.22	1.0	2.2	uF
VCC pin capacity	CVCC	10	33	100	uF
Operating ambient temperature	Ta	-30		85	℃

(3) Electric characteristics (in case nothing specified : Tj=25℃,VCC=18V)

Switching oscillator section (FB pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Oscillation frequency	Fosc	FB=2V	90	100	110	kHz
Voltage stability	Fdv	VCC=10V to 24V	-2	—	+2	%
Temperature stability	Fdt	Tj= -30 to 125℃	-5	—	+5	%
Jitter range	⊿Fm		±4.0	±6.5	±9.0	%
FB pin threshold voltage for light load mode	Vfbm		1.05	1.20	1.35	V
FB pin voltage at minimum frequency	Vfmin		0.7	0.8	0.9	V
Oscillation frequency reduction ratio	kf	Δf/ΔVFB	200	240	280	kHz/V
Minimum oscillation frequency	Fmin		0.25	0.45	0.65	kHz

External latch shutdown signal (LAT pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Source current of LAT pin	Ilat	LAT=1.15V	-80	-70	-60	uA
Latch-off level	VthLAT		1.00	1.05	1.10	V
VthLAT/Ilat	RLAT		12	15	18	kΩ
Latch-off delay timer	TdLAT		50	65	80	us

Soft start signal (LAT pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Minimum pulse output voltage	Vss1	Start/Restart	1.9	2.1	2.3	V
Minimum pulse hold voltage	Vss2	Start/Restart	2.3	2.5	2.7	V
Soft start end voltage	Vss3		1.5	1.6	1.7	V

Pulse width modulation section (FB pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Maximum duty cycle	Dmax	VFB=4.5V	75	85	95	%
Minimum duty cycle	Dmin	VFB=0V	—	—	0	%
Input threshold voltage	VthFB0	DUTY=0%	340	400	460	mV
FB pin source current	Ifb0	VFB=0V	-320	-260	-200	uA

Over load protection (OLP) circuit section (FB pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Over load detection threshold voltage	VthOLP	VIS=VthIS1	3.7	4.2	4.7	V
Over load detection Delay time	TdOLP	VFB=4.7V	170	200	230	ms

Current sense section (IS pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Voltage gain	AvIS	ΔVFB/ΔVIS	-2.7	-2.3	-1.9	V/V
Maximum threshold voltage	VthIS1	VFB=4.7V	-1.07	-1.00	-0.93	V
Input bias current	IIS	VIS=0V	-50	-40	-30	uA
Minimum ON pulse width	Tmin1	Steady	650	900	1150	ns
	Tmin2	Start/Restart /OLP	180	280	380	
Delay to output	TpdIS	Tj=25℃	100	200	300	ns

VCC circuit section (VCC pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Start-up threshold voltage	VCCon		16	18	20	V
Shutdown threshold voltage	VCCoff		7.5	8.0	8.5	V
Hysteresis width	Vhys		8.0	10	12	V
VCC over-voltage protection threshold voltage	Vthovp	Tj=25℃	25	26	27	V

Output circuit section (OUT pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Low output voltage	VOL	IOL=100mA, VCC=18V	0.4	0.8	1.6	V
High output voltage	VOH	IOH= -100mA,VCC=18V	14.5	16	18	V
Rise time	tr	CL=1nF,Tj=25℃	30	60	100	ns
Fall time	tf	CL=1nF,Tj=25℃	20	40	70	ns

High-voltage input section (VH pin , VCC pin)

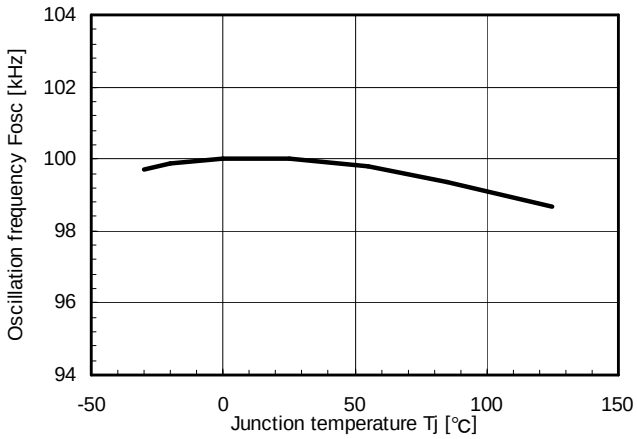
Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Current of VH pin	IHrun	VH=450V,VCC>VCCon	60	100	140	uA
	IHstb	VH=120V,VCC=0V	3.5	6.5	9.5	mA
VCC voltage at Latch	VCCLHH	1time clamp	13	14.5	16	V
	VCCLH	VCC rising	12	13	14	
	VCCLL	VCC falling	11	12	13	
VCC clamp voltage at operating by Start-up Circuit	VCCclp3	VCC rising	11.5	12.5	13.5	V
	VCCclp4	VCC falling	10	11	12	
Charge current for VCC pin	Ipre1	VCC=16V,VH=120V	-14	-8.0	-3.5	mA
	Ipre2	VCC=11V,VH=120V	-18	-12	-6.0	

Power supply current (VCC pin)

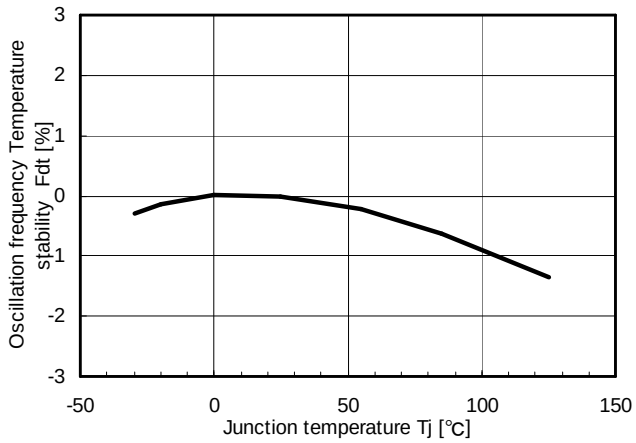
Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Operating-state supply current	ICCop1	Duty cycle=Dmax FB=2V OUT=No Load	1.0	1.45	1.75	mA
	ICCop2	Duty cycle=0% FB=0V	0.95	1.35	1.65	mA
Latch mode supply current	ICClat	FB=open, VCC=11V	600	900	1100	uA
VCC pin zenner clamp voltage	VCCzd		28	30	34	V

7. Characteristic curve

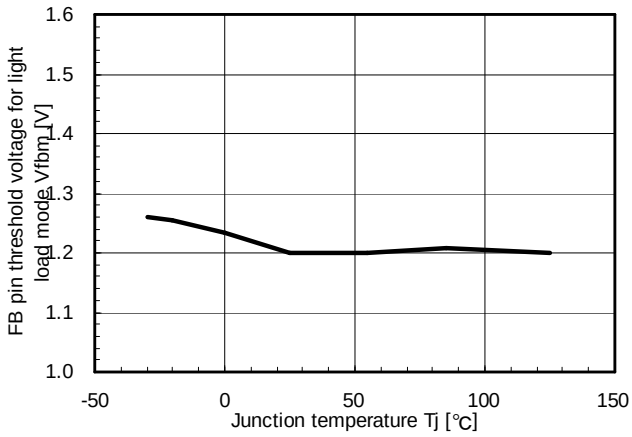
Oscillation frequency vs Junction temperature (Tj)



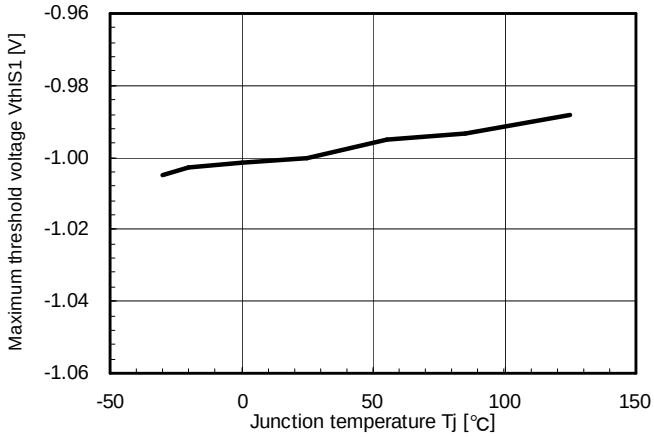
Fdt vs Junction temperature (Tj)



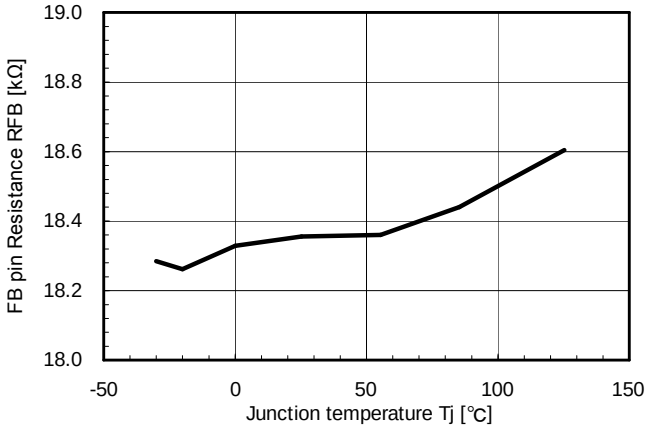
Vfbm vs Junction temperature(Tj)



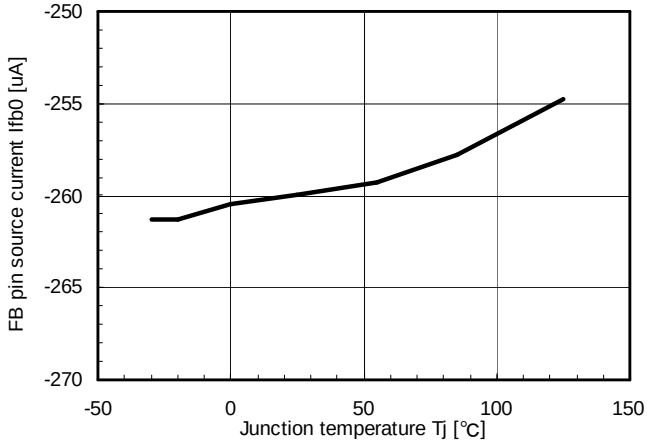
Maximum threshold voltage vs Junction temperature (Tj)



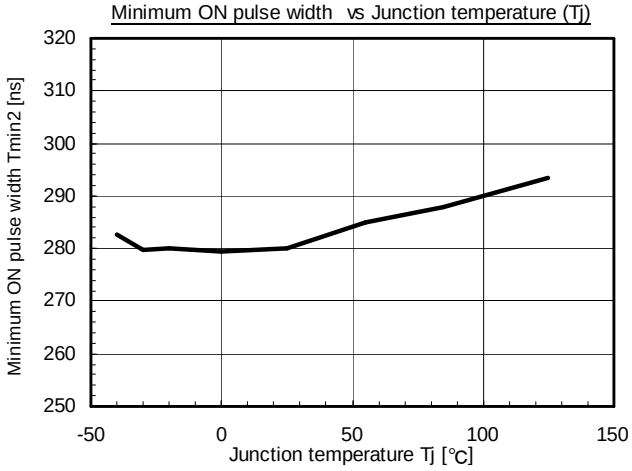
FB pin Resistance (RFB) vs Junction temperature (Tj)



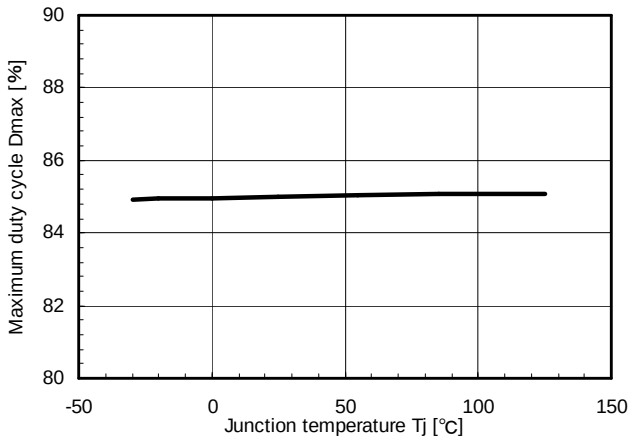
FB pin source current vs Junction temperature(Tj)



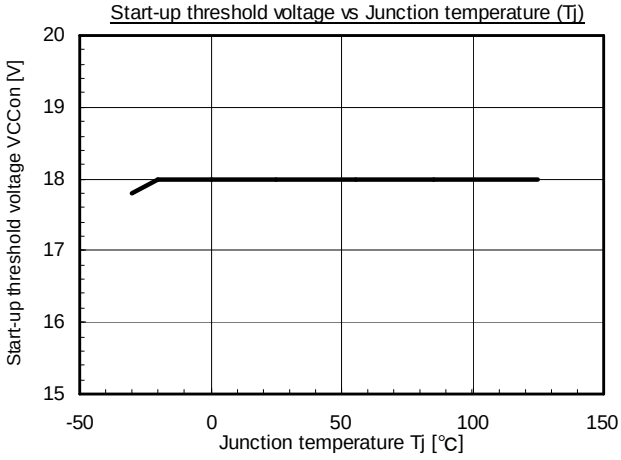
Minimum ON pulse width vs Junction temperature (Tj)



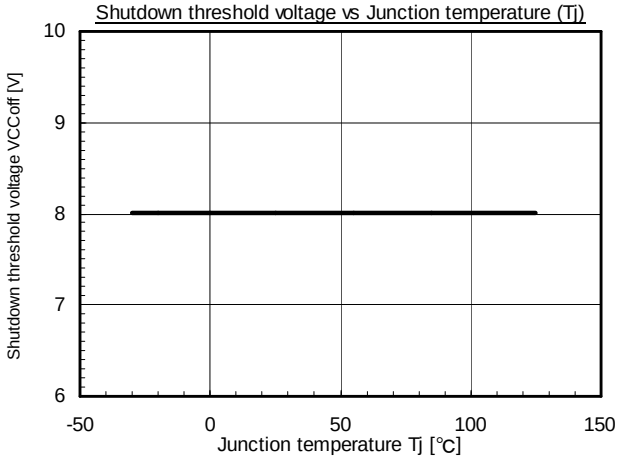
Maximum duty cycle vs Junction temperature (Tj)



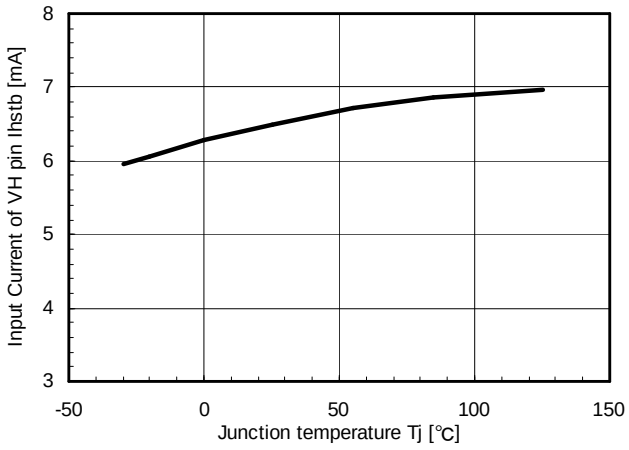
Start-up threshold voltage vs Junction temperature (Tj)



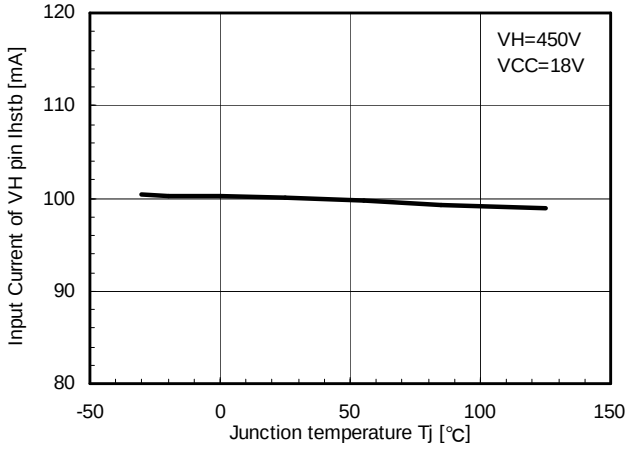
Shutdown threshold voltage vs Junction temperature (Tj)



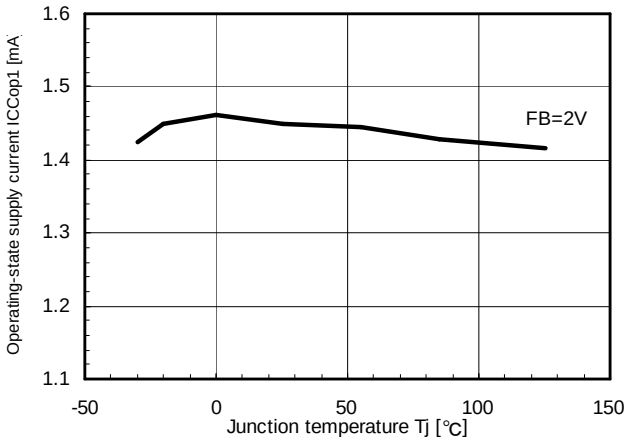
Input Current of VH pin vs Junction temperature (Tj)



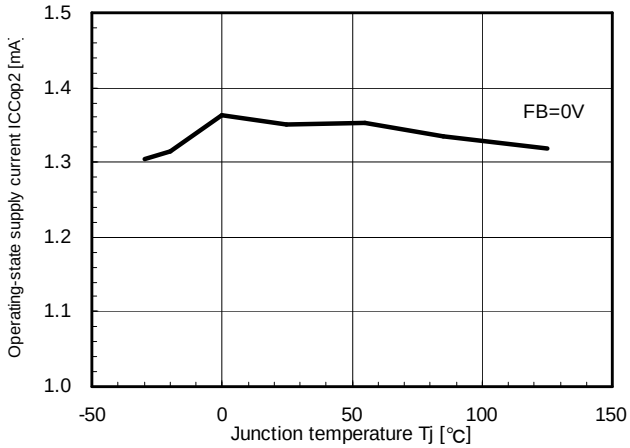
Input Current of VH pin vs Junction temperature (Tj)



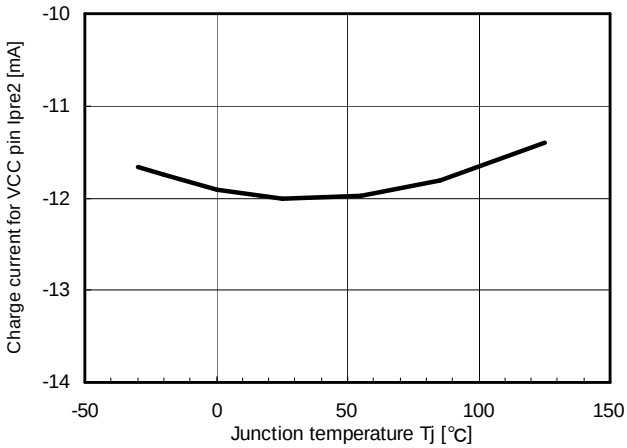
Operating-state supply current vs Junction temperature (Tj)



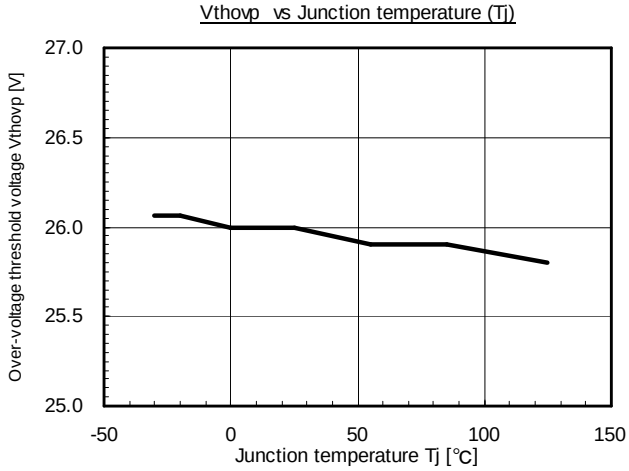
Operating-state supply current vs Junction temperature (Tj)



Charge current for VCC pin vs Junction temperature (Tj)



Vthovp vs Junction temperature (Tj)



8. Operation of each block

(1) Startup circuit

The IC integrates a startup circuit having withstand voltage of 750V to achieve low power consumption.
Fig.1 to Fig.3 show connections.
Turning on the power, capacitor C2 connected to the VCC terminal is charged and the voltage increases due to the current fed from the startup circuit to the VCC terminal. If the ON threshold voltage of the under-voltage lockout circuit (UVLO) is exceeded, the power for internal operation is turned on, and the IC starts operating.
The current supplied from the VH terminal to the VCC terminal is approximately 6.5mA(Typ.) when VCC = 0V. As the VCC voltage increases, the supply current decreases.
A resister of 2kΩ is connected in series to the VH terminal for short-circuit protection of the VCC terminal.

Fig.1 shows a typical connection where the VH terminal is connected to the half-wave rectifier circuit of AC input voltage.
The startup time of this connection is the longest in 3 types of connection.

Fig.2 shows the connection where the VH terminal is connected to the full-wave rectifier circuit of AC input voltage. The startup time of this connection is approximately half of the connection shown in Fig.1.

Fig.3 shows the connection where the VH terminal is connected to the back of rectification and smoothing of AC input voltage. The startup time of this connection is the shortest in 3 types. In this connection, however, even if the AC input voltage is shut down after the IC enters the latch mode, the voltage charged in C1 is kept impressed to the VH terminal, requiring much time for the latch mode to be reset. It takes approximately several minutes to reset the latch mode, although the time varies depending on conditions.

If the VCC terminal voltage exceeds the ON threshold voltage and the IC starts operating, the startup circuit is shut down and the VH terminal current decreases to several 10 to several 100uA.

After the startup, the IC goes into switching operation, and is operated with the power supplied from the auxiliary winding. If the overload or overvoltage protection is actuated, causing the IC to enter the latch mode, then the startup circuit is subjected to ON/OFF control to maintain the VCC voltage within the 12V to 13V (typ.) range.

At light load or during OCP delay time, the Vcc voltage avoids dropping to UVLO off threshold level.
Then the startup circuit is subjected to ON/OFF control to maintain the VCC voltage within the 11V to 12.5V (typ.) range.

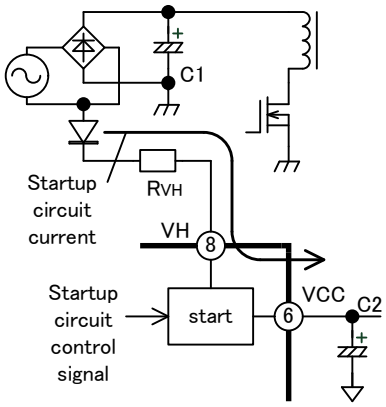


Fig.1 Startup circuit 1 (Half-wave)

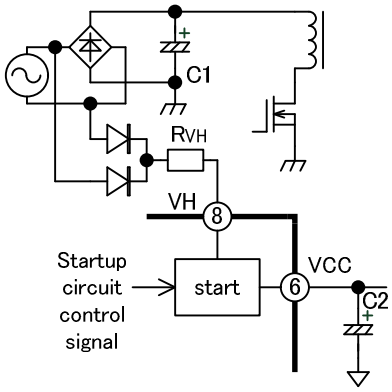


Fig.2 Startup circuit 2 (Full-wave)

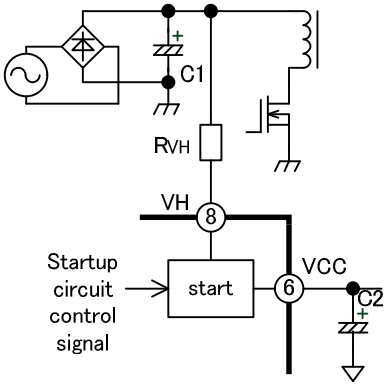


Fig.3 Startup circuit 3 (Rectification)

(2) Oscillator

This oscillator is used to determine the switching frequency. The switching frequency in the normal operation mode is set to 100kHz within the IC.

To minimize the loss of power in the standby state, this IC is equipped with a function of automatically decreasing the switching frequency under light load.

When the FB terminal voltage decreases down to 1.2V (typ.) or lower under light load, the frequency decreases almost linearly proportional to the FB terminal voltage.(See Fig.4) The minimum frequency, Fmin, has been set to 0.45kHz (typ.).

In addition to trigger signals for determining switching frequency, the oscillator generates pulse signals for determining the maximum duty cycle and ramp signals for performing slope compensation.

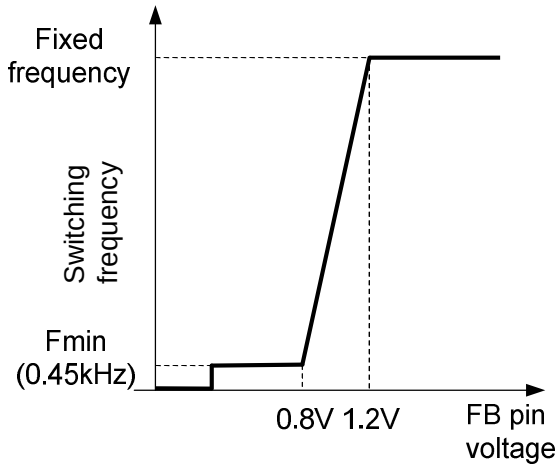


Fig.4 Oscillation frequency

(3) Current comparator & PWM latch circuit

The IC performs current mode control. Fig.5 shows a circuit block for basic operations, and Fig.6 shows a timing chart.

The polarity of the current detection voltage of the IS terminal is negative. The GND of the IC is connected between the current detection resistor Rs and the MOSFET. (See Fig.5)

A trigger signal having the switching frequency that is output from the oscillator is input to the PWM latch (F.F.) through the one-shot circuit as a set signal. Then the output of the PWM latch as well as the OUT terminal voltage reaches the High state.

On the other hand, the current comparator (IS comp.) monitors the MOSFET current, and if the threshold voltage is reached, a reset signal is output. When a reset signal is input, the output of PWM latch (F.F.) as well as the OUT terminal voltage reaches the Low state.

The ON pulse width of the OUT terminal is thus controlled with the threshold voltage of the current comparator (IS comp.).

The output is controlled by changing the threshold voltage of this IS comp. with feedback signals.

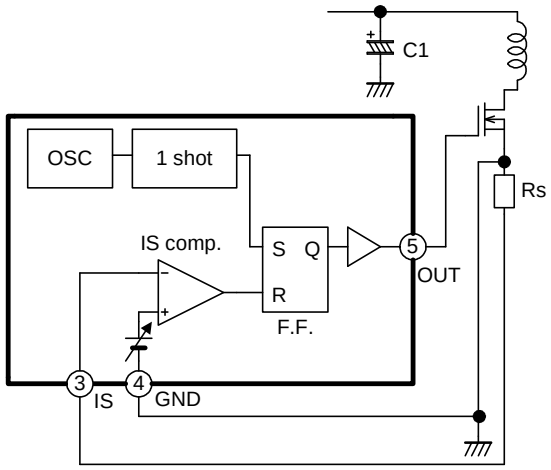


Fig.5 Current mode basic operation circuit block

As shown in Fig.7, the FB terminal voltage is level-shifted by a reverse amplifier and input into the current comparator (IS comp.) as the threshold voltage. In addition, -1V reference voltage is input inside the IC to regulate the maximum input threshold voltage of the IS terminal, VthIS1 (overcurrent control threshold).

The reverse amplifier output or the maximum IS terminal input threshold voltage, VthIS1, whichever is higher, is given precedence as the IS terminal threshold voltage.

(Example: When the output of the reverse amplifier is -0.5V in a product whose maximum threshold voltage of the IS terminal, VthIS1, is -0.5V, the output of the reverse amplifier is given precedence and thus the current comparator is reversed when the IS terminal voltage reaches -0.5V.)

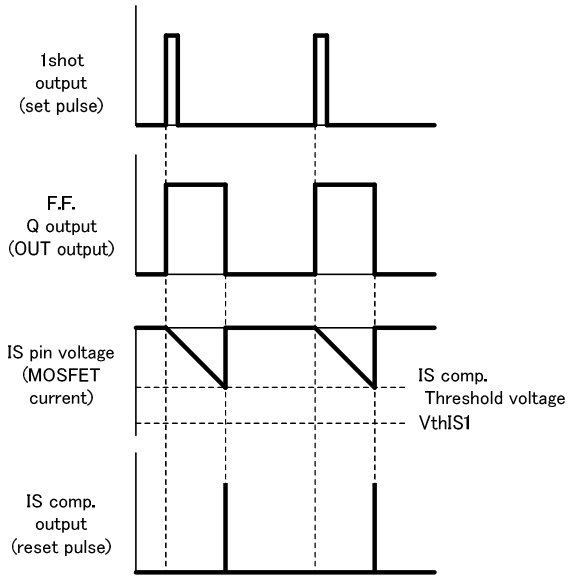


Fig.6 Current mode basic operation timing chart

In normal operation, the output voltage of the power supply is maintained constant by changing the threshold voltage of the current comparator via the FB terminal voltage.
When the output voltage decreases, the feedback circuit increases the FB voltage to allow the threshold voltage of the current comparator to scale out to Low, thus increasing the MOSFET current.
The maximum input threshold voltage of the IS terminal, VthIS1 (-1V) controls the maximum current of the MOSFET.
If the FB terminal voltage increases under overload, the output of the reverse amplifier scales out to Low, decreasing down to lower than VthIS1. The threshold voltage of the IS terminal is thus controlled not to exceed VthIS1.
The oscillator outputs pulses for determining the maximum duty cycle. Using these pulses, the maximum duty cycle has been set to 85% (typ.).

(4) One shot circuit (minimum ON width)

When the MOSFET is turned on, a surge current is generated due to discharge corresponding to the capacitance of the main circuit and gate drive current. If this surge current reaches the IS terminal threshold voltage, the current comparator output is reversed, and consequently normal pulses may not be generated from the OUT terminal.
To avoid this phenomenon, a minimum ON width of OUT terminal output is set within the one-shot circuit block of the IC.
If a trigger signal having the switching frequency is input from the oscillator, a pulse having a specific width is output as a PWM latch (F.F.) set signal.
Since the set signal has priority over the input signal of the PWM latch, the output of the PWM latch (F.F.) is not reversed while the set signal from the one-shot circuit is being input, even if a reset signal is input from the current comparator (IS comp.) (See Fig.5)
As a result, the input to the IS terminal is kept invalid for the specified period of time immediately after the output pulse is generated from the OUT terminal (minimum ON width), and made not to respond to the surge current at turn-on. (See Fig.8)
This minimum ON width function eliminates the need of a noise filter for the IS terminal in principle.
The minimum ON width is usually set to 900ns (typ.) in normal operations, and to 280ns (typ.) at startup or rebooting to prevent the transient MOSFET drain voltage from surging.

In addition, an exclusive comparator is integrated to keep the output pulse at zero under no load. (See Fig.9)
This comparator reverses its output when the FB terminal voltage decreases down to 400mV (typ.), preventing a set pulse to be input to the PWM latch (F.F.). The output is thus maintained in Low state and switching is stopped.

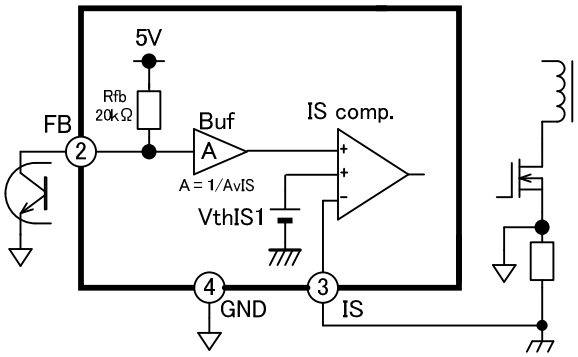


Fig.7 Current comparator

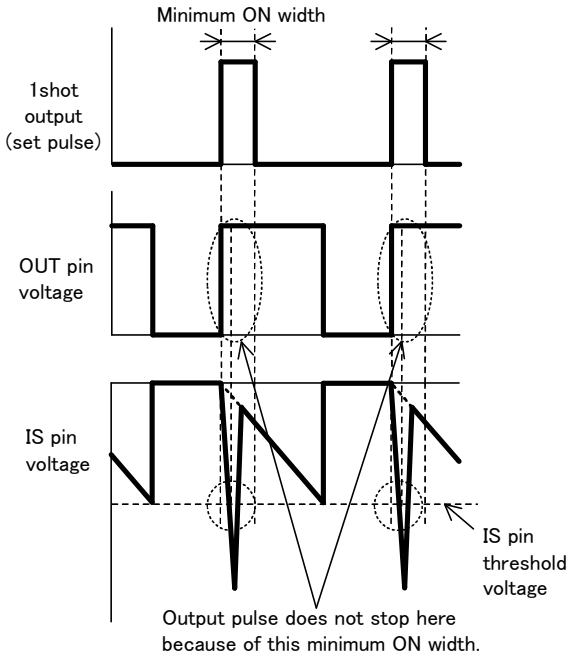


Fig.8 Minimum ON width

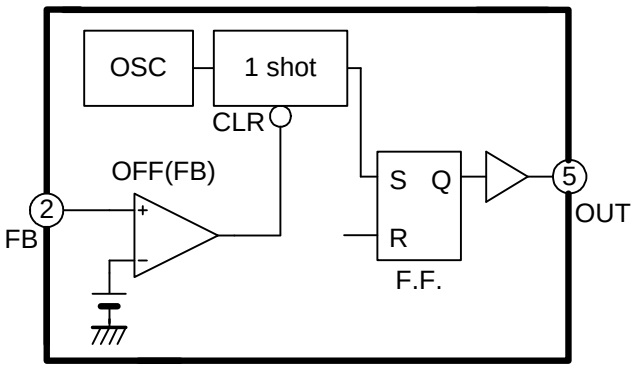


Fig.9 Output shutdown function of FB pin

(5)Overload protection circuit

Detecting overload, the overload protection (OLP) circuit stops switching in case overload is continued for a specified period of time (200ms typ.) to protect the circuit. Overload detection is performed based on the FB terminal voltage.
Fig.10 is a conceptual diagram of the operation. Fig.11 shows a circuit block.

The overload protection is actuated when FB terminal voltage processed into a signal is detected with the OLP comparator, based on the overload delay time TdOLP (200ms typ.),which is the period from the overload detection with the built-in OLP timer to switching pulse stop

When the output current increases and the FB terminal voltage increases up to VthOLP (4.2V typ.), overload is detected. Since the IS terminal voltage is equivalent to the maximum input threshold voltage VthIS1 (-1.0V typ.) at this time, the MOSFET current is limited, and the output voltage is no longer maintained. As soon as the overload is detected, the OLP timer starts counting the delay time up to the stop of the switching pulse. When specified overload protection delay time TdOLP (200ms typ.) has elapsed, the switching pulse output is stopped. If overload is reset and the FB voltage decreases down to VthOLP (4.2V typ.) before the overload protection delay time expires, switching continues.

By interrupting the input voltage to decrease the VCC voltage to the OFF threshold voltage (8V typ.) or lower, the latch mode can be reset.

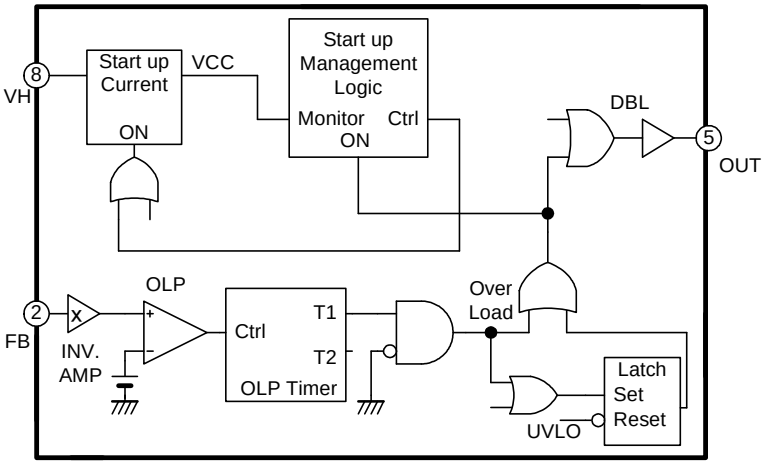


Fig.10 Overload protection circuit

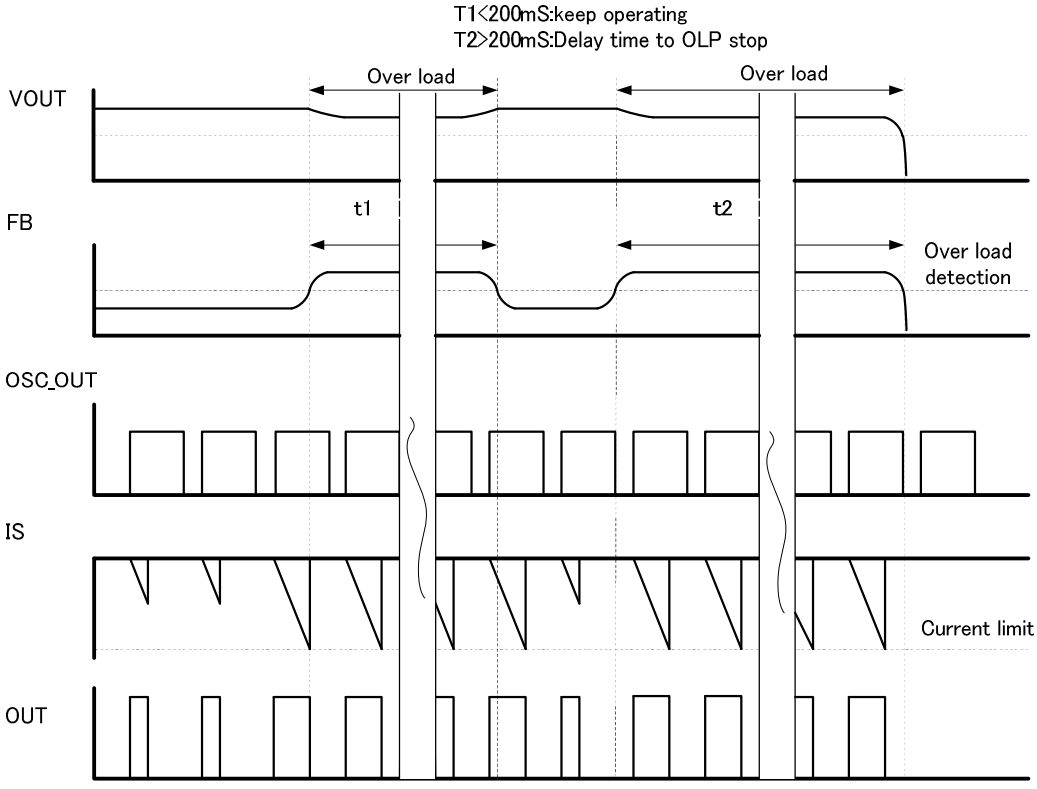


Fig.11 Overload protection timing chart (latch)

(6) Overvoltage protection circuit (VCC terminal)

The IC integrates an overvoltage protection circuit for monitoring the VCC terminal voltage. (See Fig.12)
If the VCC voltage increases and exceeds 26V typ., which is the reference voltage of the comparator (OVP), the comparator output is reversed to High level, setting the latch circuit to perform latch shutdown.
At this time, the startup circuit is subjected to ON/OFF control to maintain the latch mode, thus keeping the VCC voltage within the 12V or 13V (typ.) range.
To cancel the latch mode, shut down the input voltage to cause brownout, as in the case of the overload protection.(latch type)
Since 65μs (typ.) delay time has been set to the set input of the latch circuit, the latch mode is not entered even if the VCC terminal exceeds the detection voltage temporarily.

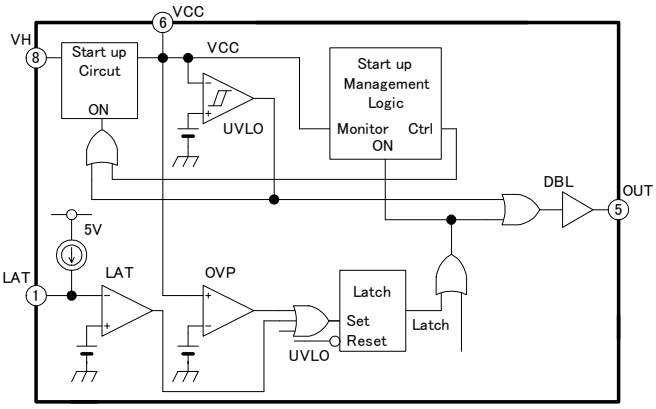


Fig.12 Overvoltage protection circuit

(7) Latch shutdown circuit by an external signal

The LAT terminal is equipped with a latch shutdown function. (See Fig.13)
By decreasing the LAT terminal voltage to 1.05V or lower, the IC enters the latch mode.
To cancel the latch mode, shut down the input voltage to cause brownout, as in the case of the OVP. (former section)

If the external latch shutdown function by the LAT terminal is not to be used, connect a capacitor only.

Connect an NTC thermistor to the LAT terminal to use the overheat protective function.

(8) Undervoltage lockout circuit (VCC terminal)

The IC integrates an undervoltage lockout (UVLO) function to prevent circuit malfunction that might occur when power supply voltage decreases. When the VCC voltage increases from 0V and reaches 18V (typ.), the circuit starts operating. When the VCC decreases down to 8V (typ.), the circuit stops operating.
In a state in which the undervoltage lockout function is actuated to stop IC operation, the OUT terminal is forcibly made to enter the Low state. The latch mode of the protection circuit is also reset.

(9) Output circuit

The push/pull structure output circuit drives the MOSFET directly. The peak output current of the OUT terminal is 0.5A (source) and 1.0A (sink) in the maximum absolute ratings.
In a state in which the IC is stopped in the undervoltage lockout circuit or operation is suspended in the latch mode, or in an auto reset wait state by overload protection function, the OUT terminal is brought into the Low level, and the MOSFET is interrupted.

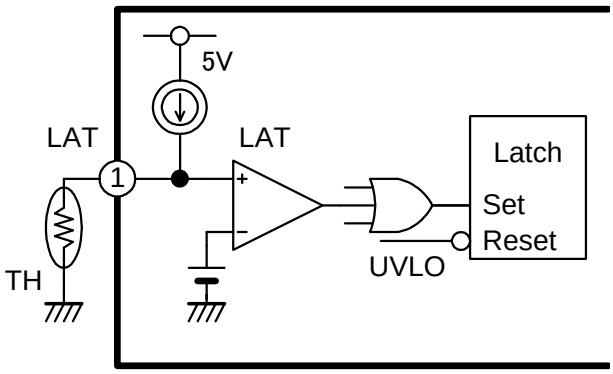


Fig.13 Overheat protection function using a thermistor

9. Advice for designing

(1) Startup

To properly start or stop the power supply, a capacitor having appropriate capacitance must be selected.
Fig.14 shows the VCC voltage at the time of startup when an appropriate capacitor is connected.
When the power is turned on, the capacitor of the VCC is charged with the current supplied from the startup circuit, and the voltage increases.
When the VCC reaches the ON threshold voltage, the IC starts operating. The IC is operated based on the voltage supplied from the auxiliary winding. Note that during the period immediately after startup until the voltage of the auxiliary winding starts up, the VCC decreases. Select a capacitor for the VCC that does not allow the VCC to decrease down to the OFF threshold voltage.
Specifically, a VCC terminal capacitor whose OFF threshold voltage is 9V or higher is recommended.

If the capacitance of the VCC terminal is too small, VCC decreases to lower than the OFF threshold voltage before the voltage of the auxiliary winding starts up as shown by Fig.15. In this case, the VCC repeats up/down operation between ON and OFF threshold voltages, and consequently the power supply cannot be turned on.

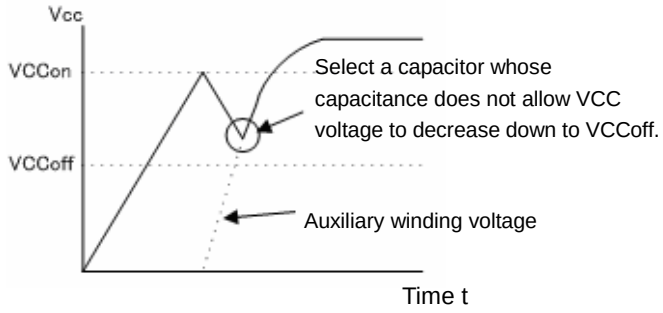


Fig.14 VCC terminal voltage at startup

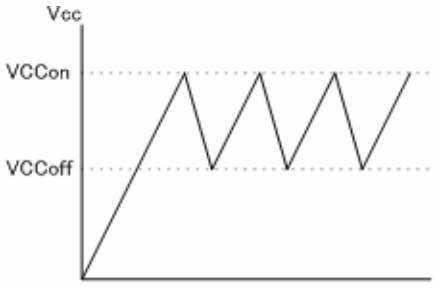


Fig.15 VCC terminal voltage at startup (when capacitance is too small)

(2) VCC hold time

To prevent the VCC terminal voltage from decreasing to lower than the UVLO OFF threshold voltage due to sudden load change and other reasons, it may be desirable that the capacitance of the capacitor to be connected to the VCC terminal be made larger.
However, if the capacitance of the capacitor of the VCC terminal is increased, the startup time is made longer.
In such cases, the circuit shown in Fig.16 can balance the capacitance and the startup time.
By setting C1 to less than C2, the startup time can be kept short. Since current is supplied via C2 after startup, the VCC terminal voltage hold time can be kept long even under sudden change conditions.

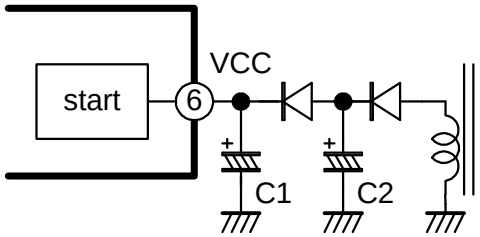


Fig.16 VCC circuit

(3) Gate drive circuit

To adjust switching speed and prevent vibration of the gate terminal, a resistor is connected between the MOSFET gate terminal and the OUT terminal of the IC in general.
In some cases, driving current for turning on the MOSFET and that for turning it off are required to be determined separately.
In this case, connect a gate drive circuit shown in Fig.17 or 18 between the gate terminal of the MOSFET and the OUT terminal.

In Fig.17, the current is limited by R1 and R2 when the power is turned on, while the current is limited only by R2 when it is turned off.
In Fig.18, the current is limited only by R1 when the power is turned on, while the current is limited by R1 and R2 connected in parallel when the power is turned off.

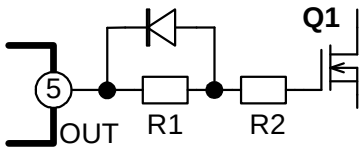


Fig.17 Gate drive circuit (1)

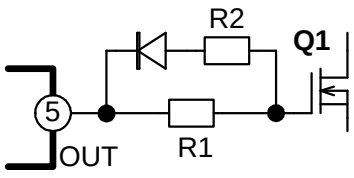


Fig.18 Gate drive circuit (2)

(4) LAT terminal

• To perform overheat protection using an NTC thermistor

As shown in Fig.13, thermistor TH1 is connected to the LAT terminal to perform overheat protection (latch shutdown).

Since the LAT terminal source current is 70μA (min.), select TH1 whose resistor Rth satisfies the following expression at the desired overheat protection temperature. If temperature setting for overheat protection is not feasible with TH1 only, connect an additional resistor in series for adjustment.

$$Rth \leq 1.05V / 70\mu A \approx 15.0k\Omega$$

In addition, the VthLAT tolerance calculates by RLAT (Min-Max) resistance.

It does not depend on the calculation of ILAT and VthLAT (Min & Max).

• To perform latch shutdown using an independent abnormality detection signal

To perform latch shutdown with an external signal, connect a peripheral circuit, allowing the LAT terminal voltage to be kept below 1.0V. Fig.19 shows a typical circuit connection.

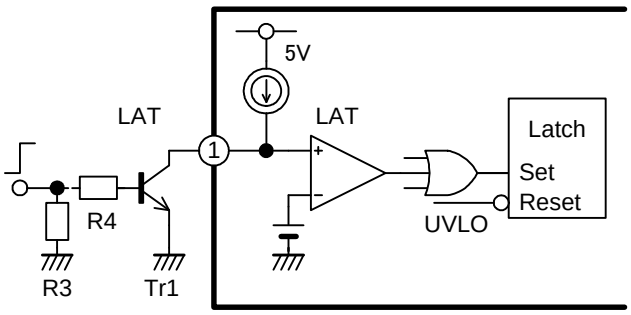


Fig19.Latch shutdown function by an external signal

(5) Feedback

Fig.20 shows the circuit configuration of the FB terminal.

A photo-coupler PC is connected as a feedback circuit that monitors the output voltage and performs PWM control.

This signal gives threshold voltage for the current comparator. Consequently, if noise is added to this signal, the output pulses are disturbed. Capacitor C3 is generally connected for protection against noise.

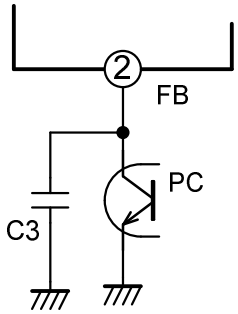


Fig.20 FB terminal circuit configuration

(6) Current sensing unit

As described in 8-(4) One-shot circuit, the minimum ON width is set for this IC to minimize malfunction due to surge current that occurs when the power MOSFET is turned on.

However, if the surge current that occurs at the time of power ON is large, or noise is applied externally at the time of power ON, malfunction might occur.

In such cases, add RC filters C6 and R7 as shown in Fig.21.

To ensure efficient operation of the capacitor C6, place it as close to the IC as possible, and lay wiring with extreme care.

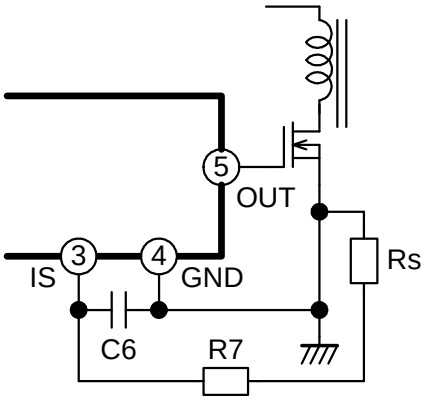


Fig.21 IS terminal filter

(7) Improvement of input power at light load

The IC integrates the function of reducing standby power consumption by lowering oscillation frequency under light load.

However, since load conditions vary depending on the power supply setting, the settings within the IC may be insufficient to reduce standby power consumption.

In such cases, connect resistor R8 as shown in Fig.22 to reduce oscillation frequency.

Since the input impedance of the IS terminal is about 100kΩ, resistor R8 shall be several 100kΩ to MΩ.

As shown in Fig.23, by connecting the resistor between the OUT terminal and the IS terminal, the same light-load correction effect can be obtained and in addition, the loss of resistor R8 can be reduced compared to the case in which it is connected to the VCC terminal.

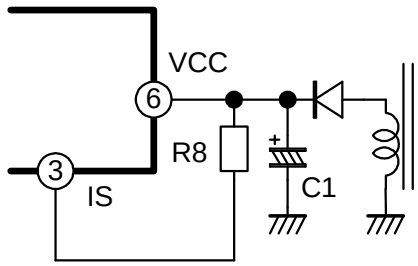


Fig.22 Correction circuit for improvement of input power under light load(1)

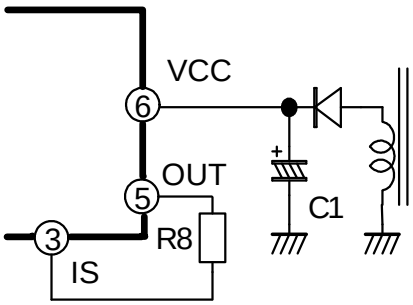


Fig.23 Correction circuit for improvement of input power under light load(2)

(8) Reduction of dependency of overload detection level on input voltage

Since the gradient of the inductor current of a transformer varies depending on the input voltage in the overload protection function, the current value determined to be overload also varies. The higher the input voltage, the higher the output current that causes overload shutdown to occur.

As shown in Fig.24. resistor R9 can be connected between the auxiliary winding and the IS terminal to minimize the dependency of the overload detection level on input voltage (IS terminal line correction).

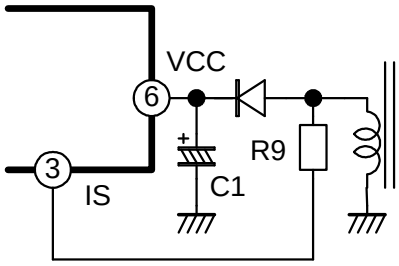


Fig.24 Reduction of dependency of overload detection level on input voltage

(9) Prevention of malfunction due to negative potential of the terminal

If large negative voltage is applied to each terminal of the IC, the parasitic element within the IC may be actuated, thus causing malfunction to occur. Be sure to maintain the voltage to be applied to each terminal within the maximum absolute ratings.

(10) Loss calculation

To use the IC within its ratings, the loss of the IC may have to be found. However, it is not feasible to measure loss directly. The following is an example of finding a rough value of loss by calculation.

The rough value of the total loss of the IC, Pd, can be calculated using the following expression:

Pd=VCC × (ICCop1 + Qg × fsw) + VVH × IHrun

where,

VVH: voltage to be applied to the VH terminal,

IHrun: current fed to the VH terminal during operation,

VCC: power voltage,

ICCop1: Consumption current of the IC

Qg: electrical charge to be input to the MOSFET gate used, and

Fsw: switching frequency.

A rough value can be found using the above expression, and the total loss found by the calculation, Pd, is slightly larger than the actual value.

Be sure to take into consideration that each characteristic value varies depending on temperatures and other factors.

Example:

When the VH terminal is connected to a half-wave rectifier circuit with 100VAC input, the average voltage to be applied to the VH terminal is calculated to be approximately 45V.

Furthermore, assuming that Tj = 25°C, VCC = 18V, and Qg = 80nC, and based on

IHrun=100uA (typ.)

ICCop1=1.45mA (typ.)

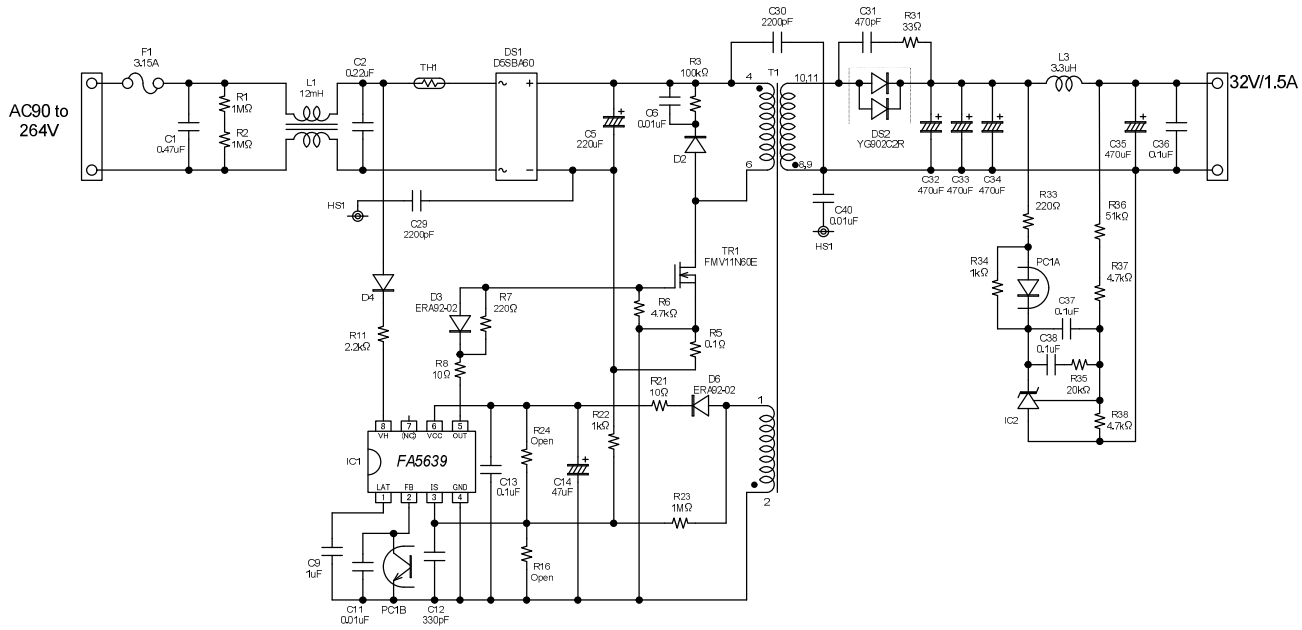
fsw=100kHz (typ.)

the loss of the IC having standard characteristics can be calculated as follows:

Pd=18V ×(1.45mA + 80nC × 100kHz) + 45V × 100uA

= 174.6 mW

10. Application circuit example



Note)

This application circuit example shows typical directions for use of this IC for reference and does not guarantee the operation and characteristics.

- Be sure to connect C13 (0.1 uF to 1 uF) to the VCC terminal in order to eliminate high-frequency noise.