



J111 J112 J113

N-CHANNEL SILICON JUNCTION FIELD EFFECT TRANSISTORS

MICRO ELECTRONICS

J111, J112, J113 are N-channel silicon junction field effect transistors designed for analog switching, choppers and commutators applications.

T0-92



DSG

ABSOLUTE MAXIMUM RATINGS

Gate-Source Voltage	V _{GS}	-35V
Gate Current	I _G	50mA
Total Power Dissipation (T _A =25°C)	P _{tot}	350mW
Power Derating (to 125°C)		3.5mW/°C
Operating Junction & Storage Temperature	T _j , T _{stg}	-55 to +125°C

ELECTRICAL CHARACTERISTICS (T_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Gate-Source Breakdown Voltage	BV _{GSS}	-35			V	I _G =-1μA V _{DS} =0
Gate Reverse Current (note 1)	I _{GSS}			-1	nA	V _{GS} =-15V V _{DS} =0
Drain Saturation Current J111	I _{DSS} *	20			mA	V _{DS} =15V V _{GS} =0
J112		5			mA	V _{DS} =15V V _{GS} =0
J113		2			mA	V _{DS} =15V V _{GS} =0
Drain Cutoff Current (note 1)	I _{D(off)}			-1	nA	V _{DS} =5V V _{GS} =10V
Gate-Source Pinchoff Voltage	V _p				V	I _D =1μA V _{DS} =5V
J111		-3	-10		V	I _D =1μA V _{DS} =5V
J112		-1	-5		V	I _D =1μA V _{DS} =5V
J113	-0.5	-3		V	I _D =1μA V _{DS} =5V	
Drain-Source On Resistance J111	r _{DS(on)}			30	Ω	V _{GS} =-10V V _{DS} ≤0.1V
J112				50	Ω	V _{GS} =-10V V _{DS} ≤0.1V
J113				100	Ω	V _{GS} =-10V V _{DS} ≤0.1V
Turn On Delay Time	t _{d(on)}		7		ns	
Rise Time	t _r		6		ns	
Turn Off Delay Time	t _{d(off)}		20		ns	
Fall Time	t _f		15		ns	

note 1 : Approximately doubles for every 10°C increase in T_A.

* Pulse Test : Pulse Width = 0.3ms, Duty Cycle = 1%

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