2A, 6.5V, Ultra Low Noise, Ultra Low Dropout Linear Regulator

General Description

The RTQ2502A is a high-current (2A), low-noise (6μVrms), high accuracy (1% over line, load, and temperature), low-dropout linear regulator (LDO) capable of sourcing 2A with extremely low dropout (max. 125mV). The device output voltage is pin-selectable (up to 3.95V) using a PCB layout without the need of external resistors, thus reducing overall component count. Designers can achieve higher output voltage with the use of external resistor divider. The device supports single input supply voltage as low to 1.1V that makes it easy to use.

The low noise, high PSRR and high output current capability makes the RTQ2502A ideal to power noise-sensitive devices such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components. With very high accuracy, remote sensing, and soft-start capabilities to reduce inrush current, the RTQ2502A is ideal for powering digital loads such as FPGAs, DSPs, and ASICs.

The external enable control and power good indicator function makes the sequence control easier. The output noise immunity is enhanced by adding external bypass capacitor on NR/SS pin. The device is fully specified over the temperature range of T_J = –40°C to 125°C and is offered in the VQFN-20L 5x5 package.

Features

- **Input Voltage Range : 1.1V to 6.5V**
- **Two Output Voltage Modes**
  - **0.8 V to 5.5V (Set by a Resistive Divider)**
  - **0.8 V to 3.95V (Set via PCB Layout, No External Resistor Required)**
- **Accurate Output Voltage Accuracy (1%) Over Line, Load and Temperature**
- **Ultra High PSRR : 40dB at 500kHz**
- **Excellent Noise Immunity**
  - **6μV_{RMS} at 0.8V Output**
- **Ultra Low Dropout Voltage : 125mV at 2A**
- **Enable Control**
- **Programmable Soft-Start Output**
- **Stable with a 22μF or Larger Ceramic Output Capacitor**
- **Support Power-Good Indicator Function**
- **RoHS Compliant and Halogen Free**

Applications

- Portable Electronic Device
- Wireless Infrastructure : SerDes, FPGA, DSP
- RF, IF Components : VCO, ADC, DAC, LVDS

Marking Information



RTQ2502AGQV : Product Number

YMDNN : Date Code

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Ordering Information

RTQ2502A □□□

- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
- Package Type
  QV : VQFN-20L 5x5 (V-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

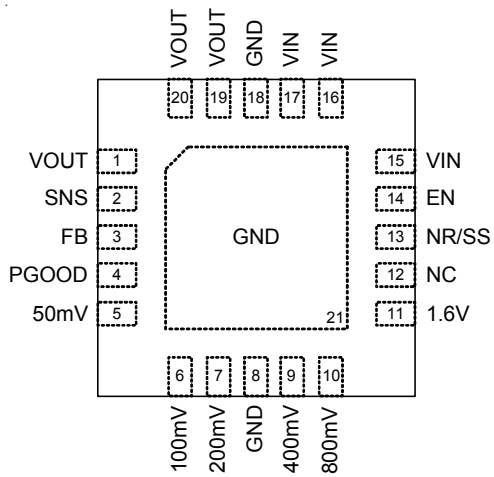
***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



VQFN-20L 5x5

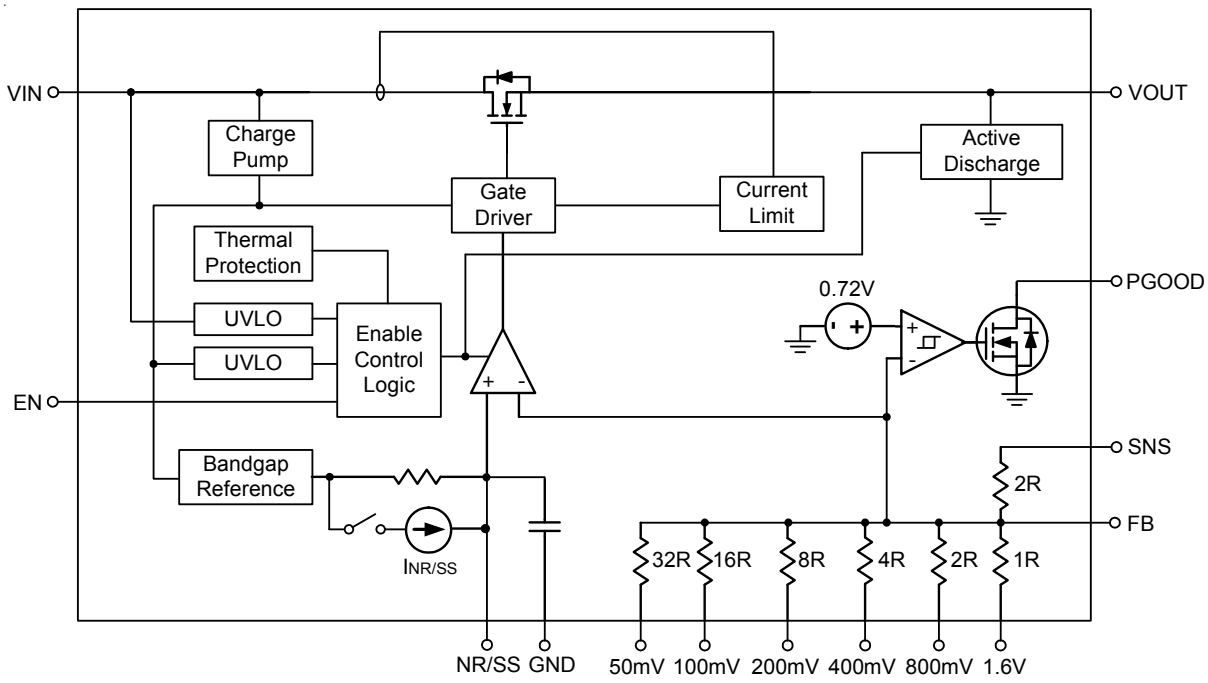
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Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 19, 20	VOUT	LDO output pins. A 22μF or greater of capacitance is required for stability. Place the output capacitor as close to the device as possible and minimize the impedance between VOUT pin to load.
2	SNS	Output voltage sense input pin. Connect this pin only if using PCB layout set the VOUT voltage (No External Resistor Required). Keep SNS pin floating if the VOUT voltage is set by external resistor.
3	FB	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.8V typically.
4	PGOOD	Power good indicator output. An open-drain output and active high when the output voltage reaches 88% of the target. The pin is pulled to ground when the output voltage is lower than its specified threshold, EN shutdown, OCP and OTP.
5, 6, 7, 9, 10, 11	50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	Output voltage setting pins. Connect these pins to ground or leave floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) if the VOUT voltage is set by external resistor.
8, 18, 21 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum the power dissipation.
12	NC	No internal connection. Leave these pins floating doesn't affect the chip functionality. By connecting these pins to GND, design engineers could extend the GND copper coverage on the PCB top layer to enhance the thermal convection.
13	NR/SS	Noise-reduction and soft-start pin. Decouple this pin to GND with an external capacitor $C_{NR/SS}$ can not only reduce output noise to very low levels but also slow down the VOUT rise like a soft-start behavior. For low noise applications, a 10nF to 1μF $C_{NR/SS}$ is suggested.
14	EN	Enable control input. Connecting this pin to logic high enables the regulator or driving this pin low puts it into shutdown mode. The device can have V_{IN} and V_{EN} sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Enabling the device after V_{IN} are present is preferred.
15, 16, 17	VIN	Supply input. A minimum of 22μF ceramic capacitor or greater of capacitance is required and should be placed as close as possible to this pin for better noise rejection.

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Functional Block Diagram



Operation

The RTQ2502A operates with single supply input ranging from 1.1V to 6.5V and capable to deliver 2A current to the output. The device features high PSRR and low noise provides a clean supply to the application.

A low-noise reference and error amplifier are included to reduce device noise. The NR/SS capacitor filters the noise from the reference and feed-forward capacitor filters the noise from the error amplifier. The high power-supply rejection ratio (PSRR) of the RTQ2502A minimize the coupling of input supply noise to the output.

Enable and Shutdown

The RTQ2502A provides an EN pin, as an external chip enable control, to enable or disable the device. V_{EN} below 0.5 V turns the regulator off and enters the shutdown mode, while V_{EN} above 1.1V turns the regulator on. When the regulator is shutdown, the ground current is reduced to a maximum of 25μA. The enable circuitry has hysteresis (typically 50mV) for use with relatively slowly ramping analog signals.

If not used, connect EN to the largest capacitance on the input as close as possible to prevent voltage droops on the VIN line from triggering the enable circuit.

VOUT Programming Pins

The RTQ2502A built-in matched feedback resistor network to set output voltage. The output voltage can be programmed from 0.8V to 3.95V in 50mV steps when tying these programming pins (Pins 5 to 11) to ground. Tying any of the VOUT programming pins to SNS can lower the value of the upper resistor divider. Hence the VOUT programming resolution is increased.

Programmable Soft-Start

The noise-reduction capacitor ($C_{NR/SS}$) accomplishes dual purpose of both noise-reduction and programming the soft-start ramp time during turn-on. When EN and UVLO exceeds the respective threshold voltage, the RTQ2502A active a quick-start circuit to charge the noise reduction capacitor ($C_{NR/SS}$) and then the output voltage ramps up.

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Power Good

The power-good circuit monitors the feedback pin voltage to indicate the status of the output voltage. The open-drain PGOOD pin requires an external pull-up resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Pull-up resistor from 10kΩ to 100kΩ is recommended. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices.

After start-up, the PGOOD pin becomes high impedance when the feedback voltage exceeds V_{PGOOD_HYS} (Typically 90% of 0.8V reference voltage level). The PGOOD is pulled to GND when the feedback pin voltage falls below the V_{IT_PGOOD}, EN low, current limit, and OTP.

Under Voltage Lockout (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from turning on before VIN rises above the V_{UVLO} threshold. The UVLO circuit also disables the output of the device when VIN fall below the lockout voltage ($V_{UVLO} - \Delta V_{UVLO}$). The UVLO circuit responds quickly to glitches on VIN and attempts to disable the output of the device if VIN collapse.

Internal Current Limit (I_{LIM})

The RTQ2502A continuously monitors the output current to protect the pass transistor against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the pass transistor's gate voltage to limit the output within the predefined range.

Thermal shutdown can activate during a current limit event because of the high power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

By reason of the build-in body diode, the pass transistor conducts current when the output voltage exceeds input voltage. Since the current is not limited, external current protection should be added if the device may work at reverse voltage state.

Over-Temperature Protection (OTP)

The RTQ2502A implements thermal shutdown protection. The device is disable when the junction temperature (T_J) exceeds 160°C (typical). The LDO automatically turn-on again when the temperature falls to 140°C (typical).

For reliable operation, limit the junction temperature to a maximum of 125°C. Continuously running the RTQ2502A into thermal shutdown or above a junction temperature of 125°C reduces long-term reliability.

Output Active Discharge

When the device is disabled, the RTQ2502A discharges the LDO output (via VOUT pins) through an internal several hundred ohms to ground. Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. External current protection should be added if the device may work at reverse voltage state.

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Absolute Maximum Ratings (Note 1)

- VIN, PGOOD, EN ---------- –0.3V to 7V
- VOUT ---------- –0.3V to (V_{IN} + 0.3V)
- NR/SS, FB ---------- –0.3V to 3.6V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-20L 5x5 ---------- 3.54W
- Package Thermal Resistance (Note 2)
  VQFN-20L 5x5, θ_{JA} ---------- 28.2°C/W
  VQFN-20L 5x5, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  CDM (Charged Device Model) ---------- 1kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 1.1V to 6.5V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), (1.1V ≤ V_{IN} < 6.5V and V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8V, VOUT connected to 50Ω to GND, V_{EN} = 1.1 V, C_{IN} = 10µF, C_{OUT} = 22µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PGOOD pin pulled up to V_{IN} with 100kΩ, unless otherwise noted. (Note 5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Input Voltage Range	V_{IN}		1.1	--	6.5	V
Feedback Reference Voltage	V_{REF}		--	0.8	--	V
NR/SS Pin Voltage	$V_{NR/SS}$		--	0.8	---	V
Under Voltage Lock-Out	V_{UVLO}	V_{IN} increasing	--	1.02	1.085	V
	ΔV_{UVLO}	Hysteresis	--	150	--	mV
Output Voltage Range		Using voltage setting pins (50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V)	0.8V –1%	--	3.95V + 1%	V
		Using external resistors	0.8V –1%	--	5V + 1%	V
Output Voltage Accuracy (Note 6)	V_{OUT}	V_{IN} = V_{OUT} + 0.3V, 0.8V ≤ V_{OUT} ≤ 5V, 5mA ≤ I_{OUT} ≤ 2A	–1	--	1	%
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 5mA, 1.4V ≤ V_{IN} ≤ 6.5 V	--	0.05	--	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	5mA ≤ I_{OUT} ≤ 2A	--	0.08	--	%/A
Dropout Voltage	V_{DROP}	I_{OUT} = 2A, V_{FB} = 0.8V – 3%	--	--	125	mV

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Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Current Limit	I_{LIM}	V_{OUT} = 90% $V_{OUT(TARGET)}$, V_{IN} = $V_{OUT(TARGET)}$ + 400mV		2.1	3.4	4.2	A
Ground Pin Current	I_{GND}	Minimum load, V_{IN} = 6.5V, I_{OUT} = 5mA		--	2.8	4	mA
		Maximum load, V_{IN} = 1.4V, I_{OUT} = 2A		--	3.7	5	
		Shutdown, PGOOD = open, V_{IN} = 6.5V, V_{EN} = 0.5V		--	--	25	µA
EN Pin Current	I_{EN}	V_{IN} = 6.5V, V_{EN} = 0V and 6.5V		–0.1	--	0.1	µA
EN Pin High-Level Input Voltage	V_{EN_H}	Enable device		1.1	--	6.5	V
EN Pin Low-Level Input Voltage	V_{EN_L}	Disable device		0	--	0.5	
PGOOD Pin Threshold	V_{IT_PGOOD}	For the direction PGOOD signal falling with decreasing V_{OUT}		0.82 x V_{OUT}	0.883 x V_{OUT}	0.93 x V_{OUT}	V
PGOOD Pin Hysteresis	V_{PGOOD_HYS}	For PGOOD signal rising		--	0.01 x V_{OUT}	--	V
PGOOD Pin Low-Level Output Voltage	V_{PGOOD_L}	V_{OUT} < V_{IT_PGOOD}, I_{PGOOD} = –1mA (current into device)		--	--	0.4	V
PGOOD Pin Leakage Current	I_{PGOOD_LK}	V_{OUT} > V_{IT_PGOOD} , V_{PGOOD} = 6.5V		--	--	1	µA
NR/SS Pin Charging Current	$I_{NR/SS}$	$V_{NR/SS}$ = GND, V_{IN} = 6.5V		4	6.2	9	µA
FB Pin Leakage Current	I_{FB}	V_{IN} = 6.5V		–100	--	100	nA
Power Supply Rejection Ratio	PSRR	V_{IN} – V_{OUT} = 0.4V, I_{OUT} = 2A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 22µF || 22µF	f = 10kHz, V_{OUT} = 0.8V	--	42	--	dB
			f = 500kHz, V_{OUT} = 0.8V	--	39	--	
			f = 10kHz, V_{OUT} = 5V	--	40	--	
			f = 500kHz, V_{OUT} = 5V	--	25	--	
Output Noise Voltage	e_{NO}	BW = 10Hz to 100kHz , V_{IN} = 1.4V, V_{OUT} = 0.8V, I_{OUT} = 1.5A, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF		--	6	--	μV_{RMS}
Thermal Shutdown Threshold	T_{SD}	Temperature increasing		--	160	--	°C
		Temperature decreasing		--	140	--	

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Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

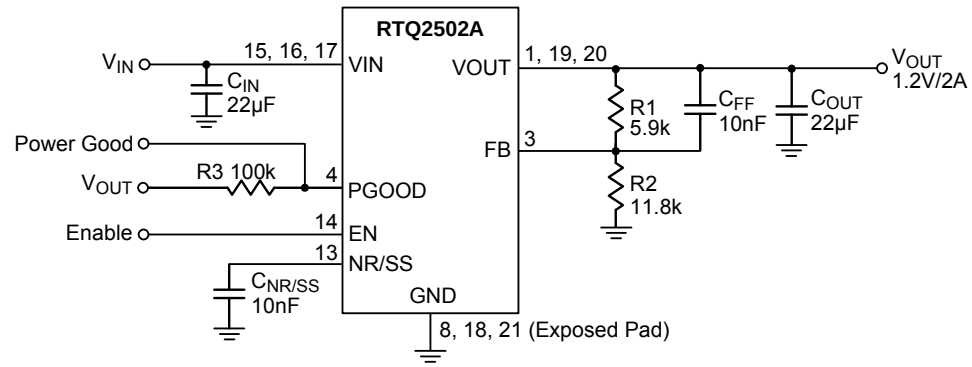
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. $V_{OUT(TARGET)}$ is the expected V_{OUT} value set by the external feedback resistors. The 50Ω load is disconnected when the test conditions specify an I_{OUT} value.

Note 6. External resistor tolerance is not taken into account.

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Typical Application Circuit

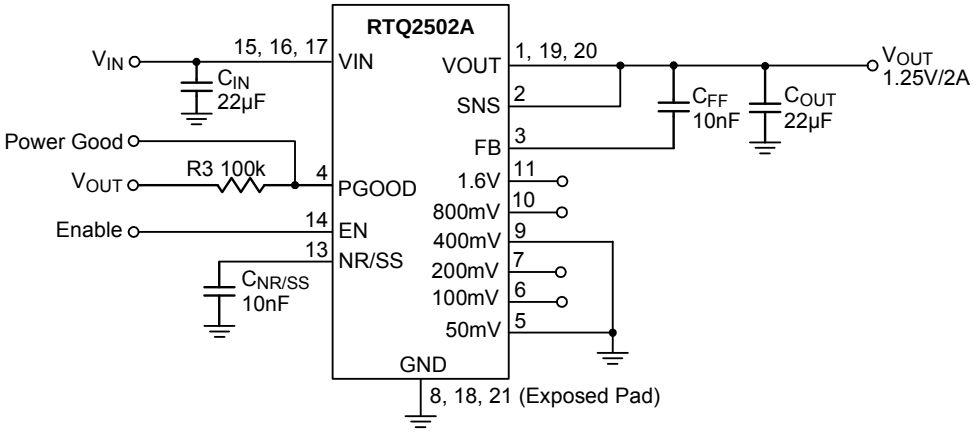


$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) = 0.8V \times \left(1 + \frac{5.9k}{11.8k}\right) = 1.2V$$

Figure 1. Configuration Circuit for V_{OUT} Adjusted by a Resistive Divider

Table 1. Recommended Feedback-Resistor Values

Output Voltage (V)	External Restive Divider Combinations	
	R1 (kΩ)	R2 (kΩ)
0.9	12.4	100
1	12.4	49.9
1.2	12.4	24.9
1.5	12.4	14.3
1.8	12.4	10
2.5	12.4	5.9
3.3	11.8	3.74
4.5	11.8	2.55
5	12.4	2.37



$V_{OUT} = V_{REF} + 50mV + 400mV = 0.8V + 50mV + 400mV = 1.25V$

(Table 2. provides a full list for different V_{OUT} target and the corresponding pin settings.)

Figure 2. Configuration Circuit for V_{OUT} Adjusted via PCB Layout

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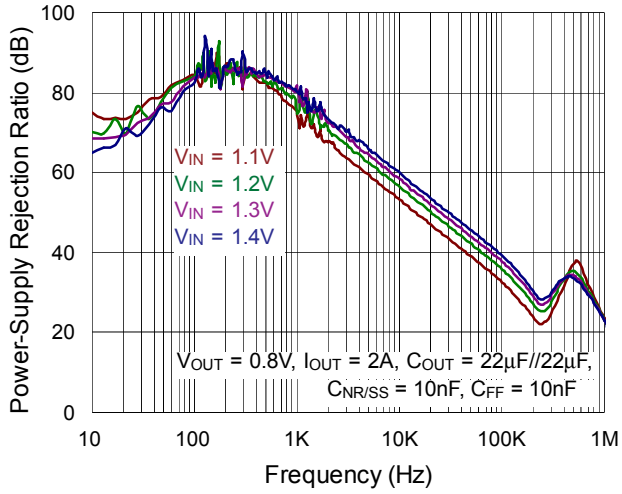
Table 2. V_{OUT} Select Pin Settings for Different Target

V_{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V	V_{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V
0.8	Open	Open	Open	Open	Open	Open	2.4	Open	Open	Open	Open	Open	GND
0.85	GND	Open	Open	Open	Open	Open	2.45	GND	Open	Open	Open	Open	GND
0.9	Open	GND	Open	Open	Open	Open	2.5	Open	GND	Open	Open	Open	GND
0.95	GND	GND	Open	Open	Open	Open	2.55	GND	GND	Open	Open	Open	GND
1	Open	Open	GND	Open	Open	Open	2.6	Open	Open	GND	Open	Open	GND
1.05	GND	Open	GND	Open	Open	Open	2.65	GND	Open	GND	Open	Open	GND
1.1	Open	GND	GND	Open	Open	Open	2.7	Open	GND	GND	Open	Open	GND
1.15	GND	GND	GND	Open	Open	Open	2.75	GND	GND	GND	Open	Open	GND
1.2	Open	Open	Open	GND	Open	Open	2.8	Open	Open	Open	GND	Open	GND
1.25	GND	Open	Open	GND	Open	Open	2.85	GND	Open	Open	GND	Open	GND
1.3	Open	GND	Open	GND	Open	Open	2.9	Open	GND	Open	GND	Open	GND
1.35	GND	GND	Open	GND	Open	Open	2.95	GND	GND	Open	GND	Open	GND
1.4	Open	Open	GND	GND	Open	Open	3	Open	Open	GND	GND	Open	GND
1.45	GND	Open	GND	GND	Open	Open	3.05	GND	Open	GND	GND	Open	GND
1.5	Open	GND	GND	GND	Open	Open	3.1	Open	GND	GND	GND	Open	GND
1.55	GND	GND	GND	GND	Open	Open	3.15	GND	GND	GND	GND	Open	GND
1.6	Open	Open	Open	Open	GND	Open	3.2	Open	Open	Open	Open	GND	GND
1.65	GND	Open	Open	Open	GND	Open	3.25	GND	Open	Open	Open	GND	GND
1.7	Open	GND	Open	Open	GND	Open	3.3	Open	GND	Open	Open	GND	GND
1.75	GND	GND	Open	Open	GND	Open	3.35	GND	GND	Open	Open	GND	GND
1.8	Open	Open	GND	Open	GND	Open	3.4	Open	Open	GND	Open	GND	GND
1.85	GND	Open	GND	Open	GND	Open	3.45	GND	Open	GND	Open	GND	GND
1.9	Open	GND	GND	Open	GND	Open	3.5	Open	GND	GND	Open	GND	GND
1.95	GND	GND	GND	Open	GND	Open	3.55	GND	GND	GND	Open	GND	GND
2	Open	Open	Open	GND	GND	Open	3.6	Open	Open	Open	GND	GND	GND
2.05	GND	Open	Open	GND	GND	Open	3.65	GND	Open	Open	GND	GND	GND
2.1	Open	GND	Open	GND	GND	Open	3.7	Open	GND	Open	GND	GND	GND
2.15	GND	GND	Open	GND	GND	Open	3.75	GND	GND	Open	GND	GND	GND
2.2	Open	Open	GND	GND	GND	Open	3.8	Open	Open	GND	GND	GND	GND
2.25	GND	Open	GND	GND	GND	Open	3.85	GND	Open	GND	GND	GND	GND
2.3	Open	GND	GND	GND	GND	Open	3.9	Open	GND	GND	GND	GND	GND
2.35	GND	GND	GND	GND	GND	Open	3.95	GND	GND	GND	GND	GND	GND

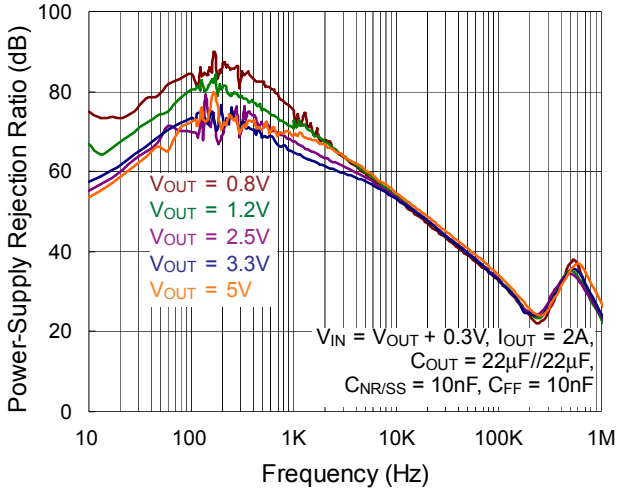
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Typical Operating Characteristics

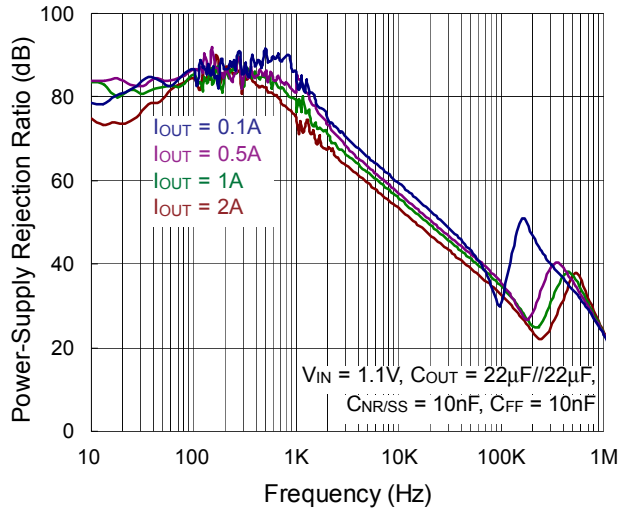
PSRR vs. Frequency and VIN



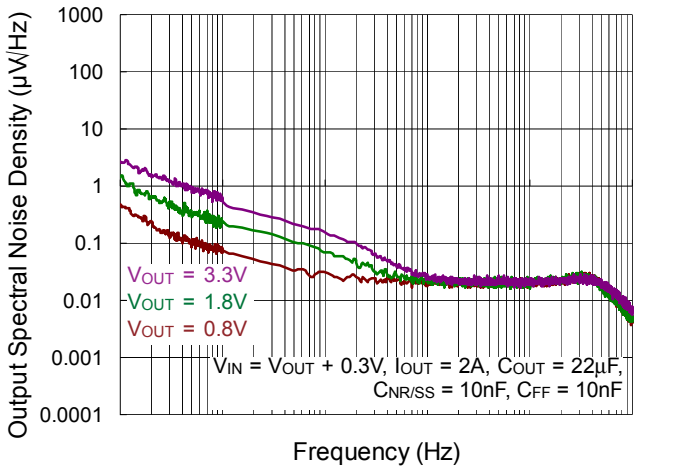
PSRR vs. Frequency and VOUT



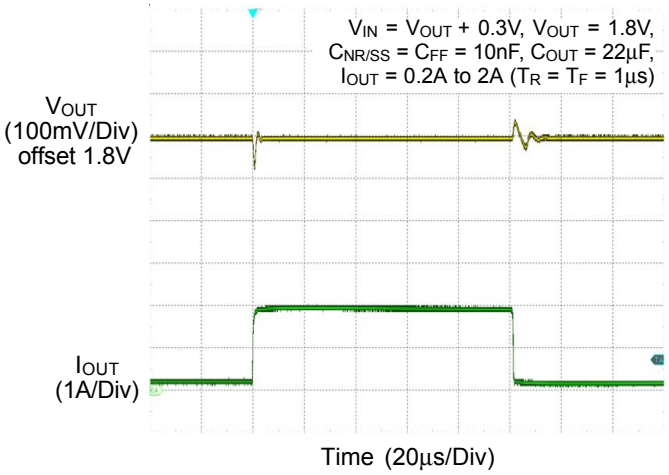
PSRR vs. Frequency and IOUT



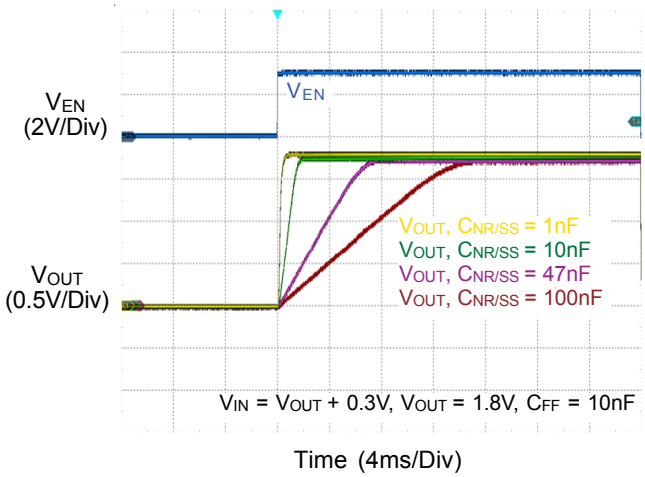
Output Noise vs. Frequency and Output Voltage



Load Transient Response

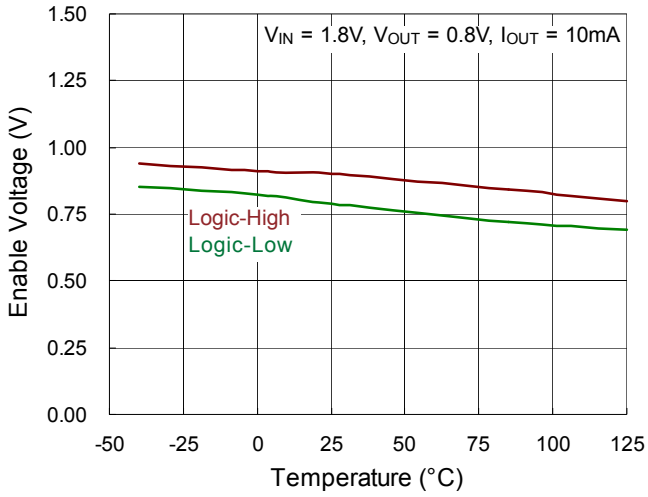


Power Up Response

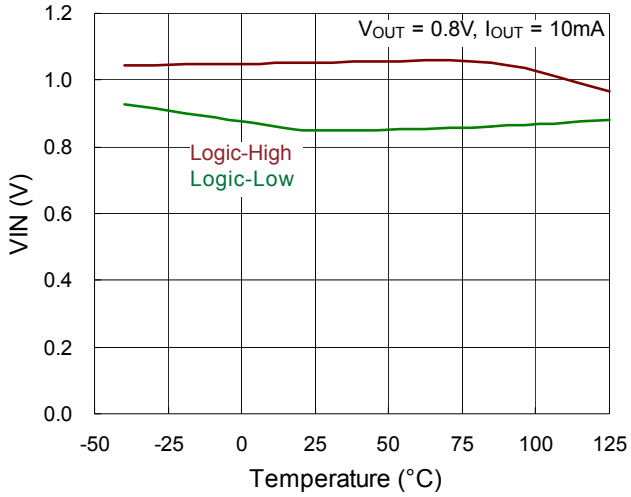


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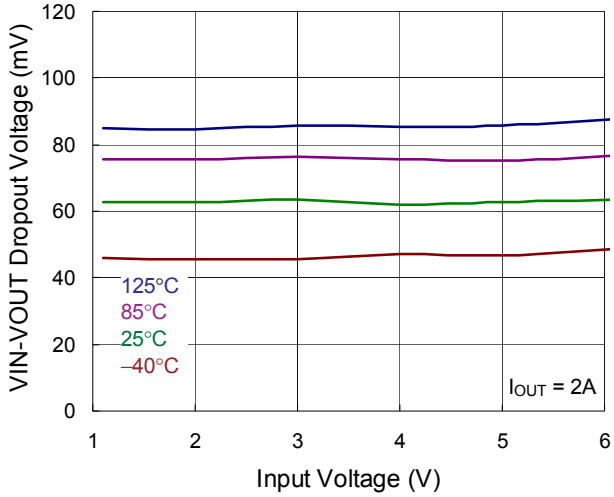
Enable Voltage vs. Temperature



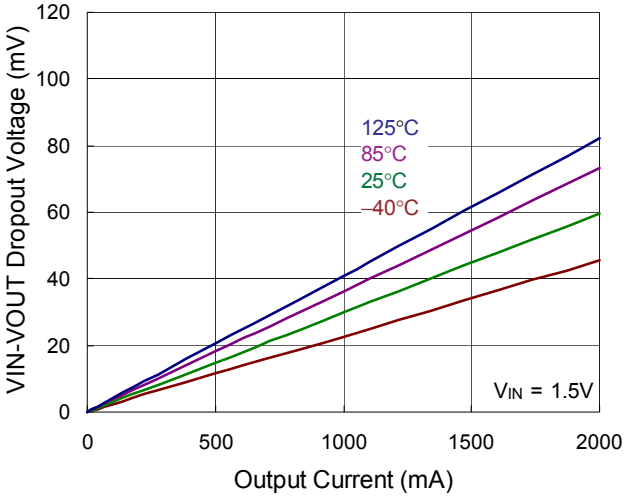
Input UVLO vs. Temperature



Dropout Voltage vs. Input Voltage



Dropout Voltage vs. Output Current



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Application Information

The RTQ2502A is a high current, low-noise, high accuracy, low-dropout linear regulator which capable of sourcing 2A with only maximum 125mV dropout. The input voltage operating range from 1.1V to 6.5V and adjustable output voltage from 0.8V to (V_{IN} – V_{DROP}) via external resistor setting or 0.8V to 3.95V via PCB Layout to short specific pins and get required output target.

Output Voltage Setting

The output voltage of the RTQ2502A can be set by external resistors or by output voltage setting pins (50mV, 100mV, 200mV, 400mV, 800mV and 1.6V) to achieve different output target.

Using external resistors, the output voltage is determined by the values of R1 and R2 as Figure 3. The values of R1 and R2 can be calculated with any voltage value via use the formula given in Equation :

$$V_{OUT} = 0.8 \times \frac{R1 + R2}{R2}$$

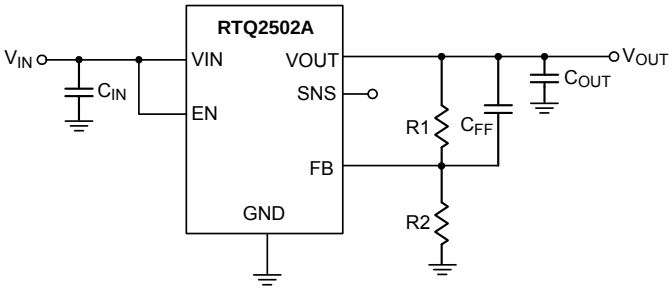
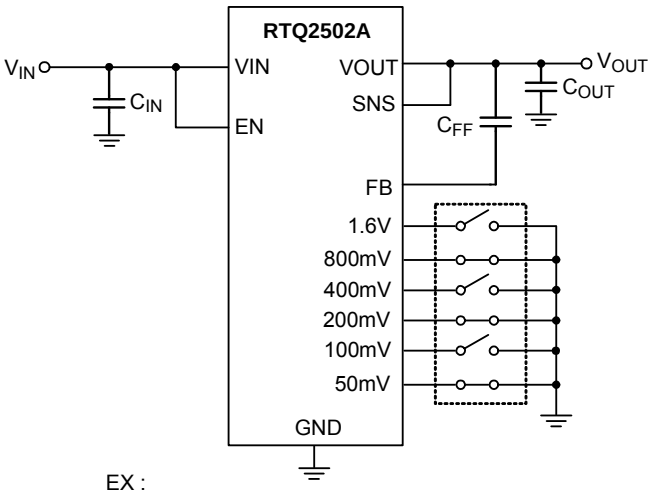


Figure 3. Output Voltage Set by External Resistors

The RTQ2502A also can short the pins 5, 6, 7, 9, 10, and 11 to ground and program the regulated output voltage level without external resistors after SNS pin is connected with VOUT pin .The pins 5, 6, 7, 9, 10, and 11 is connected with internal resistor pairs, each pin is either connected to ground (active) or left open (floating).

The voltage programming is set as the sum of the internal reference voltage (V_{REF} = 0.8V) plus the accumulated sum of the respective voltages assigned to each active pin as illustrated in figure 4.



EX :

V_{OUT} = 0.8V + (Σ Output setting pins to Ground)
= 0.8V + (0.8V + 0.2V + 0.05V) = 1.85V

Figure 4. Output Setting without External Resistors

Table 2. summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{REF} (0.8V). The maximum output target can be supported up to 3.95V after all pins 5, 6, 7, 9, 10 are shorted with ground at the same time.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DROP} also can be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance $R_{DS(ON)}$. Thus the dropout voltage can be defined as (V_{DROP} = V_{IN} – V_{OUT} = $R_{DS(ON)}$ x I_{RATED}). For normal operation, the suggested LDO operating range is (V_{IN} > V_{OUT} + V_{DROP}) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

C_{IN} and C_{OUT} Selection

The RTQ2502A is designed to support the low equivalent series resistance (ESR) ceramic capacitors for application. The X7R, X5R, and COG-rated ceramic capacitors is recommended due to its good capacitive stability across

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temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

However, ceramic capacitance varies with operating voltage and temperature and the design engineer must be aware of these characteristics. Ceramic capacitors are usually recommended to be derated by 50%. A 22μF or greater ceramic capacitor (or 10μF effective capacitance) for output is suggested to ensure the stability. Input capacitance is selected to minimize transient input droop during load current steps. For general applications, an input capacitor of at least 22μF is highly recommended for minimal input impedance. If the trace inductance between the RTQ2502A input supply is high, a fast load transient any cause VIN voltage level ringing and above the absolute maximum voltage rating that also damage the device. Adding more input capacitors is available to restrict the ringing and to keep it not above the device absolute maximum ratings.

Feed-Forward Capacitor (C_{FF})

The RTQ2502A is designed to be stable without the external feed-forward capacitor (C_{FF}). However, a 10nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} can be also used, but the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled.

Soft-Start and Noise Reduction ($C_{NR/SS}$)

The RTQ2502A is designed for a programmable, monotonic soft-start time of output rising, it can be achieved via an external capacitor ($C_{NR/SS}$) on NR/SS pin. Using an external $C_{NR/SS}$ is recommended for general application, not only for the in-rush current minimization but also helps reduce the noise component from internal reference.

During the monotonic start-up procedure, the error amplifier of the RTQ2502A tracks the voltage ramp of the external soft-start capacitor($C_{NR/SS}$) until the voltage approaches the internal reference 0.8V. The soft-start ramp time can be calculated with Equation a1 and which is depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference 0.8V (V_{REF}).

$$t_{SS} = \frac{(V_{REF} \times C_{NR/SS})}{I_{NR/SS}} \quad (a1)$$

For noise-reduction consideration, the $C_{NR/SS}$ also conjunction with an internal noise-reduction resistor that forms a low-pass filter (LPF) and filters out the noise from the internal bandgap reference before it being gained up via the error amplifier, thus reducing the total device noise floor.

Input Inrush Current

During start-up process, the input Inrush current into VIN pin is consists of the sum of load current and the charging current of the output capacitor. The inrush current is difficult to measure that the input capacitor must be removed and which is not recommended. Generally, the soft-start inrush current can be estimated by Equation b1, which $V_{OUT}(t)$ is the instantaneous output voltage of the power-up ramp, $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp and R_{LOAD} is the resistive load impedance.

$$I_{OUT}(t) = \frac{(C_{OUT} \times dV_{OUT}(t))}{dt} + \left(\frac{V_{OUT}(t)}{R_{LOAD}}\right) \quad (b1)$$

Under Voltage Lockout (UVLO)

The Under Voltage Lockout (UVLO) threshold is the minimum input operational voltage range that ensure the device stays disabled. Figure 5 explain the UVLO circuits being triggered between three different input voltage events(duration a, b and c), assuming $V_{EN} \geq V_{EN_H}$ for all time duration. For duration "a", input power starts rising and V_{IN} over the UVLO rising threshold, the V_{OUT} starts power on then reached the target level and under regulated. Duration "b" is assume V_{IN} occurs instant power line unstable and have droop severely, the V_{IN} droop level not lower than UVLO falling threshold, the device maintain normal work status, V_{OUT} still under regulated. The duration "c" is happens V_{IN} droop level lower than UVLO falling threshold, the control loop of device is disabled and don't have the regulation ability either, the V_{OUT} droop in the mean time. For general application, instant power line transient with long power trace between VIN pin may have V_{IN} level unstable force the device trap into duration c and makes output voltage collapse. In this case, adding more input capacitance or improving input trace layout on PCB are effectively to make sure input power stabilization.

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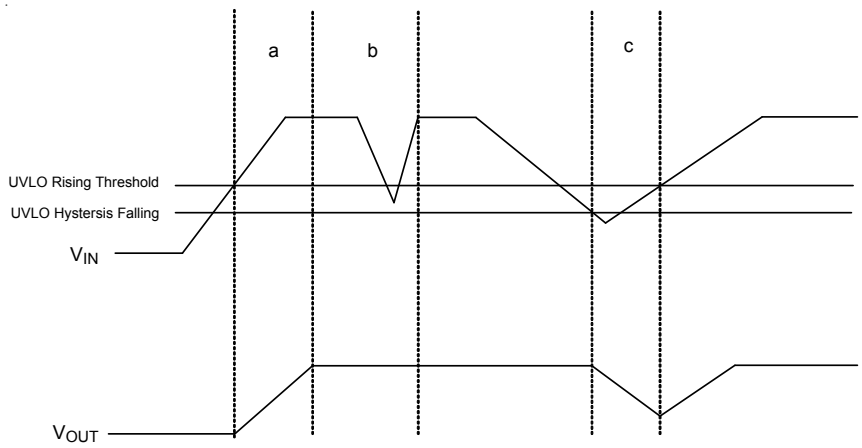


Figure 5. Under Voltage Lockout Trigging Conditions and Output Variation

Power-Good (PGOOD) Function

The Power-Good function is monitors the voltage level at the feedback pin to indicate the output voltage status is works normal or not, this function enables others devices receive the RTQ2502A's Power-Good signal as a logic signal that can be used for the sequence design of the system application. The PGOOD pin is an open-drain structure and an external pull-up resistor connecting to an external supply is necessary. The pulled-up resistor value between 10kΩ to 100kΩ is recommended for proper operation. The lower limit of 10kΩ results from the maximum pulled-down strength of the power-good transistor, and the upper limit of 100kΩ results from the maximum leakage current at the power-good node.

Figure 6 demonstrates some PGOOD scenarios versus the VIN, EN and protection status. Duration "a" is present the device is under the operation while V_{EN} is higher than V_{EN_H} threshold, the output voltage V_{OUT} start rising(the rising time has related with soft-start capacitor $C_{NR/SS}$), after V_{OUT} over PGOOD hysteresis threshold, the reflected feedback voltage V_{FB} exceeds V_{PGOOD_HYS} threshold, the PGOOD pin is high impedance. The duration "b" indicates some unpredictable operation happens (ex: OTP, OCP or output voltage droop severely caused by very fast load variation). Where the V_{FB} lower than V_{IT_PGOOD} threshold and the V_{PGOOD} is pulled to GND for the indication that output voltage status is not ready. While duration "c" is assume V_{OUT} have small droop that not lower than PGOOD falling threshold, the PGOOD pin remain high impedance. After V_{EN} goes logic low level, V_{PGOOD} pulled to GND as duration "d" presented.

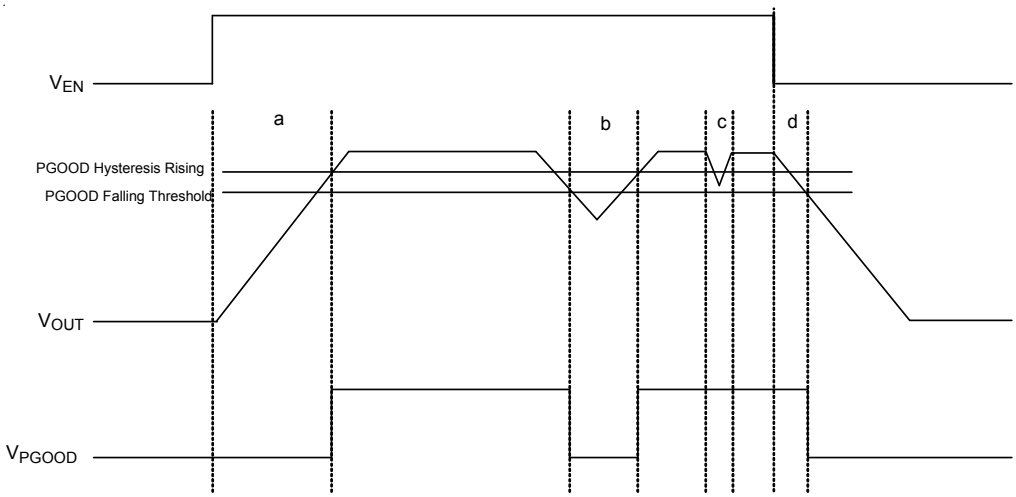


Figure 6. PGOOD Trigger Scenario with Different Operating Status

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Reverse Current Protection

If the maximum V_{OUT} exceeds V_{IN} + 0.3V, that may induce reverse current from VOUT to VIN that flows through the body diode of pass element instead of the normal conducting channel. In this case, the pass element may be damaged. For example, the output is biased above input supply voltage level or input supply has instant collapse at light load operation that makes $V_{IN} < V_{OUT}$. As shown in Figure 7, an external Schottky diode could be added to prevent the pass element be damaged from the reverse current.

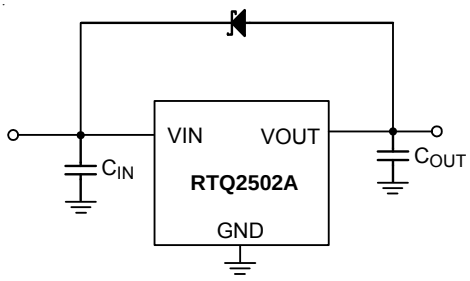


Figure 7. Application Circuit for Reverse Current Protection

Thermal Considerations

Thermal protection limits power dissipation in the RTQ2502A. When power dissipation on pass element (P_{DIS} = (V_{IN} – V_{OUT}) x I_{OUT}) is too much that raise the operation junction temperature exceeds 160°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature cools down by 20°C. The RTQ2502A output voltage will be closed to zero when output short circuit occurs as shown in Figure 8. It can reduce the chip temperature and provides maximum safety to end users when output short circuit occurs.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-20L 5x5 package, the thermal resistance, θ_{JA}, is 28.2°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (28.2°C/W) = 3.54W for a VQFN-20L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

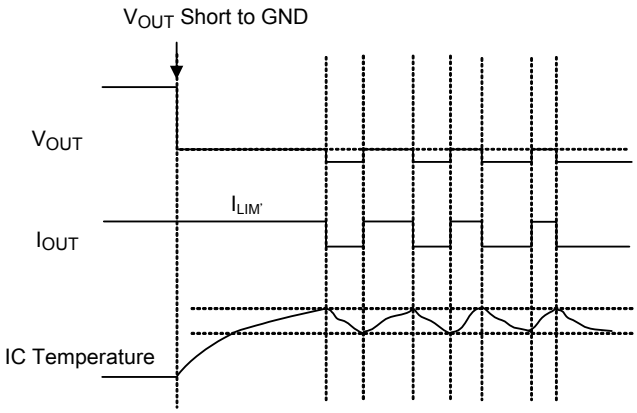


Figure 8. Short-Circuit Protection when Output Short-Circuit Occurs

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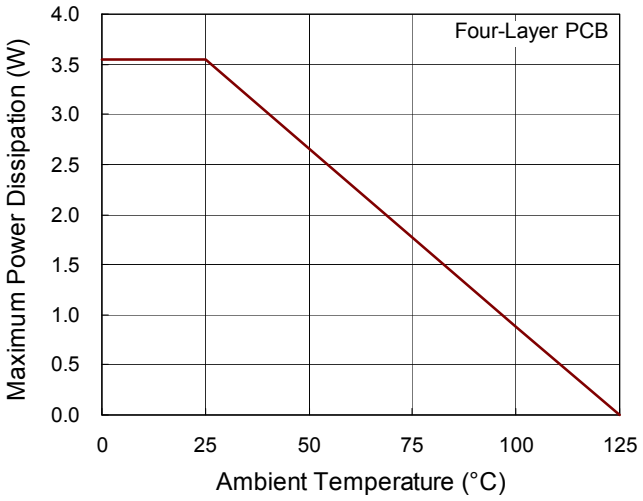


Figure 9. Derating Curve of Maximum Power Dissipation

Layout Consideration

For best performance of the RTQ2502A, the PCB layout suggestions below are highly recommend. All circuit components placed on the same side and as near to the respective LDO pin as possible, place the ground return path connection to the input and output capacitor, the ground plane connected by a wide copper surface for good thermal dissipation. Using vias and long power traces for the input and output capacitors connection is discouraged and have negatively affects on performance. Figure 10 shows an example for the layout reference that reduce conduction trace loop, helping inductive parasitic minimize, load transient reduction and good circuit stability.

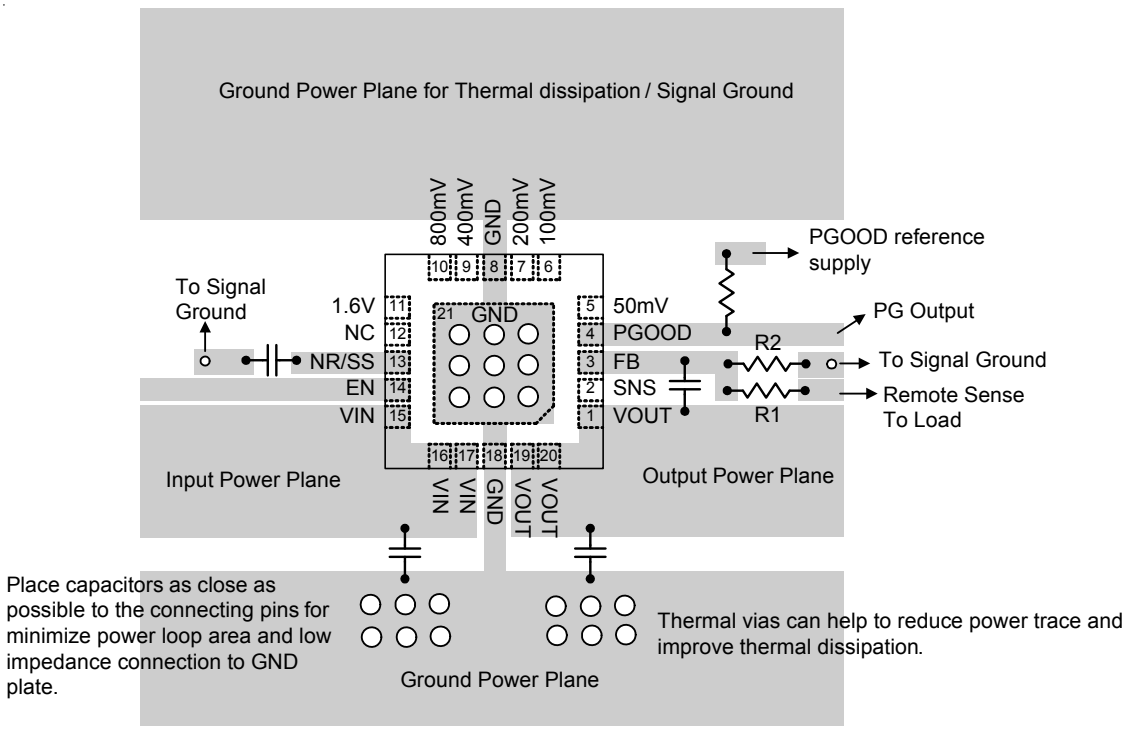
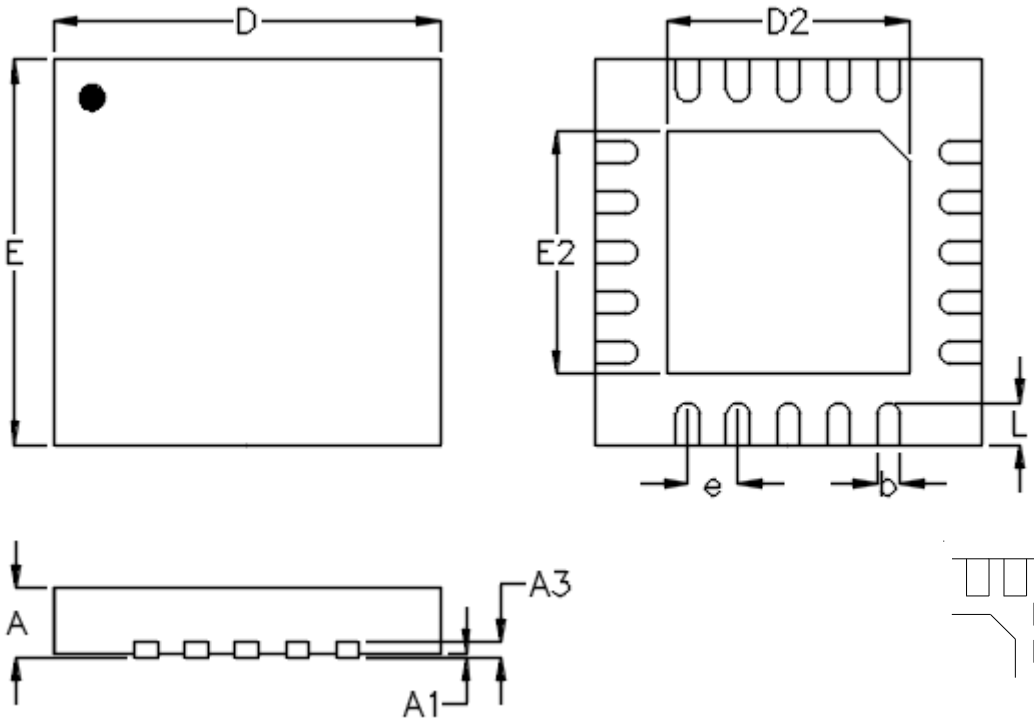
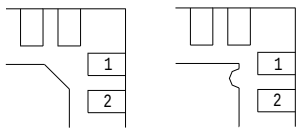


Figure 10. PCB Layout Guide

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Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

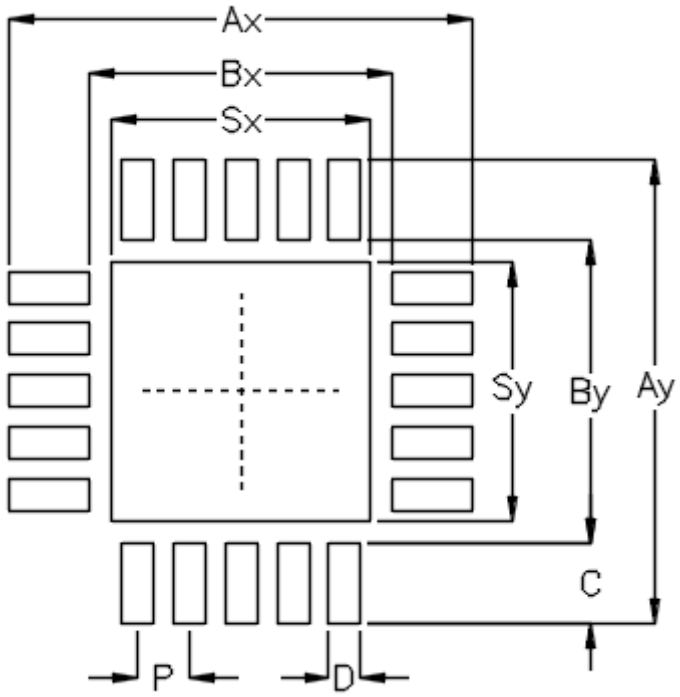
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.350	0.010	0.014
D	4.950	5.050	0.195	0.199
D2	3.100	3.200	0.122	0.126
E	4.950	5.050	0.195	0.199
E2	3.100	3.200	0.122	0.126
e	0.650		0.026	
L	0.500	0.600	0.020	0.024

V-Type 20L QFN 5x5 Package

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Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-20	20	0.65	5.80	5.80	3.80	3.80	1.00	0.40	3.25	3.25	±0.05

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