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OPAx191 36-V, Low Power, Precision, CMOS, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp

1 Features

- Low Offset Voltage: ±5 µV
- Low Offset Voltage Drift: ±0.1 µV/°C
- Low Noise: 15 nV/√Hz at 1 kHz
- High Common-Mode Rejection: 140 dB
- Low Bias Current: ±5 pA
- Rail-to-Rail Input and Output
- Wide Bandwidth: 2.5-MHz GBW
- High Slew Rate: 5 V/µs
- Low Quiescent Current: 140 µA per Amplifier
- Wide Supply: ±2.25 V to ±18 V, 4.5 V to 36 V
- EMI/RFI Filtered Inputs
- Differential Input Voltage Range to Supply Rail
- High Capacitive Load Drive Capability: 1 nF
- Industry Standard Packages:
  - Single in SOIC-8, SOT-5, and VSSOP-8
  - Dual in SOIC-8 and VSSOP-8
  - Quad in SOIC-14 and TSSOP-14

2 Applications

- Multiplexed Data-Acquisition Systems
- Test and Measurement Equipment
- High-Resolution ADC Driver Amplifiers
- SAR ADC Reference Buffers
- Programmable Logic Controllers
- High-Side and Low-Side Current Sensing
- High Precision Comparator

3 Description

The OPAx191 family (OPA191, OPA2191, and OPA4191) is a new generation of 36-V, e-trim operational amplifiers.

These devices offer outstanding dc precision and ac performance, including rail-to-rail input/output, low offset voltage (±5 µV, typ), low offset drift (±0.2 µV/°C, typ), and 2-MHz bandwidth.

Unique features, such as differential input-voltage range to the supply rail, high output current (±65 mA), high capacitive load drive of up to 1 nF, and high slew rate (5 V/µs), make the OPAx191 a robust, high-performance operational amplifier for high-voltage industrial applications.

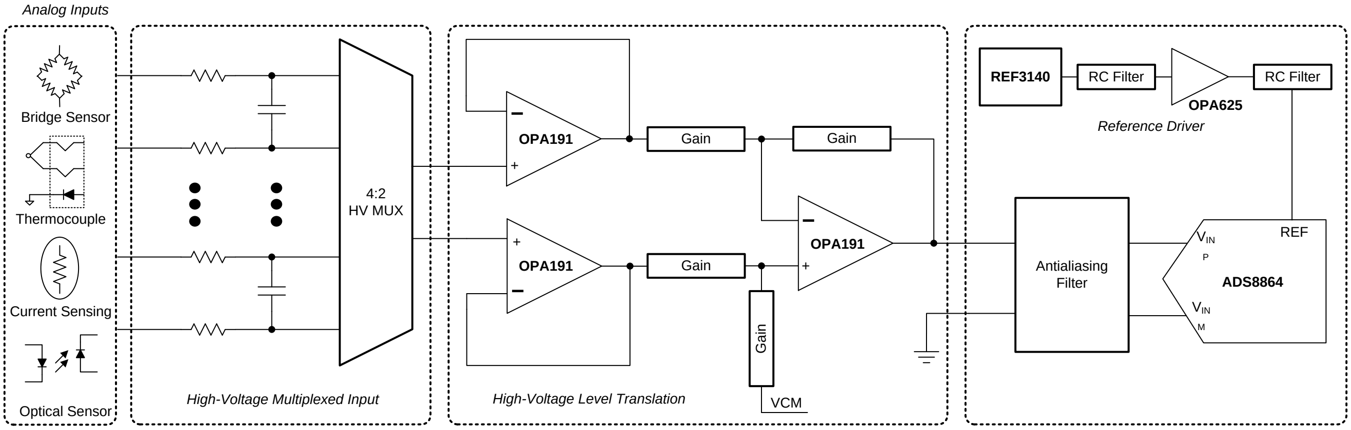
The OPAx191 family of op amps is available in standard packages and is specified from –40°C to +125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA191	SOIC (8)	4.90 mm × 3.90 mm
	SOT (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA2191	SOIC (8)	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA4191	SOIC (14)	8.65 mm x 3.90 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

OPA191 in a High-Voltage, Multiplexed, Data-Acquisition System



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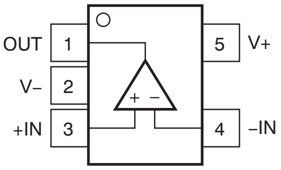
4 Revision History

Changes from Original (December 2015) to Revision A **Page**

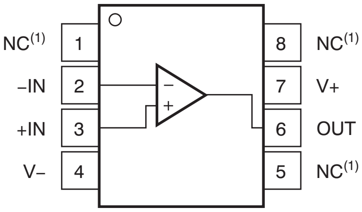
- Changed DBV and DGK packages from product preview to production data 1
- Added input offset voltage drift values for DBV and DGK packages to both electrical characteristics tables 5
- Added crosstalk values to both electrical characteristics tables 5
- Updated Figure 23, 0.1-Hz to 10-Hz Noise graph 14
- Added text regarding capacitive load drive to the *Capacitive Load and Stability* section 26
- Added Figure 56 26

5 Pin Configuration and Functions

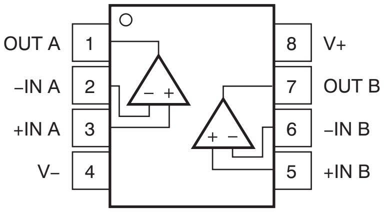
DBV Package: OPA191
5-Pin SOT
Top View



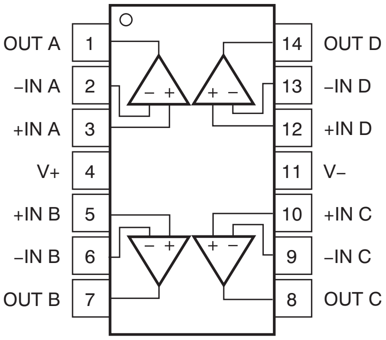
D and DGK Packages: OPA191
8-Pin SOIC and VSSOP
Top View



D and DGK Packages: OPA2191
8-Pin SOIC and VSSOP
Top View



D and PW Packages: OPA4191
14-Pin SOIC and TSSOP
Top View



(1) NC = No internal connection.

Pin Functions: OPA191

PIN			I/O	DESCRIPTION
NAME	OPA191			
	D (SOIC), DGK (VSSOP)	DBV (SOT)		
+IN	3	3	I	Noninverting input
–IN	2	4	I	Inverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V+	7	5	—	Positive (highest) power supply
V–	4	2	—	Negative (lowest) power supply

Pin Functions: OPA2191 and OPA4191

PIN			I/O	DESCRIPTION
NAME	OPA2191	OPA4191		
	D (SOIC), DGK (VSSOP)	D (SOIC), PW (TSSOP)		
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	—	10	I	Noninverting input, channel C
+IN D	—	12	I	Noninverting input, channel D
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	—	9	I	Inverting input,,channel C
–IN D	—	13	I	Inverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V+	8	4	—	Positive (highest) power supply
V–	4	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		Dual supply		±20	V
		Single supply		40	
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
Output short circuit[2]			Continuous		mA
Temperature	Operating		–40	150	°C
	Junction			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Dual supply	±2.25		±18	V
	Single supply	4.5		36	
Operating temperature		–40		125	°C

6.4 Thermal Information: OPA191

THERMAL METRIC[1]		OPA191			UNIT
		8 PINS		5 PINS	
		D (SOIC)	DGK (VSSOP)	DBV (SOT)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	180.4	158.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	60.1	67.9	60.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	102.1	44.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	10.4	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.9	100.3	4.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA2191

THERMAL METRIC(1)		OPA2191		UNIT
		8 PINS		
		D (SOIC)	DGK (VSSOP)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.9	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53.9	48.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.3	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Thermal Information: OPA4191

THERMAL METRIC(1)		OPA4191		UNIT
		14 PINS		
		D (SOIC)	PW (TSSOP)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.4	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.3	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.0	33.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.3	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.7	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±18 V			±5	±25	µV
			T_A = 0°C to 85°C		±8	±75	
			T_A = –40°C to +125°C		±10	±125	
		(V+) – 3.0 V < V_{CM} < (V+) – 1.5 V			See *Common-Mode Voltage Range* section		
		V_S = ±18 V, V_{CM} = (V+) – 1.5 V			±10	±50	
			T_A = 0°C to 85°C		±25	±150	
			T_A = –40°C to +125°C		±50	±250	
dV_{OS}/dT	Input offset voltage drift	V_S = ±18 V, D package only	T_A = 0°C to 85°C		±0.1	±0.8	µV/°C
			T_A = –40°C to +125°C		±0.15	±1.2	
		V_S = ±18 V, DGK and DBV packages only	T_A = 0°C to 85°C		±0.1	±0.9	
			T_A = –40°C to +125°C		±0.15	±1.3	
		V_S = ±18 V, V_{CM} = (V+) – 1.5 V	T_A = –40°C to +125°C		±0.5		
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±0.3	±1.0	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±9	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 0.1 Hz to 10 Hz		1.4		$µV_{PP}$
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 0.1 Hz to 10 Hz		7		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		18		nV/√Hz
			f = 1 kHz		15		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		53		
			f = 1 kHz		24		
i_n	Input current noise density	f = 1 kHz			1.5		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 3 V		120	140		dB
		V_S = ±18 V, (V–) < V_{CM} < (V+) – 3 V	T_A = –40°C to +125°C	114	126		
		V_S = ±18 V, (V+) – 1.5 V < V_{CM} < (V+)		96	120		
			T_A = –40°C to +125°C	86	100		
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V			See *Typical Characteristics*		
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±18 V, (V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 2 kΩ		124	134		dB
			T_A = –40°C to +125°C	114	126		
		V_S = ±18 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ		126	140		
			T_A = –40°C to +125°C	120	134		

Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V) (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				2.5		MHz
SR	Slew rate	V_S = ±18 V, G = 1, 10-V step	Rising		7.5		V/µs
			Falling		5.5		
t_s	Settling time	To 0.01%, C_L = 20 pF	V_S = ±18 V, G = 1, 2-V step		0.7		µs
			V_S = ±18 V, G = 1, 5-V step		1		
		To 0.001%, C_L = 20 pF	V_S = ±18 V, G = 1, 2-V step		1.8		
			V_S = ±18 V, G = 1, 5-V step		3.7		
t_{OR}	Overload recovery time	V_{IN} × G = V_S	From overload to negative rail		0.4		µs
			From overload to positive rail		1		
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.0012%		
	Crosstalk	OPA2191 and OPA4191, at dc			150		dB
		OPA2191 and OPA4191, f = 100 kHz			130		dB
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_L = 10 kΩ		50	110	
			R_L = 2 kΩ		200	500	
		Negative rail	No load		5	15	
			R_L = 10 kΩ		50	110	
			R_L = 2 kΩ		200	500	
I_{SC}	Short-circuit current	V_S = ±18 V			±65		mA
C_L	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, See Figure 31			700		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			140	200	µA
			T_A = –40°C to +125°C			250	
TEMPERATURE							
	Thermal protection				180		°C
	Thermal hysteresis				30		°C

6.8 Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±2.25 V, V_{CM} = (V+) – 3 V			±5	±25	µV
			T_A = 0°C to 85°C		±8	±75	
			T_A = –40°C to +125°C		±10	±125	
		(V+) – 3.0 V < V_{CM} < (V+) – 1.5 V			See *Common-Mode Voltage Range* section		
		V_S = ±3 V, V_{CM} = (V+) – 1.5 V			±10	±50	
			T_A = 0°C to 85°C		±25	±150	
			T_A = –40°C to +125°C		±50	±250	
dV_{OS}/dT	Input offset voltage drift	V_S = ±2.25 V, V_{CM} = (V+) – 3 V, D package only	T_A = 0°C to 85°C		±0.1	±0.8	µV/°C
			T_A = –40°C to +125°C		±0.15	±1.2	
		V_S = ±2.25 V, V_{CM} = (V+) – 3 V, DGK and DBV packages only	T_A = 0°C to 85°C		±0.1	±0.9	
			T_A = –40°C to +125°C		±0.15	±1.3	
		V_S = ±2.25 V, V_{CM} = (V+) – 1.5 V	T_A = –40°C to +125°C		±0.5		
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C, V_{CM} = V_S / 2 – 0.75 V			±1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±9	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 0.1 Hz to 10 Hz		1.4		$µV_{PP}$
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 0.1 Hz to 10 Hz		7		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		18		nV/√Hz
			f = 1 kHz		15		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		53		
			f = 1 kHz		24		
i_n	Input current noise density		f = 1 kHz		1.5		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = ±2.25 V, (V–) – 0.1 V < V_{CM} < (V+) – 3 V		96	110		dB
		V_S = ±2.25 V, (V–) < V_{CM} < (V+) – 3 V	T_A = –40°C to +125°C	90	104		
		V_S = ±2.25 V, (V+) – 1.5 V < V_{CM} < (V+)		96	120		
			T_A = –40°C to +125°C	84	100		
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V			See *Typical Characteristics*		
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±2.25 V, (V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 2 kΩ		110	120		dB
			T_A = –40°C to +125°C	100	114		
		V_S = ±2.25 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ		110	126		
			T_A = –40°C to +125°C	106	120		

Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V) (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				2.2		MHz
SR	Slew rate	V_S = ±2.25 V, G = 1, 1-V step	Rising		6.5		V/µs
			Falling		5.5		
t_{OR}	Overload recovery time	V_{IN} × G = V_S	From overload to negative rail		0.4		µs
			From overload to positive rail		1		
	Crosstalk	OPA2191 and OPA4191, at dc			150		dB
		OPA2191 and OPA4191, f = 100 kHz			130		dB
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_L = 10 kΩ		15	110	
			R_L = 2 kΩ		60	500	
		Negative rail	No load		5	15	
			R_L = 10 kΩ		15	110	
			R_L = 2 kΩ		60	500	
I_{SC}	Short-circuit current	V_S = ±2.25 V			±30		mA
C_L	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, see Figure 31			700		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			140	200	µA
			T_A = –40°C to +125°C			250	
TEMPERATURE							
	Thermal protection				180		°C
	Thermal hysteresis				30		°C

6.9 Typical Characteristics

Table 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6
Offset Voltage Drift Distribution	Figure 7, Figure 8,
Offset Voltage vs Temperature	Figure 9, Figure 10
Offset Voltage vs Common-Mode Voltage	Figure 11, Figure 12
Offset Voltage vs Power Supply	Figure 13
Open-Loop Gain and Phase vs Frequency	Figure 14
Closed-Loop Gain and Phase vs Frequency	Figure 15
Input Bias Current vs Common-Mode Voltage	Figure 16
Input Bias Current vs Temperature	Figure 17
Output Voltage Swing vs Output Current (maximum supply)	Figure 18, Figure 19
CMRR and PSRR vs Frequency	Figure 20
CMRR vs Temperature	Figure 21
PSRR vs Temperature	Figure 22
0.1-Hz to 10-Hz Noise	Figure 23
Input Voltage Noise Spectral Density vs Frequency	Figure 24
THD+N Ratio vs Frequency	Figure 25
THD+N vs Output Amplitude	Figure 26
Quiescent Current vs Supply Voltage	Figure 27
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Open Loop Gain vs Temperature	Figure 29, Figure 30
Open Loop Output Impedance vs Frequency	Figure 31
Small Signal Overshoot vs Capacitive Load (100-mV output step)	Figure 32, Figure 33
No Phase Reversal	Figure 34
Overload Recovery	Figure 35
Small-Signal Step Response (100 mV)	Figure 36, Figure 37
Large-Signal Step Response	Figure 38, Figure 39
Settling Time	Figure 40, Figure 41, Figure 42, Figure 43
Short-Circuit Current vs Temperature	Figure 44
Maximum Output Voltage vs Frequency	Figure 45
Propagation Delay Rising Edge	Figure 46
Propagation Delay Falling Edge	Figure 47

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

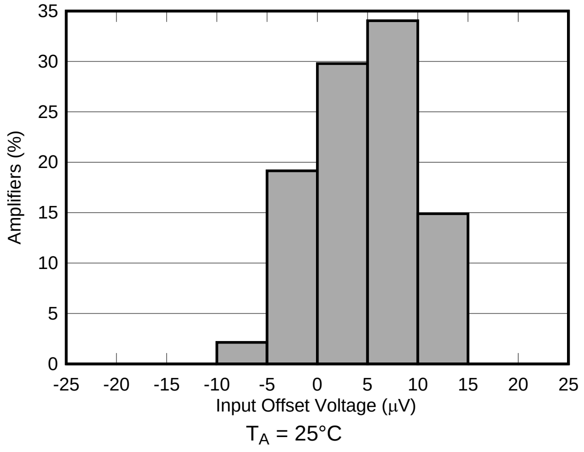


Figure 1. Offset Voltage Production Distribution

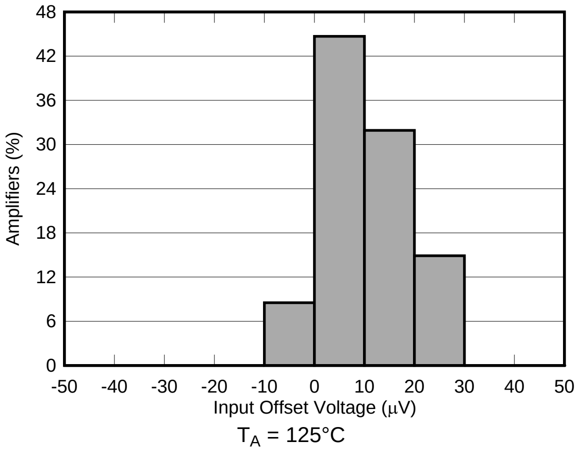


Figure 2. Offset Voltage Production Distribution

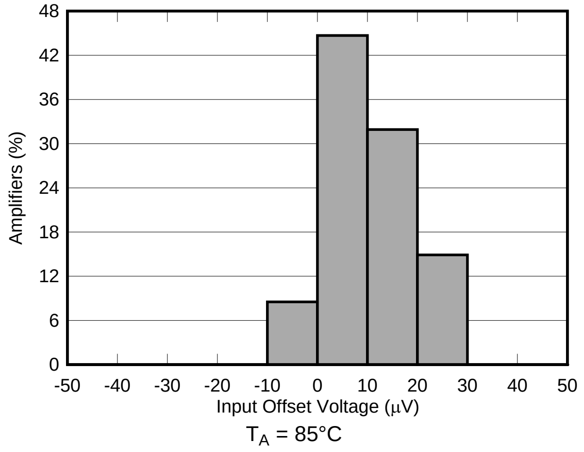


Figure 3. Offset Voltage Production Distribution

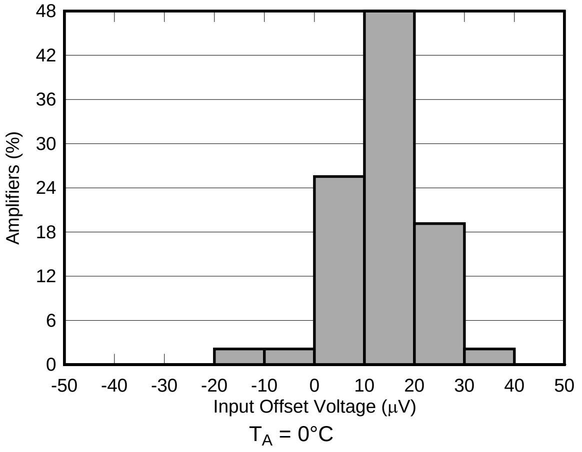


Figure 4. Offset Voltage Production Distribution

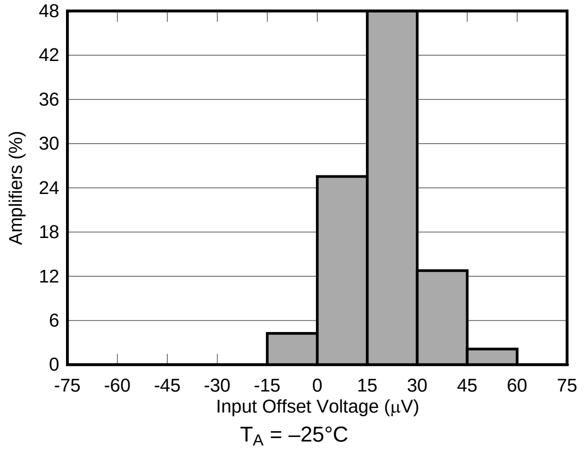


Figure 5. Offset Voltage Production Distribution

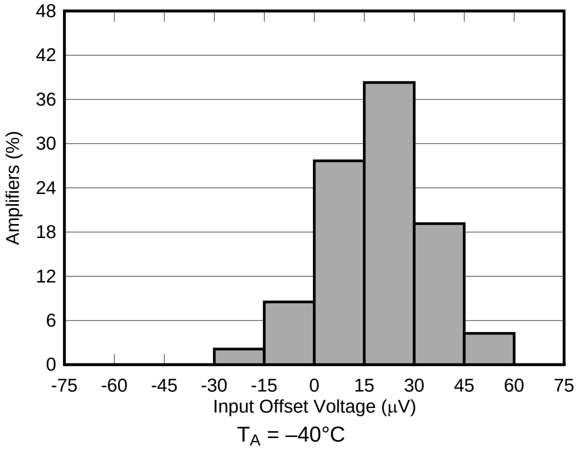
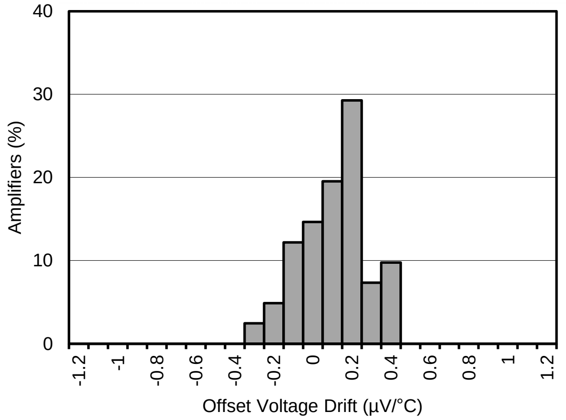


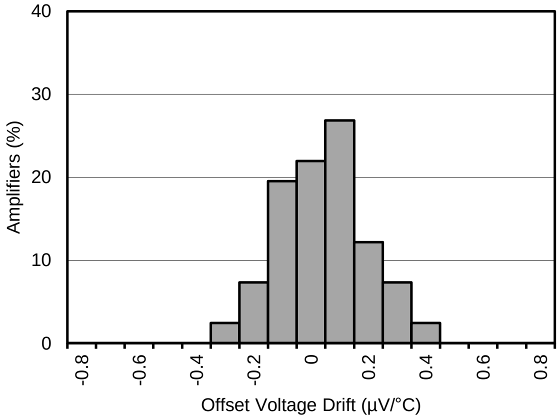
Figure 6. Offset Voltage Production Distribution

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.



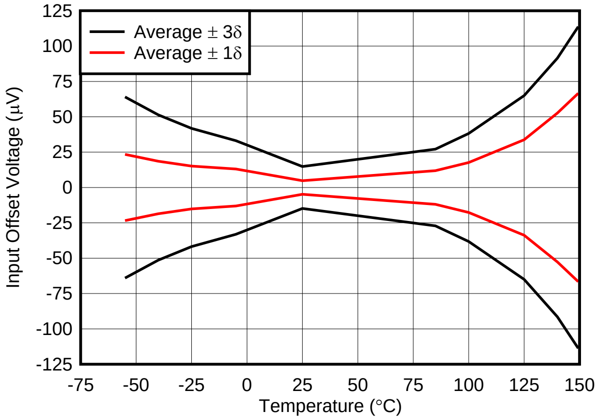
T_A = –40°C to +125°C, SOIC package

Figure 7. Offset Voltage Drift Distribution



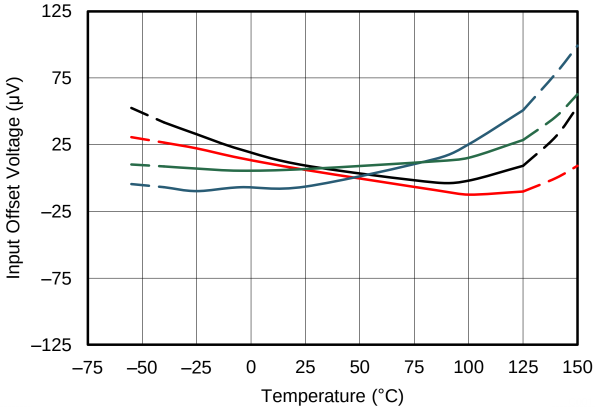
T_A = 0°C to 85°C, SOIC package

Figure 8. Offset Voltage Drift Distribution



Statistical Distribution

Figure 9. Offset Voltage vs Temperature



4 typical units

Figure 10. Offset Voltage vs Temperature

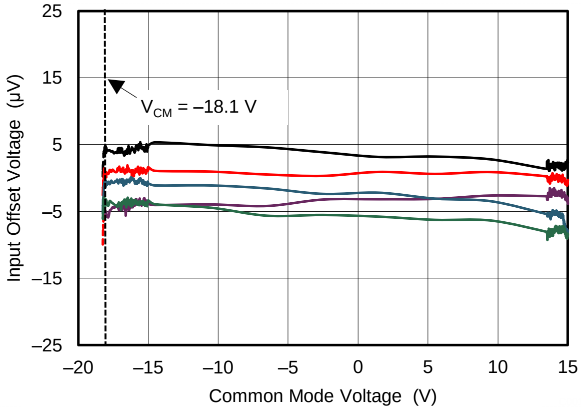


Figure 11. Offset Voltage vs Common-Mode Voltage

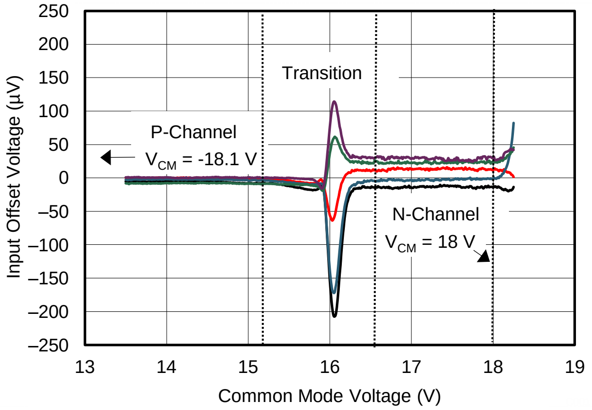
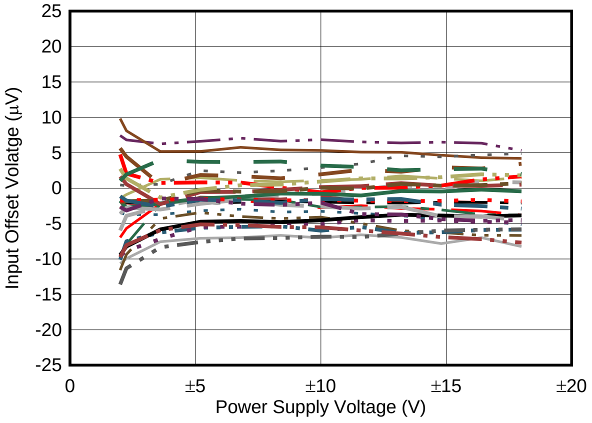


Figure 12. Offset Voltage vs Common-Mode Voltage in Transition Region

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.



30 typical units

Figure 13. Offset Voltage vs Power Supply

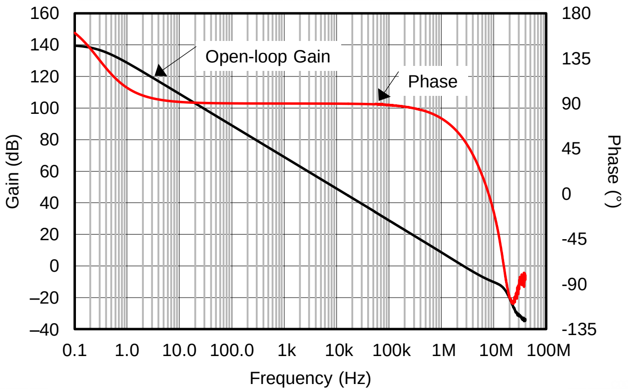


Figure 14. Open-Loop Gain and Phase vs Frequency

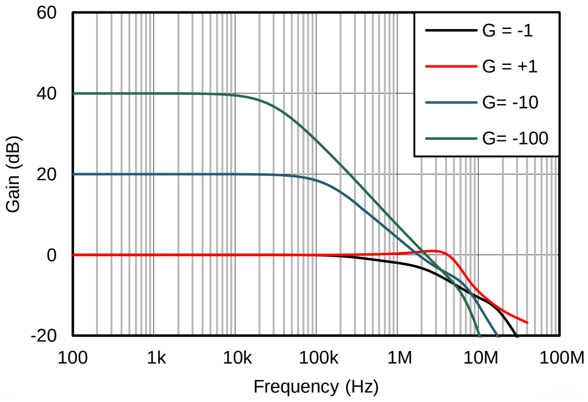


Figure 15. Closed-Loop Gain vs Frequency

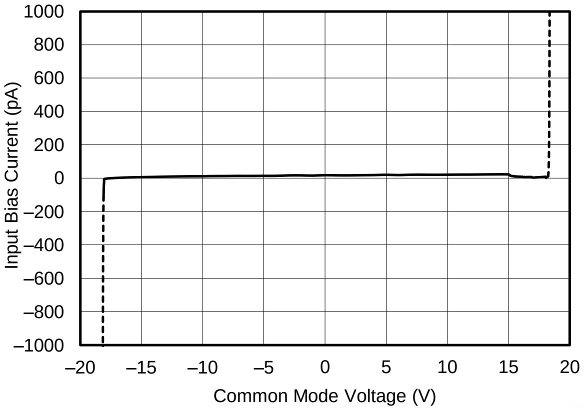


Figure 16. Input Bias Current vs Common-Mode Voltage

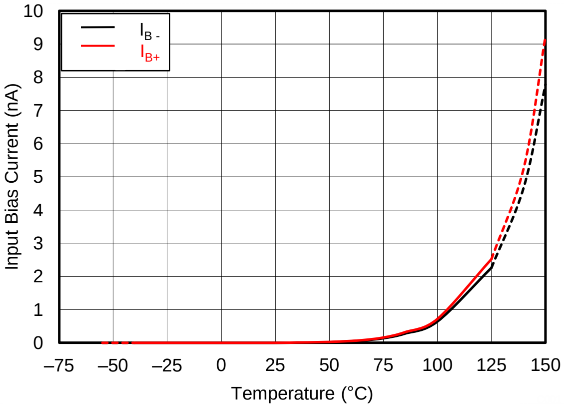
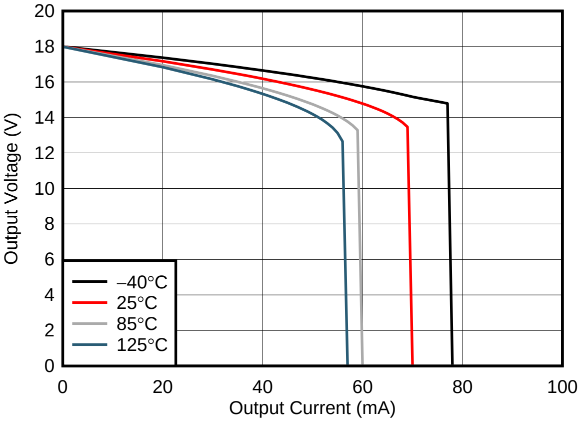


Figure 17. Input Bias Current vs Temperature



Sourcing

Figure 18. Output Voltage Swing vs Output Current

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

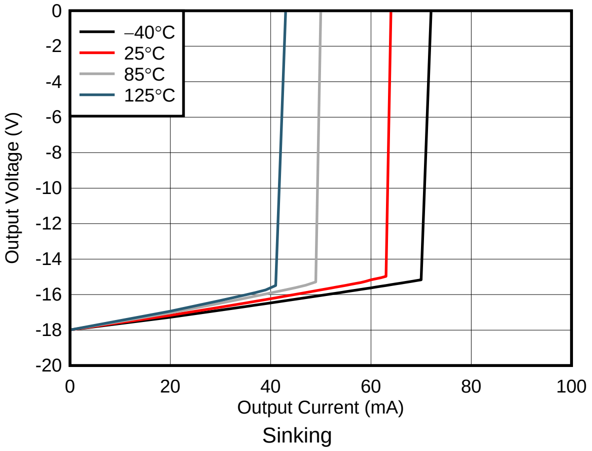


Figure 19. Output Voltage Swing vs Output Current

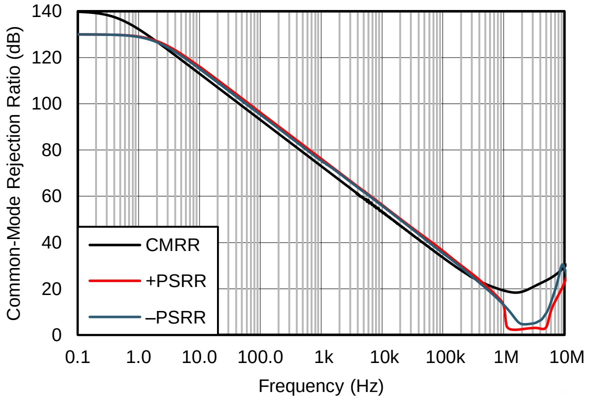


Figure 20. CMRR and PSRR vs Frequency

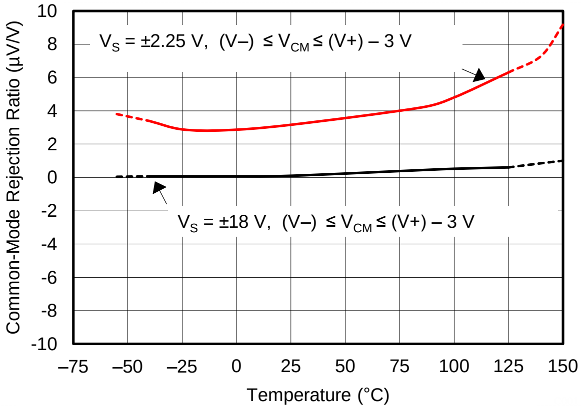


Figure 21. CMRR vs Temperature

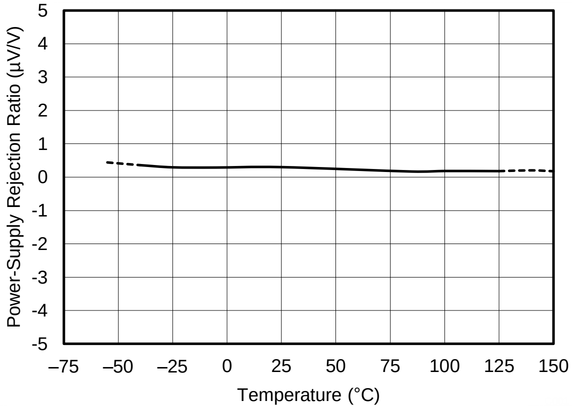


Figure 22. PSRR vs Temperature

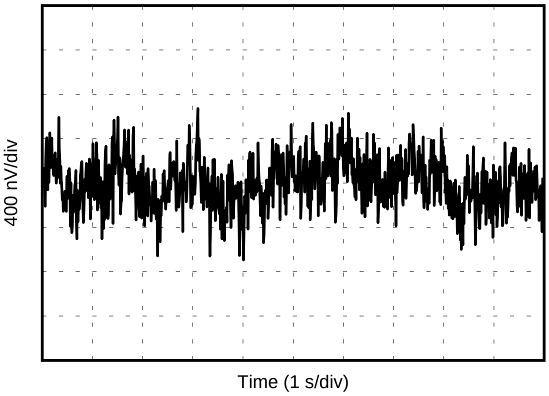


Figure 23. 0.1-Hz to 10-Hz Noise

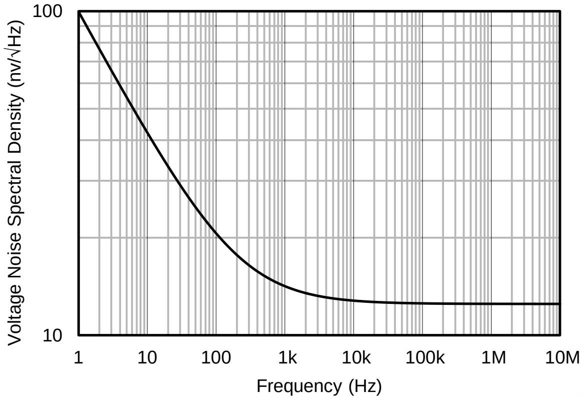


Figure 24. Input Voltage Noise Spectral Density vs Frequency

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

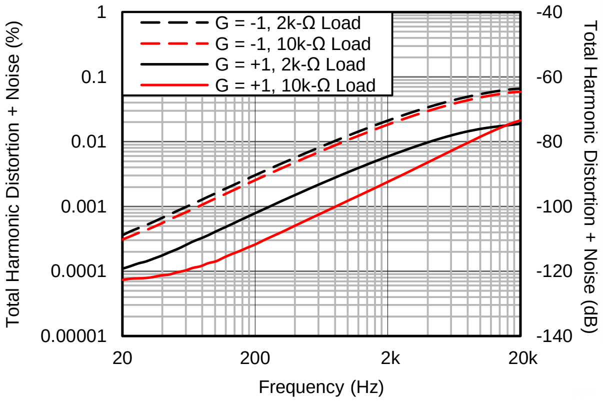


Figure 25. THD+N vs Frequency

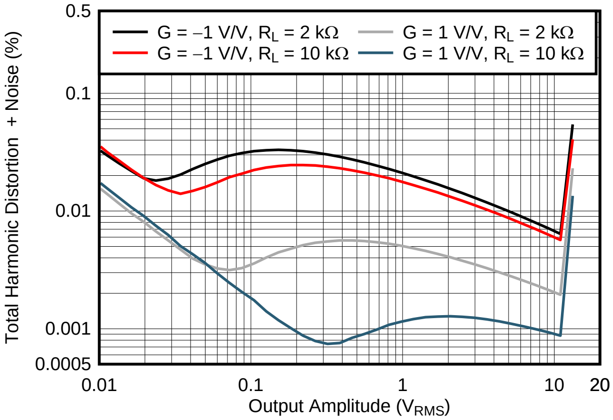


Figure 26. THD+N vs Output Amplitude

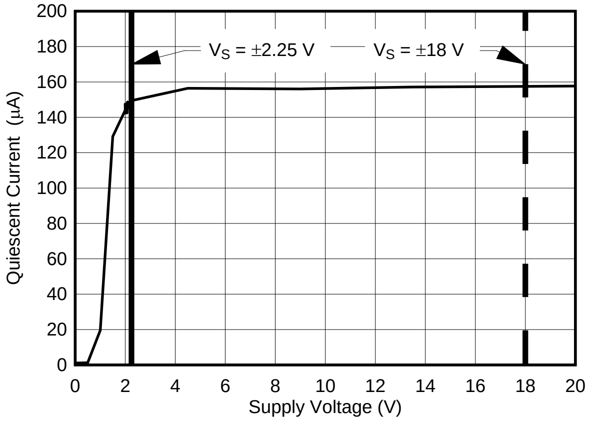


Figure 27. Quiescent Current vs Supply Voltage

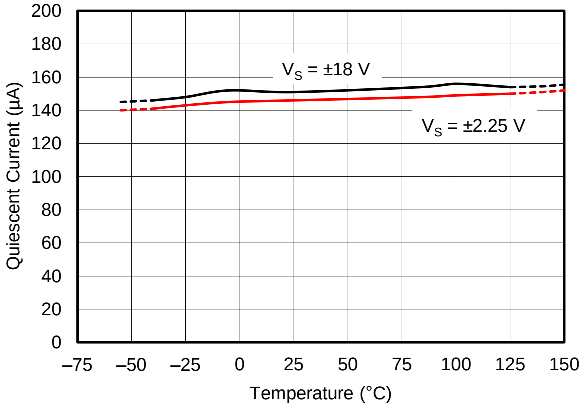
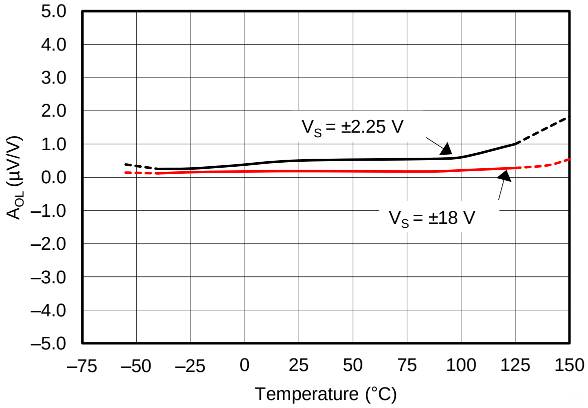
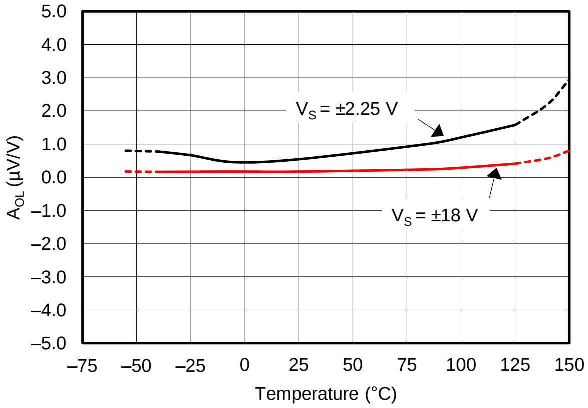


Figure 28. Quiescent Current vs Temperature



R_L = 10k Ω

Figure 29. Open-Loop Gain vs Temperature



R_L = 2k Ω

Figure 30. Open-Loop Gain vs Temperature

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

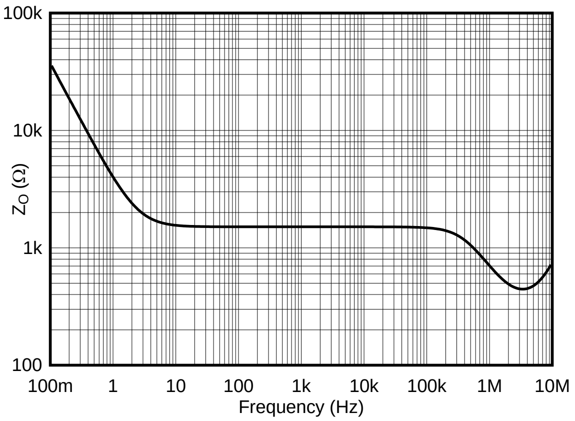
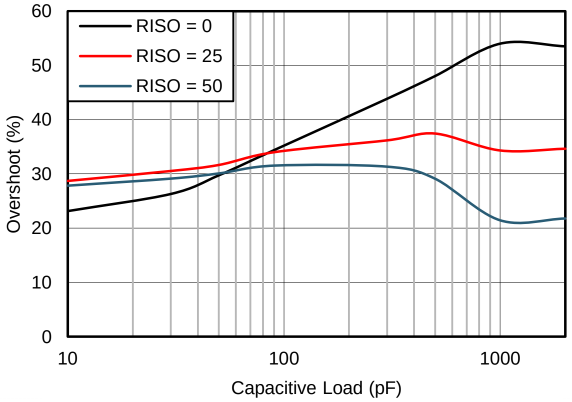
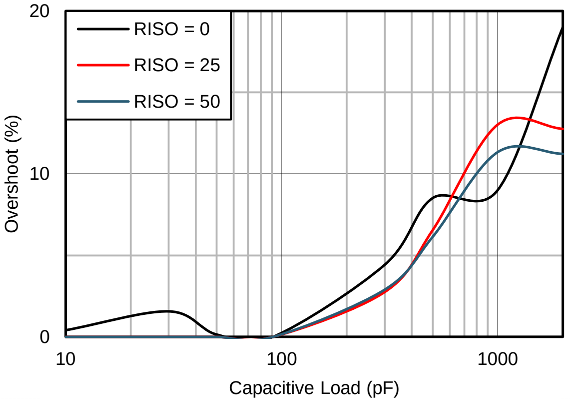


Figure 31. Open-Loop Output Impedance vs Frequency



G = –1, 100-mV output step

Figure 32. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)



G = 1, 100-mV output step

Figure 33. Small-Signal Overshoot vs Capacitive Load

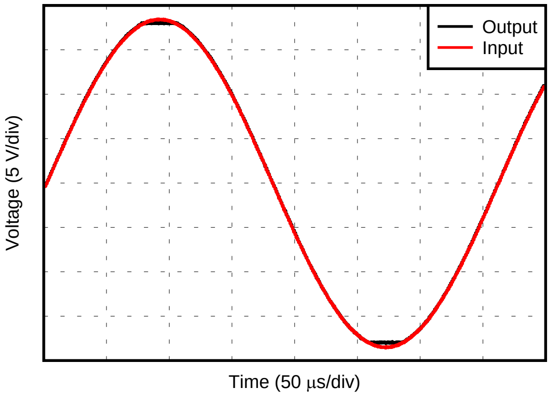
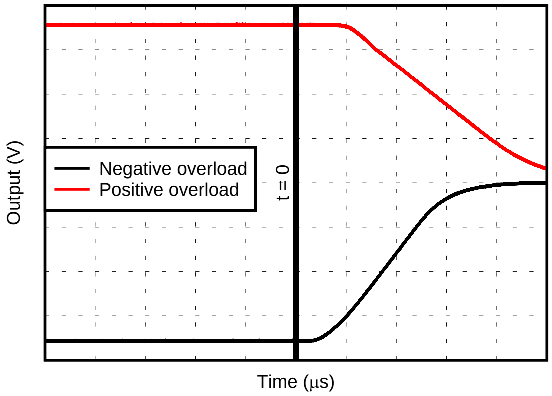
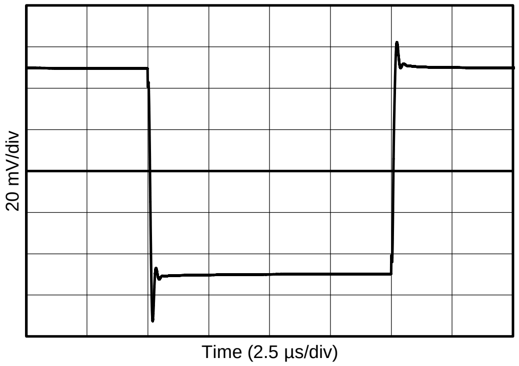


Figure 34. No Phase Reversal



V_S = ±18 V, G = –10 V/V

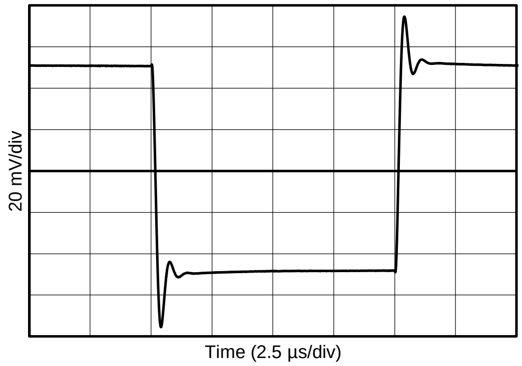
Figure 35. Overload Recovery



G = 1, C_L = 10 pF

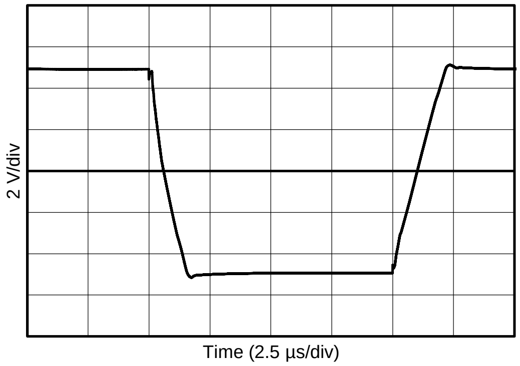
Figure 36. Small-Signal Step Response

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.



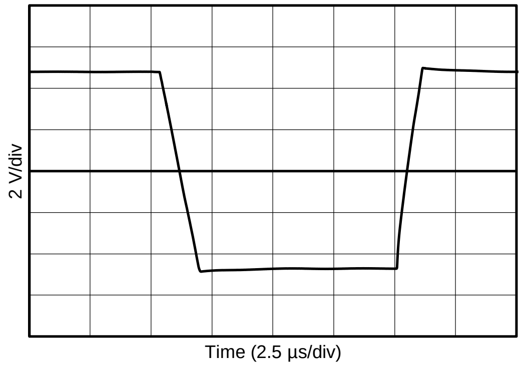
G = –1, R_L = 1 kΩ, C_L = 10 pF

Figure 37. Small-Signal Step Response



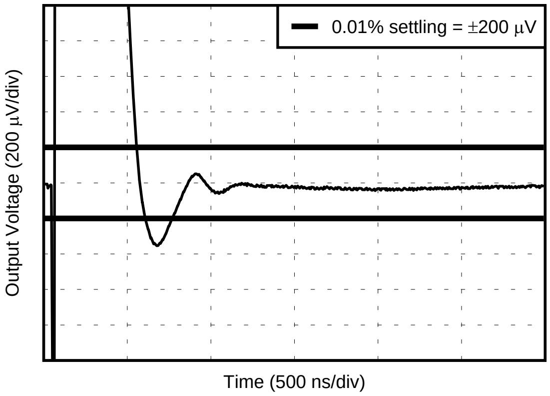
G = 1, C_L = 10 pF

Figure 38. Large-Signal Step Response



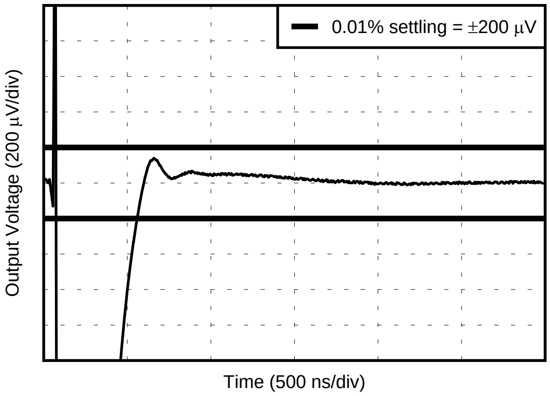
G = –1, R_L = 1 kΩ, C_L = 10 pF

Figure 39. Large-Signal Step Response



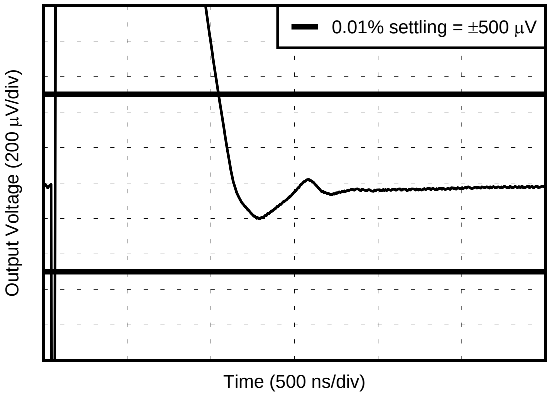
Gain = 1, 2-V step, rising, step applied at t = 0 µs on all four plots

Figure 40. 0.01% Settling Time



Gain = 1, 2-V step, falling, step applied at t = 0 µs

Figure 41. 0.01% Settling Time



Gain = 1, 5-V step, rising, step applied at t = 0 µs

Figure 42. 0.01% Settling Time

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

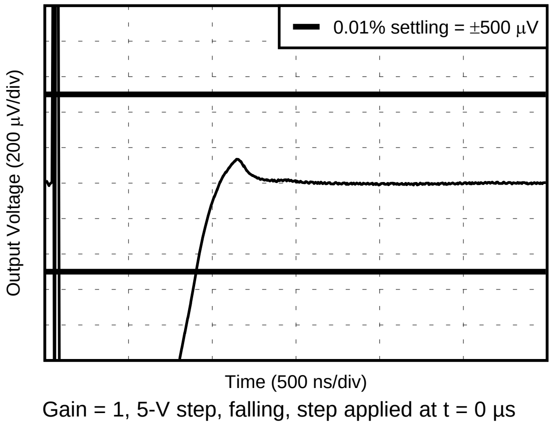


Figure 43. 0.01% Settling Time

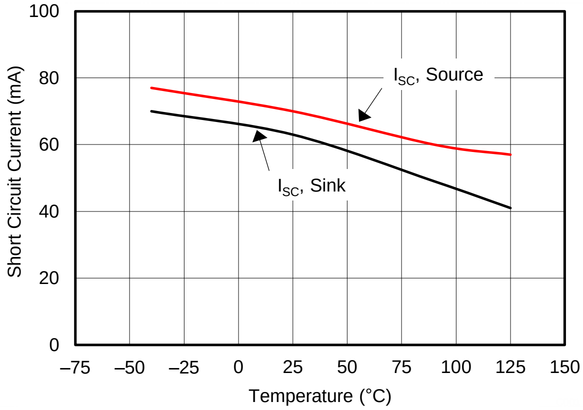


Figure 44. Short-Circuit Current vs Temperature

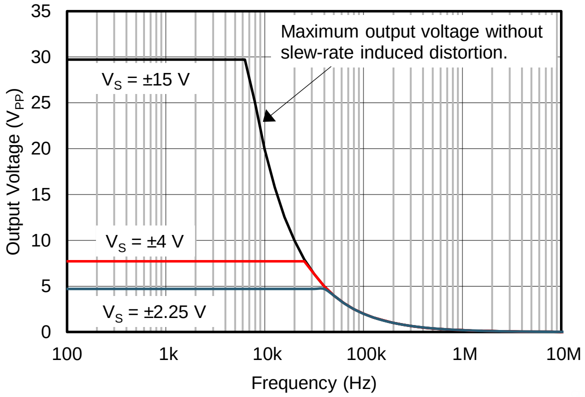


Figure 45. Maximum Output Voltage vs Frequency

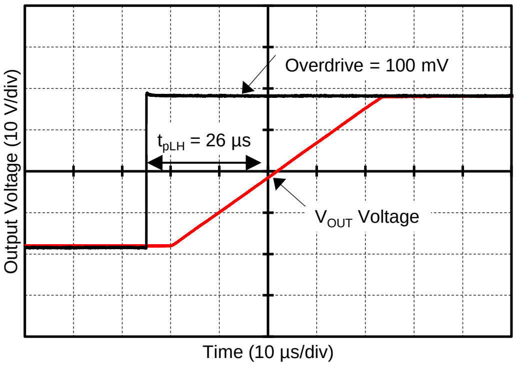


Figure 46. Propagation Delay Rising Edge

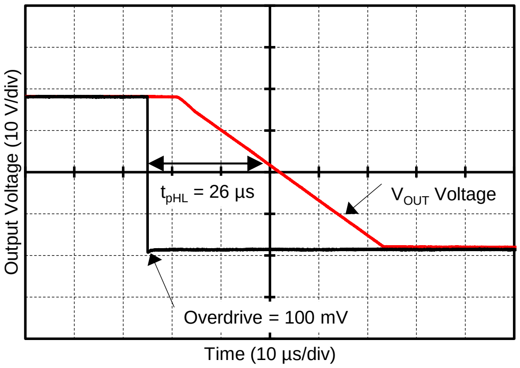


Figure 47. Propagation Delay Falling Edge

7 Parameter Measurement Information

7.1 Input Offset Voltage Drift

The OPAx191 family of operational amplifiers is manufactured using TI's *e-trim* technology. The e-trim technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing. Each amplifier input offset voltage and input offset voltage drift is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift. When trimming input offset voltage drift, the systematic or linear drift error on each device is trimmed to zero. Figure 48 illustrates this concept.

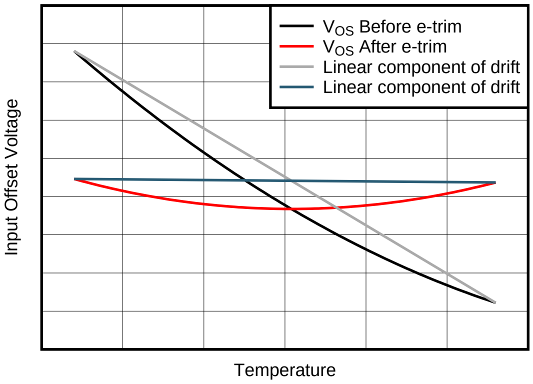


Figure 48. Input Offset Before and After Drift Trim

A common method of specifying input offset voltage drift is the *box method*. The box method estimates a maximum input offset drift by bounding an offset voltage versus temperature curve with a box and using the corners of this bounding box to determine the drift. The slope of the line connecting the diagonal corners of the box corresponds to the input offset voltage drift. Figure 49 illustrates the box method concept. The box method works particularly well when the input offset drift is dominated by the linear component of drift, but because the OPA191 family uses TI's e-trim technology to remove the linear component input offset voltage drift, the box method is not a particularly useful method of accurately performing an error analysis. Shown in Figure 49 are 30 typical units of OPAx191 with the box method superimposed for illustrative purposes. The boundaries of the box are determined by the specified temperature range along the x-axis and the maximum specified input offset voltage across that same temperature range along the y-axis. Using the box method predicts an input offset voltage drift of 0.9 µV/°C. As shown in Figure 49, the slopes of the actual input offset voltage versus temperature are much less than that predicted by the box method. The box method predicts a pessimistic value for the maximum input offset voltage drift and is not recommended when performing an error analysis.

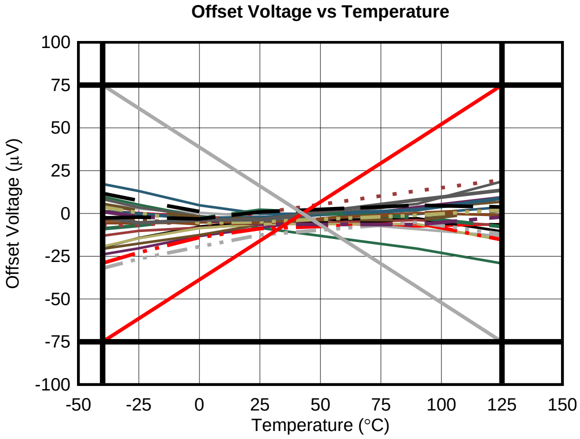


Figure 49. The Box Method

Input Offset Voltage Drift (continued)

Instead of the box method, a convenient way to illustrate input offset drift is to compute the slopes of the input offset voltage versus temperature curve. This is the same as computing the input offset drift at each point along the input offset voltage versus temperature curve. The results for the OPAx191 family are illustrated in Figure 50.

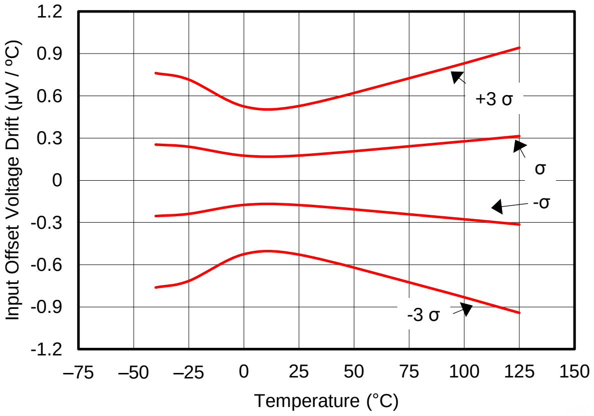


Figure 50. Input Offset Voltage Drift vs Temperature (SOIC Package)

As illustrated in Figure 50, the input offset drift is typically less than ±0.3 µV/°C over the range from –40°C to +125°C. When performing an error analysis over the full specified temperature range, use the typical and maximum values for input offset voltage drift as described in the *Electrical Characteristics* tables. If a reduced temperature range is applicable, use the information illustrated in Figure 50 when performing an error analysis. To determine the change in input offset voltage, use Equation 1:

$$\Delta V_{OS} = \Delta T \times dV_{OS}/dT$$

where

- ΔV_{OS} = Change in input offset voltage
- ΔT = Change in temperature
- dV_{OS}/dT = Input offset voltage drift (1)

For example, determine the amount of OPA191ID input offset voltage change over the temperature range of 25°C to 75°C for 1 σ (68%) of the units. As shown in Figure 50, the input offset drift is typically 0.25 µV/°C. This input offset drift results in a typical input offset voltage change of (75°C – 25°C) × 0.25 µV/°C = 12.5 µV.

For 3 σ (99.7%) of the units, Figure 50 shows a typical input offset drift of approximately 0.75 µV/°C. This input offset drift results in a typical input offset voltage change of (75°C – 25°C) × 0.75 µV/°C = 37.5 µV.

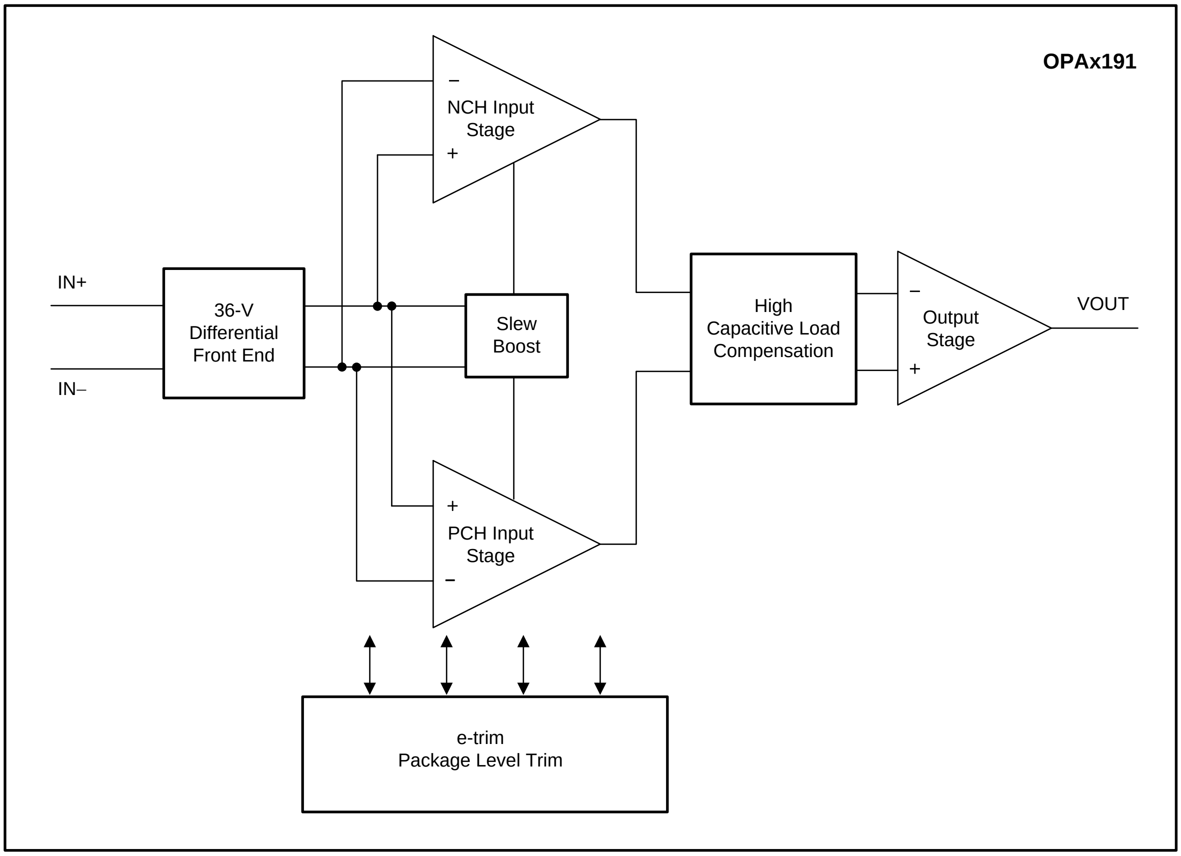
8 Detailed Description

8.1 Overview

The OPAx191 family of operational amplifiers use *e-trim*, a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding. The trim communication occurs on the output pin of the standard pinout, and after the trim points are set, further communication to the trim structure is permanently disabled. The *Functional Block Diagram* section shows the simplified diagram of the OPA191 with e-trim.

Unlike previous e-trim op amps, the OPAx191 uses a patented two-temperature trim architecture to achieve a very low offset voltage and low voltage offset drift over the full specified temperature range. This level of precision performance at wide supply voltages makes these amplifiers useful for high-impedance industrial sensors, filters, and high-voltage data acquisition.

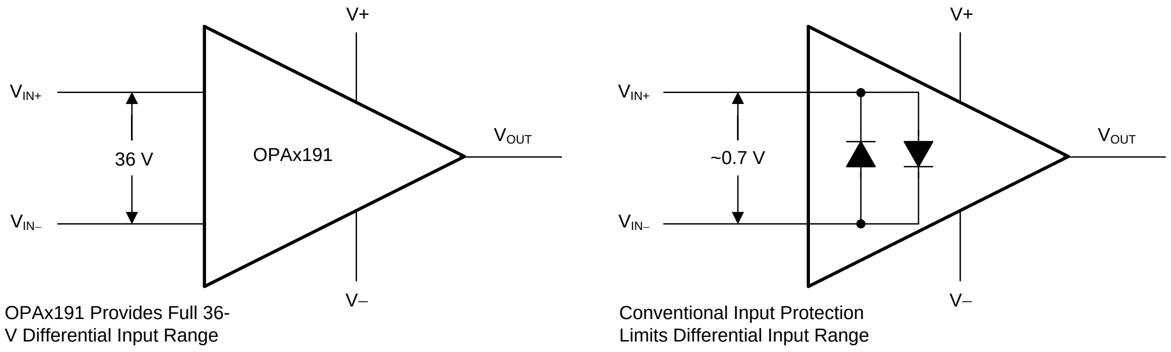
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Protection Circuitry

The OPAx191 uses a unique input architecture to eliminate the need for input protection diodes but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 51 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 52. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current, resulting in extended settling time.



OPAx191 Provides Full 36-V Differential Input Range

Conventional Input Protection Limits Differential Input Range

Figure 51. OPA191 Input Protection Does Not Limit Differential Input Capability

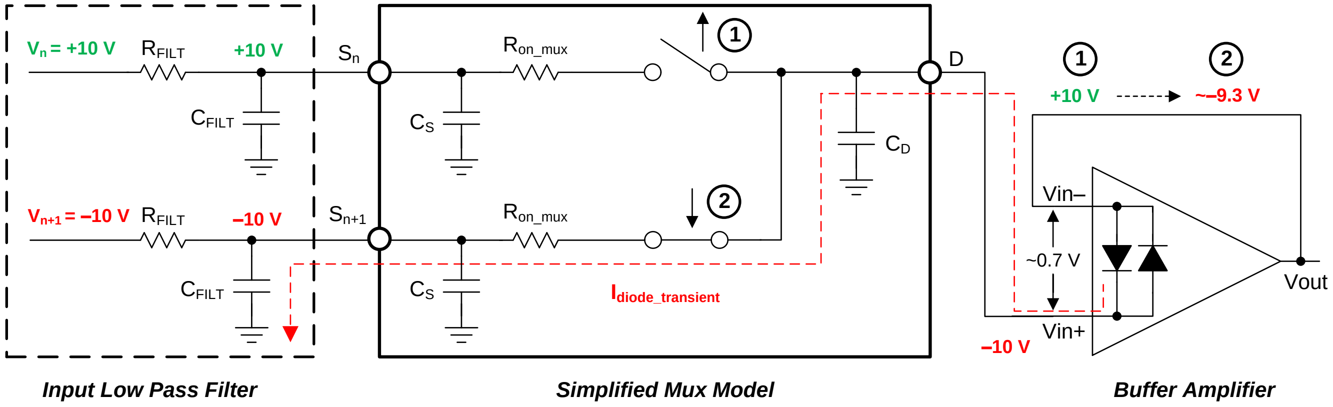


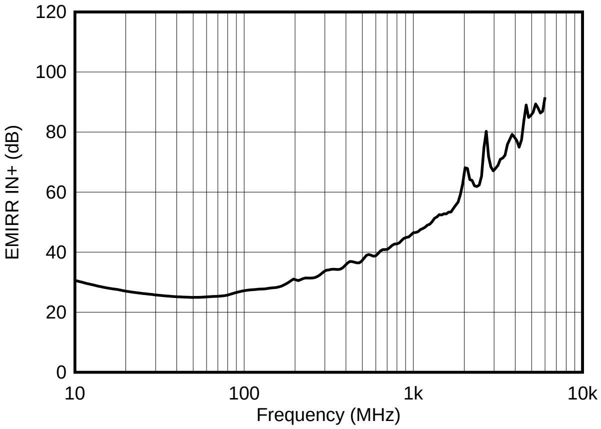
Figure 52. Back-to-Back Diodes Create Settling Issues

The OPAx191 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPA191 can tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 36 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as multiplexed data-acquisition systems (see Figure 64.

Feature Description (continued)

8.3.2 EMI Rejection

The OPAx191 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx191 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 53 shows the results of this testing on the OPAx191. Table 2 shows the EMIRR IN+ values for the OPAx191 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the application report *EMI Rejection Ratio of Operational Amplifiers*, SBOA128, available for download from www.ti.com.



P_{RF} = –10 dBm, V_S = ±15 V, V_{CM} = 0 V

Figure 53. EMIRR Testing

Table 2. OPA191 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	36 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	45 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	57 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	62 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	76 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	86 dB

8.3.3 Phase Reversal Protection

The OPAx191 family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx191 is a rail-to-rail input op amp, and therefore the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 54.

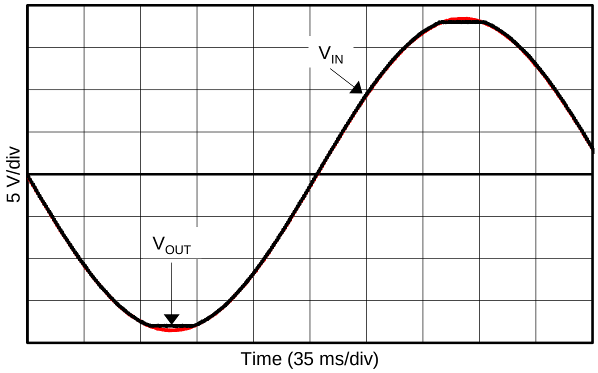


Figure 54. No Phase Reversal

8.3.4 Thermal Protection

The internal power dissipation of any amplifier causes the internal (junction) temperature to rise. This phenomenon is called *self heating*. The OPAx191 has a thermal protection feature that prevents damage from self heating.

This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive for temperatures above approximately 180°C. Thermal protection forces the output to a high-impedance state. The OPAx191 is also designed with approximately 30°C of thermal hysteresis. Thermal hysteresis prevents the output stage from cycling in and out of the high-impedance state. The OPAx191 returns to normal operation when the output stage temperature falls below approximately 150°C.

The absolute maximum junction temperature of the OPAx191 is 150°C. Exceeding the limits shown in the *Absolute Maximum Ratings* table may cause damage to the device. Thermal protection triggers at 180°C because of unit-to-unit variance, but does not interfere with device operation up to the absolute maximum ratings. This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

8.3.5 Capacitive Load and Stability

The OPAx191 features a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, directly drives up to 1 nF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 55. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

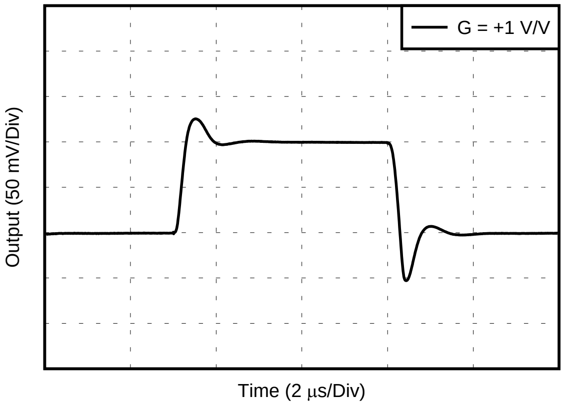


Figure 55. Transient Response with a Purely Capacitive Load of 1 nF

Like many low-power amplifiers, some ringing can occur even with capacitive loads less than 100 pF. In unity-gain configurations with no or very light dc loads, place an RC snubber circuit at the OPAx191 output to reduce any possibility of ringing in lightly-loaded applications. Figure 56 illustrates the recommended RC snubber circuit.

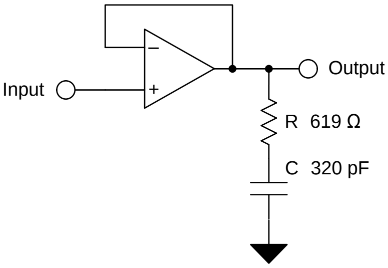


Figure 56. RC Snubber Circuit for Lightly-Loaded Applications in Unity Gain

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small, 10-Ω to 20-Ω resistor (R_{ISO}) in series with the output, as shown in Figure 57. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPA191 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 57 uses R_{ISO} to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin. Results using the OPA191 are summarized in Table 3. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIDU032 details complete design goals, simulation, and test results.

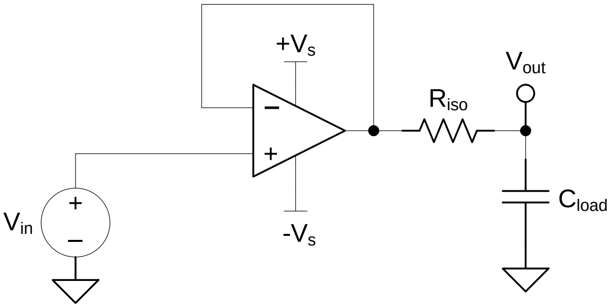


Figure 57. Extending Capacitive Load Drive With the OPA191

Table 3. OPA191 Capacitive Load Drive Solution Using Isolation Resistor Comparison of Calculated and Measured Results

PARAMETER	VALUE								
Capacitive Load	**100 pF**	**1000 pF**		**0.01 µF**		**0.1 µF**		**1 µF**	
Phase Margin	**45°**	**45°**	**60°**	**45°**	**60°**	**45°**	**60°**	**45°**	**60°**
R_{ISO} (Ω)	280	113	432	68	210	17.8	53.6	3.6	10
Measured Overshoot (%)	23	23	8	23	8	23	8	23	8

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design TIDU032, *Capacitive Load Drive Solution using an Isolation Resistor* .

8.3.6 Common-Mode Voltage Range

The OPAx191 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 58. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 3 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.5 V. There is a small transition region, typically (V+) –3 V to (V+) – 1.5 V in which both input pairs are active. This transition region varies modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance are degraded compared to operation outside this region.

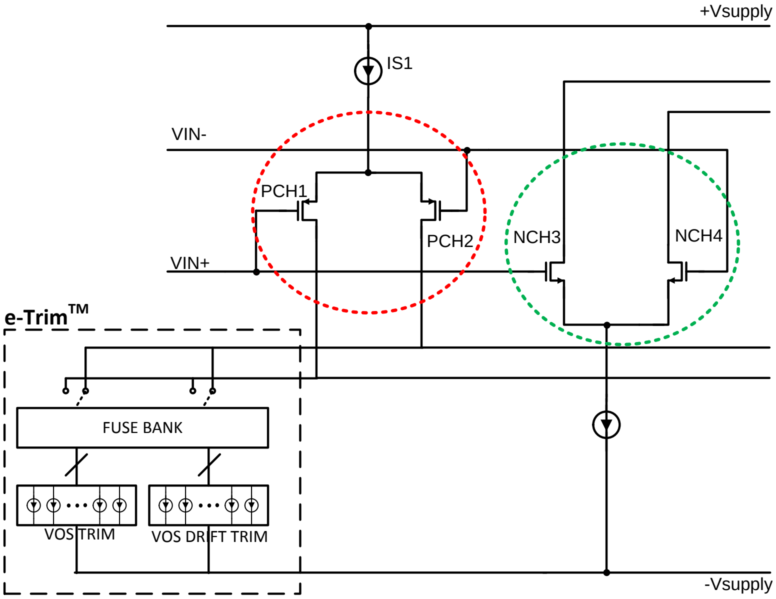


Figure 58. Rail-to-Rail Input Stage

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPAx191 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range, as shown in Figure 59.

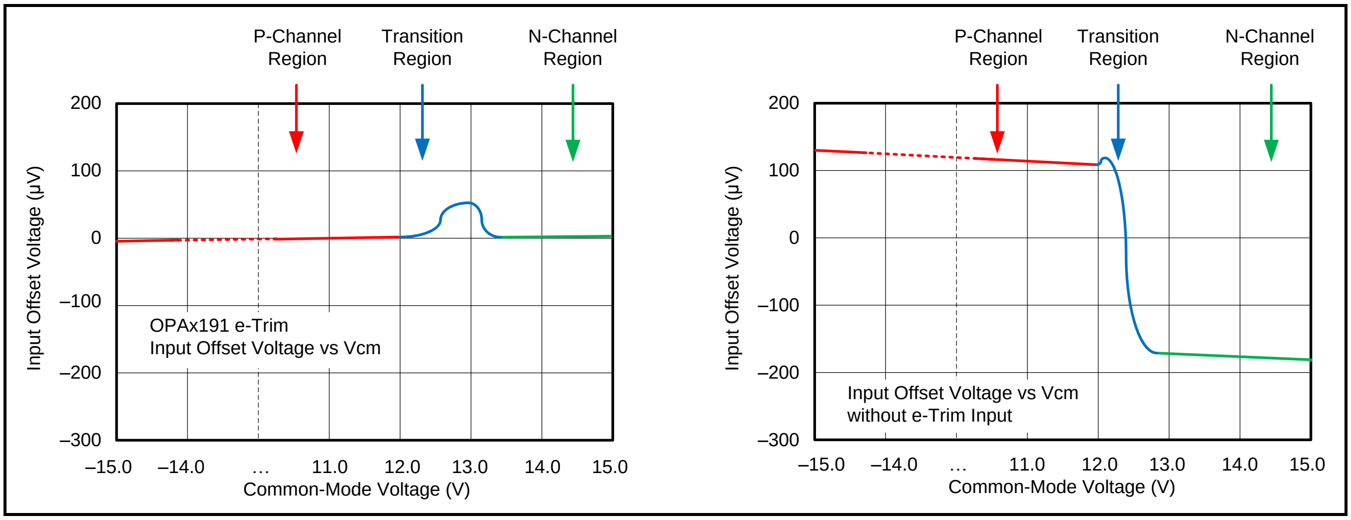


Figure 59. Common-Mode Transition vs Standard Rail-to-Rail Amplifiers

8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See Figure 60 for an illustration of the ESD circuits contained in the OPAx191 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

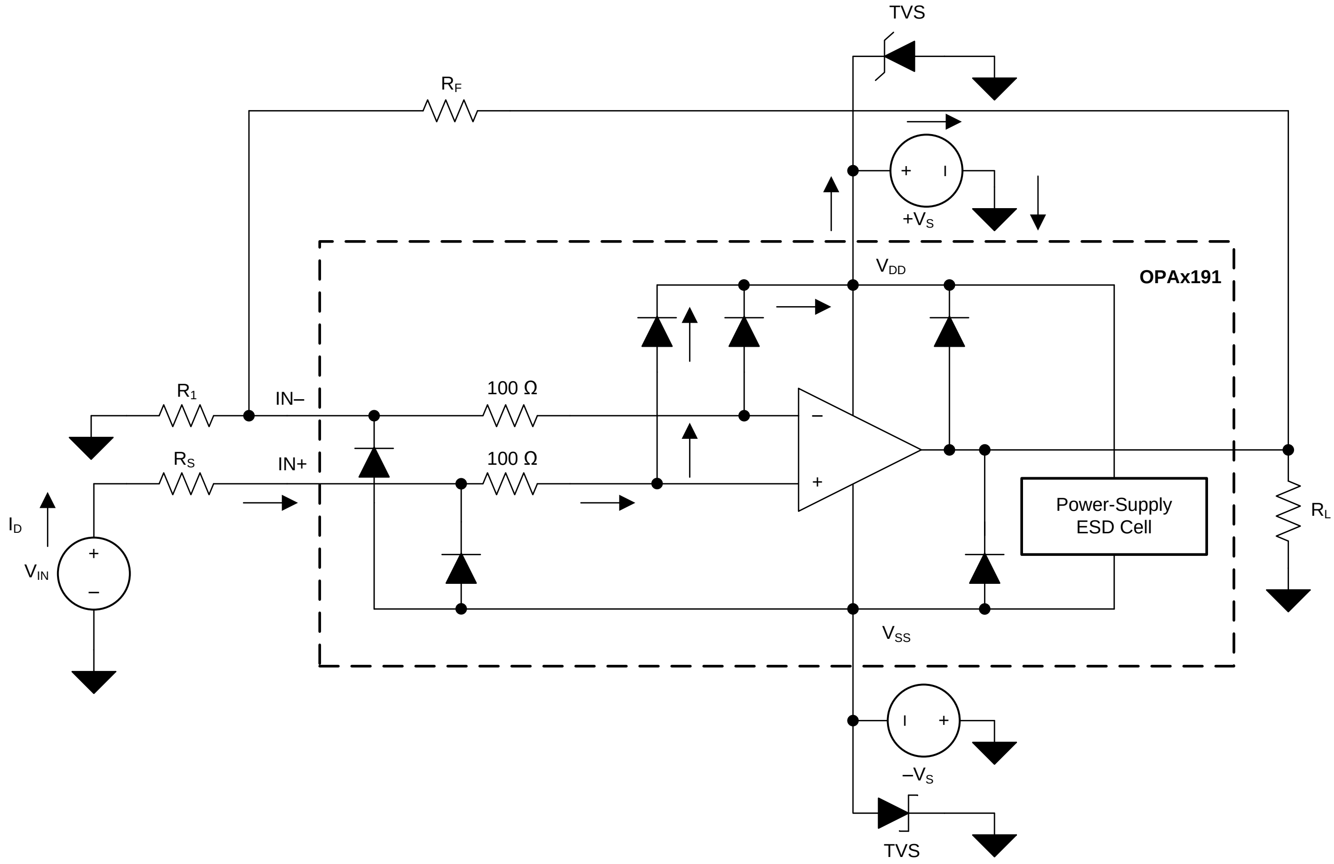


Figure 60. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very high voltage for a very short duration (for example, 1 kV for 100 ns); whereas, an EOS event is lower voltage for a longer duration (for example, 50 V for 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit labeled ESD power-supply circuit. The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressor (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

8.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time.

8.4 Device Functional Modes

The OPAx191 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx191 is 36 V (±18 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx191 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer true rail-to-rail input/output, ultralow offset voltage and offset voltage drift, as well as 2-MHz bandwidth and high capacitive load drive. These features make the OPAx191 a robust, high-performance operational amplifier for high-voltage industrial applications.

9.2 Typical Applications

9.2.1 Low-side Current Measurement

Figure 61 shows the OPA191 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 61 including theory, calculations, simulations, and measured data see the 0-1A, single-supply, low-side, current sensing solutionTIPD129.

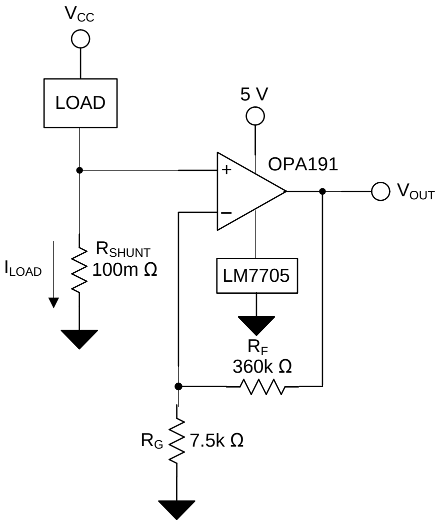


Figure 61. OPA191 in a Low-Side, Current-Sensing Application

9.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 61 is given in Equation 2

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{2}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 3.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{3}$$

Using Equation 3, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPA191 to produce an output voltage of 0 V to 4.9 V. The gain needed by the OPA191 to produce the necessary output voltage is calculated using Equation 4:

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \tag{4}$$

Using Equation 4, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. Equation 5 is used to size the resistors, R_F and R_G, to set the gain of the OPA191 to 49 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \tag{5}$$

Choosing R_F as 360 kΩ, R_G is calculated to be 7.5 kΩ. R_F and R_G were chosen as 360 kΩ and 7.5 kΩ because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. Figure 2 shows the measured transfer function of the circuit shown in Figure 61.

9.2.1.3 Application Curves

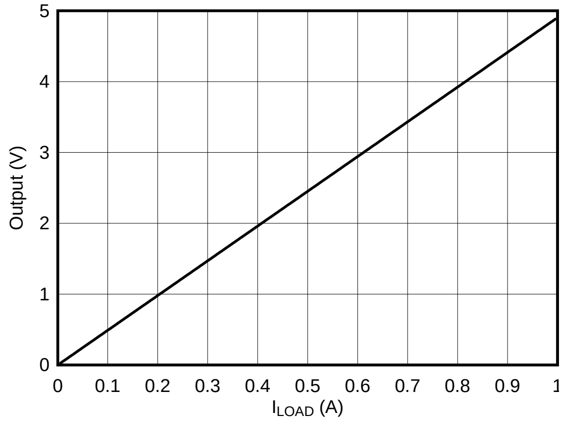


Figure 62. Low-Side, Current-Sense, Transfer Function

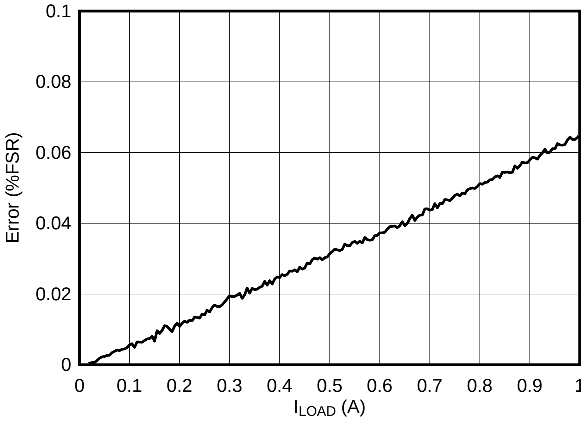


Figure 63. Low-Side, Current-Sense, Full-Scale Error

Typical Applications (continued)

9.2.2 16-Bit Precision Multiplexed Data-Acquisition System

Figure 64 shows a 16-bit, differential, 4-channel, multiplexed, data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR), analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front-end, and a 4-channel differential multiplexer (mux). This application example shows the process for optimizing the precision, high-voltage, front-end drive circuit using the OPA191 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864. The full TI Precision Design can be found in TIDU181.

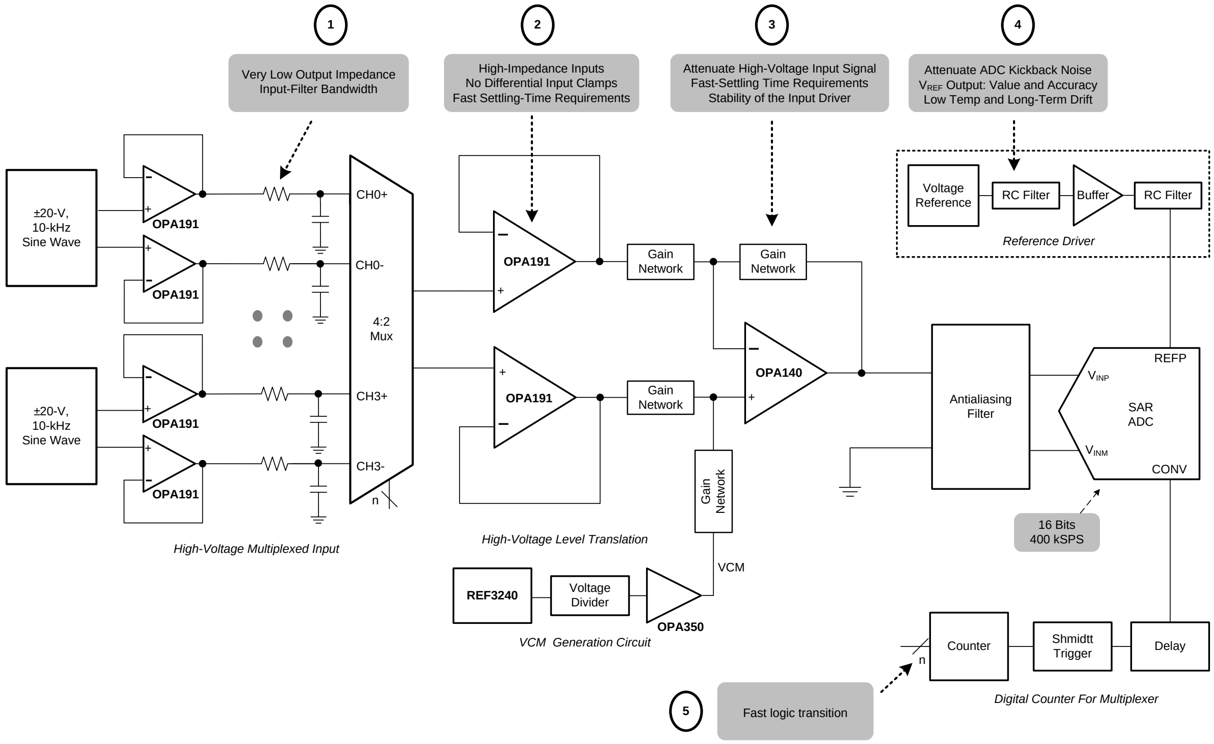


Figure 64. OPA191 in 16-Bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High-Voltage Inputs With Lowest Distortion

9.2.2.1 Design Requirements

The primary objective is to design a ±20-V, differential, 4-channel, multiplexed, data acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10-kHz, full-scale, pure sine-wave input. The design requirements for this block design are:

- System supply voltage: ±15 V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 10 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

9.2.2.2 Detailed Design Procedure

The purpose of this application example is to design an optimal, high-voltage, multiplexed, data-acquisition system for highest system linearity and fast settling. The overall system block diagram is shown in Figure 64. The circuit is a multichannel, data-acquisition, signal chain consisting of an input low-pass filter, multiplexer (mux), mux output buffer, attenuating SAR ADC driver, digital counter for the mux, and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. The two

Typical Applications (continued)

primary design considerations to maximize the performance of a precision, multiplexed, data-acquisition system are the mux input analog front-end and the high-voltage, level translation, SAR ADC driver design. However, carefully design each analog circuit block based on the ADC performance specifications in order to achieve the fastest settling at 16-bit resolution and lowest distortion system. Figure 64 includes the most important specifications for each individual analog block.

This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. The first step in the design is to understand the requirement for an extremely-low-impedance input-filter design for the mux. This understanding helps in the decision of an appropriate input filter and selection of a mux to meet the system settling requirements. The next important step is the design of the attenuating analog front-end (AFE) used to level translate the high-voltage input signal to a low-voltage ADC input while maintaining the amplifier stability. Then, the next step is to design a digital interface to switch the mux input channels with minimum delay. The final design challenge is to design a high-precision, reference-driver circuit that provides the required REFP reference voltage with low offset, drift, and noise contributions.

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIDU181, *16-bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High Voltage Inputs with Lowest Distortion*.

9.2.3 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx191 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems.Figure 65 shows the OPA191 in a slew-rate limit design.

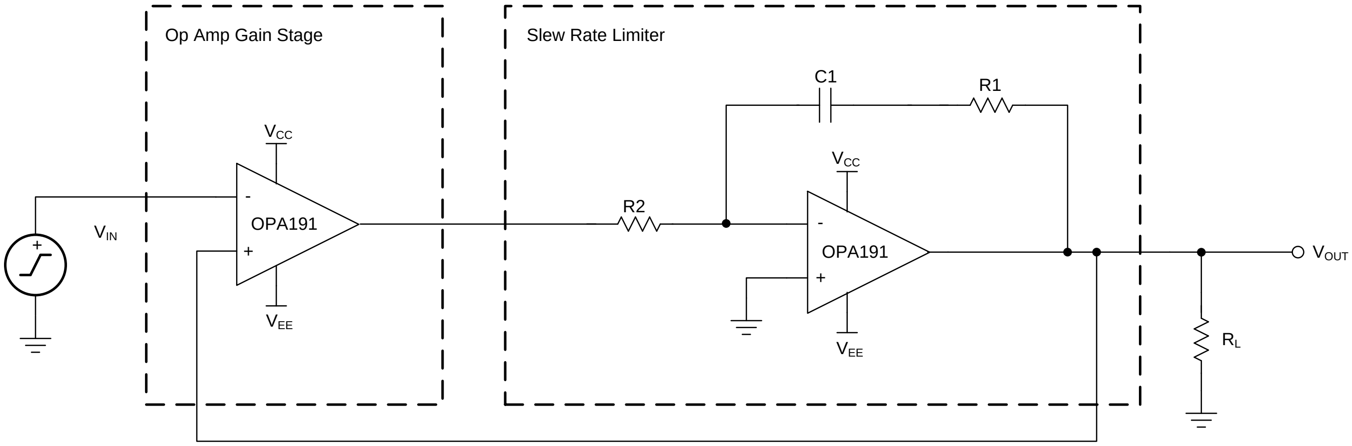


Figure 65. Slew Rate Limiter Uses One Op Amp

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIDU026, *Slew Rate Limiter Uses One Op Amp*.

10 Power-Supply Recommendations

The OPAx191 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 67, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

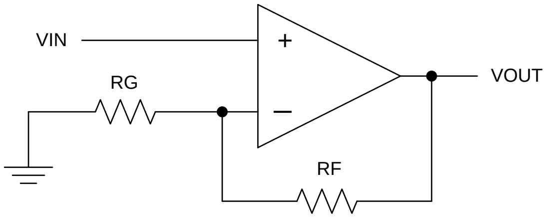


Figure 66. Schematic Representation

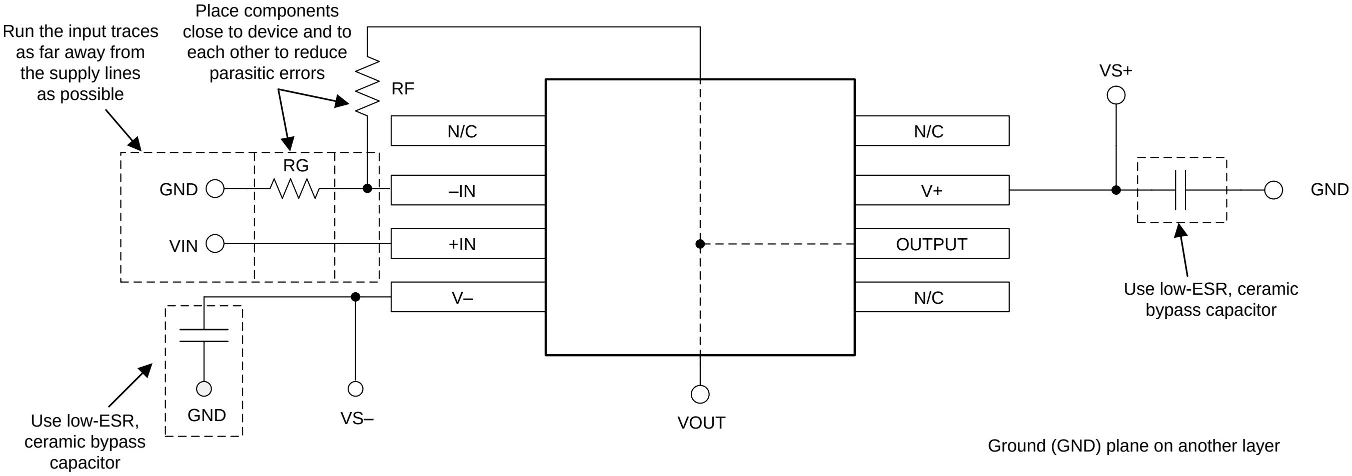


Figure 67. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder at http://www.ti.com/tool/tina-ti.

12.1.1.2 TI Precision Designs

TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/, are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

12.2 Documentation Support

12.2.1 Related Documentation

- *Circuit Board Layout Techniques*, SLOA089.
- *Op Amps for Everyone*, SLOD006.

12.3 Related Links

Table 4 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA191	Click here	Click here	Click here	Click here	Click here
OPA2191	Click here	Click here	Click here	Click here	Click here
OPA4191	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA191ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA191	Samples
OPA191IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZAMV	Samples
OPA191IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZAMV	Samples
OPA191IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZANV	Samples
OPA191IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZANV	Samples
OPA191IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA191	Samples
OPA2191ID	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191	
OPA2191IDR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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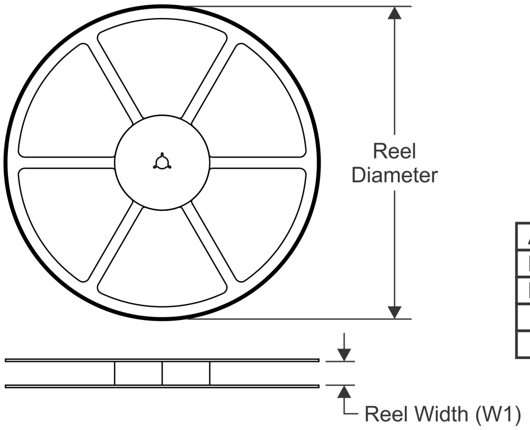
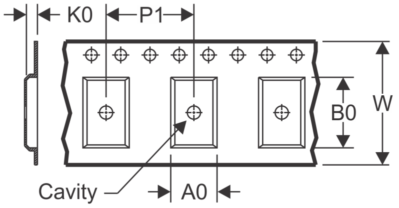
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

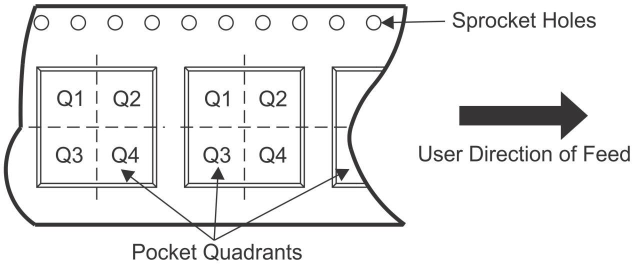


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

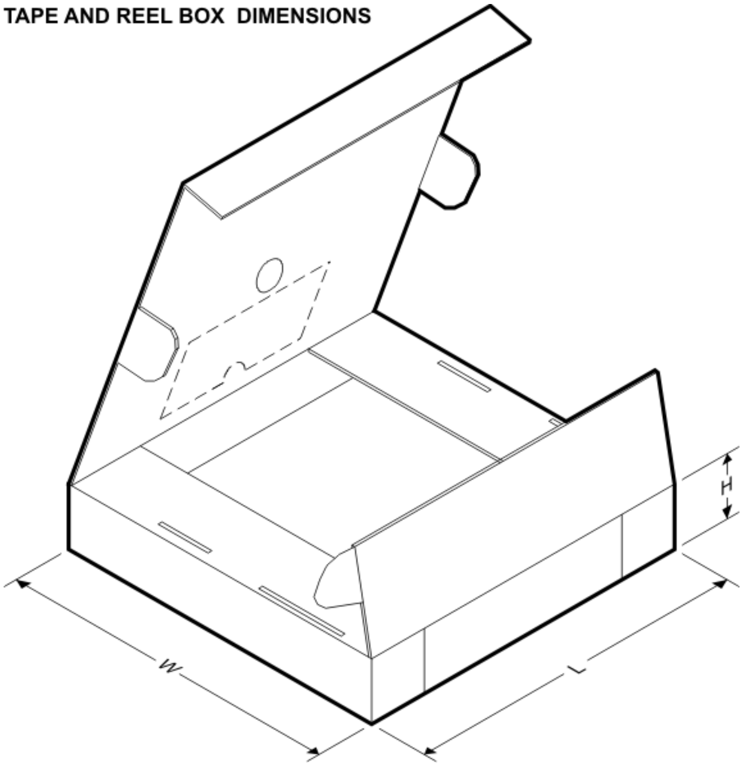
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA191IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA191IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA191IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA191IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA191IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

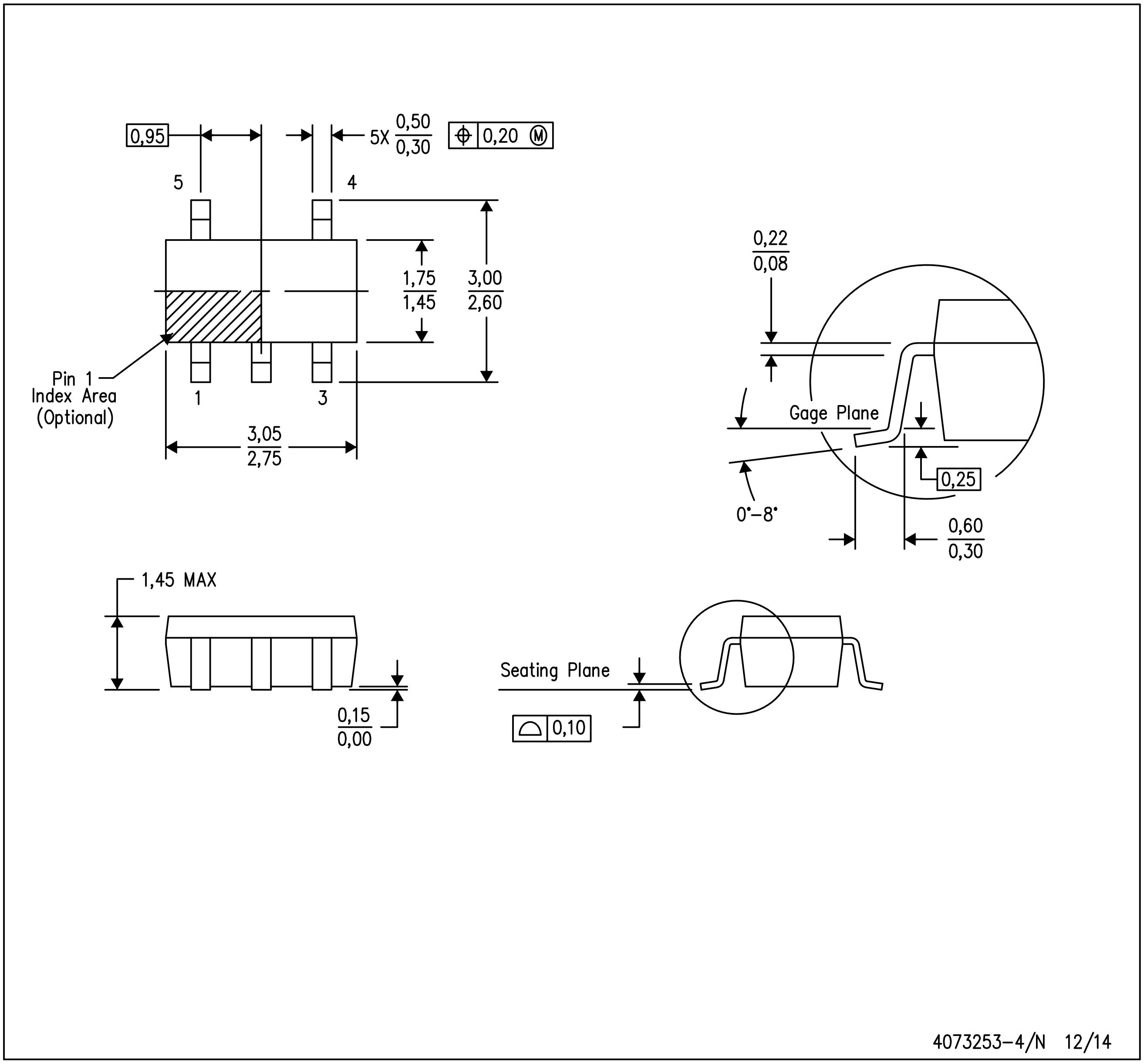
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

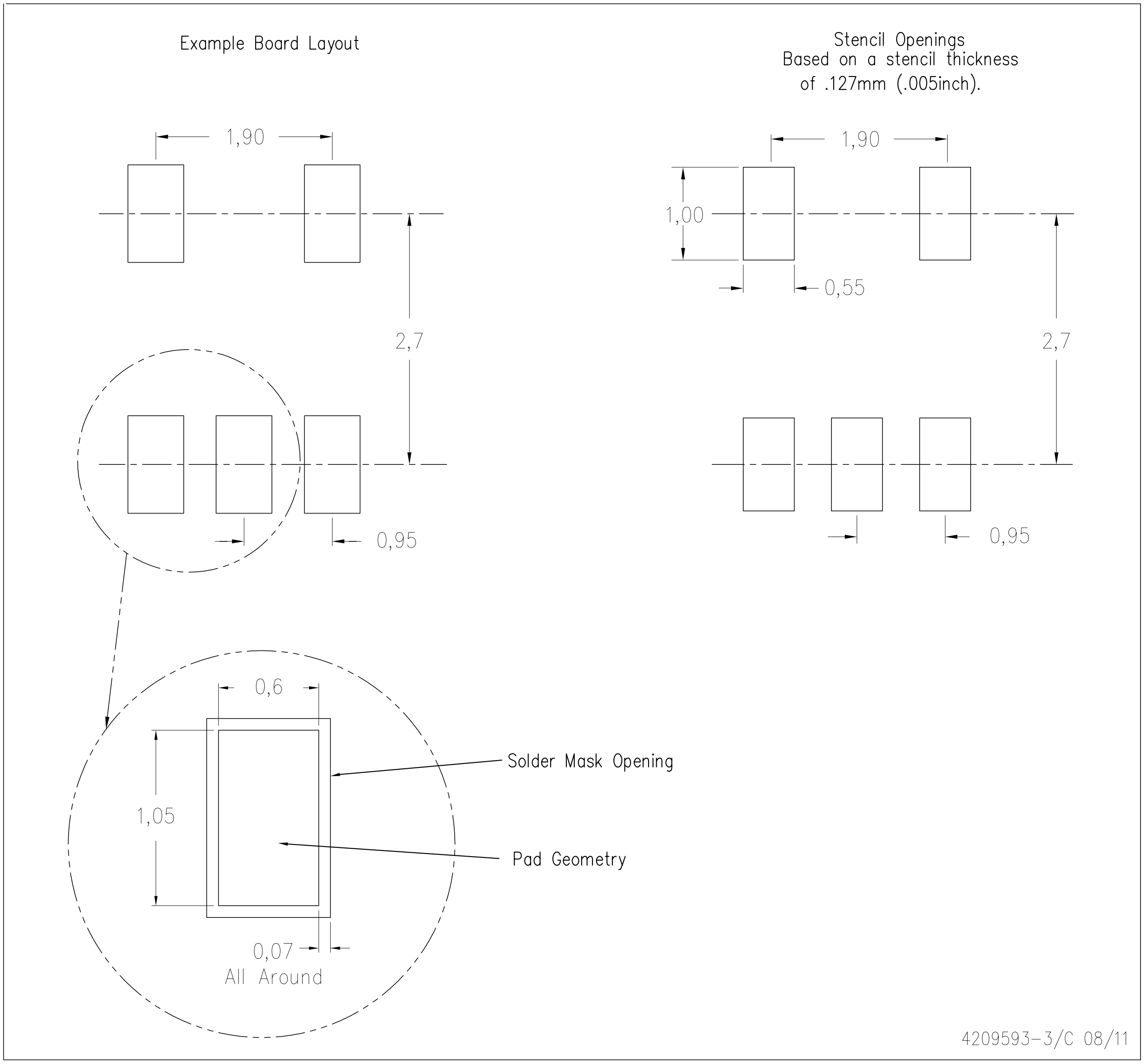
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA191IDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA191IDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA191IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
OPA191IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
OPA191IDR	SOIC	D	8	2500	367.0	367.0	35.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



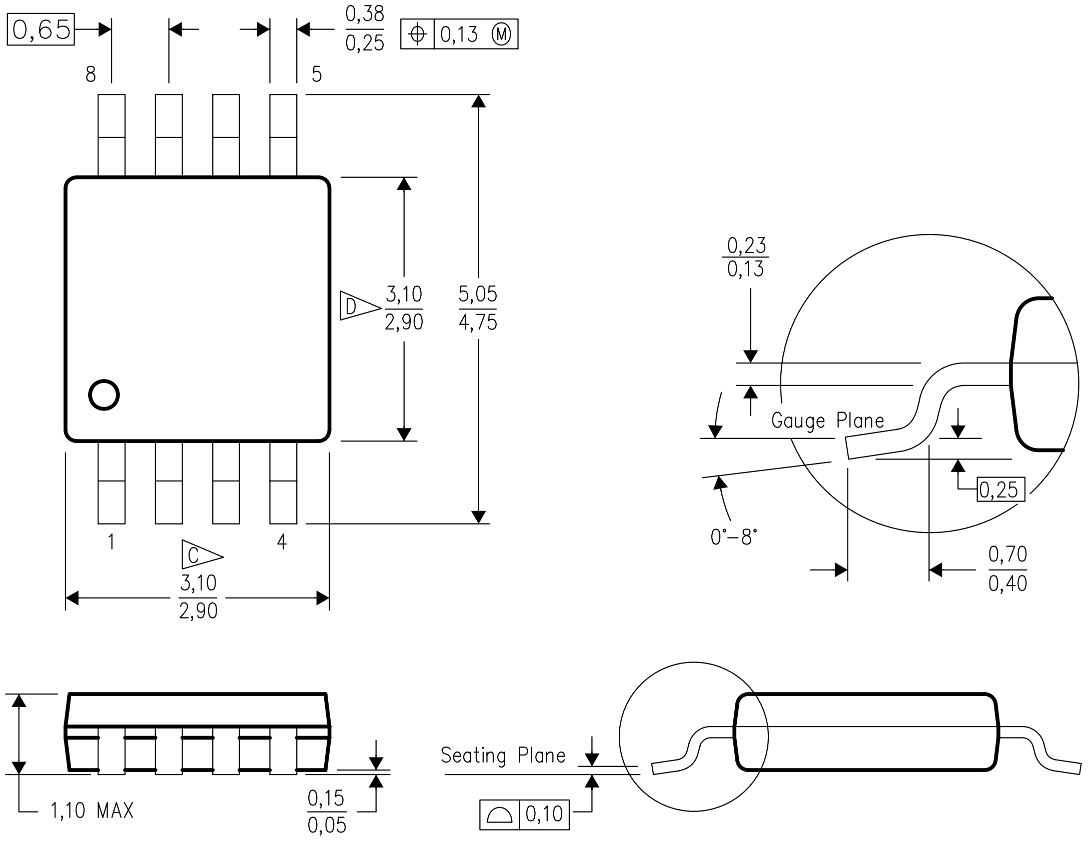
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO–178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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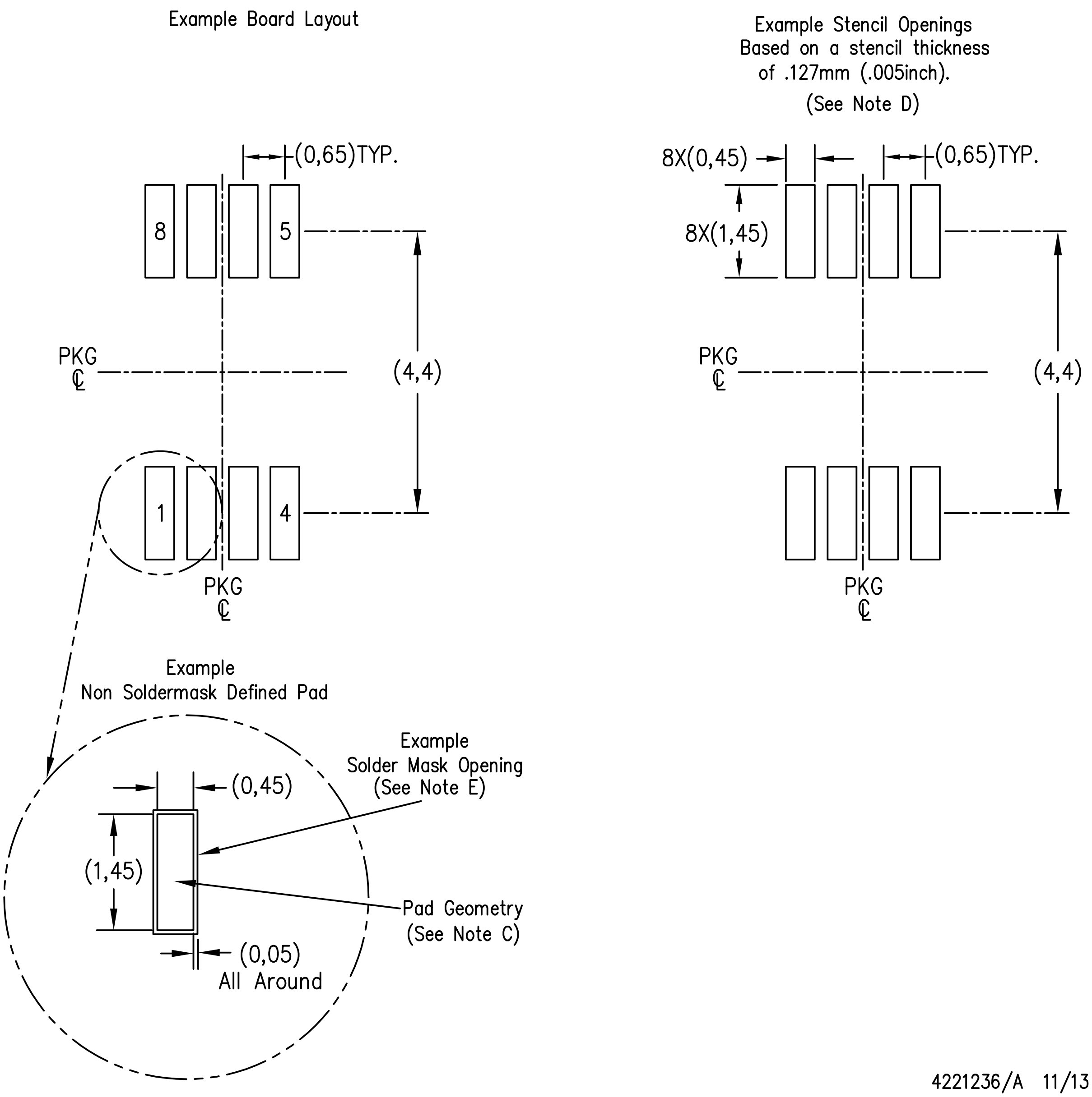
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



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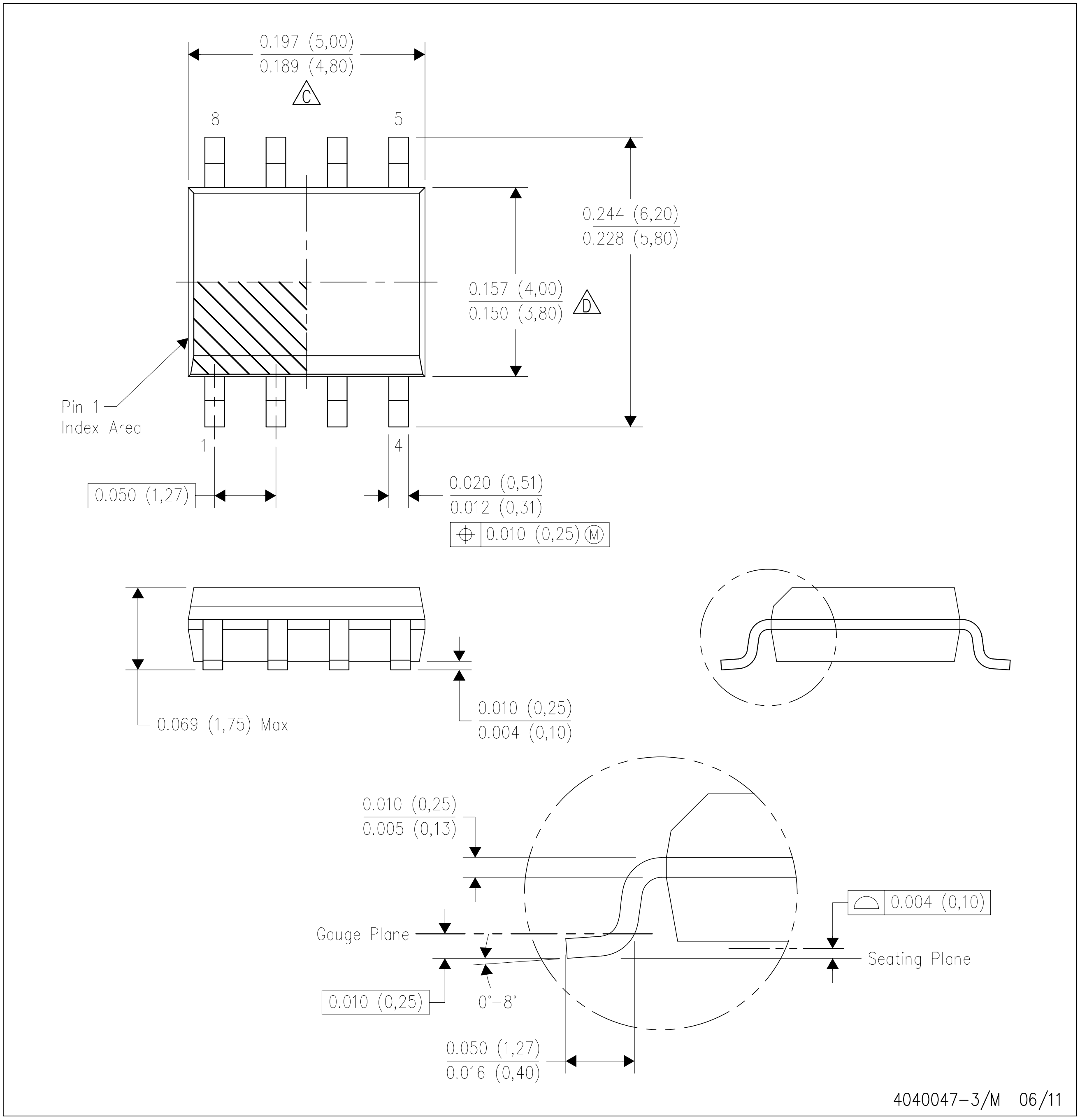
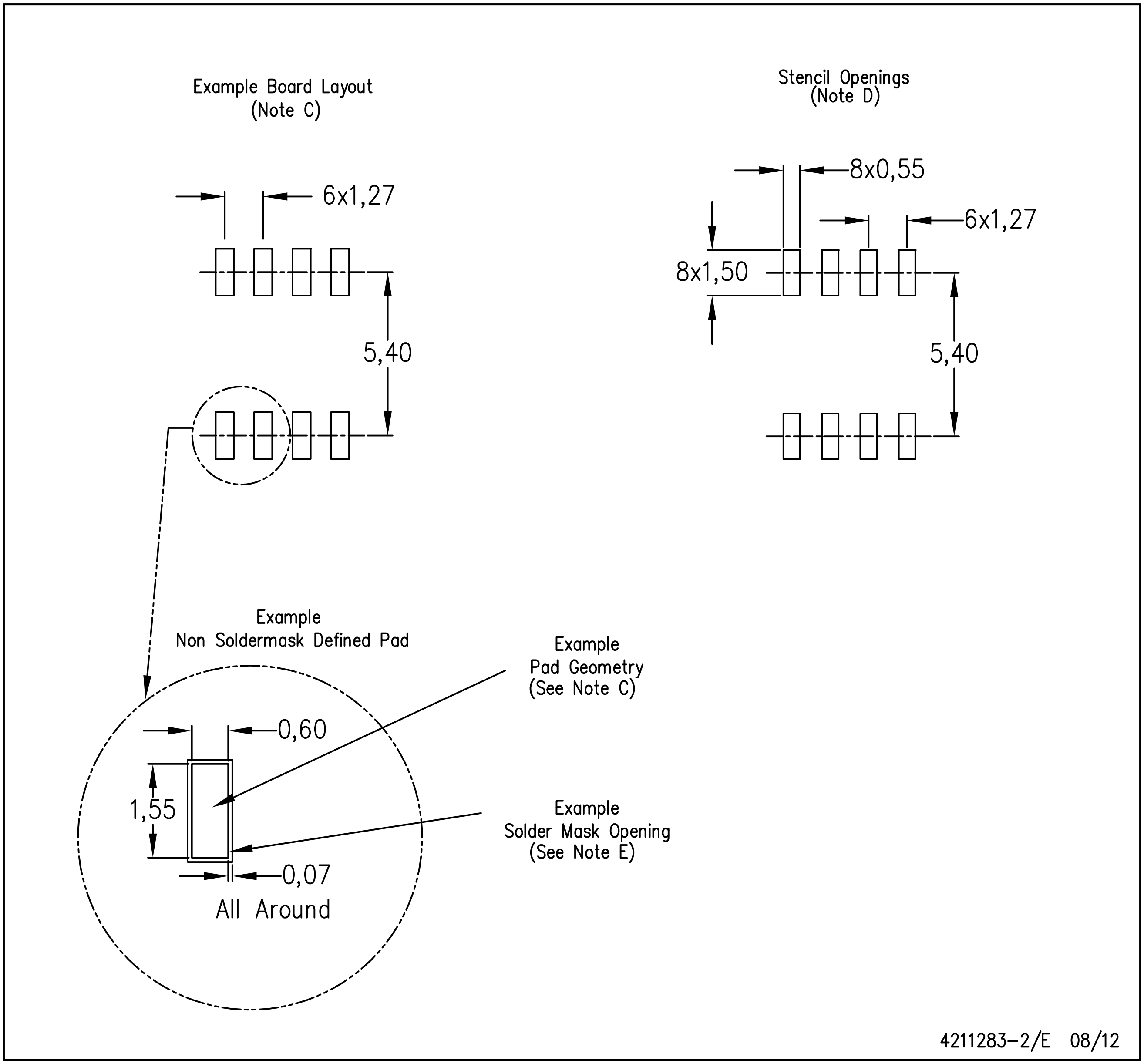
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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