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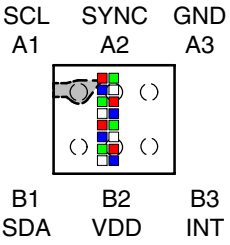
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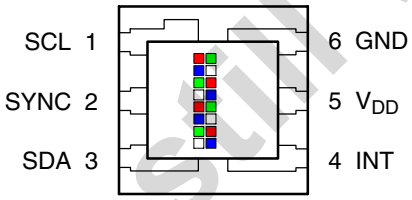
Features

- Programmable Interrupt Function with User-Defined Upper and Lower Threshold Settings
- Internal Filter Eliminates Signal Fluctuation Due to AC Lighting Flicker — No External Capacitor Required
- In-Package Trim Provides an Easy and Accurate Means to Achieve System-to-System Repeatability
- 16-Bit Digital Output with I^2C at 400 kHz
- Programmable Analog Gain and Integration Time Supporting 1,000,000-to-1 Dynamic Range
- SYNC Input Synchronizes Integration Cycle to Modulated Light Sources (e.g. PWM)
- Operating Temperature Range
  - –40°C to 85°C (CS Package)
  - –30°C to 70°C (FN Package)
- Operating voltage of 2.7 V to 3.6 V
- Available in Both an FN and a CS Package. The CS Package is the Industry's Smallest Digital RGB Color Sensor

PACKAGE CS
6-LEAD CHIPSCALE
(TOP VIEW)



PACKAGE FN
DUAL FLAT NO-LEAD
(TOP VIEW)



Package Drawings are Not to Scale

Applications

- Provides Method to Derive Chromaticity Coordinates to Manage Display Backlighting (i.e. RGB LED, CCFL, etc.)
- Provides Means to Derive Color Temperature to White-Color Balance Displays Under Various Lighting Conditions

End Products and Market Segments

- HDTVs
- Tablets, Laptops, Monitors
- Medical Instrumentation
- Consumer Toys
- Industrial/Commercial Lighting
- Industrial Process Control

Description

The TCS3404 and TCS3414 digital color light sensors are designed to accurately derive the color chromaticity and illuminance (intensity) of ambient light and provide a digital output with 16-bits of resolution. The devices include an 8 × 2 array of filtered photodiodes, analog-to-digital converters, and control functions on a single monolithic CMOS integrated circuit. Of the 16 photodiodes, 4 have red filters, 4 have green filters, 4 have blue filters, and 4 have no filter (clear). With the advanced patent pending in-package trim capability, device-to-device and system-to-system tolerance can be minimized allowing very precise repeatability to be attained.

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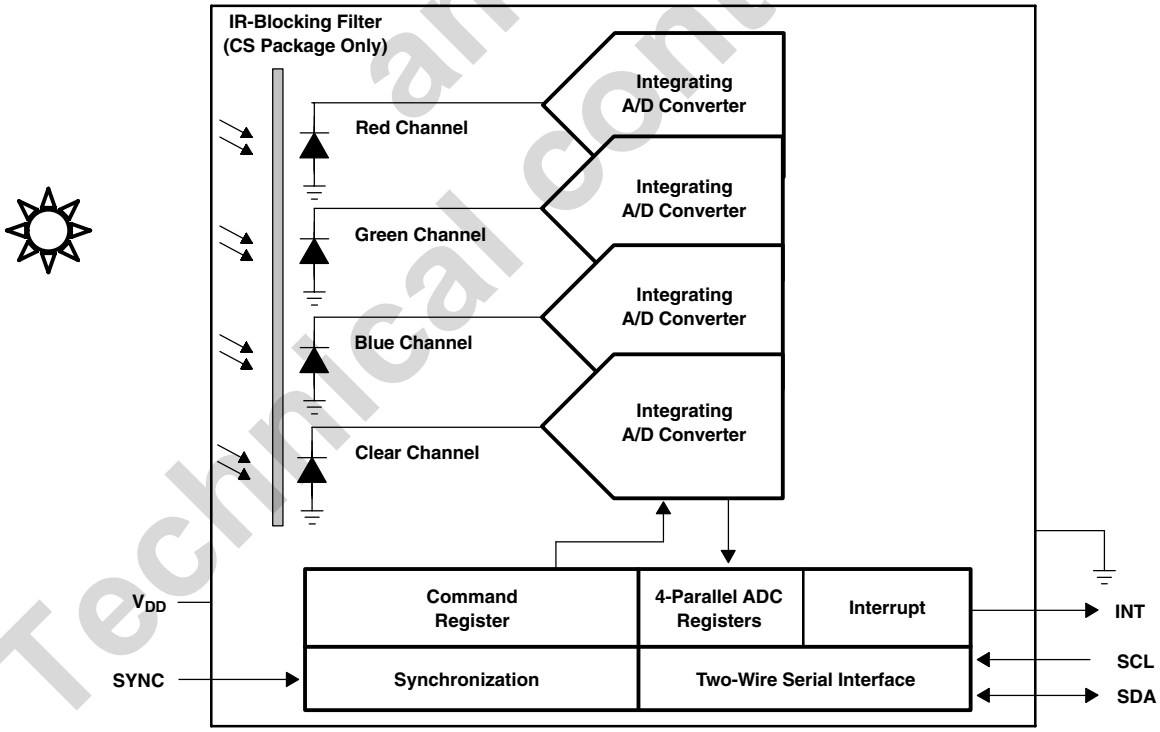
A synchronization input (SYNC) provides precise external control of sensor integration allowing the internal conversion cycles to be synchronized to a pulsed light source. Furthermore, the synchronization feature supports the following advanced modes of operation to maximize flexibility across a broad range of hardware systems: (1) sync for one internal-time cycle, and (2) accumulate for specified number of pulses. The device also supports free-running and serial-bus-controlled integration modes if precise coupling between the sensor and light source is not required.

Four parallel analog-to-digital converters (ADC) transform the photodiode currents to an SMBus (TCS3404) or I^2C (TCS3414) digital output that, in turn, can be input to a microprocessor. The RGB values can be read in a single read cycle to minimize the number of read command protocols defined in the communication interface. The slave address for this device is 39h (0111001b). A single SMB-Alert style interrupt (TCS3404) as well as a single traditional *level*-style interrupt (TCS3414) can be dynamically configured for any one of the four channels including a corresponding high/low threshold setting. The interrupt will remain asserted until the firmware clears the interrupt.

The TCS3404/14 devices can help (1) automatically adjust the display brightness of a backlight to extend battery, increase lamp life, and provide optimum viewing in diverse lighting conditions, (2) white-color balance display panel and/or captured images in diverse lighting conditions, and (3) manage RGB LED backlighting to maintain color consistency over a long period of time.

These devices are also ideal in controlling keyboard illumination in low ambient light conditions. Chromaticity coordinates (x,y) can be used to derive color temperature for the purpose of white-color balancing of displays and/or captured images. Illuminance, in lux, can be used to approximate the human eye response of ambient light and to manage exposure control in digital cameras. The TCS3404/14 devices are ideal in notebook/tablet PCs, LCD monitors, flat-panel televisions, cell phones, and digital cameras. Additional applications include street light control, security lighting, sunlight harvesting, and automotive instrumentation clusters.

Functional Block Diagram



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Terminal Functions

TERMINAL NAME	CS PKG NO.	FN PKG NO.	TYPE	DESCRIPTION
GND	A3	6		Power supply ground. All voltages are referenced to GND.
INT	B3	4	O	Level interrupt — open drain.
SCL	A1	1	I	Serial clock input terminal — clock signal for I^2C serial data.
SDA	B1	3	I/O	Serial data I/O terminal — serial data I/O for I^2C.
SYNC	A2	2	I	Synchronous input.
V_{DD}	B2	5		Supply voltage.

Available Options

DEVICE	INTERFACE	I^2C ADDRESS	PACKAGE – LEADS	PACKAGE DESIGNATOR	ORDERING NUMBER
TCS3404	SMBus	–	Chipscale–6	CS	TCS3404CS
TCS3404	SMBus	–	Dual Flat No-Lead–6	FN	TCS3404FN
TCS3413	I^2C	0x29	Chipscale–6	CS	TCS3413CS
TCS3413	I^2C	0x29	Dual Flat No-Lead–6	FN	TCS3413FN
TCS3414†	I^2C	0x39	Chipscale–6	CS	TCS3414CS
TCS3414†	I^2C	0x39	Dual Flat No-Lead–6	FN	TCS3414FN
TCS3415	I^2C	0x49	Chipscale–6	CS	TCS3415CS
TCS3415	I^2C	0x49	Dual Flat No-Lead–6	FN	TCS3415FN
TCS3416	I^2C	0x59	Chipscale–6	CS	TCS3416CS
TCS3416	I^2C	0x59	Dual Flat No-Lead–6	FN	TCS3416FN

† Recommended device for single-device systems..

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 3.8 V
Digital output voltage range, V_O . . . . . –0.5 V to 3.8 V
Digital output current, I_O . . . . . –1 mA to 20 mA
Storage temperature range, T_{stg} . . . . . –40°C to 85°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.7	3	3.6	V
Operating free-air temperature, T_A (CS PAckage)	–40		85	°C
Operating free-air temperature, T_A (FN PAckage)	–30		70	°C
SCL, SDA input low voltage, V_{IL}	–0.5		0.8	V
SCL, SDA input high voltage, V_{IH}	2.1		3.6	V

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Electrical Characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current @ V_{DD} = 3.6 V	Power on (ADC inactive)		7.7	10	mA
		Power on (ADC active)		8.7	11	mA
		Power down		700	1000	µA
V_{OL}	INT, SDA output low voltage	3 mA sink current	0		0.4	V
I_{LEAK}	Input leakage current (SDA, SCL, SYNC)	$V_{IH} = V_{DD}$, V_{IL} = GND	–5		5	µA

AC Electrical Characteristics, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER†		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SCL)}$	Clock frequency 400 kHz (I^2C)		0		400	kHz
	Clock frequency 100 kHz (SMBus)		10		100	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			µs
$t_{(SUSTO)}$	Stop condition setup time		0.6			µs
$t_{(HDDAT)}$	Data hold time		0		0.9	µs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			µs
$t_{(HIGH)}$	SCL clock high period		0.6			µs
$t_{(TIMEOUT)}$	Detect clock/data low timeout (SMBus only)		25		35	ms
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF
$t_{LOW\ (SYNC)}$	SYNC low period (see Figure 1)			50		µs
$t_{HIGH\ (SYNC)}$	SYNC high period (see Figure 1)			50		µs
$t_{F\ (SYNC)}$	SYNC fall time (see Figure 1)			50		ns
$t_{R\ (SYNC)}$	SYNC rise time (see Figure 1)			50		ns

† Specified by design and characterization; not production tested.

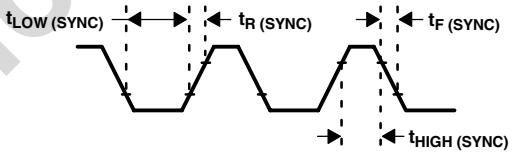


Figure 1. Timing Diagram for Sync

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Optical Characteristics, V_{DD} = 3 V, T_A = 25°C, GAIN = 64×, Tint = 12ms (unless otherwise noted) (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	Red Channel			Green Channel			Blue Channel			Clear Channel			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
R_e	Irradiance responsivity (CS package)	λ_p = 470 nm, See Note 3	0%		15%	15%		50%	65%		90%	59.0	65.6	72.5	(counts/ µW/ cm^2)
		λ_p = 524 nm, See Note 4	0%		15%	60%		90%	0%		35%	71.2	76.9	82.7	
		λ_p = 640 nm, See Note 5	80%		110%	0%		15%	0%		15%	80.6	90.1	99.5	
R_e	Irradiance responsivity (FN package)	λ_p = 470 nm, See Note 3	0%		15%	10%		50%	65%		90%	56.3	62.5	69.1	(counts/ µW/ cm^2)
		λ_p = 524 nm, See Note 4	0%		15%	60%		90%	0%		35%	72.5	78.4	84.3	
		λ_p = 640 nm, See Note 5	80%		110%	0%		15%	0%		15%	94.2	105.3	116.3	

NOTES: 1. The percentage shown represents the ratio of the respective red, green, or blue channel value to the clear channel value.
2. Optical measurements are made using small-angle incident radiation from a light-emitting diode (LED) optical source.
3. The 470 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: peak wavelength λ_p = 470 nm, spectral halfwidth $\Delta\lambda$½ = 35 nm, and luminous efficacy = 75 lm/W.
4. The 524 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: peak wavelength λ_p = 524 nm, spectral halfwidth $\Delta\lambda$½ = 47 nm, and luminous efficacy = 520 lm/W.
5. The 640 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: peak wavelength λ_p = 640 nm, spectral halfwidth $\Delta\lambda$½ = 17 nm, and luminous efficacy = 155 lm/W.
6. Illuminance responsivity R_v is calculated from the irradiance responsivity R_e by using the LED luminous efficacy values stated in notes 3, 4, and 5 and using 1 lx = 1 lm/m^2.

Operating Characteristics, V_{DD} = 3 V, T_A = 25°C, (unless otherwise noted) (see Notes 2, 3, and 4)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain scaling, relative to 1× gain setting	4×		3.8	4	4.2	
		16×		15.2	16	16.8	
		64×		60.8	64	67.2	
	Dark ADC count value		E_e = 0, 64× gain setting, T_{int} = 400 ms	0	3	15	counts
	Maximum digital count value		Prescale = 1, T_{int} = 400 ms (Note 1)			65535	counts
f_{osc}	Oscillator frequency			4.2	4.4	4.6	MHz
	Internal integration time tolerance			–5		5	%
	Temperature coefficient of responsivity (SYNC mode)		$\lambda \leq$ 700 nm, –40°C $\leq T_A \leq$ 85°C		± 200		ppm/°C

NOTES: 1. At shorter integration times and/or higher Prescale settings, the device will reach saturation of the analog section before the digital count reaches the maximum 16-bit value. The worst-case (lowest) analog saturation value can be obtained using the formula: Analog saturation = (fosc(min) ×Tint) ÷Prescale, where Fosc(min) is the minimum oscillator frequency in Hz, and tint is the actual integration time (internal, manually-timed, or sync-generated) in seconds.
2. Gain is controlled by the gain register (07h) described in the Register section.
3. Measurements taken when the Photodiode field value in the Photodiode Register (06h) is 00b and when the Prescaler field value in the Gain Register (07h) is 000b.
4. The full scale ADC count value is slew-rate limited for short integration times and is limited by the 16-bit counter for long integration times. The nominal transition between the two regions is t_{int} = 65535/5000 = 13.1 ms.

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PARAMETER MEASUREMENT INFORMATION

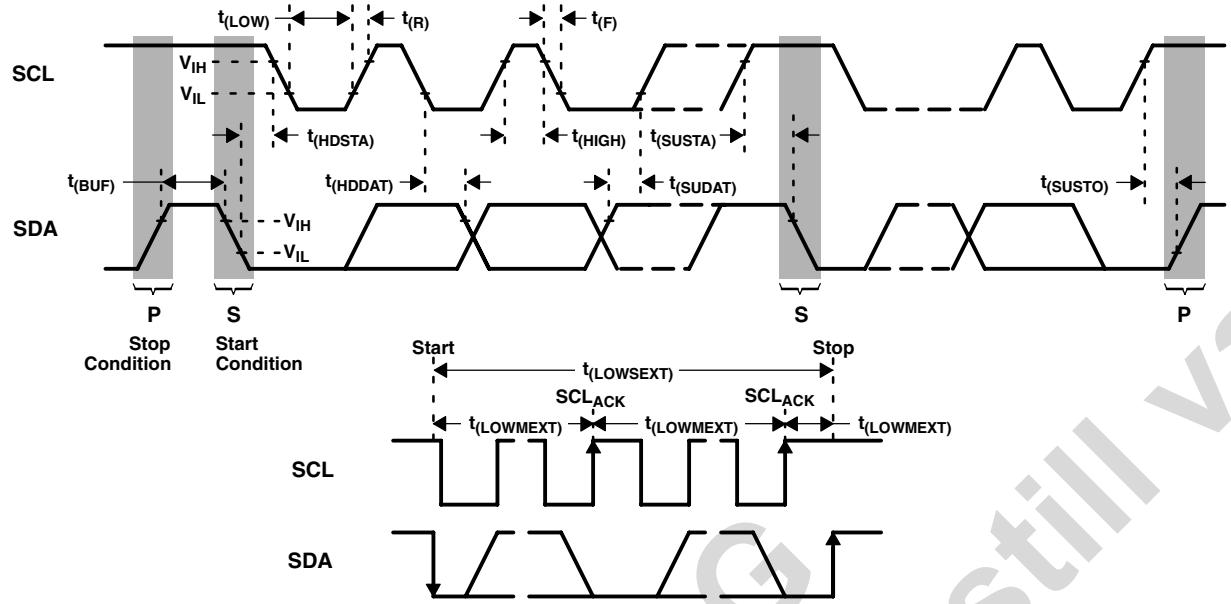


Figure 2. Timing Diagrams

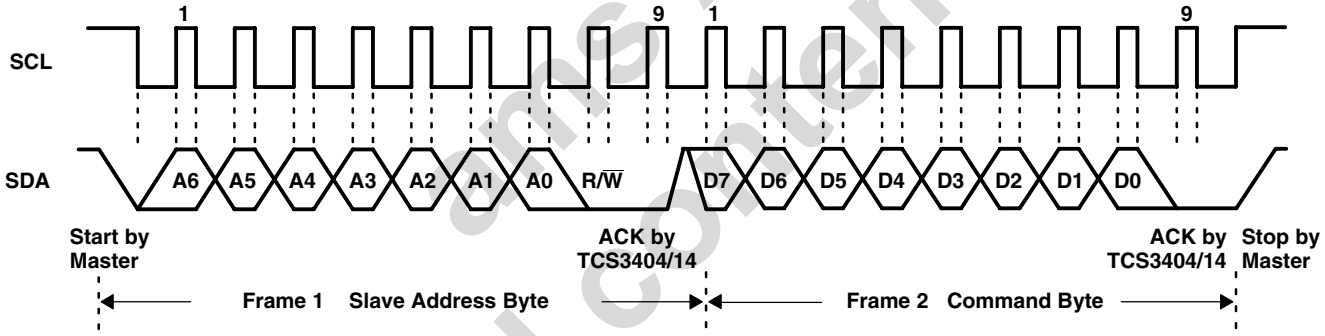


Figure 3. Example Timing Diagram for Send Byte Format

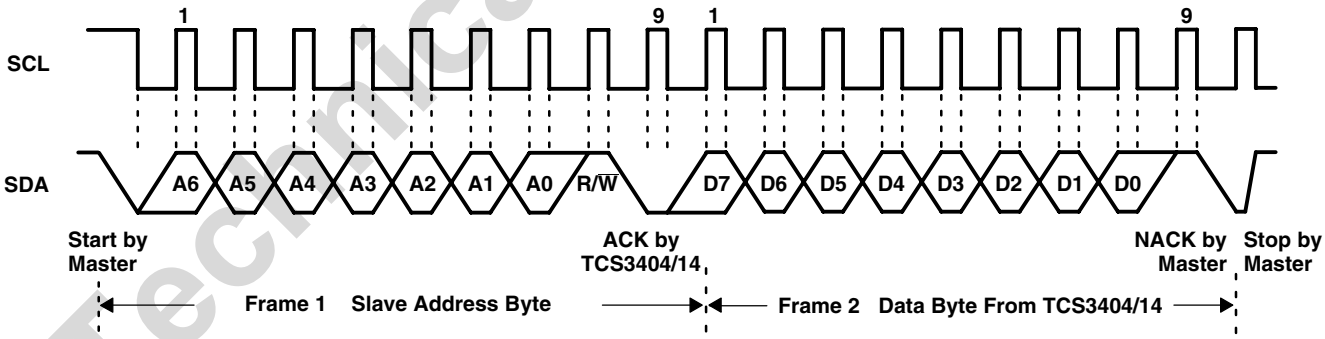


Figure 4. Example Timing Diagram for Receive Byte Format

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TYPICAL CHARACTERISTICS

SPECTRAL RESPONSIVITY CS PACKAGE

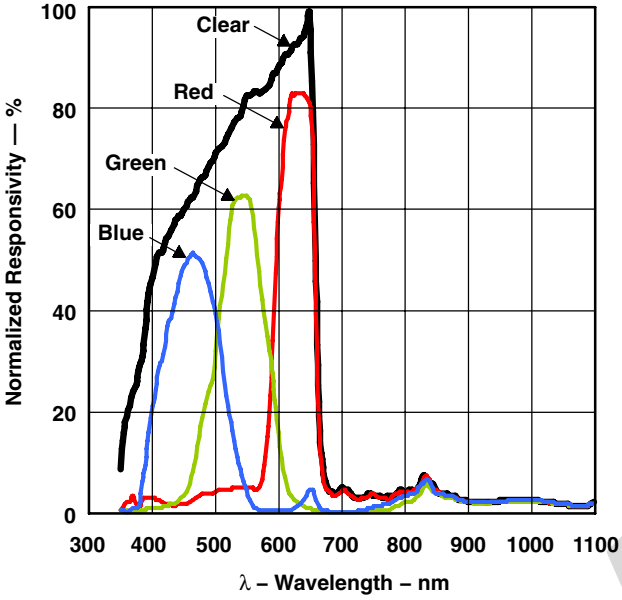


Figure 5

Note: Spectral responsivity is normalized at 655 nm.

SPECTRAL RESPONSIVITY FN PACKAGE

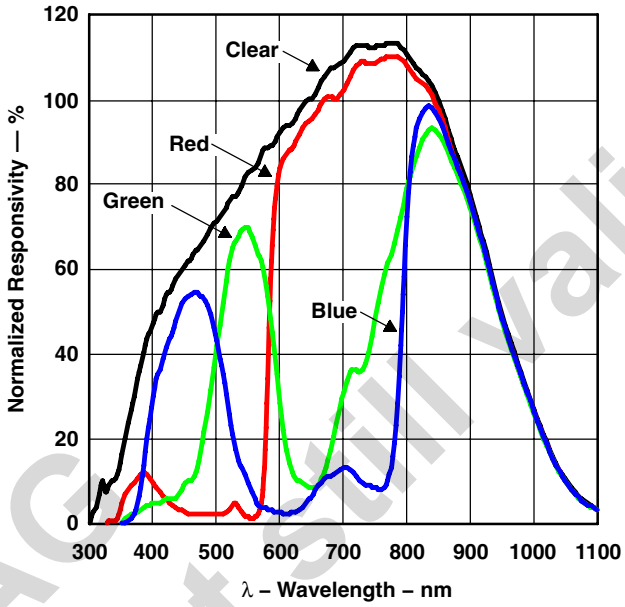


Figure 6

Note: Spectral responsivity is normalized at 850 nm.

I_{DD} OFF vs. FREE-AIR TEMPERATURE (Power Down)

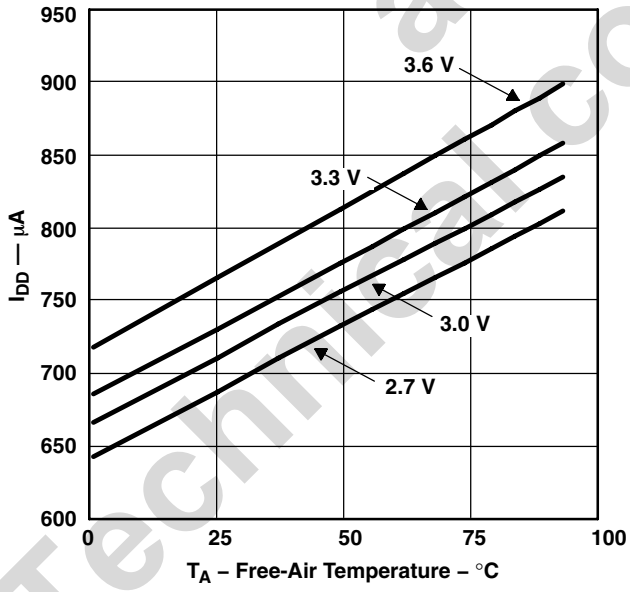


Figure 7

I_{DD} ON vs. FREE-AIR TEMPERATURE (Power On — ADC Inactive)

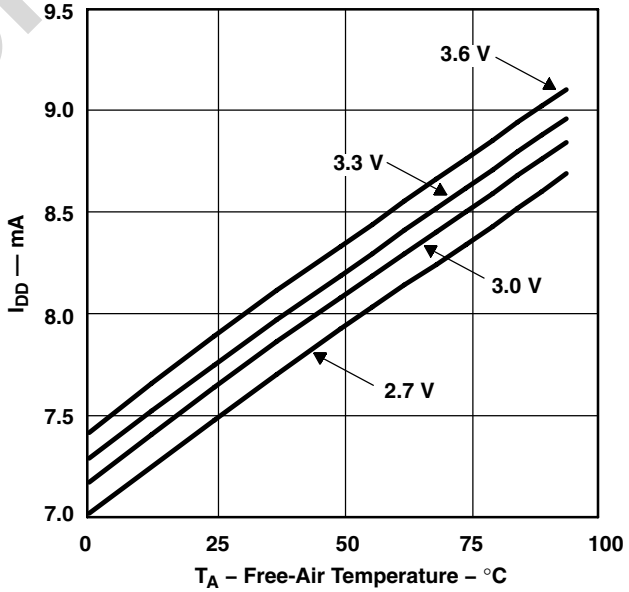


Figure 8

Note: When the device is powered on and the ADC is active, I_{DD} is approximately 1 mA higher.

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TYPICAL CHARACTERISTICS

NORMALIZED INTEGRATION TIME
vs.
FREE-AIR TEMPERATURE

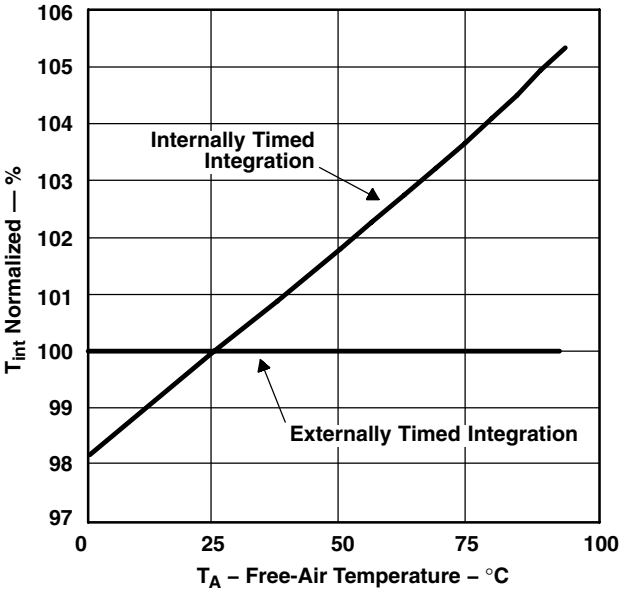


Figure 9

NORMALIZED RESPONSIVITY
vs.
ANGULAR DISPLACEMENT — FN PACKAGE

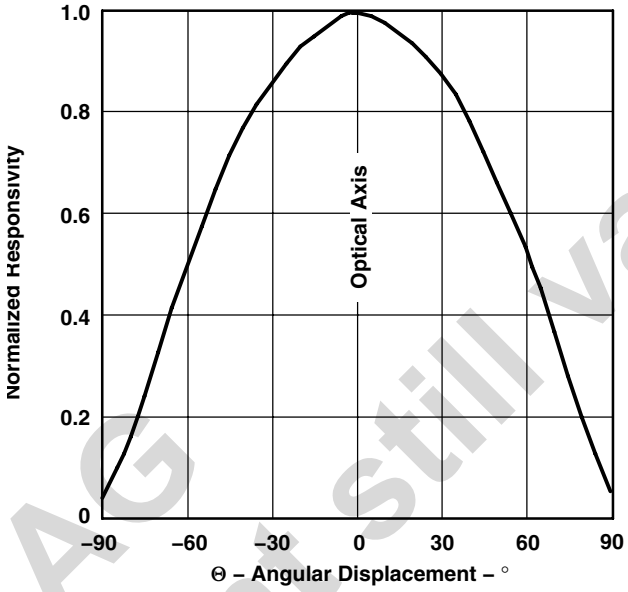


Figure 10

NORMALIZED RESPONSIVITY
vs.
ANGULAR DISPLACEMENT—CS PACKAGE

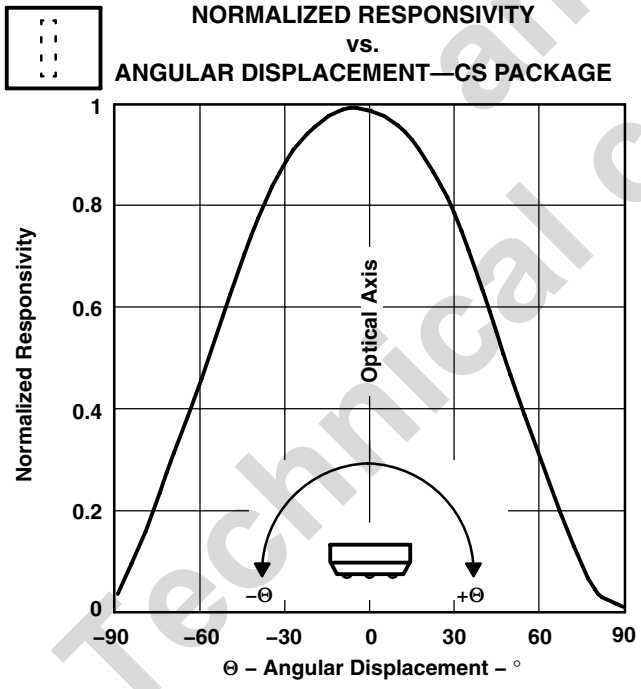


Figure 11

NORMALIZED RESPONSIVITY
vs.
ANGULAR DISPLACEMENT—CS PACKAGE

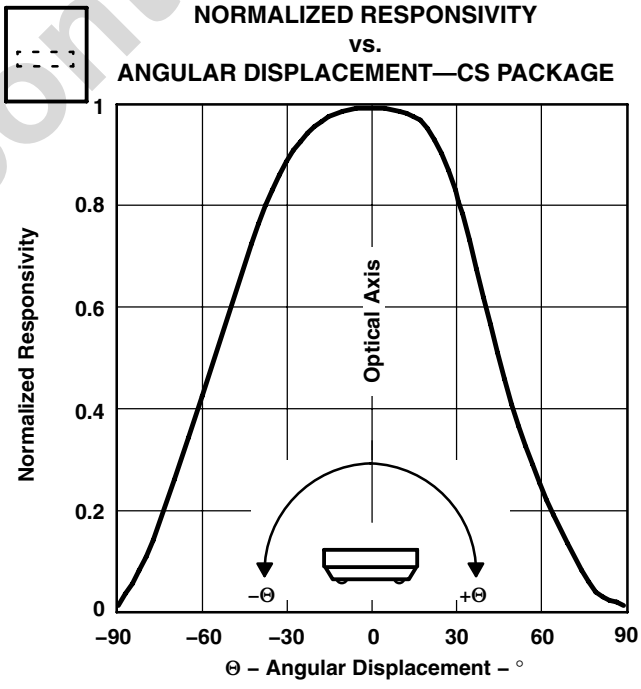


Figure 12

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PRINCIPLES OF OPERATION

Analog-to-Digital Converter

The TCS3404/14 contains four integrating analog-to-digital converters (ADC) that integrate the currents from the four photodiodes (channel 1 through channel 4). Integration of all four channels occurs simultaneously, and upon completion of the conversion cycle the conversion results are transferred to the channel data registers, respectively. The transfers are double-buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically begins the next integration cycle.

There are two ways to control the integration cycles: internally timed and externally timed. Internally-timed integration cycles can either be continuous back-to-back conversions or can be externally triggered as a single event using the SYNC pin. Externally-timed integrations can be controlled by setting and clearing a register bit (i.e. ADC_EN in Control Register) using the serial interface, or by 1 or more pulses input to the SYNC pin. Integration options are configured through the Timing Register (see the Timing Register section for more information).

Digital Interface

Interface and control of the TCS3404/14 is accomplished through a two-wire serial interface to a set of registers that provide access to device control functions and output data. The serial interface is compatible with System Management Bus (SMBus) versions 1.1 and 2.0, and I^2C bus Fast-Mode.

The TCS3404/14 device supports a single slave address outlined in Table 1. Additional devices shown in the Available Options table on page 3 support additional I^2C slave addresses for systems requiring more than one device.

Table 1. Slave Address

SLAVE ADDRESS	SMB ALERT ADDRESS
0111001	0001100

NOTE: The slave and SMB Alert addresses are 7 bits. Please note the SMBus and I^2C protocols on the following pages. A read/write bit should be appended to the slave address by the master device to communicate properly with the device.

Interrupt

Although the ADC channel data registers can be read at any time to obtain the most recent conversion value, in some applications, periodic polling of the device may not be desirable. For these types of applications, the device supports a variety of interrupt options allowing the user to configure the device to signal when a change in light intensity has occurred. High and low threshold registers allow a range of light levels to be defined, outside of which the device generates an interrupt. A persistence setting allows the user to specify a time duration that the measured value must remain outside of the defined range before generating an interrupt. The interrupt function can be assigned to any one of the four ADC color channels. See Interrupt Control Register for more information on configuring the interrupt functions.

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SMBus and I²C Protocols

Each *Send* and *Write* protocol is, essentially, a series of bytes. A byte sent to the TCS3404/14 with the most significant bit (MSB) equal to 1 will be interpreted as a COMMAND byte. The lower four bits of the COMMAND byte form the register select address (see Table 1), which is used to select the destination for the subsequent byte(s) received. The TCS3404/14 responds to any Receive Byte requests with the contents of the register specified by the stored register select address.

The TCS3404/14 implements the following protocols of the SMB 2.0 specification:

- Send Byte Protocol
- Receive Byte Protocol
- Write Byte Protocol
- Write Word Protocol
- Read Word Protocol
- Block Write Protocol
- Block Read Protocol

The TCS3404/14 implements the following protocols of the I²C specification:

- I²C Write Protocol
- I²C Read (Combined Format) Protocol

When an SMBus Block Write or Block Read is initiated (see description of COMMAND Register), the byte following the COMMAND byte is ignored but is a requirement of the SMBus specification. This field contains the byte count (i.e. the number of bytes to be transferred). The TCS3404 (SMBus) device ignores this field and extracts this information by counting the actual number of bytes transferred before the Stop condition is detected.

When an I²C Write or I²C Read (Combined Format) is initiated, the byte count is also ignored but follows the SMBus protocol specification. Data bytes continue to be transferred from the TCS3414 (I²C) device to Master until a NACK is sent by the Master.

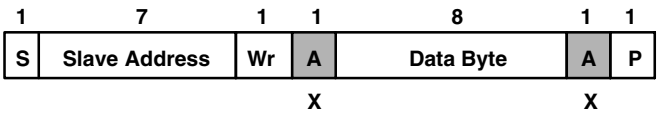
The data formats supported by the TCS3404 and TCS3414 devices are:

- Master transmitter transmits to slave receiver (SMBus and I²C):
  - The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte (SMBus only):
  - At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.
- Combined format (SMBus and I²C):
  - During a change of direction within a transfer, the master repeats both a START condition and the slave address but with the R/W bit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

For a complete description of SMBus protocols, please review the SMBus Specification at http://www.smbus.org/specs. For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c–bus.org/references/.

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A Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK)

P Stop Condition

Rd Read (bit value of 1)

S Start Condition

Sr Repeated Start Condition

Wr Write (bit value of 0)

X Shown under a field indicates that that field is required to have a value of X

... Continuation of protocol

Master-to-Slave

Slave-to-Master

Figure 13. SMBus and I²C Packet Protocol Element Key

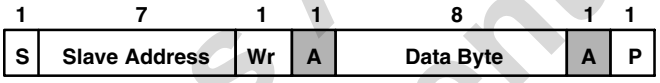


Figure 14. SMBus Send Byte Protocol

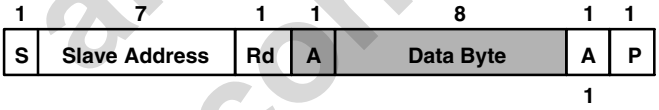


Figure 15. SMBus Receive Byte Protocol

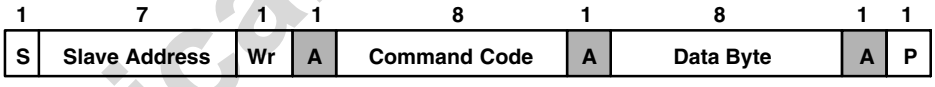


Figure 16. SMBus Write Byte Protocol

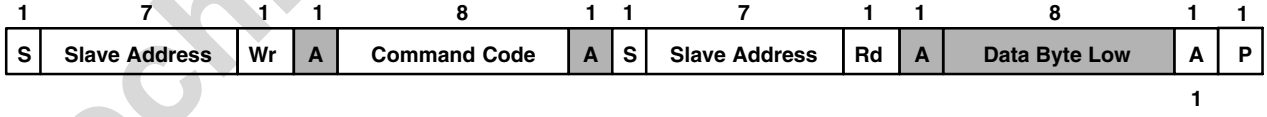


Figure 17. SMBus Read Byte Protocol

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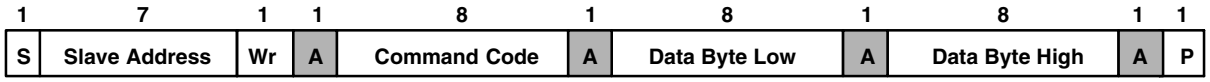


Figure 18. SMBus Write Word Protocol

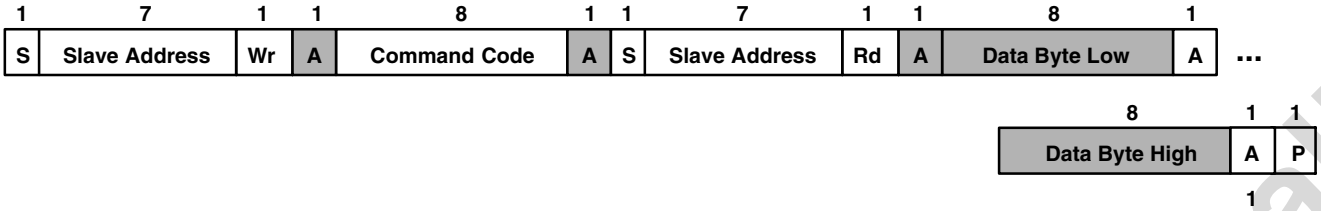


Figure 19. SMBus Read Word Protocol

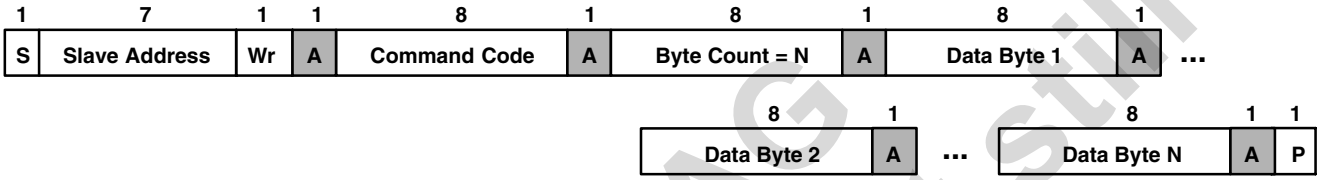


Figure 20. SMBus Block Write or I²C Write Protocols

NOTE: The I²C write protocol does not use the Byte Count packet, and the Master will continue sending Data Bytes until the Master initiates a Stop condition. See the Command Register on page 13 for additional information regarding the Block Read/Write protocol.

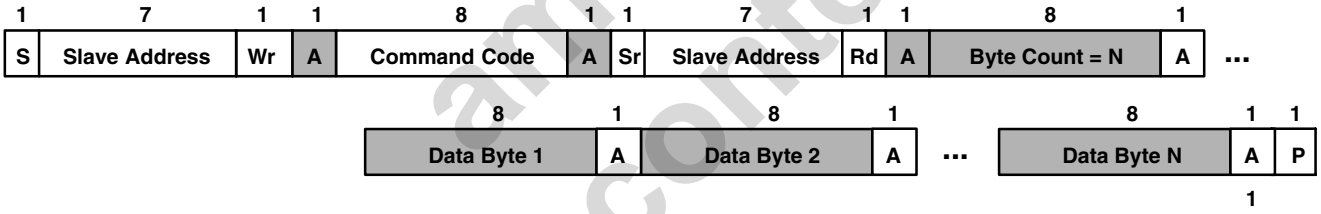


Figure 21. SMBus Block Read or I²C Read (Combined Format) Protocols

NOTE: The I²C read protocol does not use the Byte Count packet, and the Master will continue receiving Data Bytes until the Master initiates a Stop Condition. See the Command Register on page 13 for additional information regarding the Block Read/Write protocol.

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Register Set

The TCS3404/14 is controlled and monitored by 18 user registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Table 2.

Table 2. Register Set

ADDRESS	REGISTER NAME	REGISTER FUNCTION
––	COMMAND	Specifies register address
00h	CONTROL	Control of basic functions
01h	TIMING	Integration time/gain control
02h	INTERRUPT	Interrupt control
03h	INT SOURCE	Interrupt source
04h	ID	Part number/ Rev ID
07h	GAIN	ADC gain control
08h	LOW_THRESH_LOW_BYTE	Low byte of low interrupt threshold
09h	LOW_THRESH_HIGH_BYTE	High byte of low interrupt threshold
0Ah	HIGH_THRESH_LOW_BYTE	Low byte of high interrupt threshold
0Bh	HIGH_THRESH_HIGH_BYTE	High byte of high interrupt threshold
0Fh	––	SMBus block read (10h through 17h)
10h	DATA1LOW	Low byte of ADC green channel
11h	DATA1HIGH	High byte of ADC green channel
12h	DATA2LOW	Low byte of ADC red channel
13h	DATA2HIGH	High byte of ADC red channel
14h	DATA3LOW	Low byte of ADC blue channel
15h	DATA3HIGH	High byte of ADC blue channel
16h	DATA4LOW	Low byte of ADC clear channel
17h	DATA4HIGH	High byte of ADC clear channel

The mechanics of accessing a specific register depends on the specific SMB protocol used. Refer to the section on SMBus protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

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Command Register

The command register specifies the address of the target register for subsequent read and write operations. This register contains eight bits as described in Table 3 and defaults to 00h at power on.

Table 3. Command Register

	7	6	5	4	3	2	1	0	
	CMD	TRANSACTION		ADDRESS					COMMAND
Reset Value:	0	0	0	0	0	0	0	0	

FIELD	BITS	DESCRIPTION		
CMD	7	Select command register. Must write as 1.		
TRANSACTION	6:5	Transaction. Selects type of transaction to follow in subsequent data transfer.		
		FIELD VALUE	TRANSACTION	DESCRIPTION
		00	Byte protocol	SMB read/write byte protocol
		01	Word protocol	SMB read/write word protocol
		10	Block protocol	SMB read/write block protocol
		11	Interrupt clear	Clear any pending interrupt and is a write-once-to-clear field
ADDRESS	4:0	Register Address. This field selects the specific control or status register for following write and read commands according to Table 2.		

NOTES: 1. An I^2C block transaction will continue until the Master sends a stop condition. See Figure 18 and Figure 19. Unlike the I^2C protocol, the TCS3404/14 SMBus read/write protocol requires a Byte Count. All eight ADC Channel Data Registers (10h through 17h) can be read simultaneously in a single SMBus transaction. This is the only 64-bit data block supported by the TCS3404 SMBus protocol. The TRANSACTION field must be set to 10, and a read condition should be initiated with a COMMAND CODE of CFh. By using a COMMAND CODE of CFh during an SMBus Block Read Protocol, the TCS3404 device will automatically insert the appropriate Byte Count (Byte Count = 8) as illustrated in Figure 18. A write condition should not be used in conjunction with the 0Fh register.

2. Only the Send Byte Protocol should be used when clearing interrupts.

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Control Register (00h)

The CONTROL register contains two bits and is primarily used to power the TCS3404/14 device up and down as shown in Table 4.

Table 4. Control Register

	7	6	5	4	3	2	1	0	
00h	Resv	Resv	Resv	ADC_VALID	Resv	Resv	ADC_EN	POWER	CONTROL
Reset Value:	0	0	0	0	0	0	0	0	

FIELD	BIT	DESCRIPTION
Resv	7:6	Reserved. Write as 0.
Resv	5	Reserved. Write as 0.
ADC_VALID	4	ADC valid. This read-only field indicates that the ADC channel has completed an integration cycle.
Resv	3:2	Reserved. Write as 0.
ADC_EN	1	ADC enable. This field enables the four ADC channels to begin integration. Writing a 1 activates the ADC channels, and writing a 0 disables the ADCs.
POWER	0	Power on. Writing a 1 powers on the device, and writing a 0 turns it off.

NOTES: 1. Both ADC_EN and POWER must be asserted before the ADC channels will operate correctly.
2. INTEG_MODE and TIME/COUNTER fields in the Timing Register (01h) should be written before ADC_EN is asserted.
3. If a value of 03h is written, the value returned during a read cycle will be 03h. This feature can be used to verify that the device is communicating properly.
4. During writes and reads, the POWER bit is overridden and the oscillator is enabled, independent of the state of POWER.

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Timing Register (01h)

The TIMING register controls the synchronization and integration time of the ADC channels. The Timing Register settings apply to all four ADC channels. The Timing Register defaults to 00h at power on.

Table 5. Timing Register

	7	6	5	4	3	2	1	0	
01h	Resv	SYNC_EDGE	INTEG_MODE		PARAM				TIMING
Reset Value:	0	0	0	0	0	0	0	0	

FIELD	BITS	DESCRIPTION
Resv	7	Reserved. Write as 0.
SYNC_EDGE	6	Sync pin edge. If SYNC_EDGE is low, the falling edge of the sync pin is used to stop an integration cycle when INTEG_MODE is 11. If SYNC_EDGE is high, the rising edge of the sync pin is used to stop an integration cycle when INTEG_MODE is 11.
INTEG_MODE	5:4	Selects preset integration time, manual integration (via serial bus), or external synchronization (SYNC IN) modes.
		FIELD VALUE / **MODE**
		00 – In this mode, the integrator is free-running and one of the three internally-generated Nominal Integration Times is selected for each conversion (see Integration Time table below).
		01 – Manually start/stop integration through serial bus using ADC_EN field in Control Register.
		10 – Synchronize exactly one internally-timed integration cycle as specified in the NOMINAL INTEGRATION TIME beginning 2.4 µs after being initiated by the SYNC IN pin.
		11 – Integrate over specified number of pulses on SYNC IN pin (See SYNC IN PULSE COUNT table below). Minimum width of sync pulse is 50 µs. SYNC IN must be low at least 3.6 µs.
PARAM	3:0	Uses single, multipurpose bitmapped field to select one of three predefined integration times or set the number of SYNC IN pulses to count when the INTEG_MODE accumulate mode (11) is selected. ***NOTE:*** *INTEG_MODE and TIME/COUNTER fields should be written before ADC_EN is asserted.*
		FIELD VALUE / **NOMINAL INTEGRATION TIME**
		0000 – 12 ms
		0001 – 100 ms
		0010 – 400 ms
		FIELD VALUE / **SYNC IN PULSE COUNT**
		0000 – 1
		0001 – 2
		0010 – 4
		0011 – 8
		0100 – 16
		0101 – 32
		0110 – 64
		0111 – 128
		1000 – 256

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Interrupt Control Register (02h)

The INTERRUPT register controls the extensive interrupt capabilities of the device. The open-drain interrupt pin is active low and requires a pullup resistor to V_{DD} in order to pull high in the inactive state. Using the Interrupt Source Register (03h), the interrupt can be configured to trigger on any one of the four ADC channels. The TCS3404/14 permits both SMB-Alert style interrupts as well as traditional level style interrupts. The Interrupt Register provides control over when a *meaningful interrupt* will occur. The concept of a *meaningful* change can be defined by the user both in terms of light intensity and time, or persistence of that change in intensity. The value must cross the threshold (as configured in the Threshold Registers 08h through 0Bh) and persist for some period of time as outlined in the table below.

When a level Interrupt is selected, an interrupt is generated whenever the last conversion results in a value outside of the programmed threshold window. The interrupt is active-low and remains asserted until cleared by writing an 11 in the TRANSACTION field in the COMMAND register.

In SMB-Alert mode, the interrupt is similar to the traditional level style and the interrupt line is asserted low. To clear the interrupt, the host responds to the SMB-Alert by performing a modified Receive Byte operation, in which the Alert Response Address (ARA) is placed in the slave address field, and the TCS3404/14 that generated the interrupt responds by returning its own address in the seven most significant bits of the receive data byte. If more than one device connected on the bus has pulled the SMBAlert line low, the highest priority (lowest address) device will win control of the bus during the slave address transfer. If the device loses this arbitration, the interrupt will not be cleared. The Alert Response Address is 0Ch.

When INTR = 11, the interrupt is generated immediately following the SMBus write operation. Operation then behaves in an SMB-Alert mode, and the software set interrupt may be cleared by an SMB-Alert cycle.

Table 6. Interrupt Control Register

	7	6	5	4	3	2	1	0	
02h	Resv	INTR_STOP	INTR		Resv	PERSIST			INTERRUPT
Reset Value:	0	0	0	0	0	0	0	0	

FIELD	BITS	DESCRIPTION		
Resv	7	Reserved. Write as 0.		
INTR_STOP	6	Stop ADC integration on interrupt. When high, ADC integration will stop once an interrupt is asserted. To resume operation (1) de-assert ADC_EN using CONTROL register, (2) clear interrupt using COMMAND register, and (3) re-assert ADC_EN using CONTROL register. **Note**: *Use this bit to isolate a particular condition when the sensor is continuously integrating.*		
INTR	5:4	INTR Control Select. This field determines mode of interrupt logic according to the table below:		
		FIELD VALUE	**INTERRUPT CONTROL**	
		00	Interrupt output disabled.	
		01	Level Interrupt.	
		10	SMB-Alert compliant.	
		11	Sets an interrupt and functions as mode 10.	
		NOTE: *Value 11 may be used to test interrupt connectivity in a system or to assist in debugging interrupt service routine software. See Application Software section for further information.*		
Resv	3	Reserved. Write as 0.		
PERSIST	2:0	Interrupt persistence. Controls rate of interrupts to the host processor:		
		FIELD VALUE	**TIMER**	**DESCRIPTION**
		000	Every	Every ADC cycle generates interrupt
		001	Single	Any value outside of threshold range.
		010	0.1 sec	Consecutively out of range for 0.1 second
		011	1 sec	Consecutively out of range for 1 second

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Interrupt Source Register (03h)

The Interrupt Source register selects which ADC channel value to use to generate an interrupt. Only one of the four ADC channels can be selected.

Table 7. Interrupt Source Register

	7	6	5	4	3	2	1	0	
03h	Resv	Resv	Resv	Resv	Resv	Resv	INT SOURCE		INT SOURCE
Reset Value:	0	0	0	0	0	0	0	0	

FIELD	BITS	DESCRIPTION	
Resv	7:2	Reserved. Write as 0.	
INT SOURCE	1:0	Interrupt Source. Selects which ADC channel to use to generate an interrupt:	
		FIELD VALUE	INTERRUPT SOURCE
		00	Green channel
		01	Red channel
		10	Blue channel
		11	Clear channel

NOTE: The INTERRUPT THRESHOLD Register (08h–0Bh) should be configured appropriately to correspond to the ADC channel value that generates an interrupt.

ID Register (04h)

The ID register provides the value for both the part number and silicon revision number for that part number. It is a read-only register, whose value never changes.

Table 8. ID Register

	7	6	5	4	3	2	1	0	
04h	PARTNO				REVNO				ID
Reset Value:	–	–	–	–	–	–	–	–	

FIELD	BITS	DESCRIPTION
PARTNO	7:4	Part Number Identification: field value 0000 = TCS3404 field value 0001 = TCS3413, TCS3414, TCS3415, and TCS3416
REVNO	3:0	Revision number identification

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Gain Register (07h)

The Gain register provides a common gain control adjustment for all four parallel ADC output channels. Two gain bits [5:4] in the Gain Register allow the relative gain to be adjusted from 1× to 64× in 4× increments. The advantage of the gain adjust is to extend the dynamic range of the light input up to a factor of 64× before analog or digital saturation occurs. If analog saturation has occurred, lowering the gain sensitivity will likely prevent analog saturation especially when the integration time is relatively short. For longer integration times, the 16-bit output could be in digital saturation (64K). If lowering the gain to 1× does not prevent digital saturation from occurring, the use of PRESCALER can be useful.

The PRESCALER is 3 bits [2:0] in the gain register that divides down the output count (i.e. shifts the LSB of the count value to the right). The PRESCALER adjustment range is divide by 1 to 64 in multiples of 2.

The most sensitive gain setting of the device would be when GAIN is set to 11b (64×), and PRESCALER is set to 000b (divide by 1). The least sensitive part setting would be GAIN 00 (1×) and PRESCALER 110 (divide by 64). If the part continues to be in digital saturation at the least sensitive setting, the integration time can be lowered (see Timing Register section).

Table 9. Gain Register

	7	6	5	4	3	2	1	0	
07h	Resv	Resv	GAIN		Resv	PRESCALER			GAIN
Reset Value:	0	0	0	0	0	0	0	0	

FIELD	BITS	DESCRIPTION	
Resv	7:6	Reserved. Write as 0.	
GAIN	5:4	Analog Gain Control. This field switches the common analog gain of the four ADC channels. Four gain modes are provided:	
		FIELD VALUE	GAIN
		00	1×
		01	4×
		10	16×
		11	64×
Resv	3	Reserved. Write as 0.	
PRESCALER	2:0	Prescaler. This field controls a 6-bit digital prescaler and divider. The prescaler reduces the sensitivity of each ADC integrator as shown in the table below:	
		FIELD VALUE	PRESCALER MODE
		000	Divide by 1.
		001	Divide by 2.
		010	Divide by 4.
		011	Divide by 8.
		100	Divide by 16.
		101	Divide by 32.
		110	Divide by 64.
		111	Not used.

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Interrupt Threshold Register (08h – 0Bh)

The interrupt threshold registers store the values to be used as the high and low trigger points for the comparison function for interrupt generation. The high and low bytes from each set of registers are combined to form a 16-bit threshold value. If the value generated by the Interrupt Source Register (03h) converges below or equal to the low threshold specified, an interrupt is asserted on the interrupt pin. If the value generated by Interrupt Source Register (03h) converges above the high threshold specified, an interrupt is asserted on the interrupt pin. Registers LOW_THRESH_LOW_BYTE and LOW_THRESH_HIGH_BYTE provide the low byte and high byte, respectively, of the lower interrupt threshold. Registers HIGH_THRESH_LOW_BYTE and HIGH_THRESH_HIGH_BYTE provide the low and high bytes, respectively, of the upper interrupt threshold. The interrupt threshold registers default to 00h on power up.

Table 10. Interrupt Threshold Register

REGISTER	ADDRESS	BITS	DESCRIPTION
LOW_THRESH_LOW_BYTE	08h	7:0	ADC interrupt source lower byte of the low threshold.
LOW_THRESH_HIGH_BYTE	09h	7:0	ADC interrupt source upper byte of the low threshold.
HIGH_THRESH_LOW_BYTE	0Ah	7:0	ADC interrupt source lower byte of the high threshold.
HIGH_THRESH_HIGH_BYTE	0Bh	7:0	ADC interrupt source upper byte of the high threshold.

NOTES: 1. The Interrupt Source Register (03h) selects which ADC channel to generate an interrupt and should correspond to the threshold setting. Both registers should be configured appropriately when setting up an interrupt service routine.
2. Since two 8-bit values are combined for a single 16-bit value for each of the high and low interrupt thresholds, the SMBus Send Byte protocol should not be used to write to these registers. Any values transferred by the Send Byte protocol with the MSB set would be interpreted as the COMMAND field and stored as an address for subsequent read/write operations and not as the interrupt threshold information as desired. The Write Word protocol should be used to write byte-paired registers. For example, the LOW_THRESH_LOW_BYTE and LOW_THRESH_HIGH_BYTE registers (as well as the HIGH_THRESH_LOW_BYTE and HIGH_THRESH_HIGH_BYTE registers) can be written together to set the 16-bit ADC value in a single transaction.

ADC Channel Data Registers (10h – 17h)

The ADC channel data are expressed as 16-bit values spread across four registers. The channel low and high provide the lower and upper bytes respectively for each ADC channel data registers. Each DATALOW and DATAHIGH register is identified below as 1, 2, 3, or 4. All channel data registers are read-only and default to 00h on power up.

Table 11. ADC Channel Data Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
GREEN_LOW	10h	7:0	ADC channel 1 lower byte
GREEN_HIGH	11h	7:0	ADC channel 1 upper byte
RED_LOW	12h	7:0	ADC channel 2 lower byte
RED_HIGH	13h	7:0	ADC channel 2 upper byte
BLUE_LOW	14h	7:0	ADC channel 3 lower byte
BLUE_HIGH	15h	7:0	ADC channel 3 upper byte
CLEAR_LOW	16h	7:0	ADC channel 4 lower byte
CLEAR_HIGH	17h	7:0	ADC channel 4 upper byte

The upper byte data registers can only be read following a read to the corresponding lower byte register. When the lower byte register is read the upper eight bits are strobed into a shadow register, which is read by a subsequent read to the upper byte. The upper register will therefore read the correct value even if additional ADC integration cycles complete between the reading of the lower and upper registers.

NOTE: The SMBus Read Word protocol can be used to read byte-paired registers. For example, the DATA1LOW and DATA1HIGH registers (as well as the other three individual register pairs) may be read together to obtain the 16-bit ADC value in a single transaction.

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APPLICATION INFORMATION: SOFTWARE

Basic Operation

After applying V_{DD}, the device will initially be in the power–down state. To operate the device, issue a command to access the control register followed by the data value 03h to the control register to set ADC_EN and POWER to power up the device. At this point, all four ADC channels will begin a conversion at the default integration time of 12 ms. After 12 ms, the conversion results will be available in ADC Channel Data Registers (10h through 17h). The following pseudo code illustrates a procedure for reading the TCS3404/14 device using Word and Byte transactions:

```
// Read ADC Channels Using Read Word Protocol - RECOMMENDED
      Address = 0x39
      Command = 0x80
      PowerUp = 0x03                              //Power Up and Enable ADC
      //Wait for integration conversion

      //Address the Ch1 lower data register and configure for Read Word
      Command = 0xB0                              //Set Command bit and Word transaction

      //Reads two bytes from sequential registers 10h and 11h
      //Results are returned in DataLow and DataHigh variables
      ReadWord (Address, Command, DataLow, DataHigh)
      Channel1 = 256 * DataHigh + DataLow

      //Address the Ch2 lower data register and configure for Read Word
      Command = 0xB2                              //Set Command bit and Word transaction

      //Reads two bytes from sequential registers 12h and 13h
      //Results are returned in DataLow and DataHigh variables
      ReadWord (Address, Command, DataLow, DataHigh)
      Channel2 = 256 * DataHigh + DataLow //Shift DataHigh to upper byte

      //Address the Ch3 lower data register and configure for Read Word
      Command = 0xB4                              //Set Command bit and Word transaction

      //Reads two bytes from sequential registers 14h and 15h
      //Results are returned in DataLow and DataHigh variables
      ReadWord (Address, Command, DataLow, DataHigh)
      Channel3 = 256 * DataHigh + DataLow

      //Address the Ch4 lower data register and configure for Read Word
      Command = 0xB8                              //Set Command bit and Word transaction

      //Reads two bytes from sequential registers 16h and 17h
      //Results are returned in DataLow and DataHigh variables
      ReadWord (Address, Command, DataLow, DataHigh)
      Channel4 = 256 * DataHigh + DataLow //Shift DataHigh to upper byte
```

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```
// Read ADC Channels Using Read Byte Protocol
      Address = 0x39                          //Slave addr – also 0x29 or 0x49
      Command = 0x90                          //Address the Ch1 lower data register
      ReadByte (Address, Command, DataLow)    //Result returned in DataLow
      Command = 0x91                          //Address the Ch1 upper data register
      ReadByte (Address, Command, DataHigh)   //Result returned in DataHigh
      Channel1 = 256 * DataHigh + DataLow     //Shift DataHigh to upper byte
      Command = 0x92                          //Address the Ch2 lower data register
      ReadByte (Address, Command, DataLow)    //Result returned in DataLow
      Command = 0x93                          //Address the Ch2 upper data register
      ReadByte (Address, Command, DataHigh)   //Result returned in DataHigh
      Channel2 = 256 * DataHigh + DataLow     //Shift DataHigh to upper byte
      Command = 0x94                          //Address the Ch3 lower data register
      ReadByte (Address, Command, DataLow)    //Result returned in DataLow
      Command = 0x95                          //Address the Ch3 upper data register
      ReadByte (Address, Command, DataHigh)   //Result returned in DataHigh
      Channel3 = 256 * DataHigh + DataLow     //Shift DataHigh to upper byte
      Command = 0x96                          //Address the Ch4 lower data register
      ReadByte (Address, Command, DataLow)    //Result returned in DataLow
      Command = 0x97                          //Address the Ch4 upper data register
      ReadByte (Address, Command, DataHigh)   //Result returned in DataHigh
      Channel4 = 256 * DataHigh + DataLow     //Shift DataHigh to upper byte
```

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APPLICATION INFORMATION: SOFTWARE

Configuring the Timing Register

The command, timing, and control registers are initialized to default values on power up. Setting these registers to the desired values would be part of a normal initialization or setup procedure. In addition, to maximize the performance of the device under various conditions, the integration time and gain may be changed often during operation. The following pseudo code illustrates a procedure for setting up the timing register for various options.

```
// Set up Timing Register
       //Low Gain (1x), integration time of 12ms (default value)
       Address = 0x39
       Command = 0x81                              //Timing Register
       Data = 0x02
       WriteByte(Address, Command, Data)

       //Low Gain (1x), integration time of 101ms
       Command = 0x81                              //Timing Register
       Data = 0x01
       WriteByte(Address, Command, Data)

       //Low Gain (1x), integration time of 12ms
       Data = 0x00
       WriteByte(Address, Command, Data)

       //High Gain (16x), integration time of 101ms
       Command = 0x81                              //Timing Register
       Data = 0x01
       WriteByte(Address, Command, Data)
       Command = 0x87                              //Gain Control Register
       Data = 0x20
       WriteByte(Address, Command, Data)

//Read data registers (see Basic Operation example)

//Perform Manual Integration of 50 us
       //Set up for manual integration
       Command = 0x80
       Data = 0x01                                 //Disable ADC_EN
       WriteByte(Address, Command, Data)

       Command = 0x81
       Data = 0x10                                 //Set manual integration
       WriteByte(Address, Command, Data)

       Command = 0x80
       Data = 0x03                                 //Enable ADC_EN and begin integration
       WriteByte(Address, Command, Data)

       //Integrate for 50ms
       Sleep (50)                                  //Wait for 50ms

       //Stop integrating
       Command 0x80
       Data = 0x01                                 //Disable ADC_EN and stop integration
       WriteByte(Address, Command, Data)

//Read data registers (see Basic Operation example)
```

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APPLICATION INFORMATION: SOFTWARE

Synchronization

There are two basic modes of operation for controlling synchronization: (1) internally timed, and (2) externally timed. Internally-timed integration cycles can either be continuous back-to-back conversions or can be externally triggered as a single event using the SYNC pin. Externally-timed integrations can be controlled by setting and clearing the ADC Enable in the Control Register using the serial interface, or by one or more pulses input to the SYNC pin. Internally-timed integration cycle times are dependent on the PARAM field value and the internal clock frequency. Nominal integration times and respective scaling between integration times scale proportionally as shown in the PARAM field in Table 5. See Operating Characteristics Table notes for detailed information regarding how the scale values were obtained.

If a particular integration time period is required that is not listed in the PARAM Integration Time field value, then the manual timing control feature can be used to manually start and stop the integration time period by setting INTEG_MODE=01b. Manual integration is performed as follows:

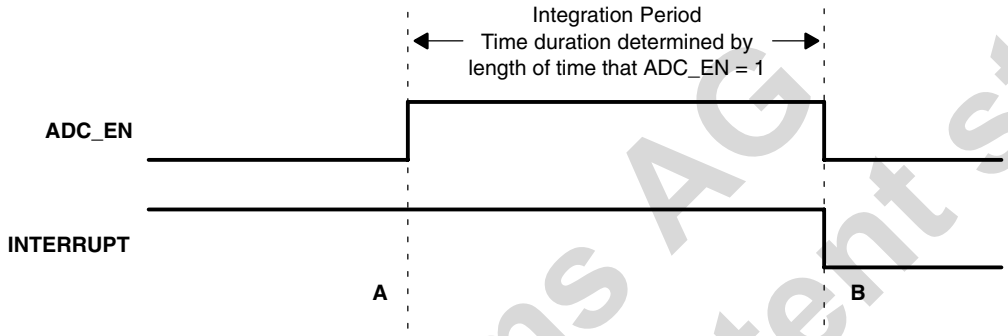


Figure 22. Manual Integration (INTEG_MODE 01b)

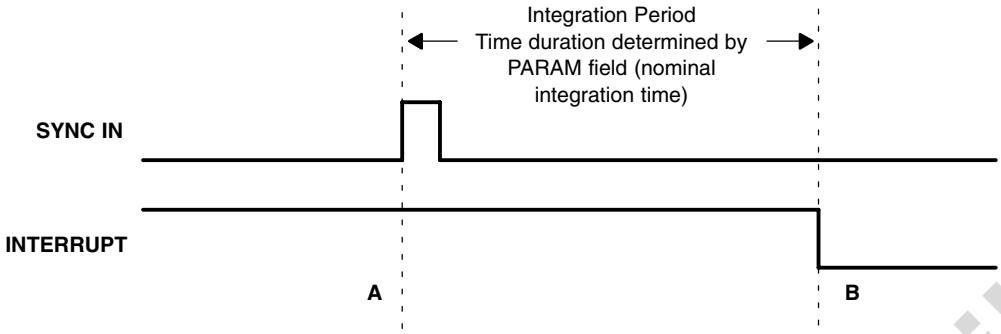
1. Disable ADC_EN (= 0) before initiating a manual integration cycle
2. Clear and enable INTR before each cycle
3. Write 01b to INTEG_MODE field
4. Set ADC_EN (= 1) to start integration
5. Clear ADC_EN (= 0) to stop integration
6. Read channel data

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When the INTEG_MODE field value is set to 10b, an externally-controlled synchronization input (SYNC) is used to trigger the start of an integration period. The integration period starts on the rising edge of the SYNC pulse, triggers a single, internally-timed integration cycle, and continues until the Nominal Integration Time, as defined in the PARAM field, is completed.



NOTE: ADC_EN must be toggled (i.e. from high to low and back to high again) before next integration cycle

Figure 23. One-Shot Integration (INTEG_MODE 10b) Falling Edge

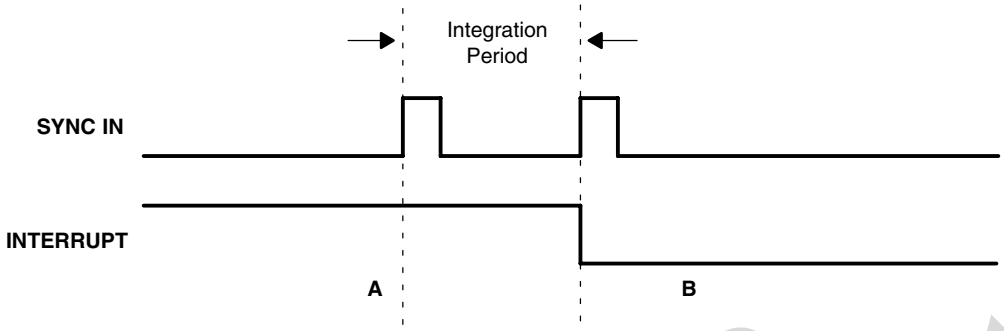
1. Enable ADC_EN (= 1)
2. Set PARAM for desired integration cycle (12ms, 100ms, or 400ms)
3. Set INTEG_MODE to 10b
4. Disable SYNC and clear INTR
5. Read channel data

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When the INTEG_MODE field value is set to 11b, the device integrates from the rising edge of the first pulse until the rising or falling edge of a subsequent pulse as specified by the SYNC_EDGE and PARAM field values. See example timing diagrams below. ADC_EN must be toggled (i.e. from high to low and back to high again) before the next integration cycle. With this device feature, the SYNC IN input pin can be used to synchronize the device with an external light source (e.g. LED).



NOTES: 1. Rising edge of second SYNC IN pulse required to terminate integration cycle
2. ADC_EN must be toggled (i.e. from high to low and back to high again) before next integration cycle

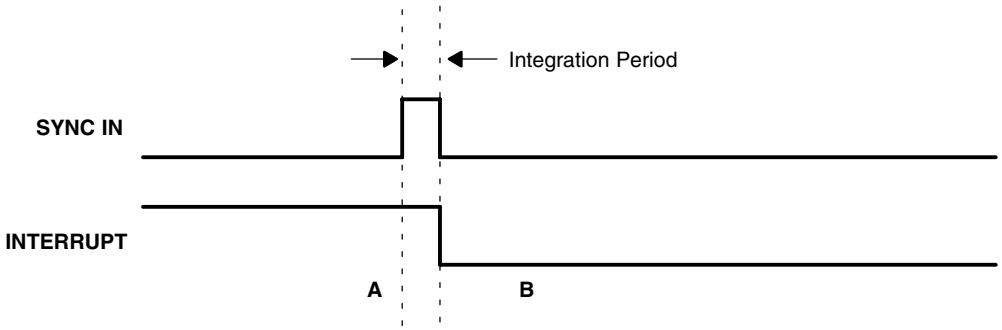
Figure 24. Integrate Over One Pulse (SYNC_EDGE 1b, INTEG_MODE 11b, PARAM 0b) Rising Edge

1. Enable ADC_EN (= 1)
2. Set SYNC EDGE to 1
3. Set PARAM for SYNC PULSE COUNT of 1
4. Set INTEG_MODE to 11b
5. Input two external SYNC pulses
6. Disable SYNC and read channels

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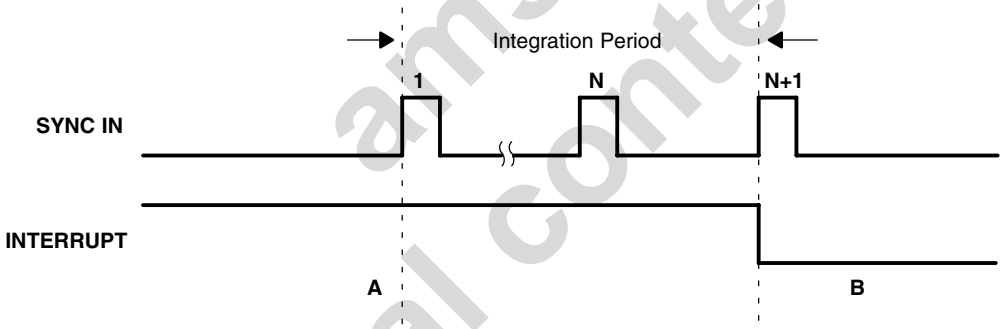
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NOTE: ADC_EN must be toggled (i.e. from high to low and back to high again) before next integration cycle

Figure 25. Integrate Over One Pulse (SYNC_EDGE 0b, INTEG_MODE 11b, PARAM 0b) Falling Edge

1. Enable ADC_EN (= 1)
2. Set SYNC EDGE to 0
3. Set PARAM for SYNC PULSE COUNT of 1
4. Set INTEG_MODE to 11b
5. Input external SYNC pulse
6. Disable SYNC and read channels



NOTES: 1. Rising edge of third SYNC IN pulse required to terminate integration cycle
2. ADC_EN must be toggled (i.e. from high to low and back to high again) before next integration cycle

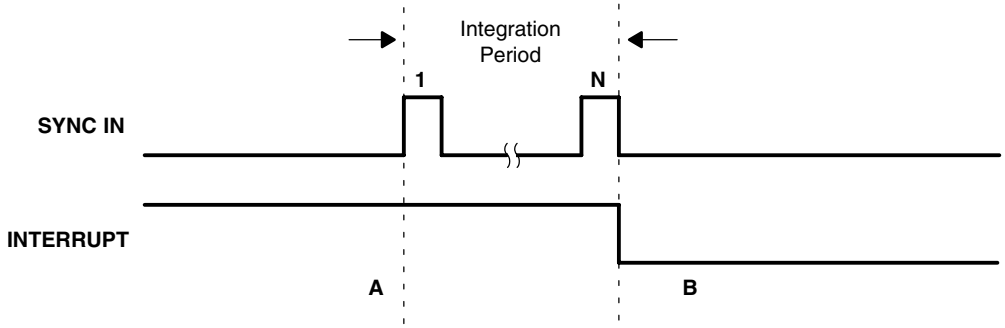
Figure 26. Integrate Over Two Pulses (SYNC_EDGE 1b, INTEG_MODE 11b, PARAM Xb) Rising Edge

1. Enable ADC_EN (= 1)
2. Set SYNC EDGE to 1
3. Set PARAM for desired SYNC PULSE COUNT
4. Set INTEG_MODE to 11b
5. Input N+1 external SYNC pulses
6. Disable SYNC and read channels

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NOTE: ADC_EN must be toggled (i.e. from high to low and back to high again) before next integration cycle

Figure 27. Integrate Over Two Pulses (SYNC_EDGE 0b, INTEG_MODE 11b, PARAM Xb) Falling Edge

1. Enable ADC_EN (= 1)
2. Set SYNC EDGE to 0
3. Set PARAM for desired SYNC PULSE COUNT
4. Set INTEG_MODE to 11b
5. Input N external SYNC pulse(s)
6. Disable SYNC and read channels

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A synchronization input (SYNC IN) is supported to precisely start/stop sensor integration and synchronize with the light source. The TIMING Register (01h) provides two synchronization modes of operation. The first mode of operation synchronizes the SYNC IN pin for one integration cycle as specified in the Timing Register (01h). When the rising edge of the signal is detected, the TCS3404/14 begins integration. The second mode accumulates a specified number of SYNC IN pulses (see Timing Register) in which the minimum pulse width is 50 μs. A pulse counter is used to count the rising and falling edges of the pulse(s) and precisely integrate the light level when the SYNC IN pulse is high.

The following pseudo code illustrates a procedure for reading the TCS3404/14 device using the synchronization feature:

```
// Synchronize one integration cycle
       // See "Basic Operation" to power-on and start device
       // See "Configuring the Timing Register" to setup environment

       Address = 0x39                          //Slave addr - also 0x29 or 0x49
       Command = 0x81                          //Set Command bit and address Timing Register
       Data = 0x21                             //Sync one 100ms integration period

       //External SYNC IN pulse initiates 100ms integration
       Sleep (100)

       // See "Basic Operation" to read Data Registers using Byte or Word Protocol


// Synchronize N number of SYNC IN pulses
       // See "Basic Operation" to power-on and start device
       // See "Configuring the Timing Register" to setup environment

       Address = 0x39                          //Slave addr - also 0x29 or 0x49
       Command = 0x81                          //Set Command bit and address Timing Register
       Data = 0x30                             //Integrate one SYNC IN pulse

       //External SYNC IN pulse synchronizes integration
       // See "Basic Operation" to read Data Registers using Byte or Word Protocol
```

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APPLICATION INFORMATION: SOFTWARE

Interrupts

The interrupt feature of the TCS3404/14 device simplifies and improves system efficiency by eliminating the need to poll the sensor for a light intensity value. Interrupt mode is determined by the INTR field in the Interrupt Control Register. The interrupt feature may be disabled by writing a field value of 00h to the Interrupt Control Register (02h) so that polling can be performed.

The versatility of the interrupt feature provides many options for interrupt configuration and usage. The primary purpose of the interrupt function is to signal a meaningful change in light intensity. However, it also be used as an end-of-conversion signal. The concept of a meaningful change can be defined by the user both in terms of light intensity and time, or persistence, of that change in intensity. The TCS3404/14 device implements two 16-bit-wide interrupt threshold registers that allow the user to define thresholds above and below a desired light level. An interrupt will then be generated when the value of a conversion exceeds either of these limits. For simplicity of programming, the threshold comparison uses the Interrupt Source Register (03h) to select which ADC channel (1 through 4) to generate the interrupt. This simplifies calculation of thresholds that are based on a percent of the current light level. For example, it is adequate to use only one channel (e.g. green channel) when calculating light intensity differences since, for a given light source, channel values are linearly proportional to each other and thus each value scales linearly with light intensity.

To further control when an interrupt occurs, the TCS3404/14 device provides an interrupt persistence feature. This feature allows the user to specify the length in time of the number of consecutive ADC channel values for which a light intensity exceeding either interrupt threshold must persist before actually generating an interrupt. This can be used to prevent transient changes in light intensity from generating an unwanted interrupt. See Table 6 regarding the number of timer values provided.

Two different interrupt styles are available: Level and SMBus Alert. The difference between these two interrupt styles is how they are cleared. Both result in the interrupt line going active low and remaining low until the interrupt is cleared. A level style interrupt is cleared by setting the Interrupt Clear field in the the COMMAND register to 11b. The SMBus Alert style interrupt is cleared by an Alert Response as described in the Interrupt Control Register section and SMBus specification.

To configure the interrupt as an end–of–conversion signal so that every ADC integration cycle generates an interrupt, the interrupt PERSIST field in the Interrupt Control Register (02h) is set to 000b. Either Level or SMBus Alert style can be used. An interrupt will be generated upon completion of each conversion. The interrupt threshold registers are ignored. The following example illustrates the configuration of a level interrupt:

```
// Set up end-of-conversion interrupt, Level style
Address = 0x39                    //Slave address - alternatively 0x29 or 0x49
Command = 0x83                    //Interrupt Source Register
Data = 0x01                       //Select Channel 2
WriteByte(Address, Command, Data)

Command = 0x82                    //Address Interrupt Register
Data = 0x10                       //Level style, every ADC cycle
WriteByte(Address, Command, Data)
```

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The following example pseudo code illustrates the configuration of an SMB-Alert style interrupt when the light intensity changes 20% from the current value, and persists for 2.5 seconds:

```
//Assume Interrupt Source as Channel 1
//Read current light level
Address = 0x39                          //Slave address – alternatively 0x29 or 0x49
Command = 0xB0                          //Set Command bit and SMBus Word read
ReadWord (Address, Command, DataLow, DataHigh)
Channel1 = (256 * DataHigh) + DataLow
//Calculate upper and lower thresholds
T_Upper = Channel1 + (0.2 * Channel1)
T_Lower = Channel1 – (0.2 * Channel1)
//Write the lower threshold register
Command = 0xA8                          //Address lower threshold register, set Word Bit
WriteWord (Address, Command, T_Lower.LoByte, T_Lower.HiByte)
//Write the upper threshold register
Command = 0xAA                          //Address upper threshold register, set Word bit
WriteWord (Address, Command, T_Upper.LoByte, T_Upper.HiByte)
//Enable interrupt
Command = 0x82                          //Address interrupt register
Data = 0x24                             //SMBAlert style, Persist 2.5 seconds
WriteByte(Address, Command, Data)
```

In order to generate an interrupt on demand during system test or debug, a test mode (INTR = 11) can be used. The following example illustrates how to generate an interrupt on demand:

```
// Generate an interrupt
      Address = 0x39                          //Slave address alternately 0x29 or 0x49
      Command = 0x82                          //Address Interrupt Control Register
      Data = 0x30                             //Test interrupt
      WriteByte(Address, Command, Data)

      //Interrupt line should now be low
```

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APPLICATION INFORMATION: HARDWARE

Power Supply Decoupling and Application Hardware Circuit

The power supply lines must be decoupled with a 0.1 μF capacitor placed as close to the device package as possible (Figure 28). The bypass capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents caused by internal logic switching.

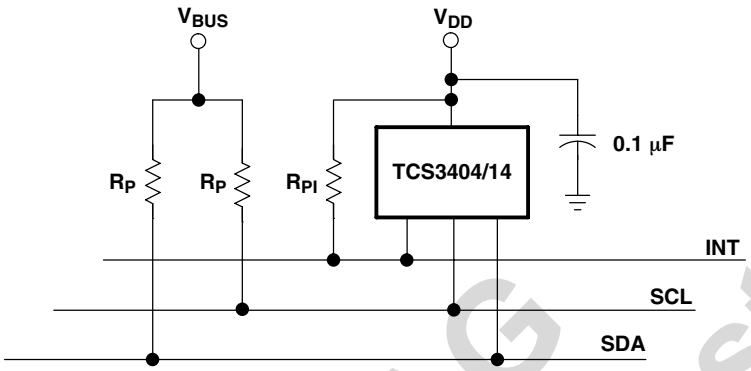


Figure 28. Bus Pull-Up Resistors

Pull-up resistors (Rp) maintain the SDA and SCL lines at a *high* level when the bus is free and ensure the signals are pulled up from a low to a high level within the required rise time. For a complete description of I^2C maximum and minimum Rp values, please review the NXP I^2C design specification at http://www.i2c–bus.org/references/.

A pull-up resistor (R_{PI}) is also required for the interrupt (INT), which functions as a wired-AND signal in a similar fashion to the SCL and SDA lines. A typical impedance value between 10 kΩ and 100 kΩ can be used. Please note that while the figure above shows INT being pulled up to V_{DD}, the interrupt can optionally be pulled up to V_{BUS}.

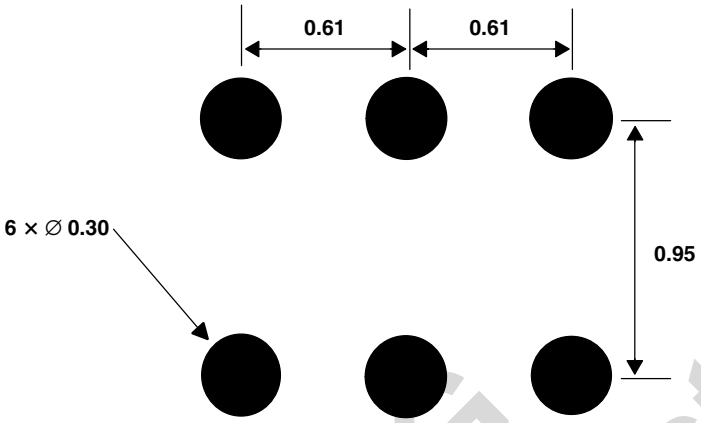
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APPLICATION INFORMATION: HARDWARE

PCB Pad Layout for CS Package

Suggested PCB pad layout guidelines for the CS package are shown in Figure 29.

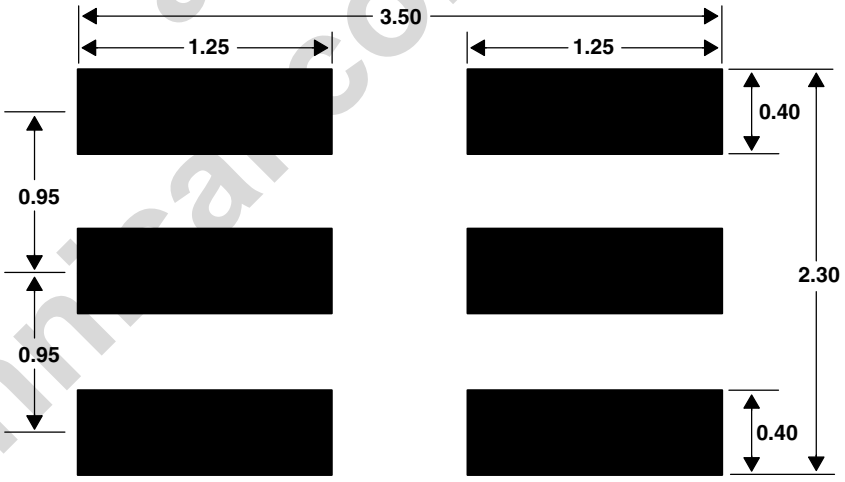


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Figure 29. Suggested CS Package PCB Layout

PCB Pad Layout for FN Package

Suggested PCB pad layout guidelines for the Dual Flat No-Lead (FN) surface mount package are shown in Figure 30.



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Figure 30. Suggested FN Package PCB Layout

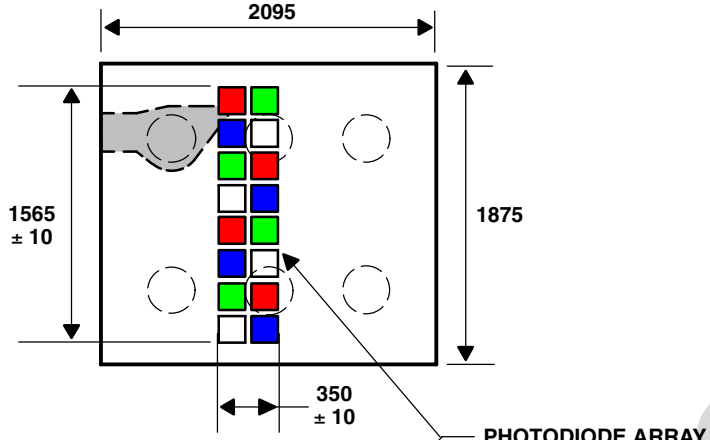
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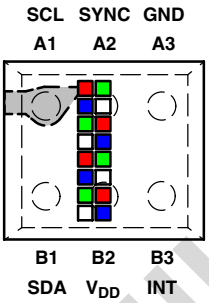
MECHANICAL DATA

PACKAGE CS — Six-Lead Chipscale

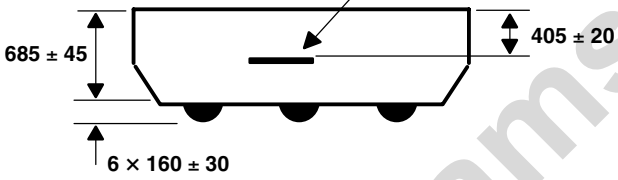
TOP VIEW



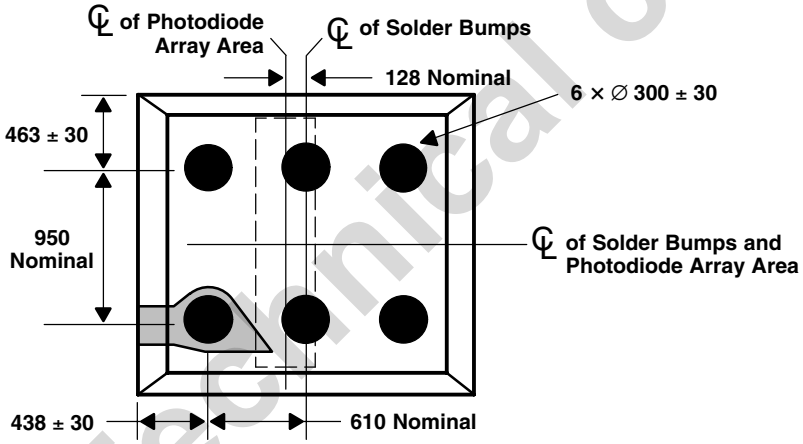
**PINOUT
TOP VIEW**



END VIEW



BOTTOM VIEW



Pb
Lead Free

NOTES: A. All linear dimensions are in micrometers. Dimension tolerance is ± 25 µm unless otherwise noted.
B. Solder bumps are formed of Sn (96.5%), Ag (3%), and Cu (0.5%).
C. The layer above the photodiode is glass and epoxy with an index of refraction of 1.53.
D. This drawing is subject to change without notice.

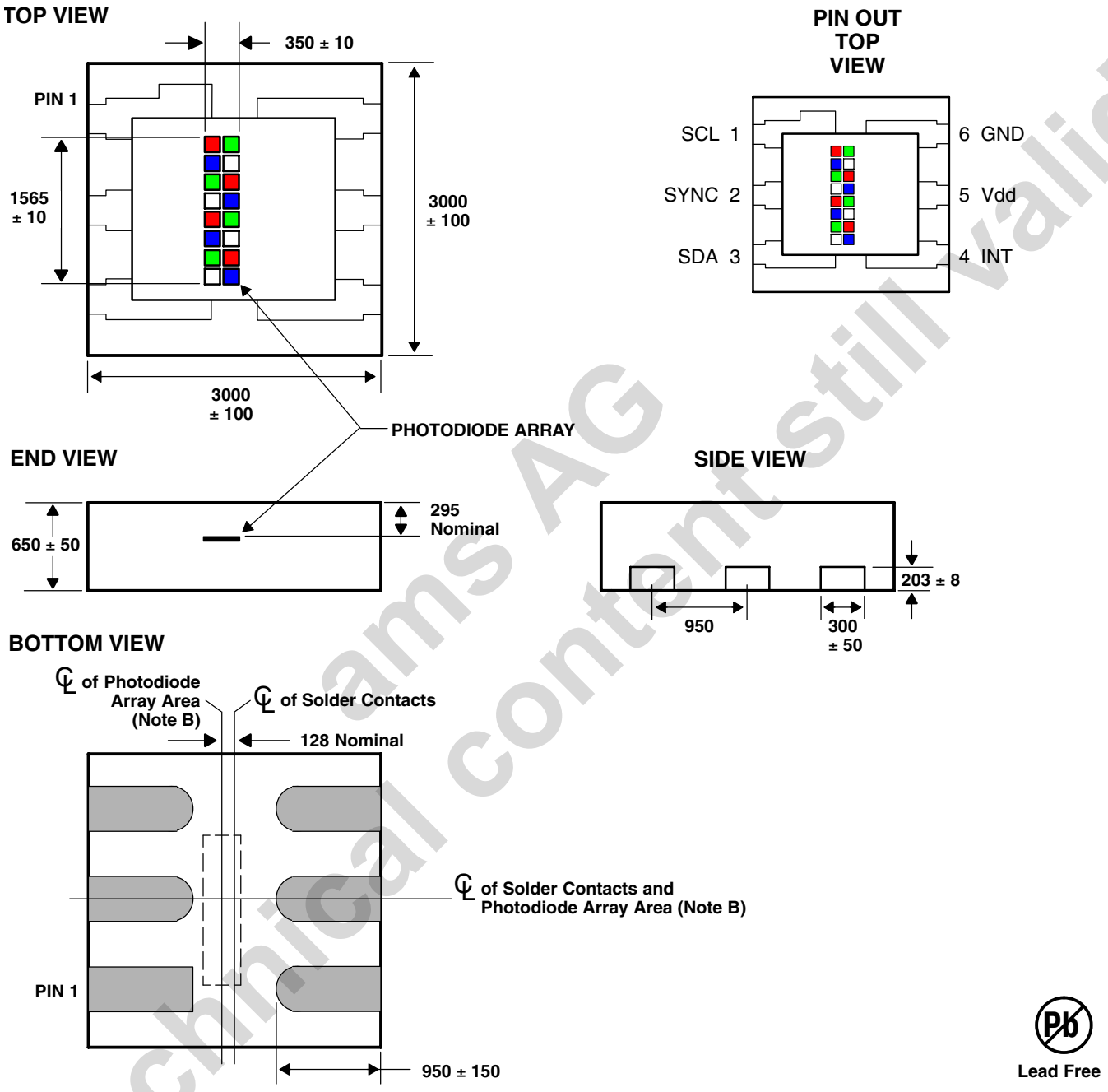
Figure 31. Package CS — Six-Lead Chipscale Packaging Configuration

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MECHANICAL DATA

PACKAGE FN — **Dual Flat No-Lead**



Pb Lead Free

NOTES: A. All linear dimensions are in micrometers. Dimension tolerance is ± 20 µm unless otherwise noted.
B. The die is centered within the package within a tolerance of ± 3 mils.
C. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
D. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
E. This package contains no lead (Pb).
F. This drawing is subject to change without notice.

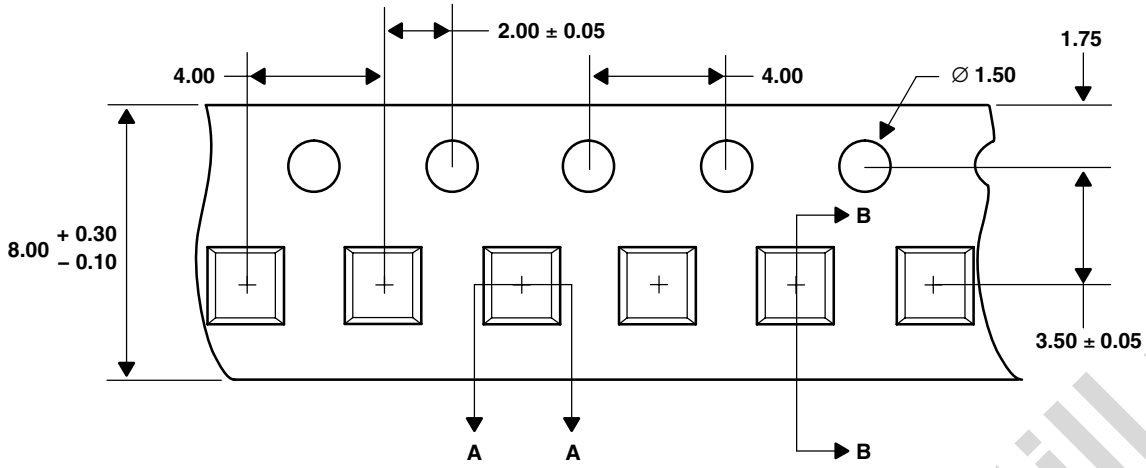
Figure 32. Package FN — Dual Flat No-Lead Packaging Configuration

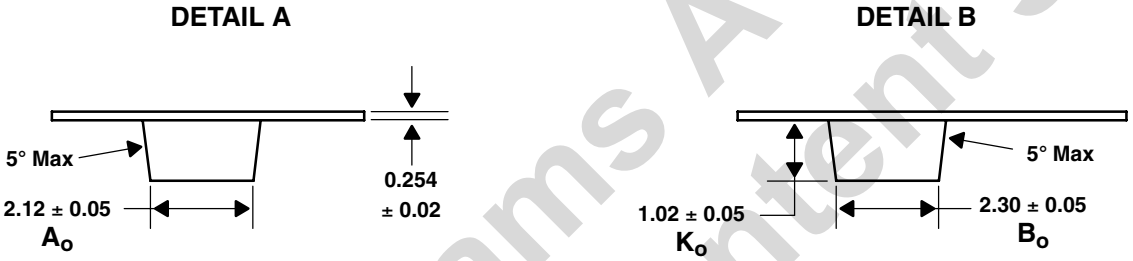
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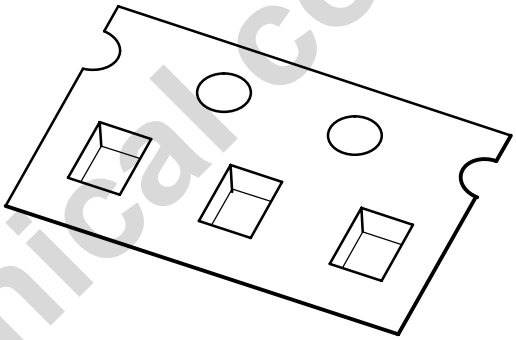
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MECHANICAL DATA

TOP VIEW







NOTES: A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
C. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481–B 2001.
D. Each reel is 178 millimeters in diameter and contains 3500 parts.
E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481–B.
F. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape
G. This drawing is subject to change without notice.

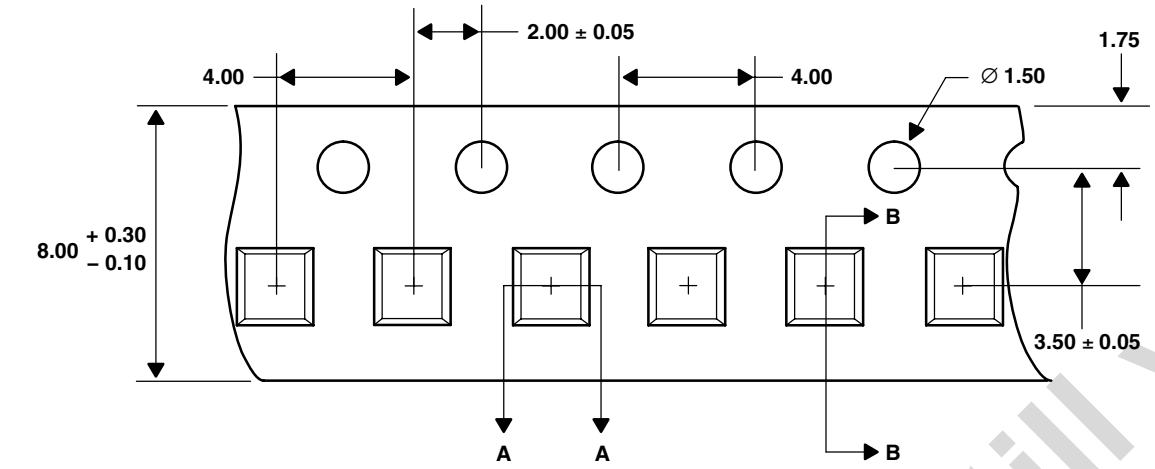
Figure 33. Package CS Carrier Tape

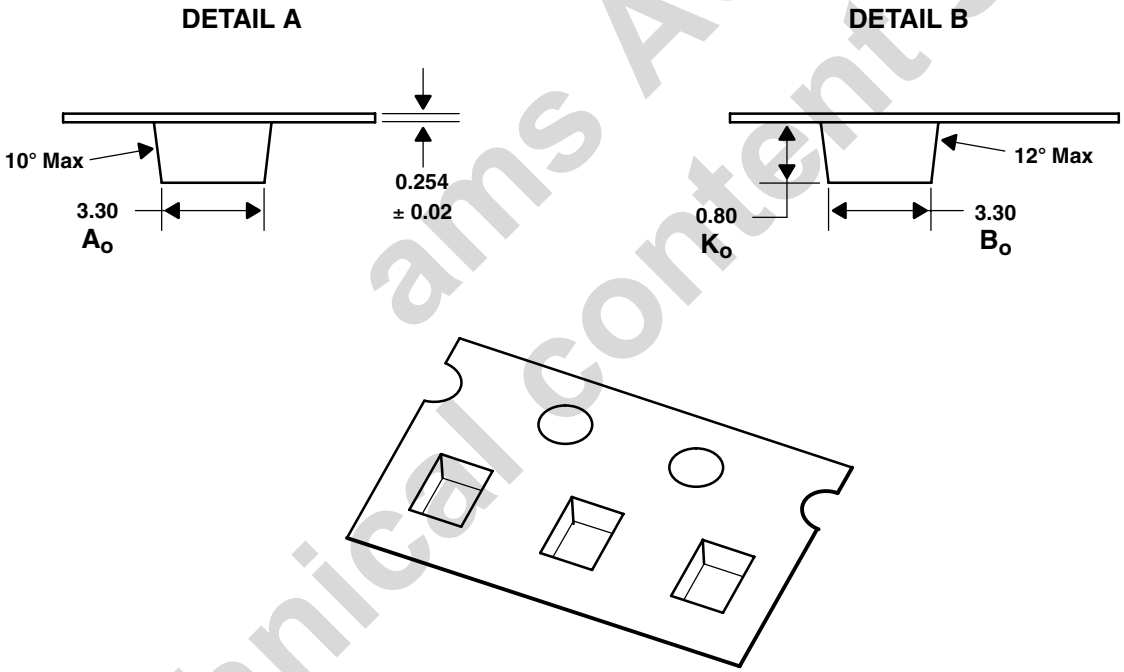
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MECHANICAL DATA

TOP VIEW





NOTES:
H. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
I. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
J. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481–B 2001.
K. Each reel is 178 millimeters in diameter and contains 3500 parts.
L. TAOS packaging tape and reel conform to the requirements of EIA Standard 481–B.
M. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape
N. This drawing is subject to change without notice.

Figure 34. Package FN Carrier Tape

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MANUFACTURING INFORMATION

The CS and FN packages have been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Table 12. Solder Reflow Profile

PARAMETER	REFERENCE	TCS3404/14
Average temperature gradient in preheating		2.5°C/sec
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T1)	t_1	Max 60 sec
Time above 230°C (T2)	t_2	Max 50 sec
Time above T_{peak} –10°C (T3)	t_3	Max 10 sec
Peak temperature in reflow	T_{peak}	260° C (–0°C/+5°C)
Temperature gradient in cooling		Max –5°C/sec

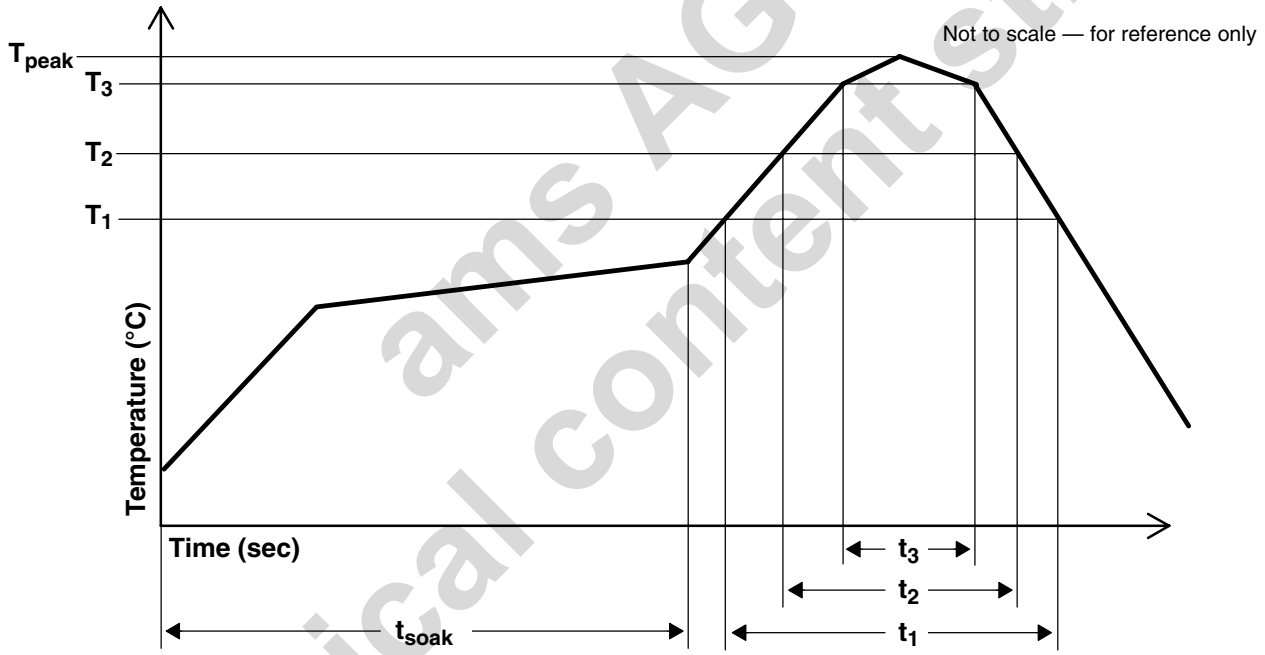


Figure 35. Solder Reflow Profile Graph

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MANUFACTURING INFORMATION

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package molding compound. To ensure the package molding compound contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

CS Package

The CS package has been assigned a moisture sensitivity level of MSL 2 and the devices should be stored under the following conditions:

Temperature Range	5°C to 50°C
Relative Humidity	60% maximum
Floor Life	1 year out of bag at ambient < 30°C / 60% RH

Rebaking will be required if the aluminized envelope has been open for more than 1 year. If rebaking is required, it should be done at 50°C for 12 hours.

FN Package

The FN package has been assigned a moisture sensitivity level of MSL 3 and the devices should be stored under the following conditions:

Temperature Range	5°C to 50°C
Relative Humidity	60% maximum
Total Time	12 months from the date code on the aluminized envelope — if unopened
Opened Time	168 hours or fewer

Rebaking will be required if the devices have been stored unopened for more than 12 months or if the aluminized envelope has been open for more than 168 hours. If rebaking is required, it should be done at 50°C for 12 hours.

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