W83601R/602R
Winbond GPI/O IC

Winbond Electronics Corp.

PRELIMINARY

W83601R/602R Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1	n.a.			n.a.	All the version before 0.30 are for internal use.
2	n.a.	99/8	0.3	n.a.	First publication.
3	P.4,5 P.6 P.10 P.13	99/8	0.31	n.a.	Change Pin Description of W83601R pin 3,4,5. Change Pin Description of W83602R pin 3,4. Update Register Table. CR16 is a reserved register. Please ignore it. Change INT output description.
4	P.10	99/9	0.32	n.a.	CR15 bit 3 description.
5	P.11	01/02	0.33	n.a.	Insert 8.1 section – Access interface
6	P.10	02/02	0.34	n.a.	Update CR21 Chip ID.
7					
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9					
10					

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LIFE SUPPORT APPLICATIONS

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Preliminary

1. GENERAL DESCRIPTION

The W83601R/602R are general purpose input/output ICs with SMBus™(I^2C). W83601R provides 15 GPI/O pins. W83602R provides 9 GPI/O pins and ACPI power control function for STR.

W83601R/602R both provides SMBus™(I^2C) address setting pins to set the address during power- on reset or from external reset.

W83601R SMBus™ Address is :

0	0	1	1	A2	A1	A0	R/W

W83602R SMBus™ Address is :

0	0	1	1	0	A1	A0	R/W

W83601R/602R also provides a interrupt to inform system that a transition occurs on General Purpose(GP) input pins.

2. FEATURES

- SMBus compliance with 3.3V voltage levels
- Two ports GPI/O which provides more flexibility
- Issue interrupt to notify system that a event occurs
- GP output can be level or pulse mode
- Interrupt output can be level or pulse mode
- Internal power-on reset or external RST# pin reset
- Programmable POWER LED output
- ACPI power management for Suspend To Ram (STR) (only for W83602R)

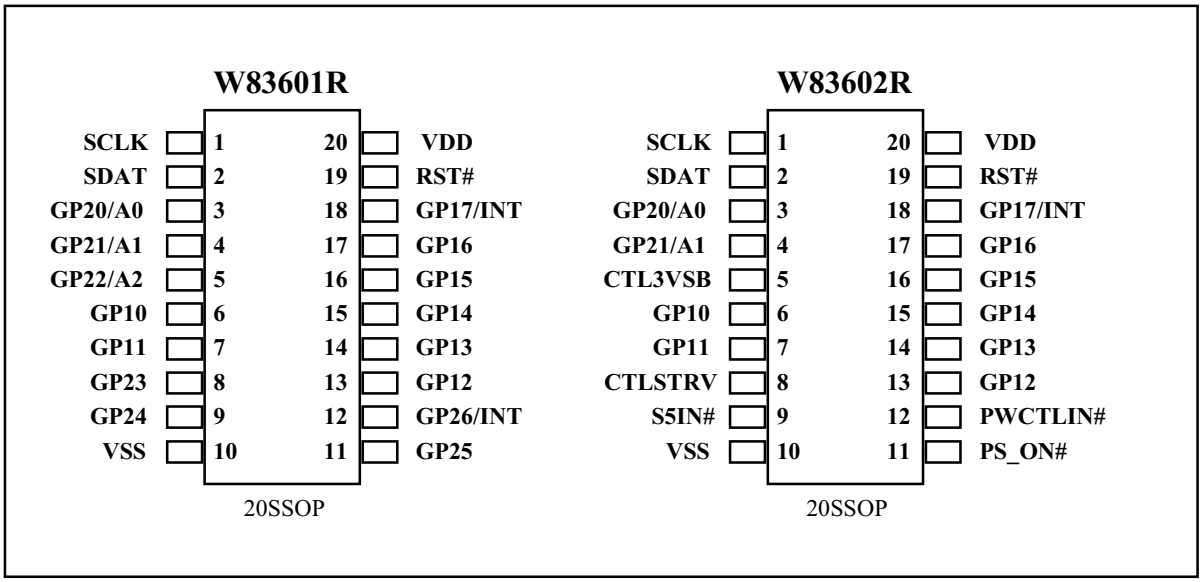
3. PACKAGE

- 20-pin SSOP

4. KEY SPECIFICATIONS

- Supply Voltage 5V
- Operating Supply Current 1 mA typ.
- Operating Temperature 0 - 70 °C

5. PIN CONFIGURATION FOR W83601R/602R



6. PIN DESCRIPTION

Note: Please refer to Section 13.2 DC CHARACTERISTICS for details.

I/OD_{24t} - TTL level bi-directional pin open drain output with 12 mA sink capability

I/O_{24t} - TTL level bi-directional pin with 24 mA source-sink capability

IN_t - TTL level input pin

IN_{td} - TTL level input pin with internal pull down resistor

IN_{ts} - TTL level Schmitt-trigger input pin

W83601R UNIVERSAL GENERAL PURPOSE I/O PORT FOR I2C BUS

PIN	SYMBOL	I/O	FUNCTION
1	SCL	IN_{ts}	SMBus Clock. (I^2C clock)
2	SDA	I/OD_{12}	SMBus bi-directional Data.(I2C data)
3	GP20 A0	I/O_{24} IN_{td}	General Purpose I/O . **This pin is a setting pin for SMBus(I^2C) address bit 0 during power-on reset or RST# pin reset.**
4	GP21 A1	I/O_{24} IN_{td}	General Purpose I/O . **This pin is a setting pin for SMBus(I^2C) address bit 1 during power-on reset or RST# pin reset.**
5	GP22 A2	I/O_{24} IN_{td}	General Purpose I/O . **This pin is a setting pin for SMBus(I^2C) address bit 2 during power-on reset or RST# pin reset.**
6	GP10	I/OD_{24}	General Purpose I/O default input.
7	GP11	I/OD_{24}	General Purpose I/O default input.
8	GP23	I/OD_{24}	General Purpose I/O default input.
9	GP24	I/OD_{24}	General Purpose I/O default input.
10	VSS	PWR	Ground Pin.
11	GP25	I/OD_{24}	General Purpose I/O default input.
12	GP26 INT	I/OD_{24} OD_{24}	General Purpose I/O default input. Auto-generate Interrupt signal when detetecting a transition on GPI inputs. This interrupt is either on pin12 or pin18.
13	GP12	I/OD_{24}	General Purpose I/O default input.
14	GP13	I/OD_{24}	General Purpose I/O default input.
15	GP14	I/OD_{24}	General Purpose I/O default input.
16	GP15	I/OD_{24}	General Purpose I/O default input.
17	GP16	I/OD_{24}	General Purpose I/O default input.
18	GP17 INT	I/OD_{24} OD_{24}	General Purpose I/O default input. Auto-generate Interrupt signal when detetecting a transition on GPI inputs. This interrupt is either on pin12 or pin18
19	RST#	IN_{ts}	Reset signal input.

20	VDD	PWR	Power Pin.

W83602R UNIVERSAL GENERAL PURPOSE I/O PORT FOR I2C BUS & ACPI POWER CONTROL

PIN	SYMBOL	I/O	FUNCTION
1	SCL	IN_{ts}	SMBus Clock. (I^2C clock)
2	SDA	I/OD_{12}	SMBus bi-directional Data.(I2C data)
3	GP20/A0	I/O_{24}	General Purpose I/O. Power on setting for SMBus(I^2C) address bit 0.
4	GP21/A1	I/O_{24}	General Purpose I/O. Power on setting for SMBus(I^2C) address bit 1.
5	CTL3VSB	OD_{24}	Control 3VSB and 3VCC power source for ACPI features.
6	GP10	I/OD_{24}	General Purpose I/O default input.
7	GP11	I/OD_{24}	General Purpose I/O default input.
8	CTLSTR	OD_{24}	Suspend to RAM power control output.
9	S5IN#	IN_t	S5# signal input.
10	VSS	PWR	Ground Pin.
11	PS_ON#	OD_{24}	ATX power power on_off control.
12	PWCTLIN#	IN_t	Connected to W83627F/HF power control output .
13	GP12	I/OD_{24}	General Purpose I/O default input.
14	GP13	I/OD_{24}	General Purpose I/O default input.
15	GP14	I/OD_{24}	General Purpose I/O default input.
16	GP15	I/OD_{24}	General Purpose I/O default input.
17	GP16	I/OD_{24}	General Purpose I/O default input.
18	GP17 INT	I/OD_{24} OD_{24}	General Purpose I/O default input. Auto-generate Interrupt signal when detetecting a transition on GPI inputs.
19	RST#	IN_{ts}	Reset signal input.
20	VDD	PWR	Power Pin.

7. REGISTERS

7.1 BRIEF OF REGISTER CONTENTS

INDEX	R/W	DEFAULT	REGISTERS DESCRIPTION
00h	R	-	GP Port 1: Input Port Data Register
01h	R/W	00	GP Port 1: Output Port Data Register
02h	R/W	f0	GP Port 1: Polarity Inversion Register
03h	R/W	ff	GP Port 1: Input/Output Configuration Register
04h	R/W	00	GP Port 1: Output style control Register.
05h	R	-	GP Port 1: Input Latched Data Register.
06-07h	-	-	Reserved Register
08h	R	-	GP Port 2: Input Port Register
09h	R/W	00	GP Port 2: Output Port Register
0Ah	R/W	70	GP Port 2: Polarity Inversion Register
0Bh	R/W	7f	GP Port 2: Input/Output Configuration Register
0Ch	R/W	00	GP Port 2: Output style control Register.
0Dh	R	-	GP Port 2: Input Latched Data Register.
0E-0Fh	-	-	Reserved Register
10h	R	00	GP Port 1: Interrupt Status Register.
11h	R	00	GP Port 2: Interrupt Status Register
12h	R/W	00	GP Port 1: Interrupt Enable Register
13h	R/W	00	GP Port 2: Interrupt Enable Register
14h	R/W	00	Mode Configuration Register
15h	R/W	00	Power LED Configuration Register
16-1Fh	-	-	Reserved Register
20h	R	60	Chip ID High Byte Register
21h	R	12	Chip ID Low Byte Register (W83601R)
		22	Chip ID Low Byte Register (W83602R)

7.2 W83601R/602R REGISTERS DESCRIPTIONS

CR00 (GP Port 1: Input port Data Register, Default 0x-- , Read Only)

This register is a data port for input only. It reflects the incoming logic levels of the pins whether the pins is defined as an input mode by CR03. It will be inverted data by CR02.

Bit 7 ~ 0: GP17 ~ GP10 Input Data Port.

CR01 (GP Port 1: Output port Data Register, Default 0x00, Read/Write)

This register is a data port for output only. It reflects the outgoing logic levels of the pins whether the pins is defined as an output mode by CR03. This register will reflect the value of output Flip-flop while read access. The output data will be inverted or changed output style by CR02 or CR04.

Bit 7 ~ 0: GP17 ~ GP10 Output Data Port.

CR02 (GP Port 1: Polarity Inversion Register, Default 0xf0, Read/Write)

This register enables polarity inversion of pins defined as input or output by CR03.

When set to a "1", the incoming/outgoing port value is inverted.

When set to a "0", the incoming/outgoing port value is the same as in data register.

Bit 7 ~ 0: GP17 ~ GP10 Polarity Iversion Register.

CR03 (GP Port 1: Input/Output Configuration Register, Default 0xff, Read/Write)

This register selects Input or Output mode of pins.

When set to a "1", respective GPIO port is programmed as an input port.

When set to a "0", respective GPIO port is programmed as an output port.

Bit 7 ~ 0: GP17 ~ GP10 Input/Output Configuration Register.

CR04 (GP Port 1: Output Style Control Register, Default 0x00, Read/Write)

This register selects Output style of pins as level or pulse.

When set to a "1", respective GPIO port is programmed as an pulse signal.

When set to a "0", respective GPIO port is programmed as an level signal.

Bit 7 ~ 0: GP17 ~ GP10 Output Style Control Register.

CR05 (GP Port 1: Input latched data Register, Default 0x--, Read Only)

This register will latch Port 1 data while power on or RST# pin low, which is controlled by CR14h bit 0 .

Bit 7 ~ 0: GP17 ~ GP10 Input latched data .

CR06-07 Reserved Register

CR08 (GP Port 2: Input port Data Register, Default 0x--, Read Only)

This register is a data port for input only. It reflects the incoming logic levels of the pins whether the pins is defined as an input mode by CR0B. It will be inverted data by CR0A.

Bit 7: Reserved.

Bit 6 ~ 0: GP26 ~ GP20 Input Data Port.

CR09 (GP Port 2: Output port Data Register, Default 0x00, Read/Write)

This register is a data port for output only. It reflects the outgoing logic levels of the pins whether the pins is defined as an output mode by CR0B. This register will reflect the value of output Flip-flop while read access. The output data will be inverted or changed output style by CR0A or CR0C.

Bit 7: Reserved.

Bit 7 ~ 0: GP26 ~ GP20 Output Data Port.

CR0A (GP Port 2: Polarity Inversion Register, Default 0x70, Read/Write)

This register enables polarity inversion of pins defined as input or output by CR0B.

When set to a "1", the incoming/outgoing port value is inverted.

When set to a "0", the incoming/outgoing port value is the same as in data register.

Bit 7: Reserved.

Bit 6 ~ 0: GP26 ~ GP20 Polarity Inversion Register.

CR0B (GP Port 2: Input/Output Configuration Register, Default 0x7f, Read/Write)

This register selects Input or Output mode of pins.

When set to a "1", respective GPIO port is programmed as an input port.

When set to a "0", respective GPIO port is programmed as an output port.

Bit 7: Reserved.

Bit 6 ~ 0: GP26 ~ GP20 Input/Output Configuration Register.

CR0C (GP Port 2: Output Style Control Register, Default 0x00, Read/Write)

This register selects Output style of pins as level or pulse.

When set to a "1", respective GPIO port is programmed as an pulse signal.

When set to a "0", respective GPIO port is programmed as an level signal.

Bit 7: Reserved.

Bit 6 ~ 0: GP26 ~ GP20 Output Style Control Register.

CR0D (GP Port 2: Input latched data Register, Default 0x--, Read Only)

This register will latch Port 2 data while power on or RST# pin low, which is controlled by CR14h bit 1 .

Bit 7: Reserved.

Bit 6 ~ 0: GP26 ~ GP20 Input latched data, which bit 2-0 are SMBus address bit A2-A0 .

CR0E-0F Reserved Register

CR10 (GP Port1: Interrupt Status Register , Default 0x00, Read Only)

Bit 7-0 : = 1, a transition occurs at pin GP17-GP10.

If GP17/INT is selected as interrupt function, bit 7 of this register will always be 0.

A read to this register will clear this register.

CR11 (GP Port2: Interrupt Status Register , Default 0x00, Read Only)

Bit 7 : = Reserved.

Bit 6-0 : = 1, a transition occurs at pin GP26-GP20.

If GP26/INT is selected as interrupt function, bit 6 of this register will always be 0.

A read to this register will clear this register.

CR12 (GP Port 1: Interrupt Enable Register , Default 0x00 , Read/Write)

Bit 7-0 : = 0, disable GP17-GP10 interrupt output when interrupt function is selected.

CR13 (GP Port 2: Interrupt Enable Register , Default 0x00 , Read/Write)

Bit 7-6 : = Reserved.

Bit 5-0 : = 0, disable GP26-GP20 interrupt output when interrupt function is selected.

CR14 Mode Configuration Register (Default 0x00, Read/Write)

Bit 7 : = 1, Set GP/INT pin as INT function. 0, set GP/INT pin as GP function.

Bit 6 : = 1, Set INT function at GP26(pin 12). 0 , Set INT function at GP17(pin 18).
W83602R INT function is only at GP17.

Bit 5 : = 1, Set INT output pin as pulse mode. 0, set INT output pin as level mode.

Bit 4 : = 1, Set INT output pin polarity is 1 (normal high) . 0, set INT output pin polarity is 0 (normal low).
This bit is only for W83601R.

Bit 3 : = 1, Port 2 (CR09h-CR0Ch,CR11h,CR13h) registers can be reset to default data by RST# pin. 0 ,Port 2 (CR09h-CR0Ch) can not be reset by RST# pin.

Bit 2 : = 1, Port 1 (CR01h-CR04h,CR10h,CR12h) registers can be reset to default data by RST# pin. 0 ,Port 1 (CR01h-CR04h) can not be reset by RST# pin.

Bit 1 : = 1, Port 2 CR0Dh can be latched not only by RST# pin but also power-on period. 0, Port 2 CR0Dh can only be latched by power-on period.

Bit 0 : = 1, Port 1 CR05h can be latched not only by RST# pin but also power-on period. 0, Port 1 CR05h can only be latched by power-on period.

CR15 Power LED Configuration Register (Default 0x00, Read/Write)

Priority of LED function is highest.

Bit 7 : = 1, Enable LED function . 0, Disable LED funciton.

When LED function is enable, GP function is ignored despite of input or output.

Bit 6-4 : LED frequency selection.

= 111, LED pin is tri-state(OD pin) or drived high(O pin).

= 110, LED pin is a 1 Hz toggle pulse with 50 duty cycle.

= 101, LED pin is a 1/2 Hz toggle pulse with 50 duty cycle.

= 100, LED pin is a 1/4 Hz toggle pulse with 50 duty cycle.

= 000, LED pin is drived low.

Bit 3 : = GP port selection.

0, Select GP port 1 as LED function if bit 7 is set to 1.

1, Select GP port 2 as LED function if bit 7 Is set to 1.

As W83602R, setting this bit 1 is meaningless.

Bit 2-0 : GP pin selection.

=110-000, GP16-GP10 can be selected as LED output when bit 3 is 0.

=101-011, GP25-GP23 can be selected as LED output when bit 3 is 1.

As W83602R, only GP16-GP10 can be selected as LED output.

CR16-1F Reserved Register

CR20 (Chip ID High Byte, Read Only)

Bit 7-0 : = 0x60.

CR21 (Chip ID Low Byte, Read Only)

Bit 7-0 : = 0x13 (for W83601R).

= 0x23 (for W83602R).

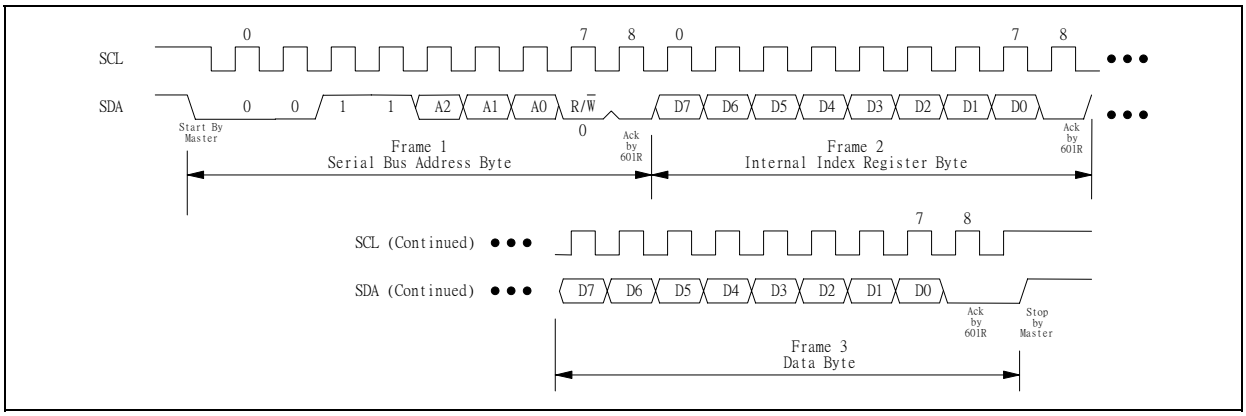
NOTE: W83602R has no GP22-GP26. All the corresponding register has no effect on W83602R.

8. FUNCTION DESCRIPTIONS

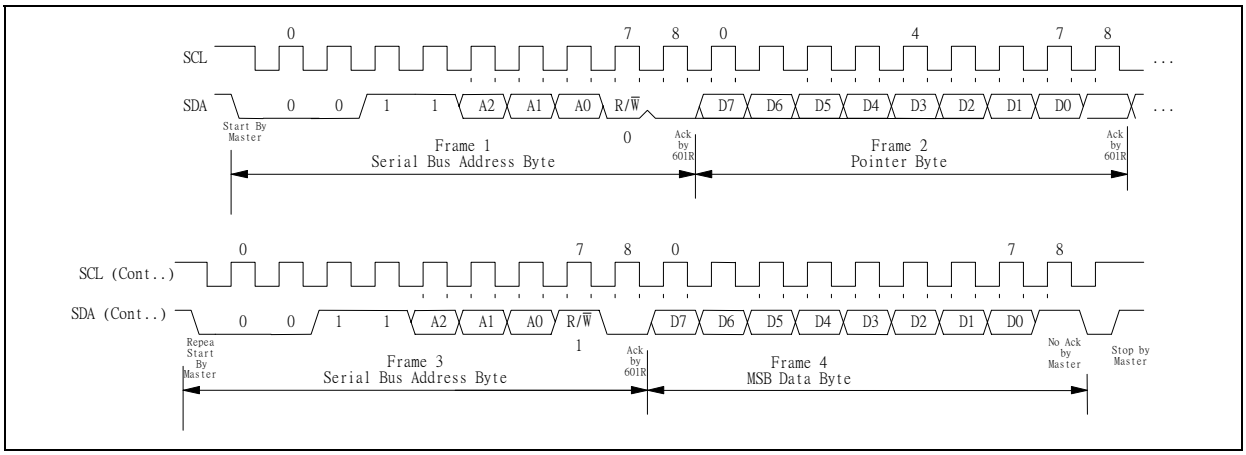
8.1 ACCESS INTERFACE

W83601R/602R provides a two-wired serial interface which is compliant with SMBus™ 1.0 Write Byte and Read Byte protocol.

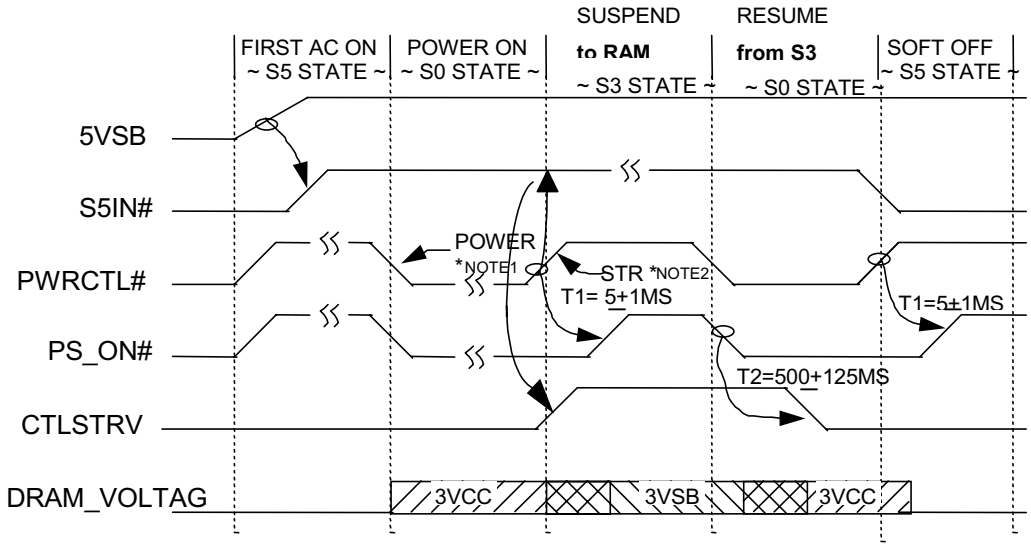
8.1.1 Write a data into W83601R/602R register



8.1.2 Read a data from W83601R/602R register



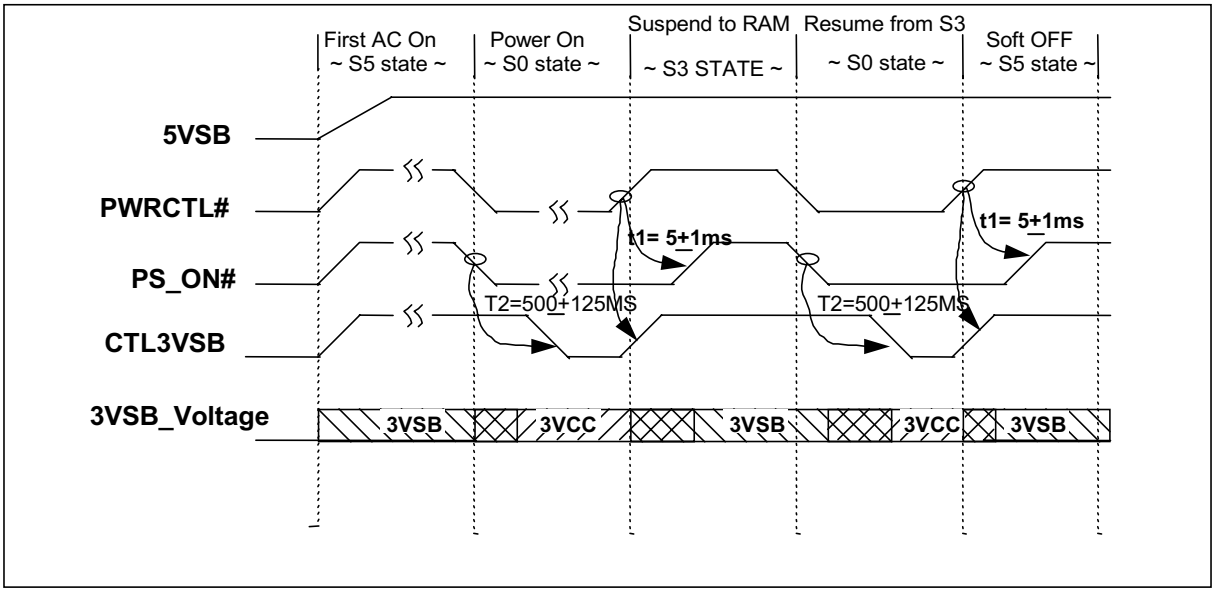
8.2 CTLSTRV TIMING WAVEFORMS (ONLY FOR W83602R)



*NOTE 1: IT CAN WAKE UP POWER FROM POWER BUTTON, KEYBOARD/MOUSE.

*NOTE 2: IT CAN SUSPEND TO RAM BY OS OR SPECIAL DEFINED

8.3 CTL3VSB Timing Waveforms(Only for W83602R)



8.4 GPI/O Output Mode :

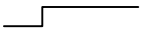
8.4.1 GPO output

Tow output modes for GPO. One is LEVEL and the other is PULSE.

GPO Output Style	Polarity	Output Port Register	Output Value at Pin	Wave
Level	0	0	0	⎯⎯⎯
		1	1	⎯⎯⎯
	1	0	1	⎯⎯⎯
		1	0	⎯⎯⎯
Pulse	0	write 1	Active	⎍
	1	write 1	Active	⎎

8.4.2 INT output

Two output modes for INT pin. One is LEVEL mode and the other is PULSE.

INT Output Mode	Polarity	Output	Wave
Level	0(normal low)	1	
	1(normal high)	0	
Pulse	0(normal low)	High Pulse	
	1(normal high)	Low Pulse	

In Level mode, if INT is activated, it will be de-activated when interrupt status registers are read.

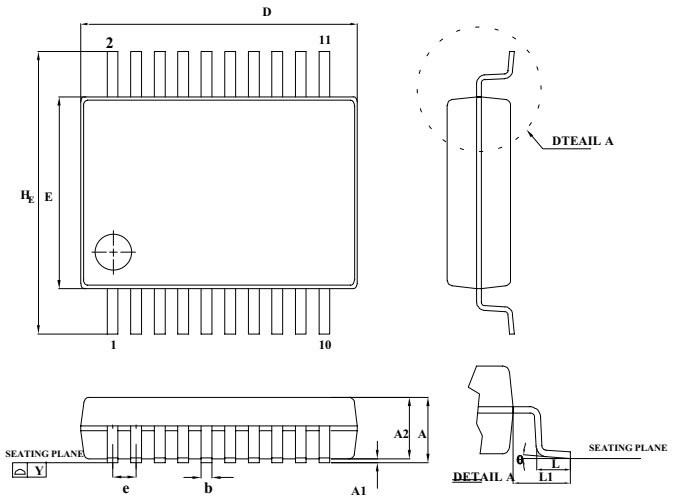
In Pulse mode, interrupt will be activated again unless all enabled interrupt status registers are read.

8.4.3 GPI interrupt status

Once a transition occurs at GPI input pins, interrupt status registers(CR10, CR11) will be set. At the mean time, if interrupt function is enable, INT pin will generate a interrupt. Reading these interrupt registers will clear themselves and reset interrupt. If an interrupt occurs but no read to interrupt status registers, interrupt will not be generated again.

9. PACKAGE DRAWING AND DIMENSIONS

20 SSOP-209 mil



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	6.90	7.20	7.50	0.272	0.283	0.295
E	5.00	5.30	5.60	0.197	0.209	0.220
H E	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

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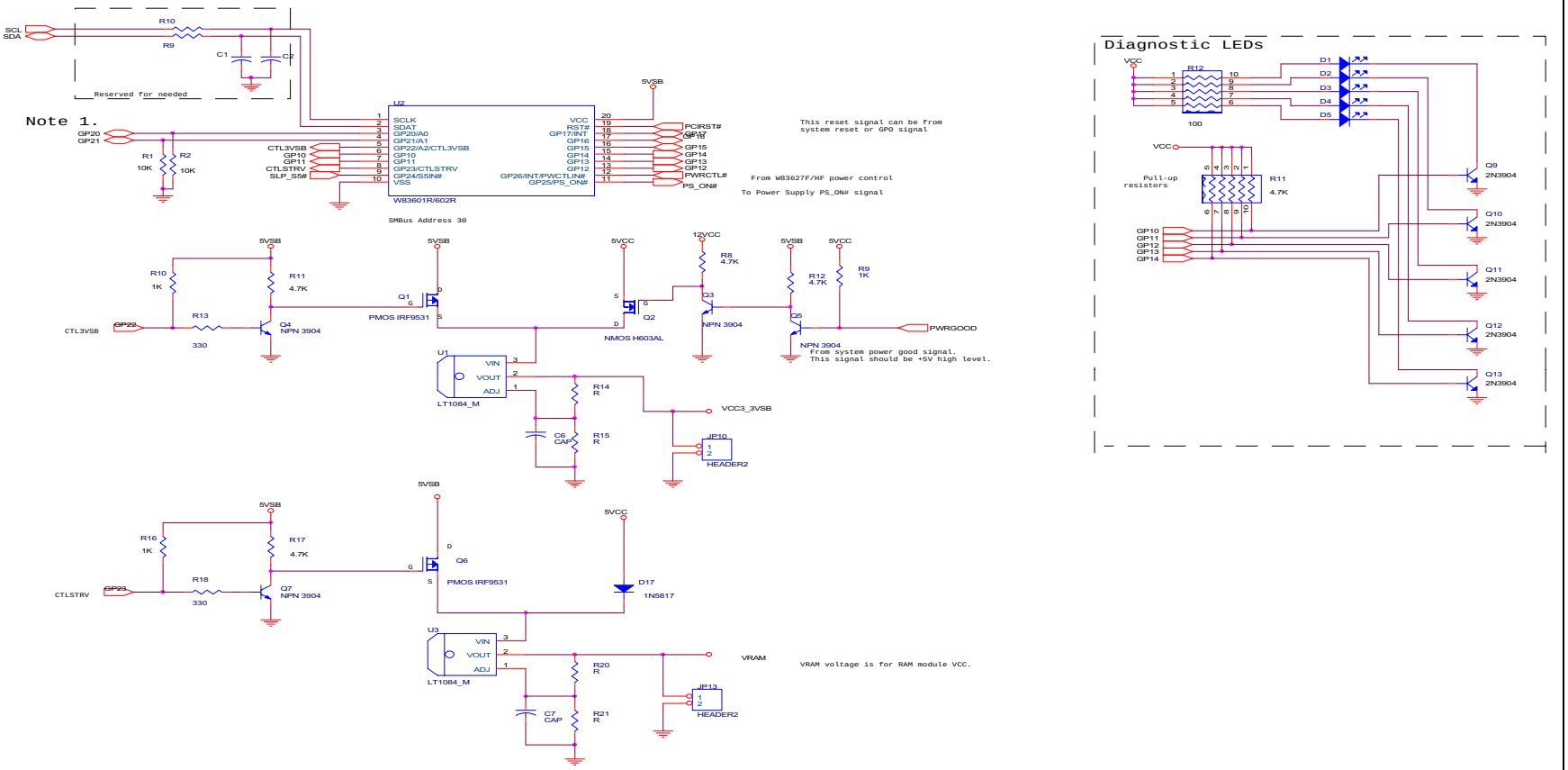
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W83602R Example Application Circuit



Note 1. : Be sure that during Power-On reset or RST# reset, GP20 and GP21 will not receive signal which will affect the SMBus address setting.

Winbond Electronic Corp.		
Title: W83602R Example Application Circuit		
Size: Custom	Document Number: 602ap.sch	Rev: 0.1
Date: Thursday, August 12, 1999	Sheet 1 of 1	

REV	Decription
0.1	First Publication
0.2	Change CTL3VSB, CTLSTRV Schematic

Winbond Electronic Corp.		
Title: W83601R/602R Example Application Circuit		
Size: Custom	Document Number: 602ap.sch	Rev: 0.2
Date: Friday, August 13, 1999	Sheet 2 of 1	