MN89201

VGA-NTSC Scan Converter

■ Overview

The MN89201 converts PC/AT VGA (640 × 480) display data into an NTSC video signal without requiring an external frame memory. It uses filtering to eliminate flicker and produce a high-quality television image.

Note: PC/AT and VGA are registered trademarks of International Business Machines Corporation.

■ Features

- Conversion of PC/AT VGA (640 × 480) display data into NTSC video signal
  - 8-bit inputs for VGA R, G, and B signals
    Horizontal frequency: 31.5 kHz
    Vertical frequency: 59.94 Hz
  - Conversion of non-interlaced display to interlaced display
  - Built-in phase-locked loop for synchronizing VGA and NTSC data clocks
  - Conversion from RGB to YCrCb (4:2:2) format
  - Data output in NTSC display format (YCrCb24 or YCrCb16-bit)
- Flicker prevention
  - Choice of line filters with 3 taps for preventing flicker
- Processing with only line memory
  - No need for external VRAM
  - All processing completes within built-in line memory
- Choice of readout clocks for NTSC output

  Choice 1: Choice of clock that has arbitrary frequency and synchronizes with VGA clock
  External voltage-controlled oscillator in addition to built-in phase-locked loop

  Choice 2: Choice of clock that has arbitrary frequency and does not synchronize with VGA clock
  External oscillator

  Choice 3: Clock with half frequency of the VGA-dot-clock

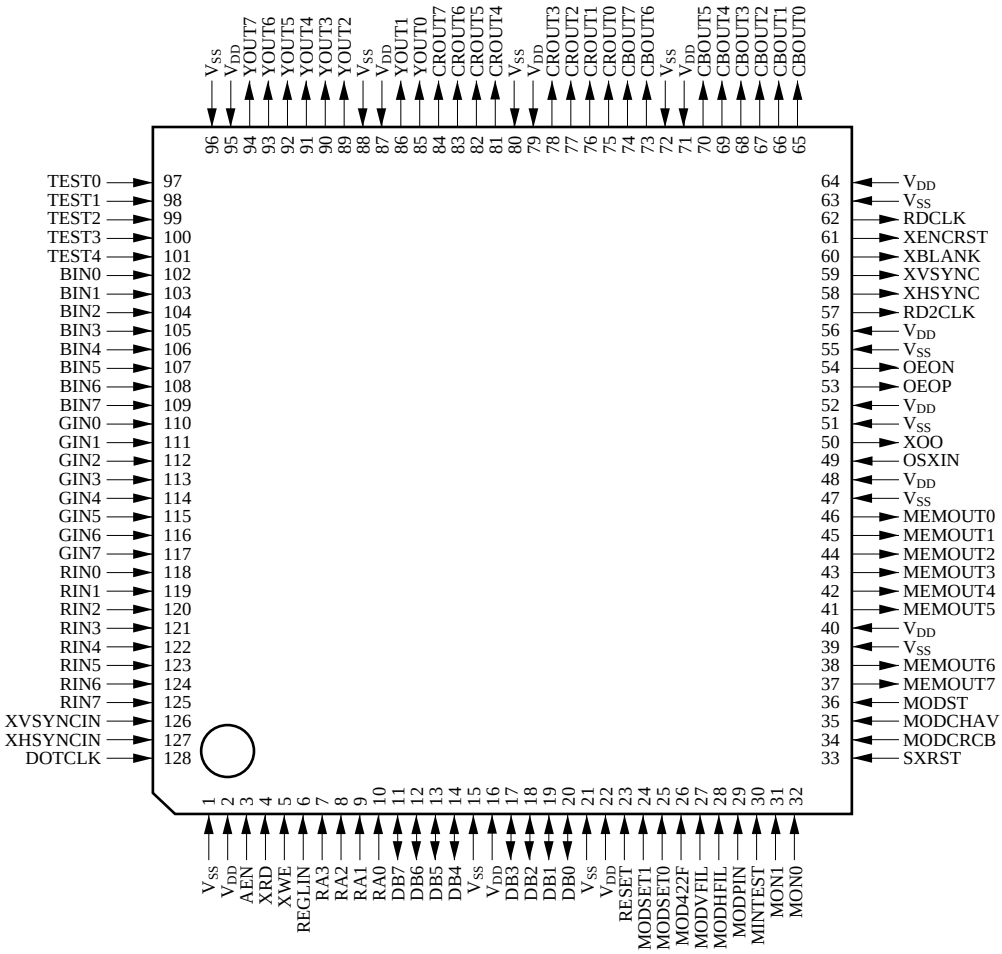
  Choose the clock matching the NTSC encoder.

The MN89201 offers high-quality NTSC-compatible output from a compact configuration.

■ Applications

- Point-of-sale terminals, Factory automation terminals, word processors, and other terminals

■ Pin Assignment

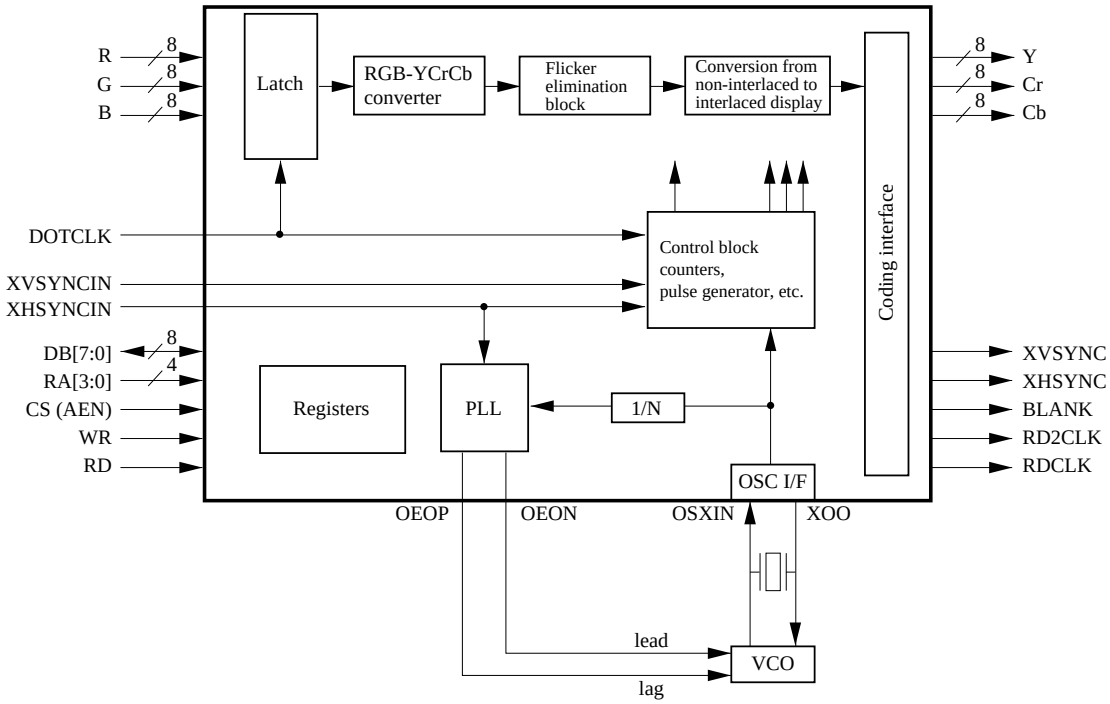


(TOP VIEW)
QFH128-P-1818

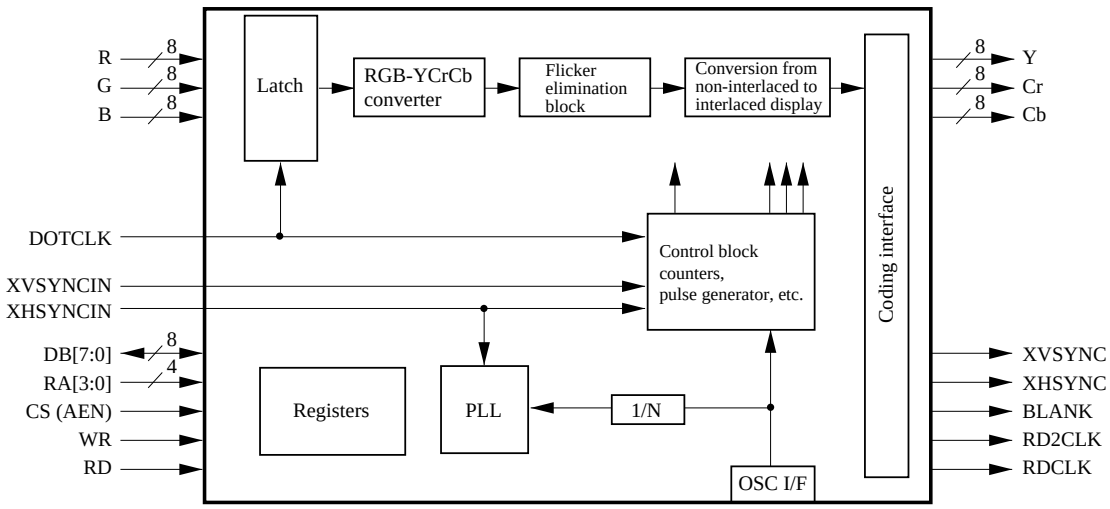
Note: Never leave V_{DD} and V_{SS} pins open.

■ Block Diagram

• RDCLK from an external VCO clock synchronized with VGA clock



• RDCLK from VGA clock



■ Pin Descriptions

Pin No.	Symbol	I/O	Function Description
3	AEN	I	Chip select signal "L" level: Register access enabled "H" level: Register access disabled
4	XRD	I	Read control signal "L" level: Read enabled
5	XWE	I	Write control signal "L" level: Write enabled
6	REGLIN	I	Register address mode specification "H" level: Obtain register address from RA[3:0] "L" level: Obtain register address from address register In the latter case, the address of the parameter/mode register are specified by the address register . Address register: 0H (4-bit decode) Data register: 1H (4-bit decode)
7 to 10	RA[3:0]	I	Register address specification
11 to 14 17 to 20	DB[7:0]	I	Host data bus
23	RESET	I	MN89201 reset signal Active "H" This signal initializes internal registers to their default values and resets internal synchronization counters.
24 ,25	MODSET[1:0]	I	Synchronization mode specification pins These specify the RDCLK synchronization mode for output signals to the NTSC encoder (1:0) 0 0: Use an external VCO clock signal synchronized with the VGA clock signal for RDCLK. The XH, XVSYNC, XBLANK, and XENRST signals are generated inside the MN89201 and are outputted. (synchronous) 0 1: Use an external oscillator clock signal not synchronized with the VGA clock signal for RDCLK. The XH and XVSYNC signals are retimed versions of the VGA H and VSYNC signals. (asynchronous) The other outputs use the VGA DOTCLK signal. 1 0: Use the VGA DOTCLK signal for RDCLK. The YCrCb data, XVSYNC, XBLANK, and XENRST signals all are dealt in the VGA clock. An external oscillator is not necessary. (synchronous)

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
26	MOD422F	I	Cr and Cb output mode specification "L" level: Cr and Cb are both 8 bits (24-bit mode) "H" level: Cr and Cb are multiplexed into 8 bits (16-bit mode) The combined output is sent to CROUT[7:0]. The MODCRCB pin specifies the multiplex order.
27	MODVFIL	I	This pin switches the vertical filter ON and OFF. "L" level: OFF; "H" level: ON
28	MODHFIL	I	This pin switches the horizontal filter ON and OFF. "L" level: OFF; "H" level: ON
29	MODPIN	I	This pin selects the setting of the filter mode. "H" level: Ignore mode register setting and take filter settings from pins. "L" level: Ignore pins and take filter settings from mode register.
30	MINTEST	I	Test pin Keep this pin at "L" level.
31 ,32	MON[1:0]	I	Test pin Keep this pin at "L" level.
33	SXRST	I	This signal resets the synchronization counter only. Active "H"
34	MODCRCB	I	This pin specifies the bit order for multiplexed Cr and Cb output data in the 16-bit mode. "H" level: Cr before Cb "L" level: Cb before Cr
35	MODCHAV	I	This pin selects the default values for the parameter registers determining the vertical position of the television image. "H" level: Use the default setting that centers the PC image in the television display. Setting value is 45 for back porch and 530 for active end. These settings cause one or two PC lines to be lost at both the top and bottom. "L" level: Use the default settings that align the center of the PC image at two or three lines below the center of the television display. Setting value is 35 for back porch and 514 for active end. These settings doesn't lose the tops of the images but cause three or four lines to be lost at the bottom.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
36	MODST	I	This pin selects the output signal to the monitor pin, MEMOUT7 (pin 37). "H" level: Pin 37 (normally "H" level) indicates the phase information of VSYNC signal in VGA when the MN89201 is in synchronization. Note: At the time when RESET (pin 23) or SXRST (pin 33) is driven (turned-ON or -OFF), the inner counter of the MN89201 begins to operate in phase with H and VSYNC of VGA. So, the phase shift in VGA after synchronization can cause wrong display. In this case you should survey the phase information in synchronization that is outputted from this pin, and detect the phase variation of the synchronous signal in VGA, then give RESET or SXRST to the MN89201. "L" level: Test signal output.
37	MEMOUT7/ SYNCINF	O	If the MODST pin (pin 36) is "H" level, this pin indicates phase information in synchronization of internal counters and VGA synchronizing signals. If pin 36 is "L" level, this pin is output for a test. Should be left open usually.
38 41 to 46	MEMOUT [6:0]	O	Test pin Normally leave this pin open.
49	OSXIN	I	External oscillator input pin If an external oscillator is not used, drive this pin at "L" level.
50	XOO	O	External oscillator output pin
53	OEOP	O	Internal PLL comparator result signal
54	OEON	O	Internal PLL comparator result signal
57	RD2CLK	O	This data clock is half the frequency of RDCLK, has the same frequency as the clock for Y, Cr, and Cb outputs. The XHSYNC, XVSYNC, and XBLANK signals have a retiming at the rising edge of this clock signal.
58	XHSYNC	O	Horizontal synchronizing output signal (Active "L")
59	XVSYNC	O	Vertical synchronizing output signal (Active "L")
60	XBLANK	O	Composite blanking output signal (Active "L")
61	XENRST	O	Encoder reset signal (Active "L") This signal has four fields interval (when both H and V are at "L" level.) Use it as necessary to control the NTSC encoder.
62	RDCLK	O	Encoder clock Y, Cr, and Cb outputs to the NTSC encoder are synchronized with the rising edge of this clock signal.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
65 to 70 73 to 74	CB OUT[7:0]	O	In the 24-bit mode, color difference output (CB: B-Y). And in the 16-bit mode, CBOUT0 gives the Cr flag: "H" level for Cr output.
75 to 78 81 to 84	CR OUT[7:0]	O	In the 24-bit mode, color difference output (CR: R-Y). And in the 16-bit mode, these pins yield multiplexed Cr/Cb output.
85 to 86 89 to 94	Y OUT[7:0]	O	Luminance signal output (Y)
97 to 101	TEST[4:0]	I	Test pins Keep these pins at "L" level.
102 to 109	BIN[7:0]	I	Blue input signals
110 to 117	GIN[7:0]	I	Green input signals
118 to 125	RIN[7:0]	I	Red input signals
126	XVSYNCIN	I	VVGA horizontal synchronizing input signal (Active "L")
127	XHSYNCIN	I	VGA vertical synchronizing input signal (Active "L")
128	DOTCLK	I	VGA dot clock The chip latches input data from VGA at the rising edge of this clock signal.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	– 0.3 to +7.0	V
Input pin voltage	V_I	– 0.3 to V_{DD}+0.3	V
Output pin voltage	V_O	– 0.3 to V_{DD}+0.3	V
Output current	I_{OL}	+12	mA
Output current	I_{OH}	– 12	mA
Power dissipation	P_D	1000	mW
Operating ambient temperature	T_{opr}	– 40 to +70	˚C
Storage temperature	T_{stg}	– 55 to +150	˚C

■ Recommended Operating Conditions

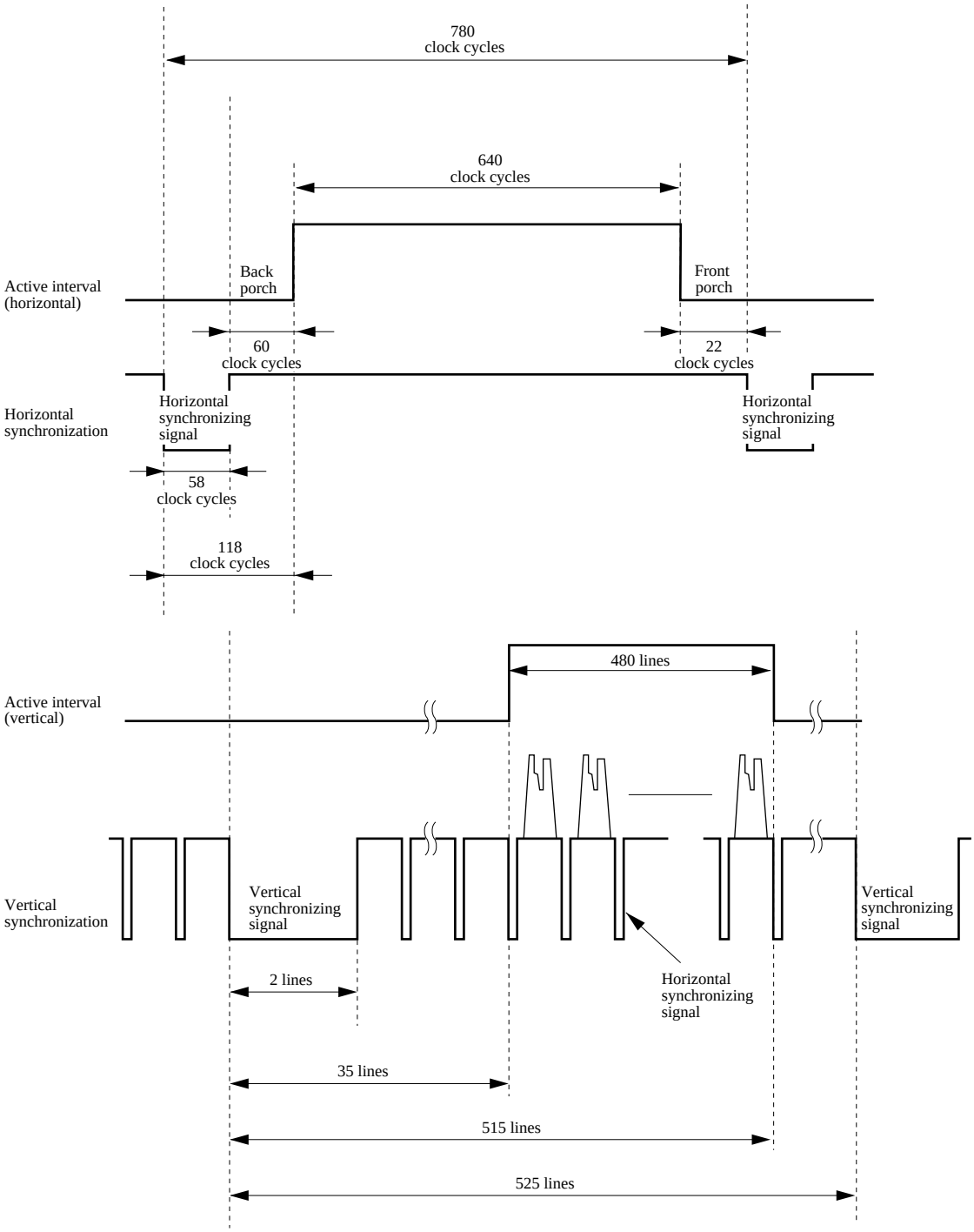
Parameter	Symbol	Conditions	min	typ	max	Unit
Power supply voltage	V_{DD}		4.75	5.0	5.25	V
Ambient temperature	Ta		0		70	˚C
Rise time for input	t_r		0		150	ns
Fall time for input	t_f		0		150	ns
Oscillation frequency	f_{osc}	Crystal oscillator 24 MHz		24		MHz
Recommended value	C_{XI}	V_{DD}=5.0V		12		pF
for external capacitance	C_{XO}	Built-in feedback resistor		12		pF

■ Electrical Characteristics

V_{DD}=4.75 to 5.25V, V_{SS}=0.00V, f=25MHz, Ta=0 to 70˚C

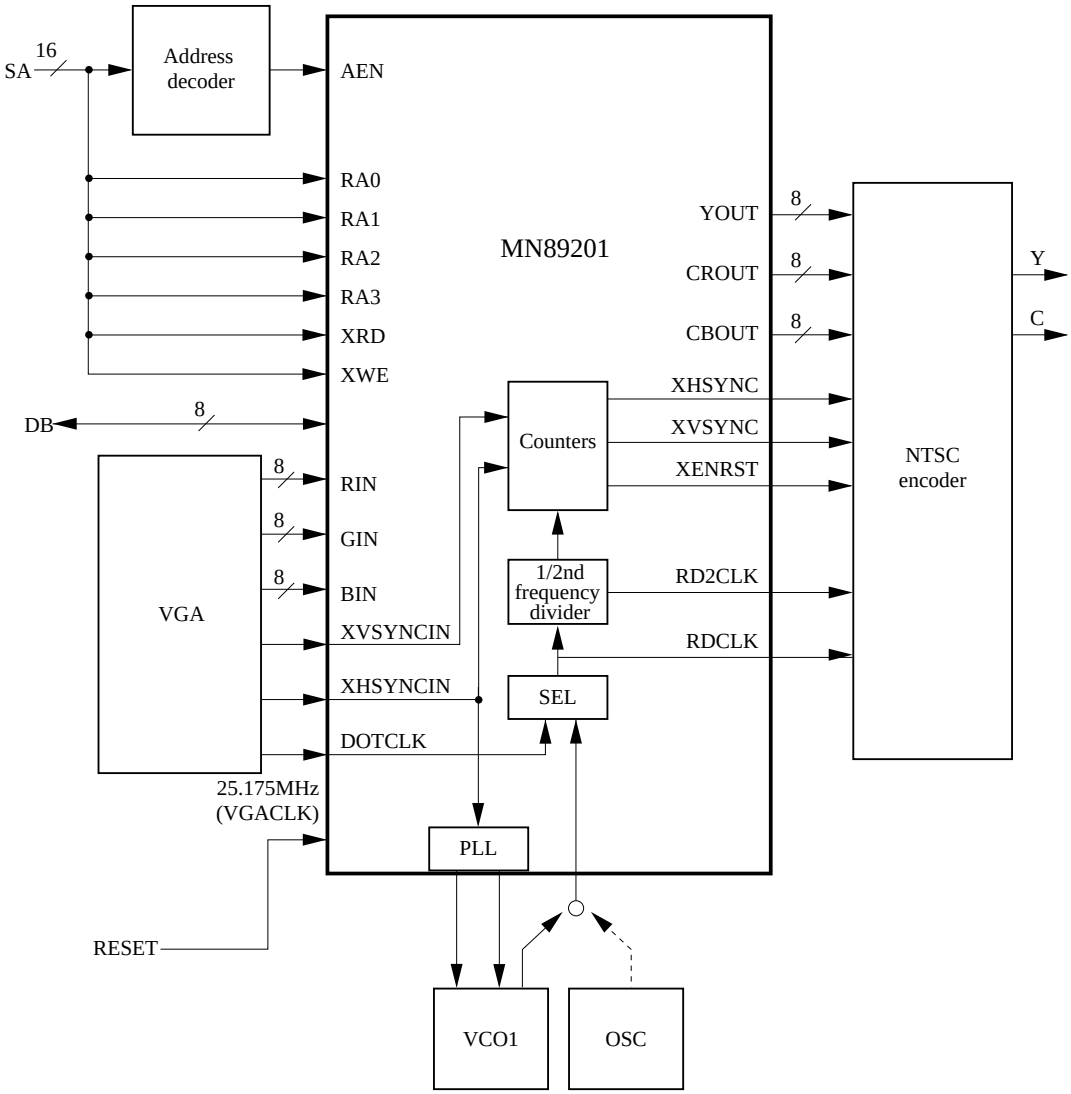
Parameter	Symbol	Conditions	min	typ	max	Unit
Power supply current during operation	I_{DD}	V_I=V_{DD} or V_{SS} f=25MHz V_{DD}=5.0V Output open			126	mA
Oscillator circuit XOO						
Built-in feedback resistance	R_{fb}	V_I=V_{DD} or V_{SS}, V_{DD}=5.0V	228	570	1430	kΩ
CMOS level input with pull-down resistor: MINTEST						
"H" level input voltage	V_{IH2}		V_{DD} × 0.7		V_{DD}	V
"L" level input voltage	V_{IL2}		0		V_{DD} × 0.3	V
Pull-down resistance	R_{PD1}	V_I=V_{DD}, V_{DD}=5.0V	12	30	75	kΩ
Input leakage current	I_{LIPD}	V_I=V_{SS}			±20	µA
TTL level inputs: RA0 to 3, AEN, BIN0 to 7, GIN0 to 7, MOD422F, RIN0 to 7, XRD, XWE, TEST0 to 4, MODST, DOTCLK, MODPIN, MODSET0 to 1, REGLIN, MODCHAV, MODCRCB, MODHFIL, MODVFIL, XHSYNCIN, XVSYNCIN						
"H" level input voltage	V_{IH1}		2.0		V_{DD}	V
"L" level input voltage	V_{IL1}		0		0.8	V
Input leakage current	I_{LI}	V_I=V_{DD} or V_{SS}			±10	µA
TTL level inputs with Schmidt input: SRST, RESET						
Input threshold voltage	V_{tHL}	V_{DD}=4.75 to 5.25V		1.8	2.4	V
	V_{tLH}		0.4	1.0		
Hysteresis width	ΔV_{tt}	V_{DD}=5.0V	0.4	0.8		V
Input leakage current	I_{LI}	V_I=V_{DD} or V_{SS}			±10	µA
Push-pull outputs: RD2CLK, OEON, OEOP, YOUT0 to 7, CBOUT0 to 7, CROUT0 to 7, RDCLK, MEMOUT0 to 7, XBLANK, XHSYNC, XVSYNC, XENRST						
"H" level output voltage	V_{OH}	I_O=–4 .0mA V_I=V_{DD} or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	I_O=4.0mA V_I=V_{DD} or V_{SS}			0.4	V
Peak output current	$I_{O\ (Peak)}$	Absolute maximum rating (not guaranteed operating value)	– 12		12	mA
CMOS level I/O: DB0 to DB7						
"H" level input voltage	V_{IH2}		V_{DD} × 0.7		V_{DD}	V
"L" level input voltage	V_{IL2}		0		V_{DD} × 0.3	V
"H" level output voltage	V_{OH}	I_O=–4.0mA V_I=V_{DD} or V_{SS}	V_{DD}–0.6			V
"L" level output voltage	V_{OL}	I_O=4.0mA V_I=V_{DD} or V_{SS}			0.4	V
Output leakage current	I_{LO}	V_O=High-impedance state V_I=V_{DD} or V_{SS} V_O=V_{DD} or V_{SS}			±10	µA
Peak output current	$I_{O\ (Peak)}$	Absolute maximum rating (not guaranteed operating value)	–12		12	mA

■ Timing Chart



(for a readout frequency of 12.27 MHz)

■ Application Circuit Example



Notes: Choose the clock frequencies to match the synchronization system for the NTSC encoder. The PLL uses the VGA XHSYNCIN (31.5 MHz) clock signal for comparison.
The XHSYNC, XVSYNC, and XENRST signals to the NTSC encoder are synchronized with the VGA outputs.

■ Package Dimensions (Unit: mm)

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