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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

September 2015

FDS89161

Dual N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 2.7 A, 105 mΩ

Features

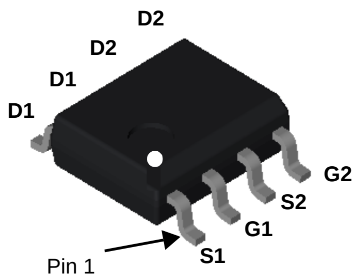
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 105 mΩ at V_{GS} = 10 V, I_D = 2.7 A
- Max $r_{DS(on)}$ = 171 mΩ at V_{GS} = 6 V, I_D = 2.1 A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- 100% UIL Tested
- RoHS Compliant

General Description

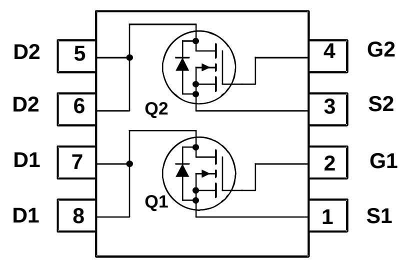
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Applications

- Synchronous Rectifier
- Primary Switch For Bridge Topology



SO-8



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous			2.7	A
	-Pulsed			15	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	13	mJ
P_D	Power Dissipation	T_C = 25 °C		31	W
	Power Dissipation	T_A = 25 °C	(Note1a)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	78	

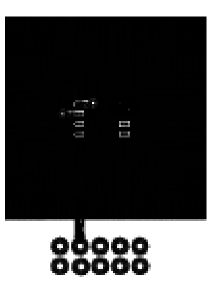
Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS89161	FDS89161	SO-8	13 "	12 mm	2500 units

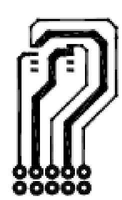
Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		67		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-9		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2.7 A		86	105	mΩ
		V_{GS} = 6 V, I_D = 2.1 A		120	171	
		V_{GS} = 10 V, I_D = 2.7 A, T_J = 125 °C		144	176	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 2.7 A		5		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1MHz		158	210	pF
C_{oss}	Output Capacitance			43	58	pF
C_{rss}	Reverse Transfer Capacitance			3	5	pF
R_g	Gate Resistance			1		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 2.7 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		4.2	10	ns
t_r	Rise Time			1.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			7.3	15	ns
t_f	Fall Time			1.9	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 2.7 A		3	4.1	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 5 V		1.7	2.4	
Q_{gs}	Gate to Source Charge			0.8		nC
Q_{gd}	Gate to Drain “Miller” Charge			0.8		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.7 A (Note 2)		0.85	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)		0.82	1.2	
t_{rr}	Reverse Recovery Time	I_F = 2.7 A, di/dt = 100 A/μs		34	54	ns
Q_{rr}	Reverse Recovery Charge			21	34	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 135°C/W when mounted on a minimun pad

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C, L = 3 mH, I_{AS} = 3 A, V_{DD} = 100 V, V_{GS} = 10 V.

Typical Characteristics (N-Channel) T_J = 25°C unless otherwise noted

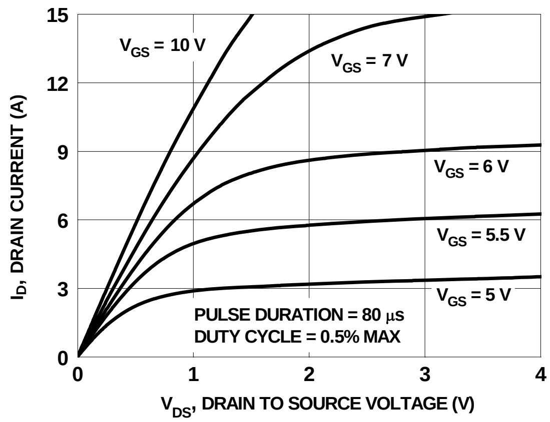


Figure 1. On-Region Characteristics

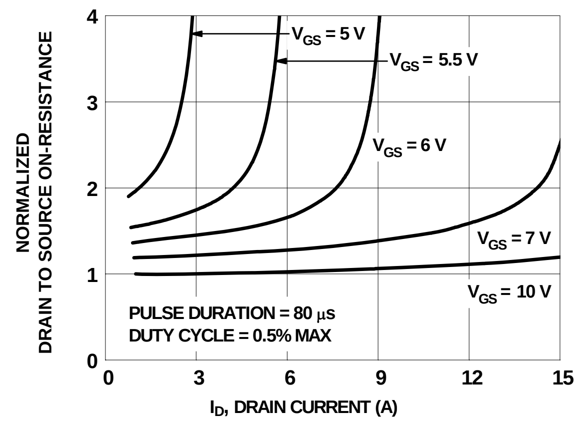


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

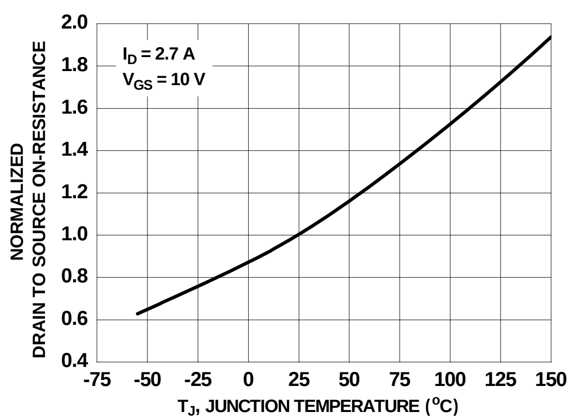


Figure 3. Normalized On-Resistance vs Junction Temperature

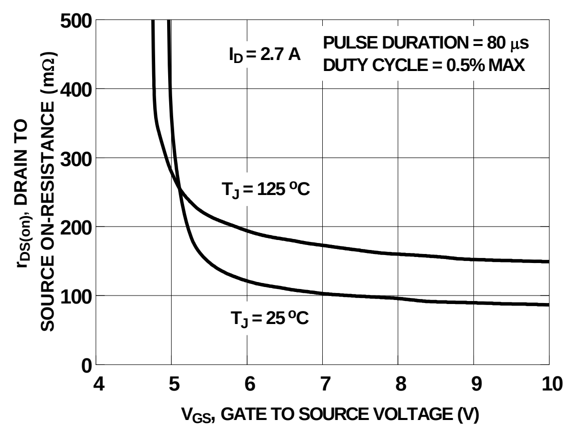


Figure 4. On-Resistance vs Gate to Source Voltage

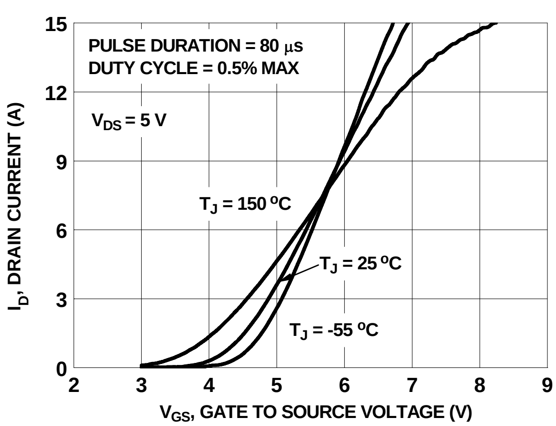


Figure 5. Transfer Characteristics

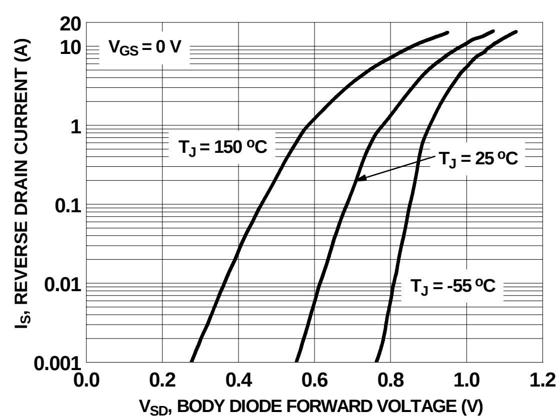


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (N-Channel) T_J = 25°C unless otherwise noted

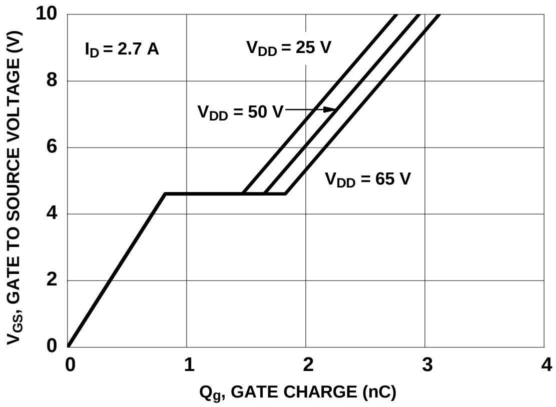


Figure 7. Gate Charge Characteristics

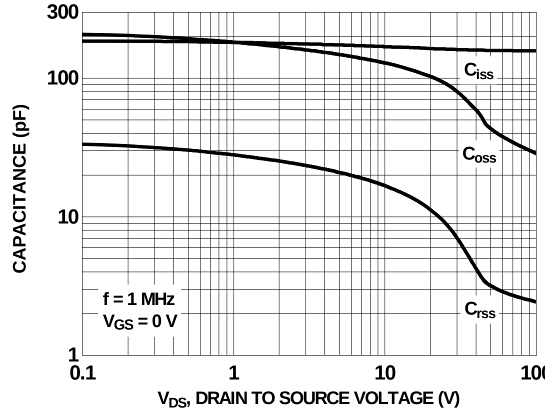


Figure 8. Capacitance vs Drain to Source Voltage

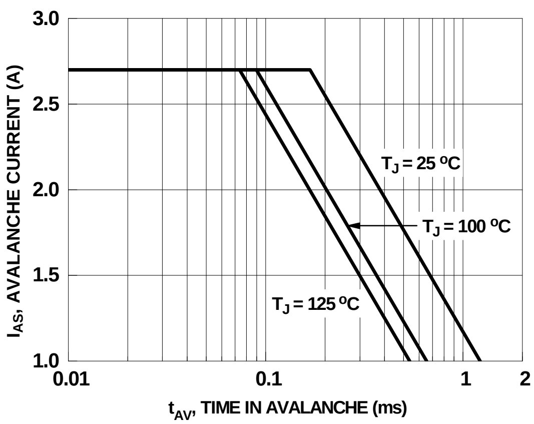


Figure 9. Unclamped Inductive Switching Capability

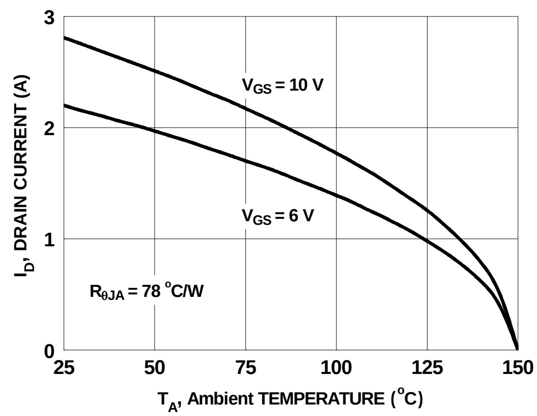


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

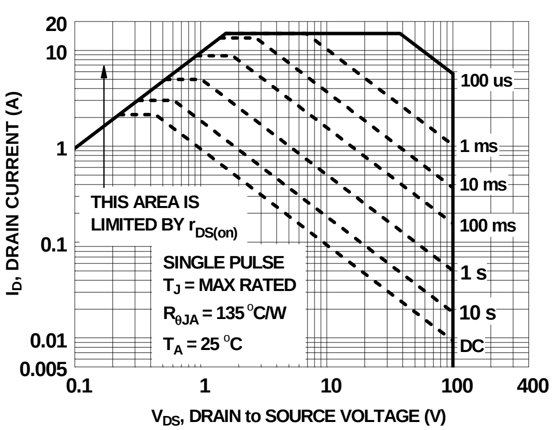


Figure 11. Forward Bias Safe Operating Area

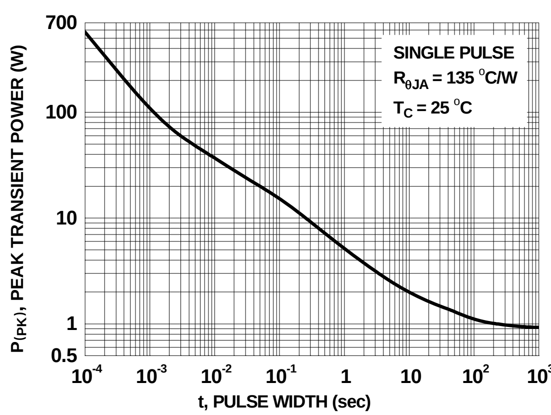


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (N-Channel) T_J = 25°C unless otherwise noted

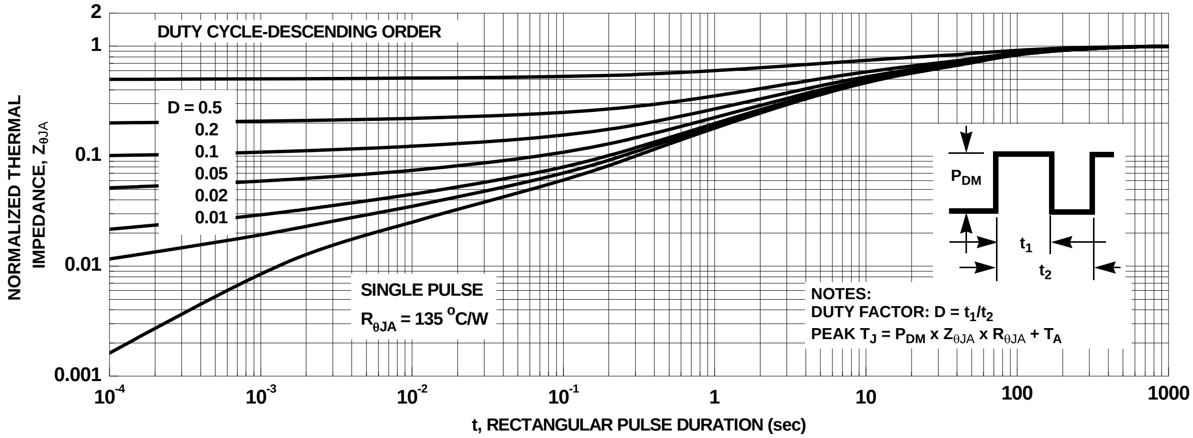
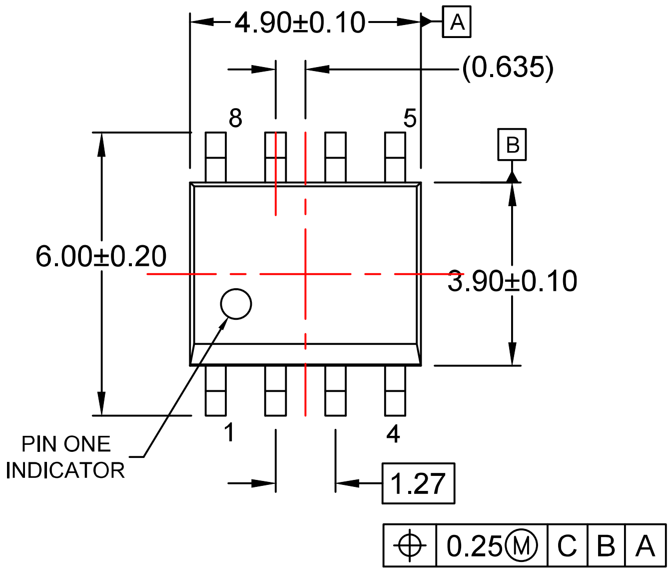
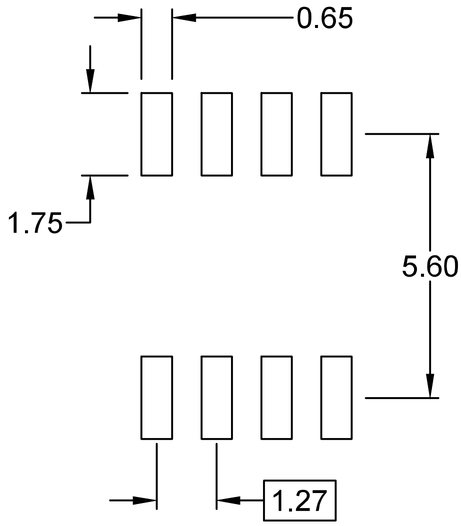
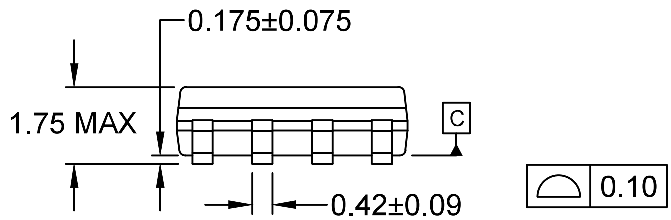


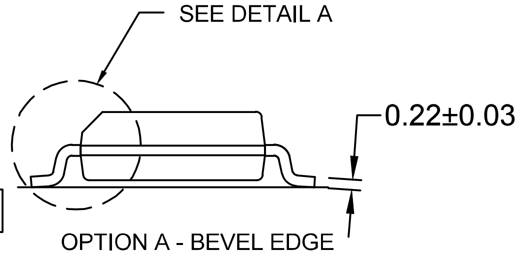
Figure 13. Junction-to-Ambient Transient Thermal Response Curve



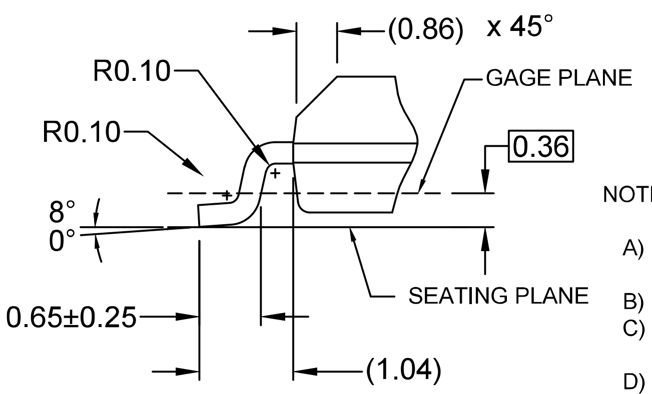


LAND PATTERN RECOMMENDATION

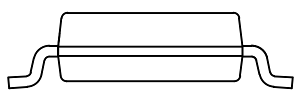




OPTION A - BEVEL EDGE



DETAIL A
SCALE: 2:1



OPTION B - NO BEVEL EDGE

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

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